DUAL-CHANNEL, ULTRA-LOW RESISTANCE LOAD SWITCH

Check for Samples: TPS22966

FEATURES

- **Integrated Dual-Channel Load Switch**
- **Input Voltage Range: 0.8V to 5.5V**
- **Ultra low R_{ON} Resistance**
  - **R_{ON} = 18 mΩ at V_{IN} = 5 V (V_{BIAS} = 5 V)**
  - **R_{ON} = 18 mΩ at V_{IN} = 3.6 V (V_{BIAS} = 5 V)**
  - **R_{ON} = 18 mΩ at V_{IN} = 1.8 V (V_{BIAS} = 5 V)**
- **6-A Maximum Continuous Switch Current per Channel**
- **Low Quiescent Current**
  - **80 µA (Both Channels)**
  - **60 µA (Single Channel)**
- **Low Control Input Threshold Enables Use of 1.2 V/1.8 V/2.5 V/3.3 V Logic**
- **Configurable Rise Time**
- **Quick Output Discharge (QOD)**
- **SON 14-pin Package With Thermal Pad**
- **ESD Performance Tested per JESD 22**
  - **2-kV HBM and 1-kV CDM**

APPLICATIONS

- **Ultrabook™**
- **Notebooks/Netbooks**
- **Tablet PC**
- **Consumer Electronics**
- **Set-top Boxes/Residental Gateways**
- **Telecom Systems**
- **Solid State Drives (SSD)**

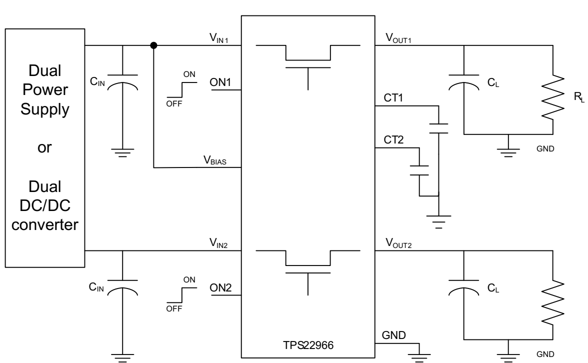


Figure 1. Typical Application

DESCRIPTION

The TPS22966 is a small, ultra-low R_{ON}, dual-channel load switch with controlled turn on. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0.8 V to 5.5 V and can support a maximum continuous current of 6 A per channel. Each switch is independently controlled by an on/off input (ON1 and ON2), which is capable of interfacing directly with low-voltage control signals. In TPS22966, a 220-Ω on-chip load resistor is added for quick output discharge when switch is turned off.

The TPS22966 is available in a small, space-saving 2mm x 3mm 14-SON package (DPU) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

Table 1. Feature List

R_{ON} Typical at 3.6 V (V_{BIAS} = 5 V)	18 mΩ
Rise Time(1)	Adjustable
Quick Output Discharge(2)	Yes
Maximum Output Current (per channel)	6 A
GPIO Enable	Active High
Operating Temperature	–40°C to 85°C

(1) See Application Information section for CT value vs. rise time.

(2) This feature discharges output of the switch to GND through a 220-Ω resistor, preventing the output from floating.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

See package option addendum for orderable part numbers.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

			VALUE	UNIT(2)
$V_{IN1,2}$	Input voltage range		–0.3 to 6	V
$V_{OUT1,2}$	Output voltage range		–0.3 to 6	V
$V_{ON1,2}$	ON-pin voltage range		–0.3 to 6	V
V_{BIAS}	VBIAS voltage range		–0.3 to 6	V
I_{MAX}	Maximum continuous switch current per channel		6	A
I_{PLS}	Maximum pulsed switch current per channel, pulse <300 µs, 2% duty cycle		8	A
T_A	Operating free-air temperature range(3)		–40 to 85	°C
T_J	Maximum junction temperature		125	°C
T_{STG}	Storage temperature range		–65 to 150	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)	2000	V
		Charged-Device Model (CDM)	1000	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $TA_{(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$

THERMAL INFORMATION

THERMAL METRIC(1)		TPS22966	UNITS
		DPU (14 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	52.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	45.9	
θ_{JB}	Junction-to-board thermal resistance	11.5	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	11.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	6.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
$V_{IN1,2}$	Input voltage range		0.8	V_{BIAS}	V
V_{BIAS}	Bias voltage range		2.5	5.5	V
$V_{ON1,2}$	ON voltage range		0	5.5	V
$V_{OUT1,2}$	Output voltage range			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	1.2	5.5	V
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	0	0.5	V
$C_{IN1,2}$	Input capacitor		1 (1)		µF

(1) Refer to Application Information section.

ELECTRICAL CHARACTERISTICS

Unless otherwise note the specification in the following table applies over the operating ambient temperature **–40°C ≤ T_A ≤ 85°C** (full) and **V_{BIAS} = 5.0 V**. Typical values are for T_A = 25°C. (unless otherwise noted)

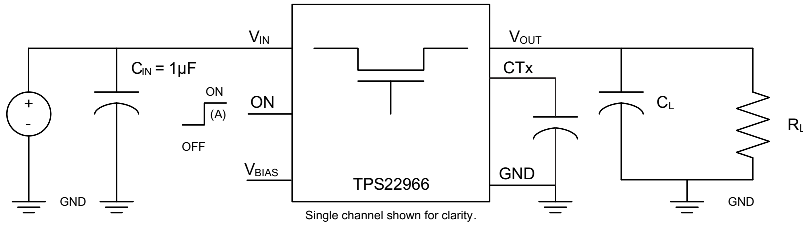
PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current (both channels)	I_{OUT1} = I_{OUT2} = 0 mA, $V_{IN1,2}$ = $V_{ON1,2}$ = V_{BIAS} = 5.0 V		Full		80	120	µA
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current (single channel)	I_{OUT1} = I_{OUT2} = 0 mA, V_{ON2} = 0 V $V_{IN1,2}$ = V_{ON1} = V_{BIAS} = 5.0 V		Full		60		µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		Full			2	µA
$I_{IN(VIN-OFF)}$	$V_{IN1,2}$ off-state supply current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 5.0 V	Full		0.5	8	µA
			$V_{IN1,2}$ = 3.3 V			0.1	3	
			$V_{IN1,2}$ = 1.8 V			0.07	2	
			$V_{IN1,2}$ = 0.8 V			0.04	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		Full			1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance (per channel)	I_{OUT} = –200 mA, V_{BIAS} = 5.0 V	V_{IN} = 5.0 V	25°C		18	25	mΩ
				Full			27	
			V_{IN} = 3.3 V	25°C		18	25	mΩ
				Full			27	
			V_{IN} = 1.8 V	25°C		18	25	mΩ
				Full			27	
			V_{IN} = 1.5 V	25°C		18	25	mΩ
				Full			27	
			V_{IN} = 1.2 V	25°C		18	25	mΩ
				Full			27	
			V_{IN} = 0.8 V	25°C		18	25	mΩ
				Full			27	
R_{PD}	Output pulldown resistance	V_{IN} = 5.0 V, V_{ON} = 0 V, I_{OUT} = 15 mA		Full		220	300	Ω

ELECTRICAL CHARACTERISTICS

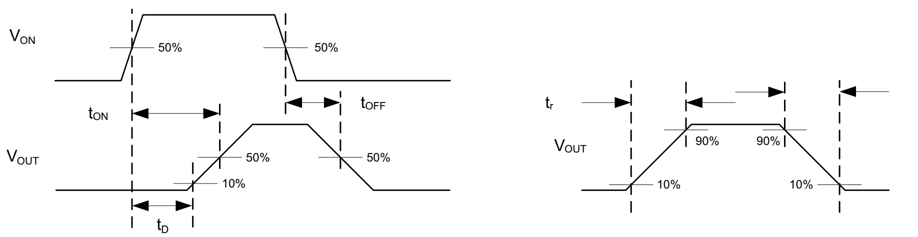
Unless otherwise noted, the specification in the following table applies over the operating ambient temp **–40°C ≤ T_A ≤ 85°C** (full) and **V_{BIAS} = 2.5 V**. Typical values are for T_A = 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current (both channels)	$I_{OUT1} = I_{OUT2}$ = 0 mA, $V_{IN1,2} = V_{ON1,2} = V_{BIAS}$ = 2.5 V		Full		32	37	µA
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current (single channel)	$I_{OUT1} = I_{OUT2}$ = 0 mA, V_{ON2} = 0 V $V_{IN1,2} = V_{ON1} = V_{BIAS}$ = 2.5 V		Full		23		µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		Full			2	µA
$I_{IN(VIN-OFF)}$	$V_{IN1,2}$ off-state supply current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 2.5 V	Full		0.13	3	µA
			$V_{IN1,2}$ = 1.8 V			0.07	2	
			$V_{IN1,2}$ = 1.2 V			0.05	2	
			$V_{IN1,2}$ = 0.8 V			0.04	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		Full			1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	25°C		22	28	mΩ
				Full			30	
			V_{IN} = 1.8 V	25°C		21	28	mΩ
				Full			30	
			V_{IN} = 1.5 V	25°C		20	27	mΩ
				Full			29	
			V_{IN} = 1.2 V	25°C		20	27	mΩ
				Full			29	
			V_{IN} = 0.8 V	25°C		19	27	mΩ
				Full			29	
R_{PD}	Output pulldown resistance	V_{IN} = 2.5 V, V_{ON} = 0 V, I_{OUT} = 1 mA		Full		260	300	Ω

SWITCHING CHARACTERISTIC MEASUREMENT INFORMATION



TEST CIRCUIT



t_{ON}/t_{OFF} WAVEFORMS

(A) Rise and fall times of the control signal is 100ns.

Figure 2. Test Circuit and t_{ON}/t_{OFF} Waveforms

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IN} = V_{ON} = V_{BIAS} = 5$ V, $T_A = 25$ºC (unless otherwise noted)						
t_{ON}	Turn-on time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		1310		
t_{OFF}	Turn-off time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		6		
t_R	V_{OUT} rise time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		1720		µs
t_F	V_{OUT} fall time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		2		
t_D	ON delay time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		460		
$V_{IN} = 0.8$ V, $V_{ON} = V_{BIAS} = 5$ V, $T_A = 25$ºC (unless otherwise noted)						
t_{ON}	Turn-on time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		550		
t_{OFF}	Turn-off time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		170		
t_R	V_{OUT} rise time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		325		µs
t_F	V_{OUT} fall time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		16		
t_D	ON delay time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		400		
$V_{IN} = 2.5$ V, $V_{ON} = 5$ V, $V_{BIAS} = 2.5$ V, $T_A = 25$ºC (unless otherwise noted)						
t_{ON}	Turn-on time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		2050		
t_{OFF}	Turn-off time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		5		
t_R	V_{OUT} rise time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		2275		µs
t_F	V_{OUT} fall time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		2.5		
t_D	ON delay time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		990		
$V_{IN} = 0.8$ V, $V_{ON} = 5$ V, $V_{BIAS} = 2.5$ V, $T_A = 25$ºC (unless otherwise noted)						
t_{ON}	Turn-on time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		1300		
t_{OFF}	Turn-off time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		130		
t_R	V_{OUT} rise time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		875		µs
t_F	V_{OUT} fall time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		16		
t_D	ON delay time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu F$, $C_T = 1000$ pF		870		

FUNCTIONAL BLOCK DIAGRAM

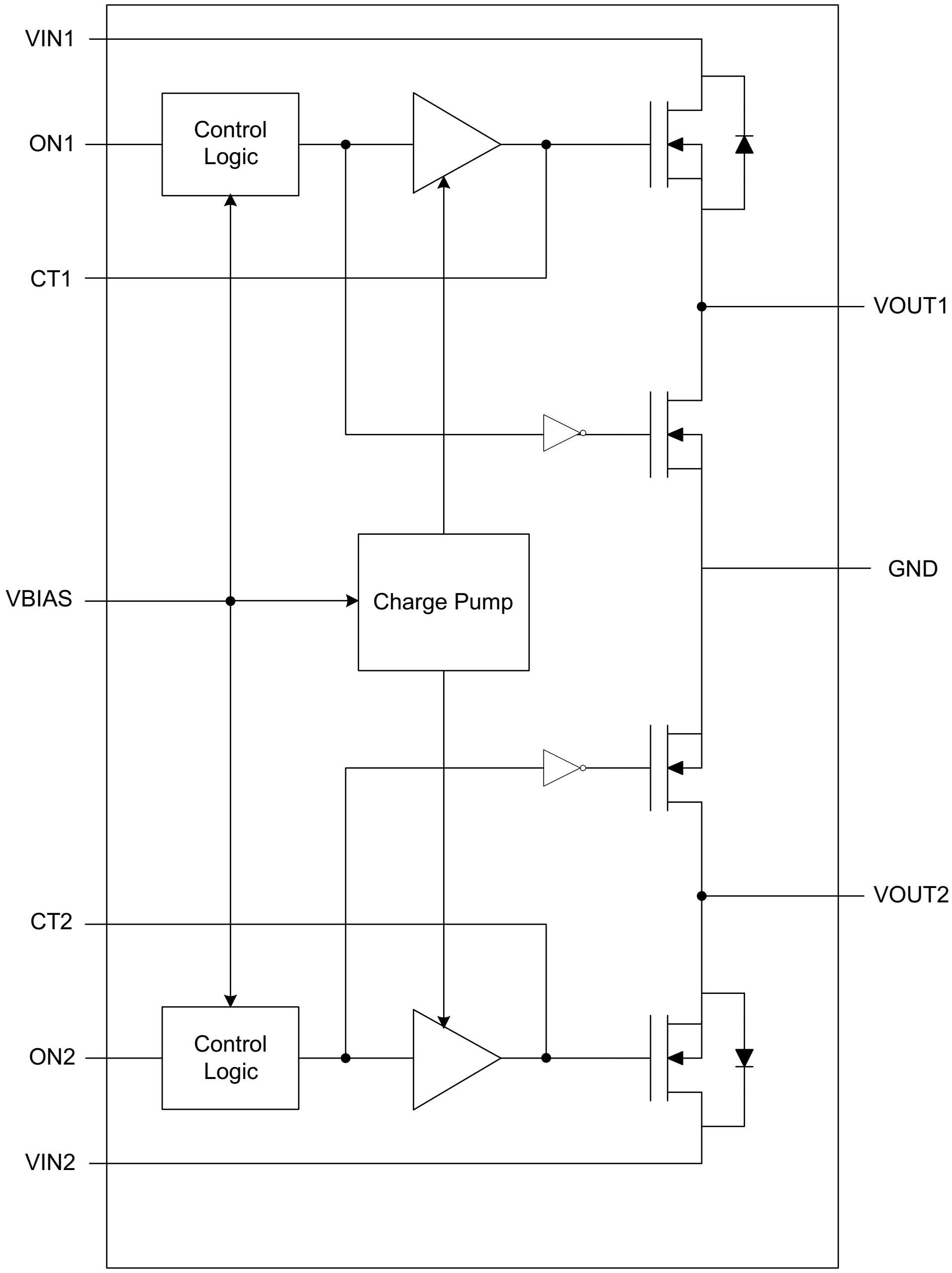
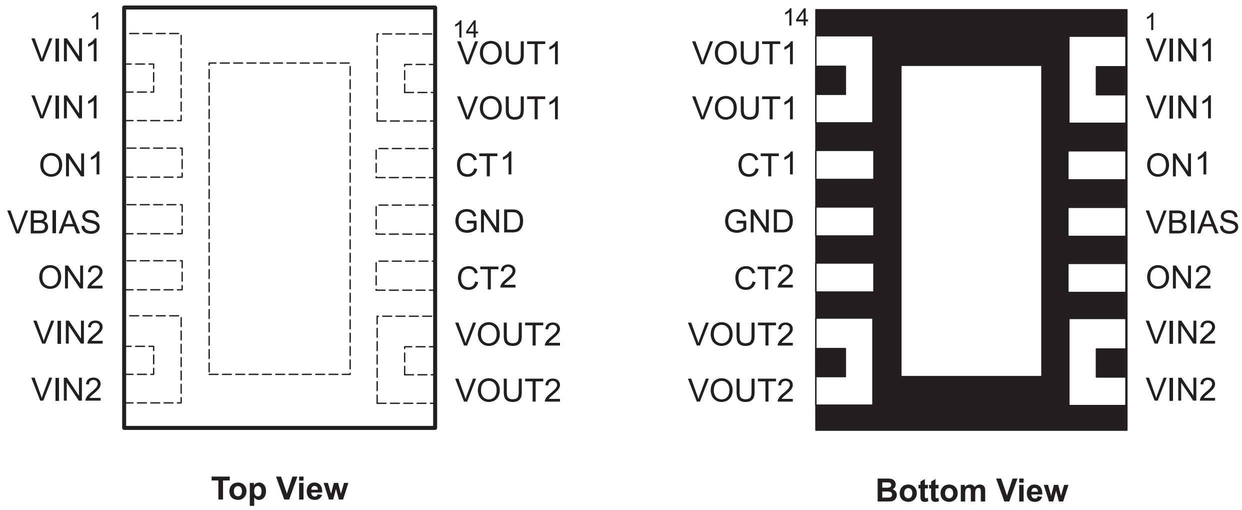


Figure 3. Functional Block Diagram

Table 2. FUNCTIONAL TABLE

ONx	VINx to VOUTx	VOUTx to GND
L	Off	On
H	On	Off

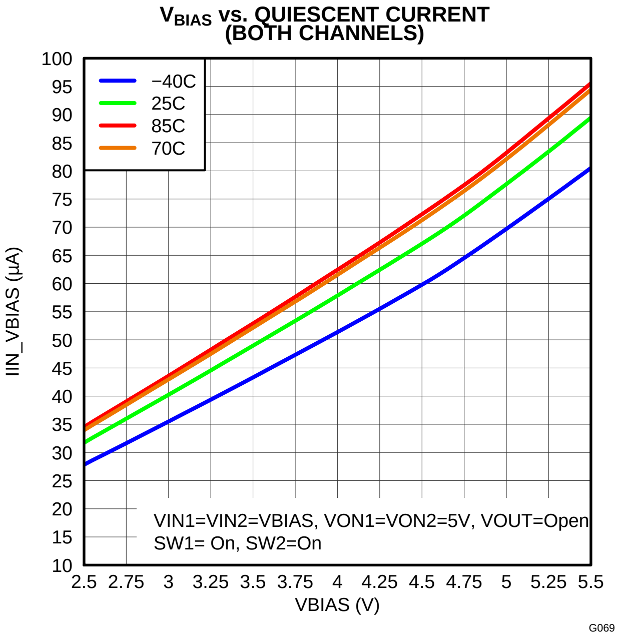
DPU PACKAGE

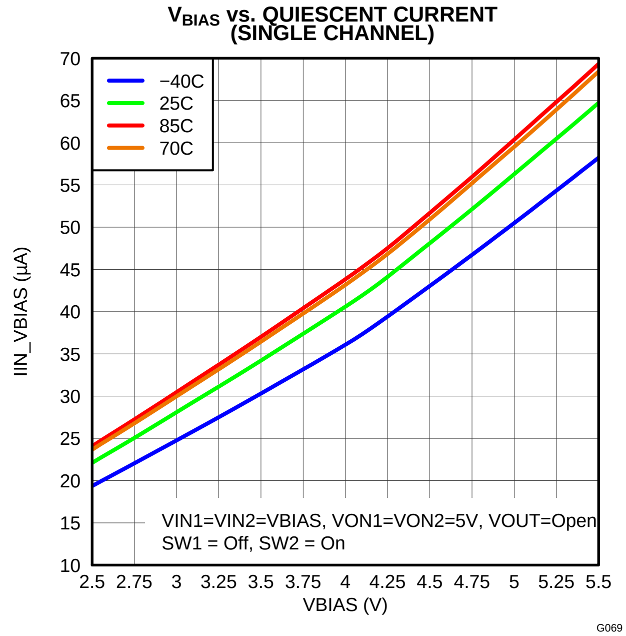


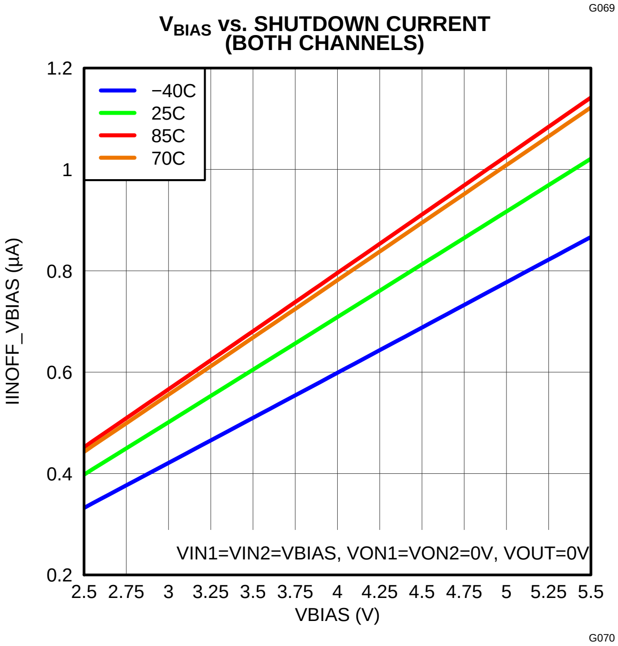
PIN TABLE

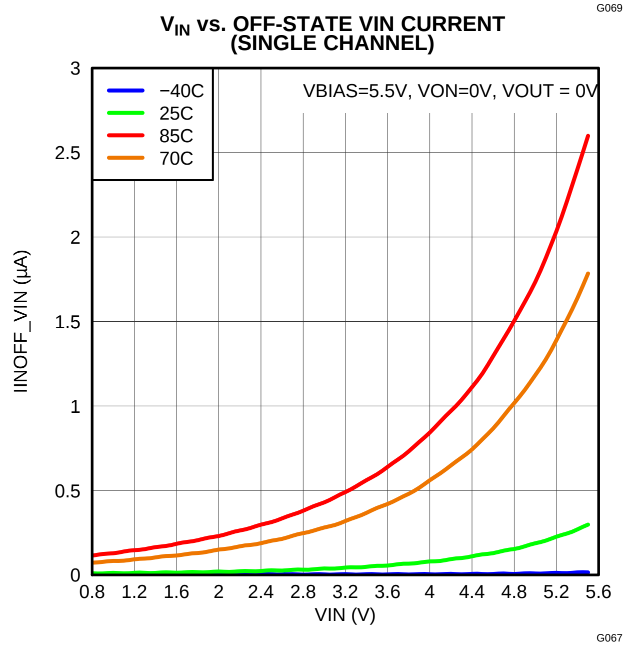
TPS22966 DPU	PIN NAME	I/O	DESCRIPTION
1	VIN1	I	Switch #1 input. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8V to V_{BIAS}. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turn-on of the channel. See Application Information section for more information.
2	VIN1	I	Switch #1 input. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8V to V_{BIAS}. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turn-on of the channel. See Application Information section for more information.
3	ON1	I	Active high switch #1 control input. Do not leave floating.
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.5V. See Application Information section.
5	ON2	I	Active high switch #2 control input. Do not leave floating.
6	VIN2	I	Switch #2 input. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8V to V_{BIAS}. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turn-on of the channel. See Application Information section for more information.
7	VIN2	I	Switch #2 input. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8V to V_{BIAS}. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turn-on of the channel. See Application Information section for more information.
8	VOUT2	O	Switch #2 output.
9	VOUT2	O	Switch #2 output.
10	CT2	O	Switch #2 slew rate control. Can be left floating. Capacitor used on this pin should be rated for a minimum of 25V for desired rise time performance.
11	GND	–	Ground
12	CT1	O	Switch #1 slew rate control. Can be left floating. Capacitor used on this pin should be rated for a minimum of 25V for desired rise time performance.
13	VOUT1	O	Switch #1 output.
14	VOUT1	O	Switch #1 output.
15	Thermal Pad	O	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See Application Information for layout guidelines.

TYPICAL CHARACTERISTICS

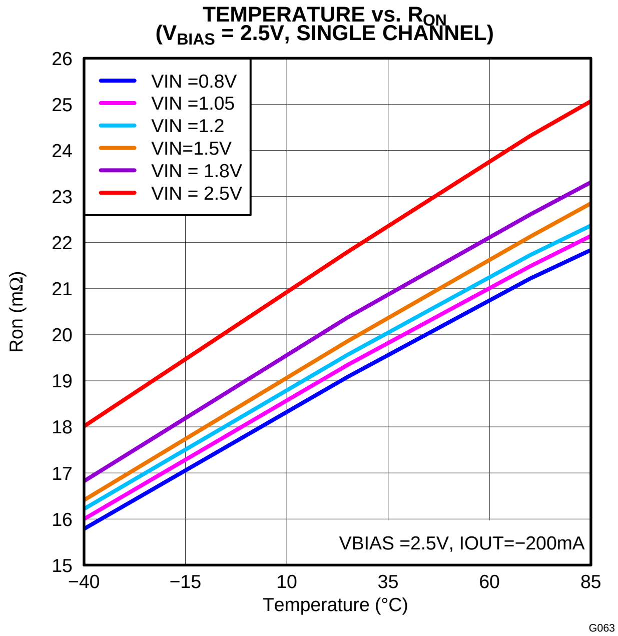


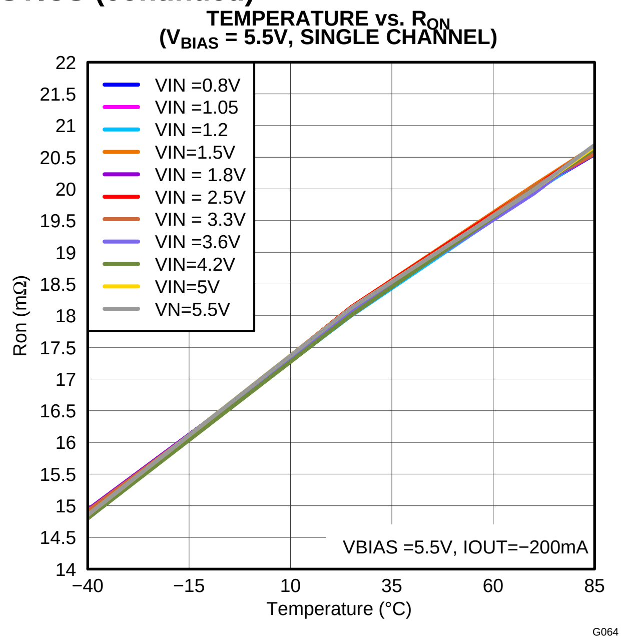


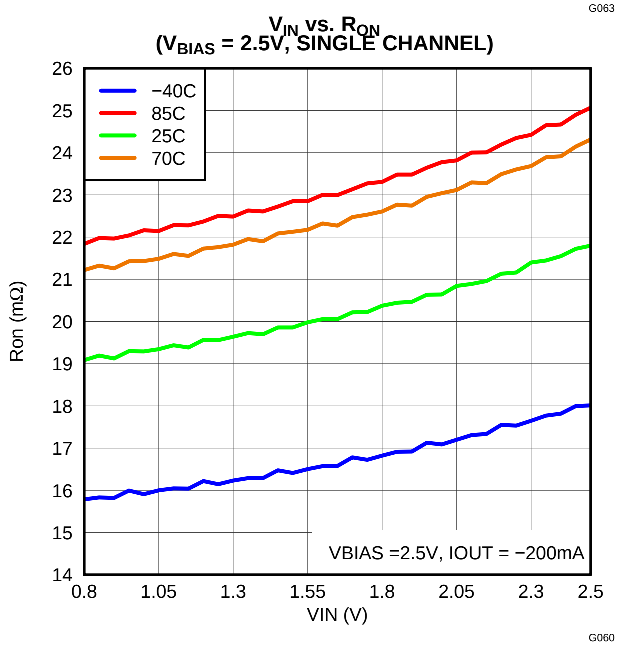


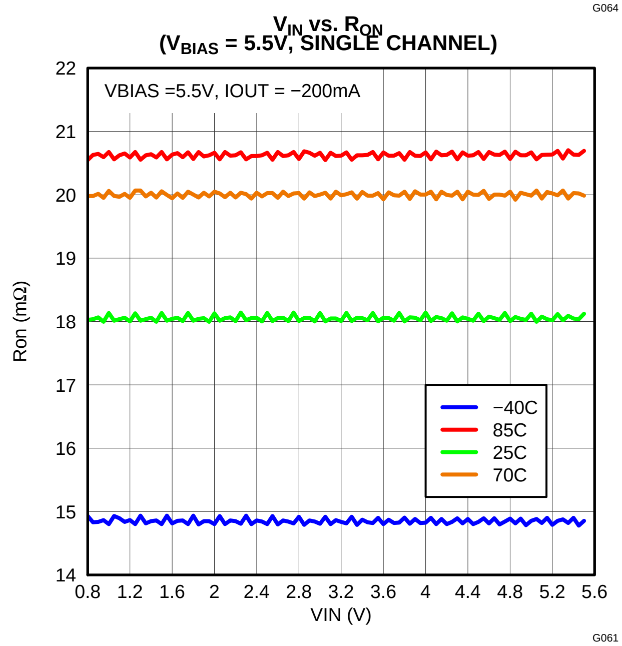


TYPICAL CHARACTERISTICS (continued)



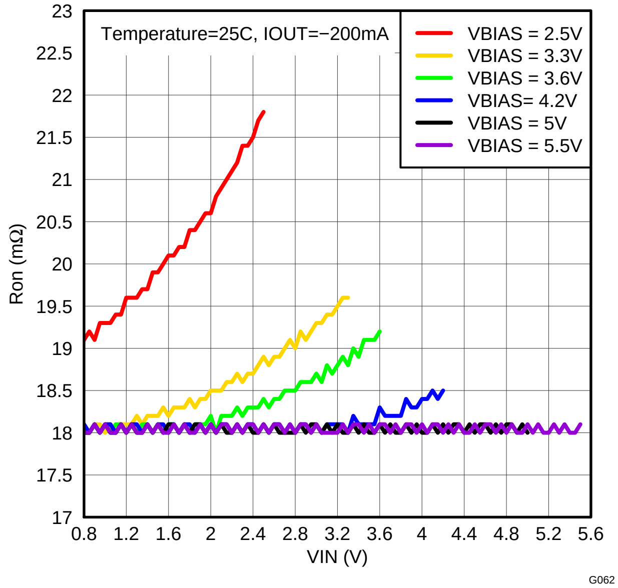




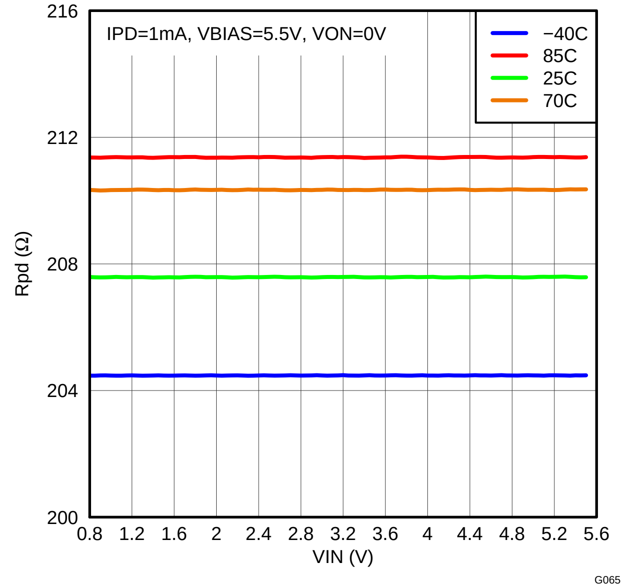


TYPICAL CHARACTERISTICS (continued)

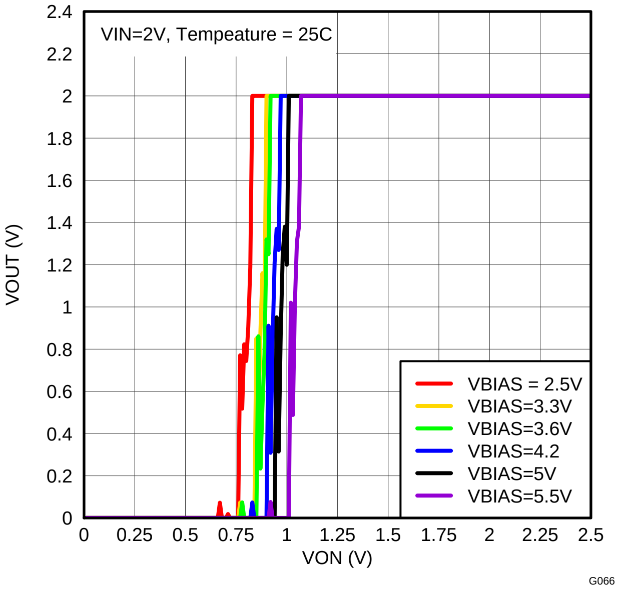
V_{IN} vs. R_{ON} (T_A = 25°C, SINGLE CHANNEL)



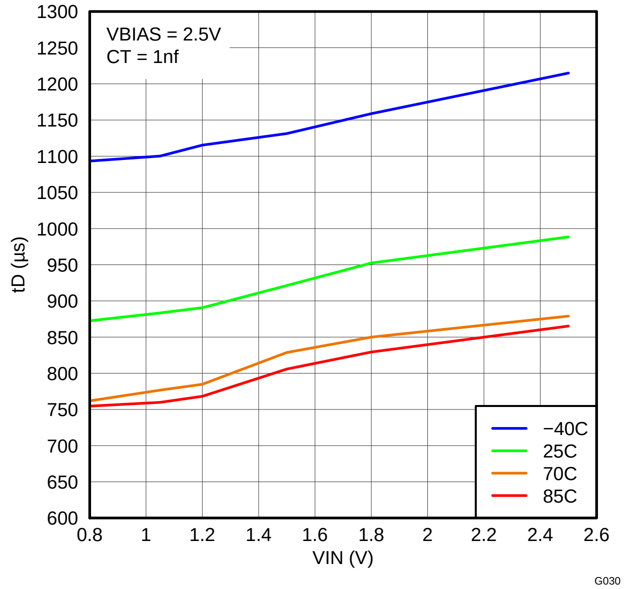
VIN vs. R_{PD} (V_{BIAS} = 5.5V, SINGLE CHANNEL)



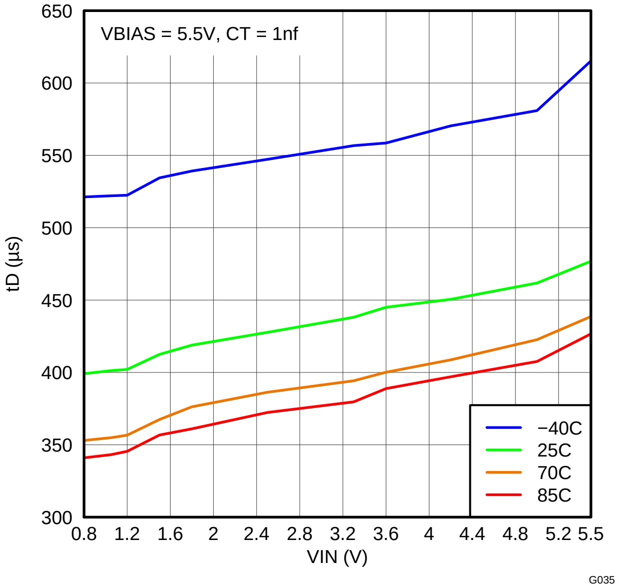
V_{ON} vs. V_{OUT} (T_A = 25°C, SINGLE CHANNEL)



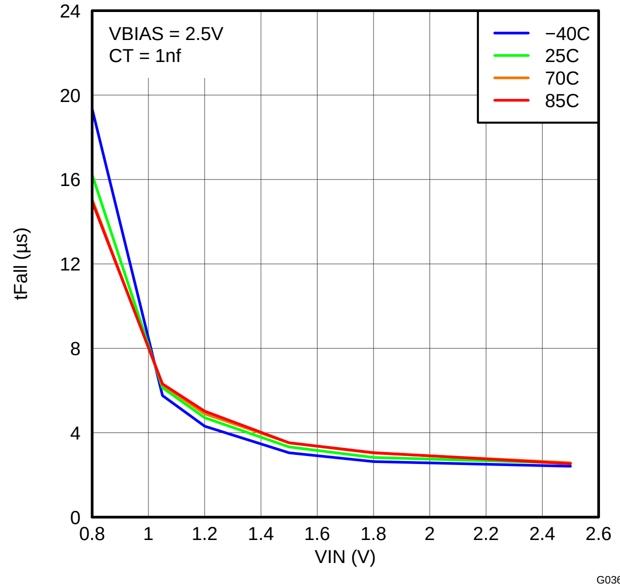
V_{IN} vs. t_D (V_{BIAS} = 2.5V, CT = 1nF)



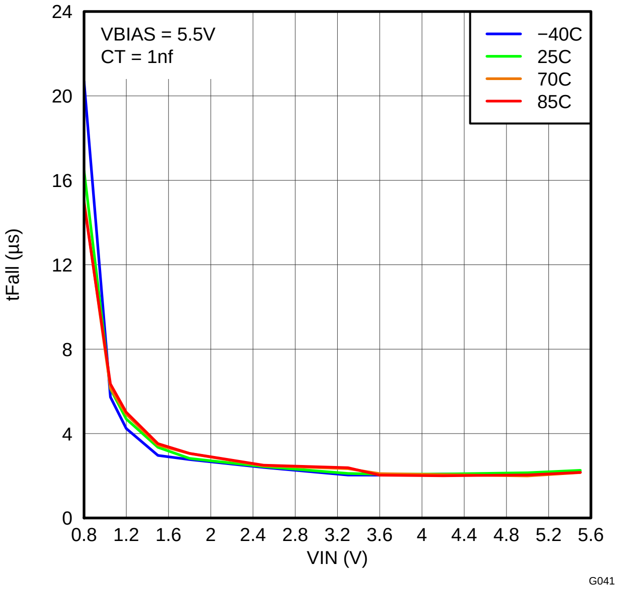
TYPICAL CHARACTERISTICS (continued)



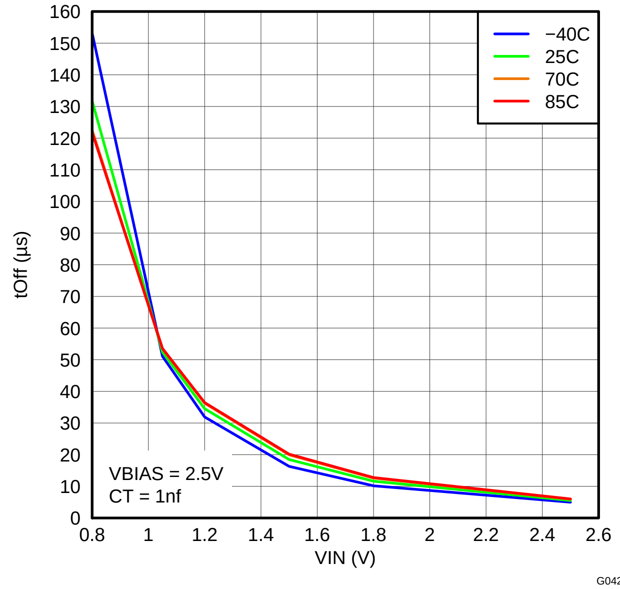
V_{IN} vs. t_D (V_{BIAS} = 5.5V, CT = 1nF)



V_{IN} vs. t_F (V_{BIAS} = 2.5V, CT = 1nF)



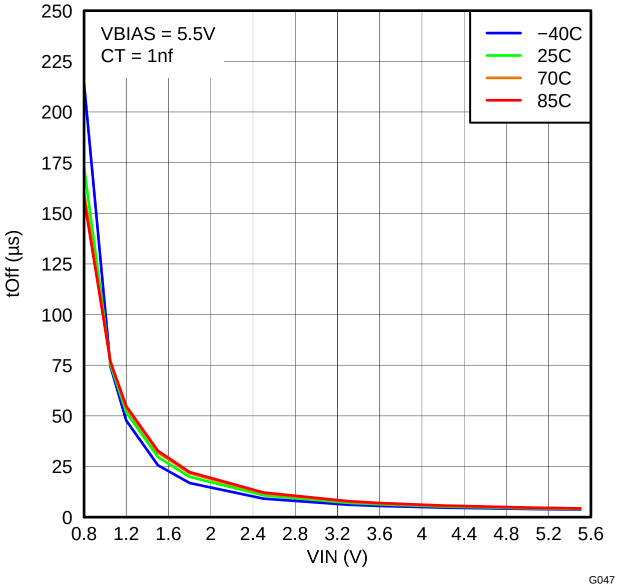
V_{IN} vs. t_F (V_{BIAS} = 5.5V, CT = 1nF)



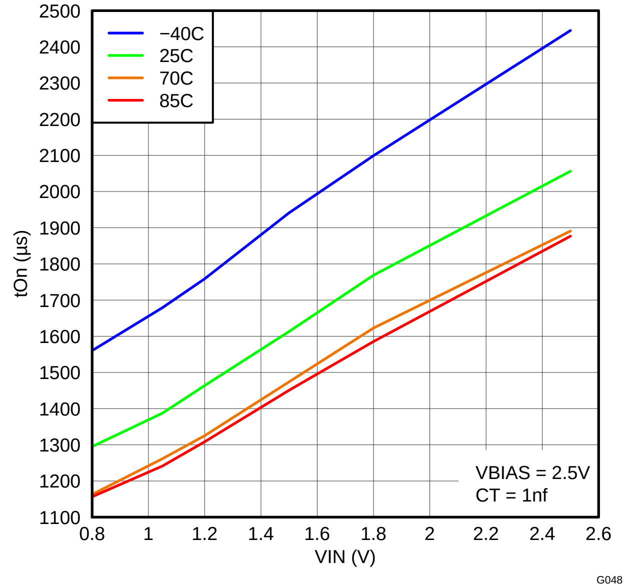
V_{IN} vs. t_{OFF} (V_{BIAS} = 2.5V, CT = 1nF)

TYPICAL CHARACTERISTICS (continued)

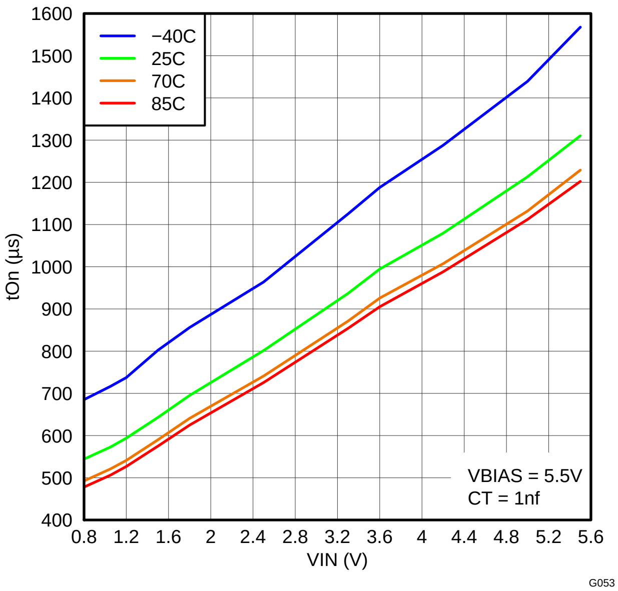
V_{IN} vs. t_{OFF} (V_{BIAS} = 5.5V, CT = 1nF)



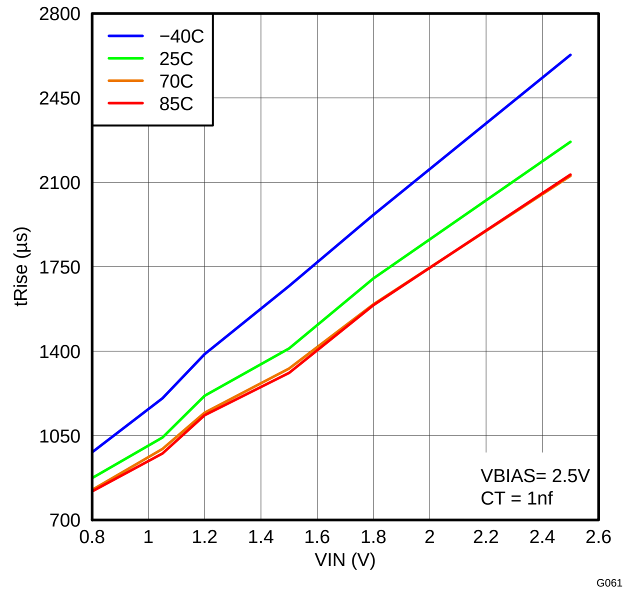
V_{IN} vs. t_{ON} (V_{BIAS} = 2.5V, CT = 1nF)



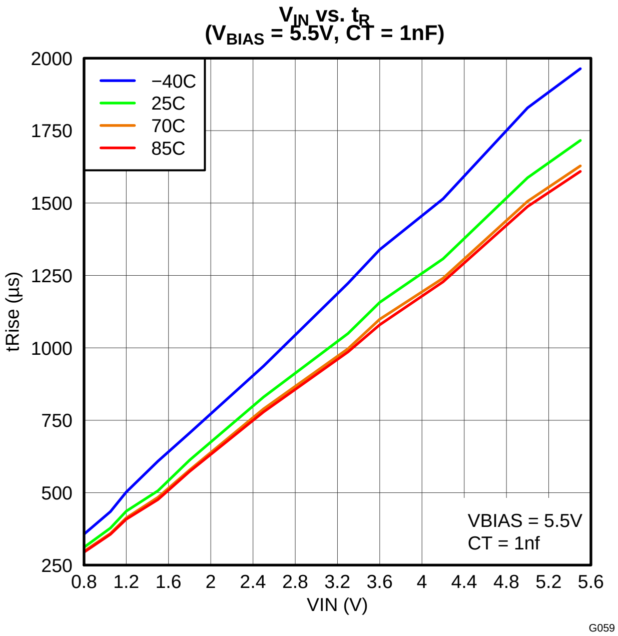
V_{IN} vs. t_{ON} (V_{BIAS} = 5.5V, CT = 1nF)

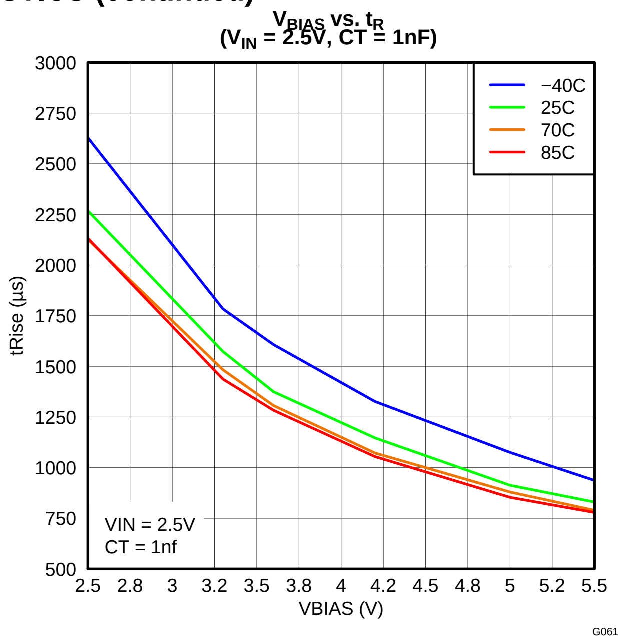


V_{IN} vs. t_R (V_{BIAS} = 2.5V, CT = 1nF)



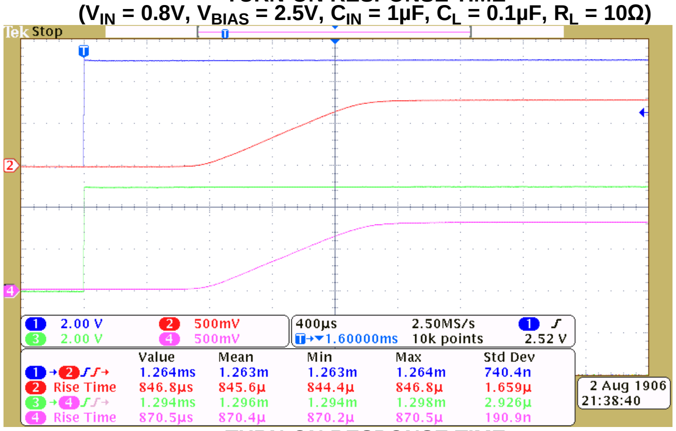
TYPICAL CHARACTERISTICS (continued)



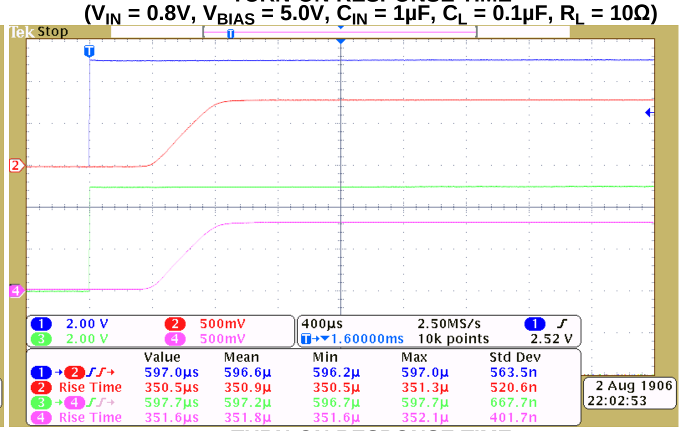


TYPICAL AC SCOPE CAPTURES @ T_A = 25ºC, CT = 1nF

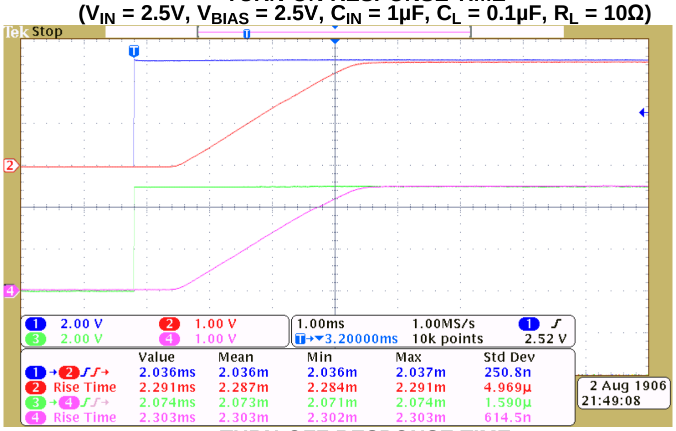
TURN-ON RESPONSE TIME
(V_{IN} = 0.8V, V_{BIAS} = 2.5V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)



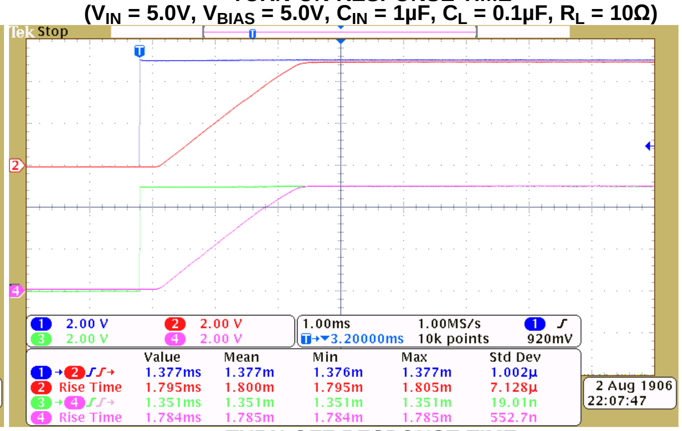
TURN-ON RESPONSE TIME
(V_{IN} = 0.8V, V_{BIAS} = 5.0V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)



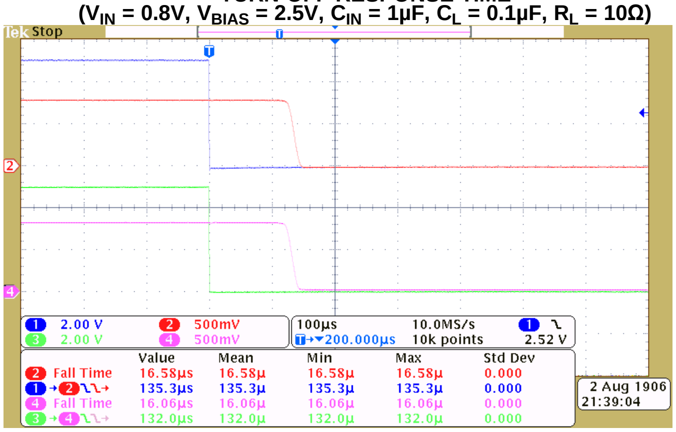
TURN-ON RESPONSE TIME
(V_{IN} = 2.5V, V_{BIAS} = 2.5V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)



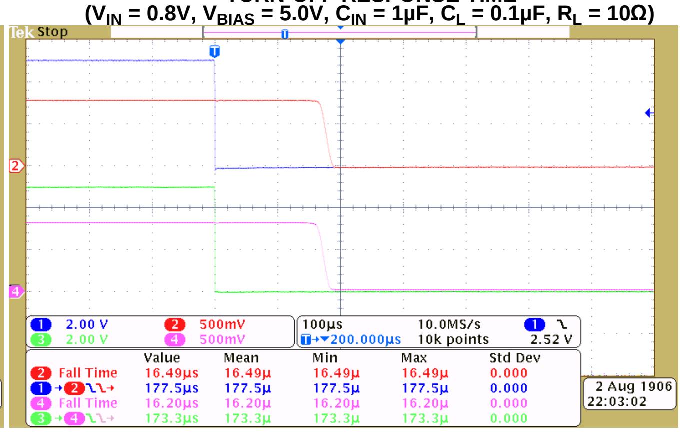
TURN-ON RESPONSE TIME
(V_{IN} = 5.0V, V_{BIAS} = 5.0V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)



TURN-OFF RESPONSE TIME
(V_{IN} = 0.8V, V_{BIAS} = 2.5V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)

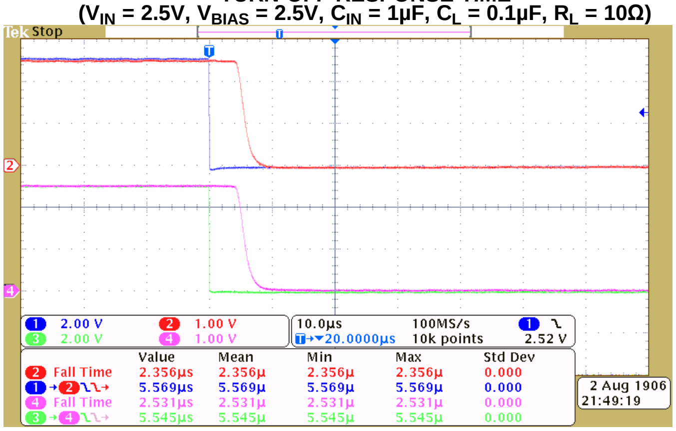


TURN-OFF RESPONSE TIME
(V_{IN} = 0.8V, V_{BIAS} = 5.0V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)

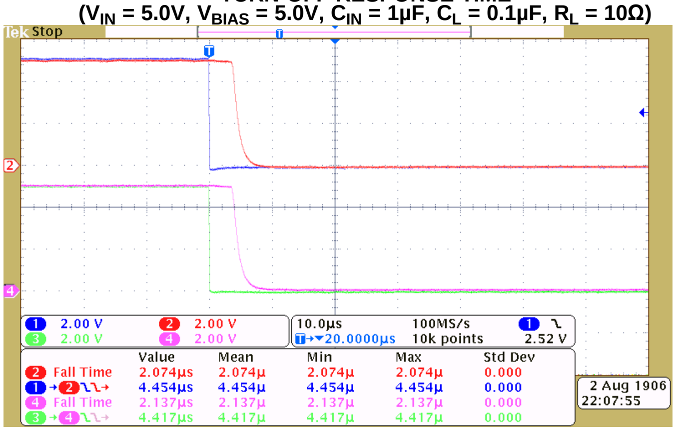


TYPICAL AC SCOPE CAPTURES @ T_A = 25ºC, CT = 1nF (continued)

TURN-OFF RESPONSE TIME (V_{IN} = 2.5V, V_{BIAS} = 2.5V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)



TURN-OFF RESPONSE TIME (V_{IN} = 5.0V, V_{BIAS} = 5.0V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)



APPLICATION INFORMATION

ON/OFF CONTROL

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

INPUT CAPACITOR (OPTIONAL)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

OUTPUT CAPACITOR (OPTIONAL)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn-on due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see Figure 4).

V_{IN} and V_{BIAS} VOLTAGE RANGE

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device will still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit R_{ON} greater than what is listed in the ELECTRICAL CHARACTERISTICS table. See Figure 4 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.

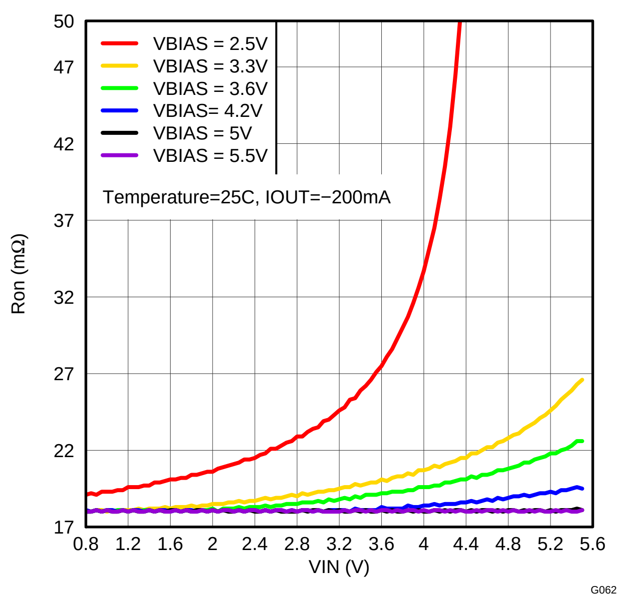


Figure 4. R_{ON} vs. V_{IN} ($V_{IN} > V_{BIAS}$, Single Channel)

ADJUSTABLE RISE TIME

A capacitor to GND on the CTx pins sets the slew rate for each channel. To ensure desired performance, a capacitor with a minimum voltage rating of 25V should be used on the CTx pin. An approximate formula for the relationship between CTx and slew rate is (the equation below accounts for 10% to 90% measurement on V_{OUT} and does **NOT** apply for CTx = 0pF. Use table below to determine rise times for when CTx = 0pF):

$$SR = 0.32 \times CT + 13.7 \quad (1)$$

Where,

SR = slew rate (in µs/V)
CT = the capacitance value on the CTx pin (in pF)
The units for the constant 13.7 is in µs/V.

Rise time can be calculated by multiplying the input voltage by the slew rate. The table below contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition, and the ON pin is asserted high.

CTx (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1µF, C_{IN} = 1µF, R_L = 10Ω TYPICAL VALUES at 25°C, V_{BIAS} = 5V, 25V X7R 10% CERAMIC CAP						
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V
0	124	88	63	60	53	49	42
220	481	323	193	166	143	133	109
470	855	603	348	299	251	228	175
1000	1724	1185	670	570	469	411	342
2200	3328	2240	1308	1088	893	808	650
4700	7459	4950	2820	2429	1920	1748	1411
10000	16059	10835	6040	5055	4230	3770	3033

BOARD LAYOUT AND THERMAL CONSIDERATIONS

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

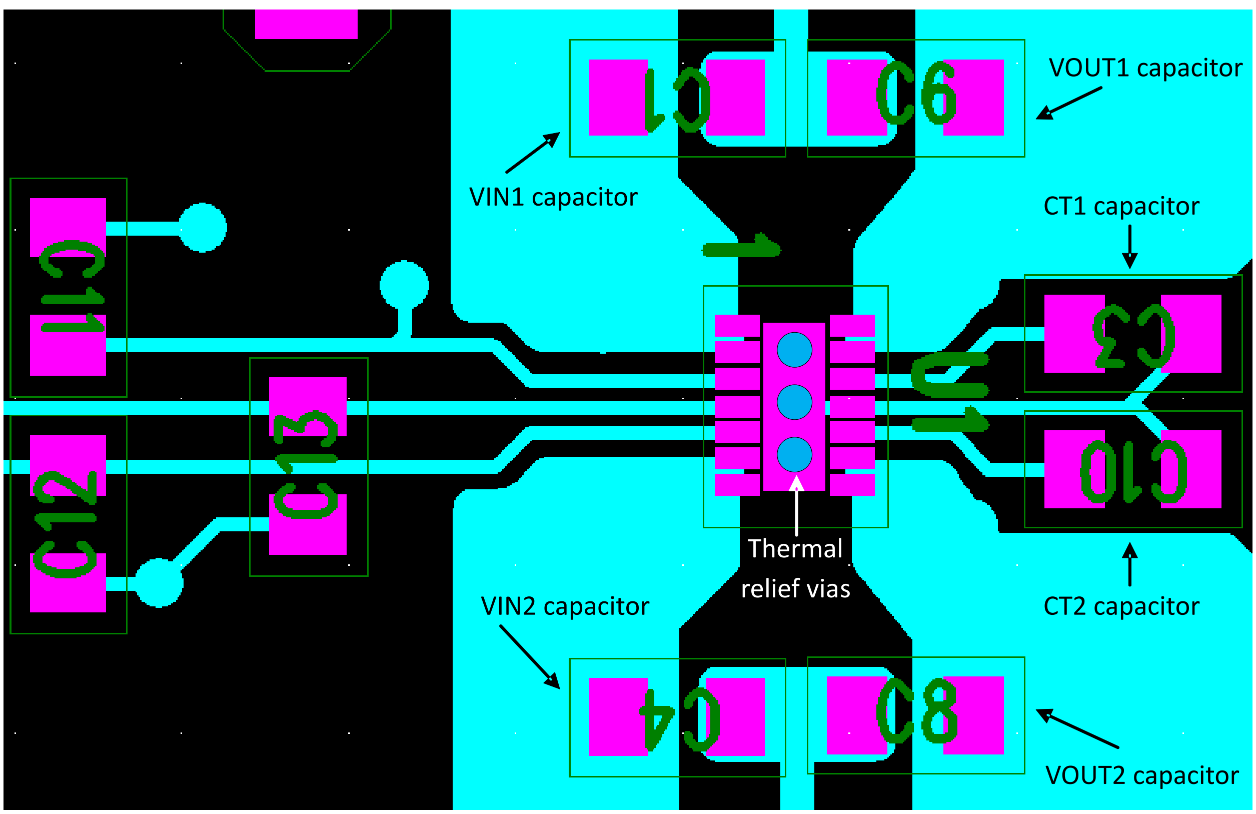
The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable power dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\Theta_{JA}} \quad (2)$$

Where:

$P_{D(max)}$ = maximum allowable power dissipation
$T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22966)
T_A = ambient temperature of the device
Θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

The figure below shows an example of a layout. Notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.



REVISION HISTORY

Changes from Original (June 2012) to Revision A **Page**

- Updated V_{BIAS} vs. QUIESCENT CURRENT (BOTH CHANNELS) Y-axis Units. 8
- Updated V_{BIAS} vs. QUIESCENT CURRENT (SINGLE CHANNEL) Y-axis Units. 8

Changes from Revision A (July 2012) to Revision B **Page**

- Updated Typical Application Schematic 1
- Updated Functional Block Diagram 6

Changes from Revision B (December 2012) to Revision C **Page**

- Added VBIAS to ABSOLUTE MAXIMUM RATINGS table. 2
- Updated SWITCHING CHARACTERISTIC MEASUREMENT INFORMATION. 5
- Updated Test Circuit Diagram. 5
- Updated Functional Block Diagram 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS22966DPUR	ACTIVE	WSON	DPU	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RB966	Samples
TPS22966DPUT	ACTIVE	WSON	DPU	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RB966	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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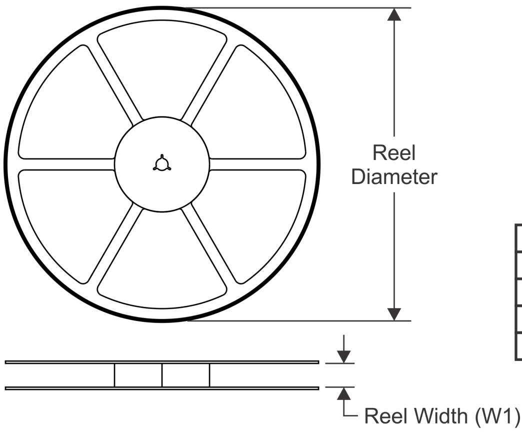
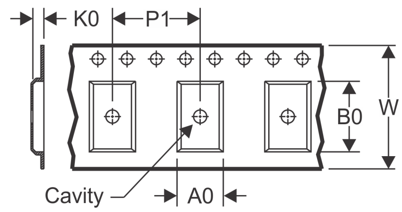
TAPE AND REEL INFORMATION

REEL DIMENSIONS

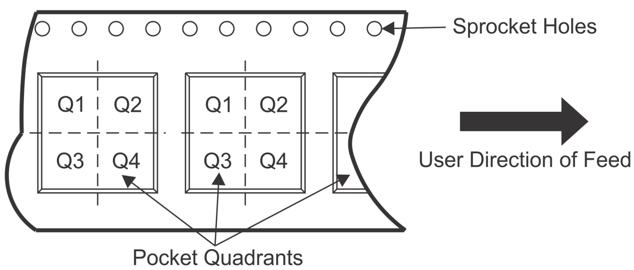


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

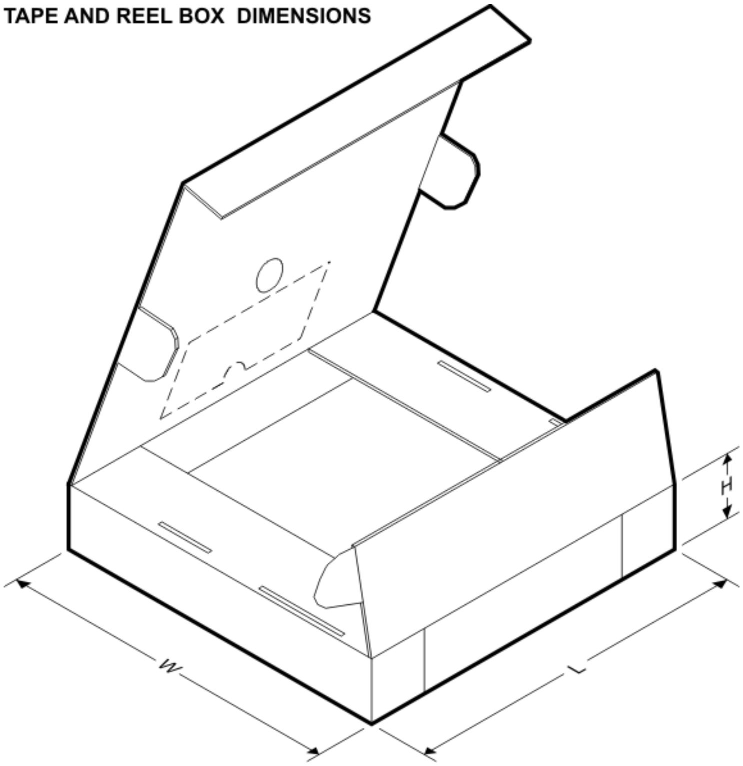
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22966DPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22966DPUT	WSON	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

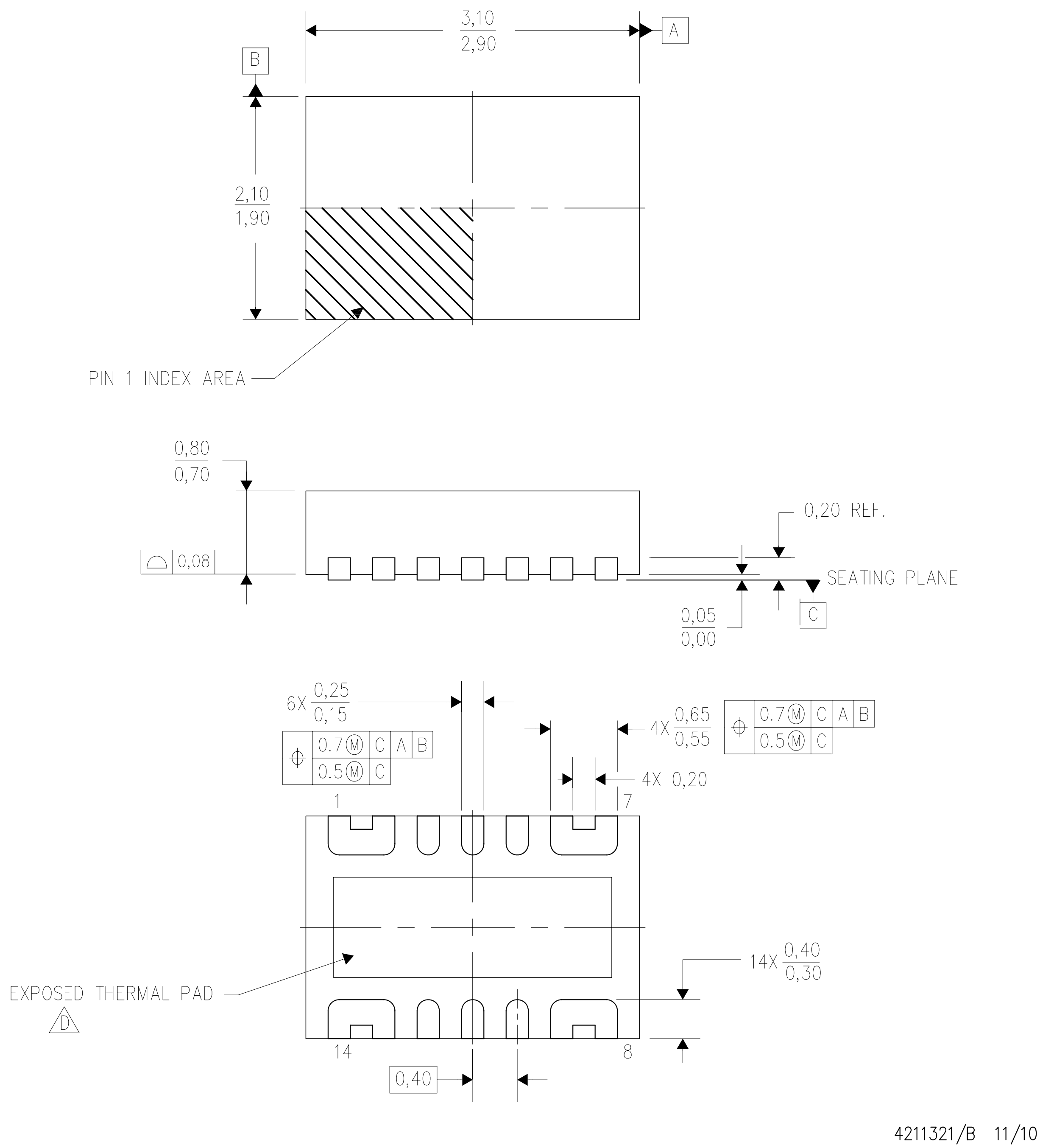
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22966DPUR	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22966DPUT	WSON	DPU	14	250	210.0	185.0	35.0

DPU (R–PWSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. This package is Pb–free.

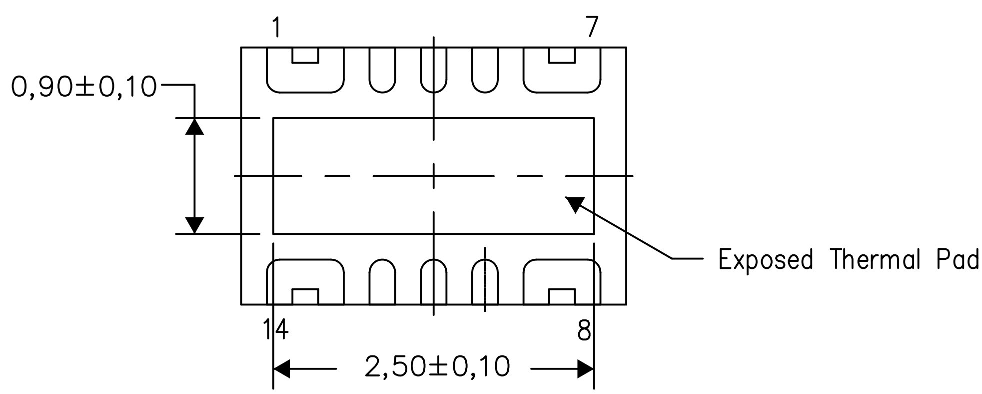
DPU (R-PWSON-N14) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



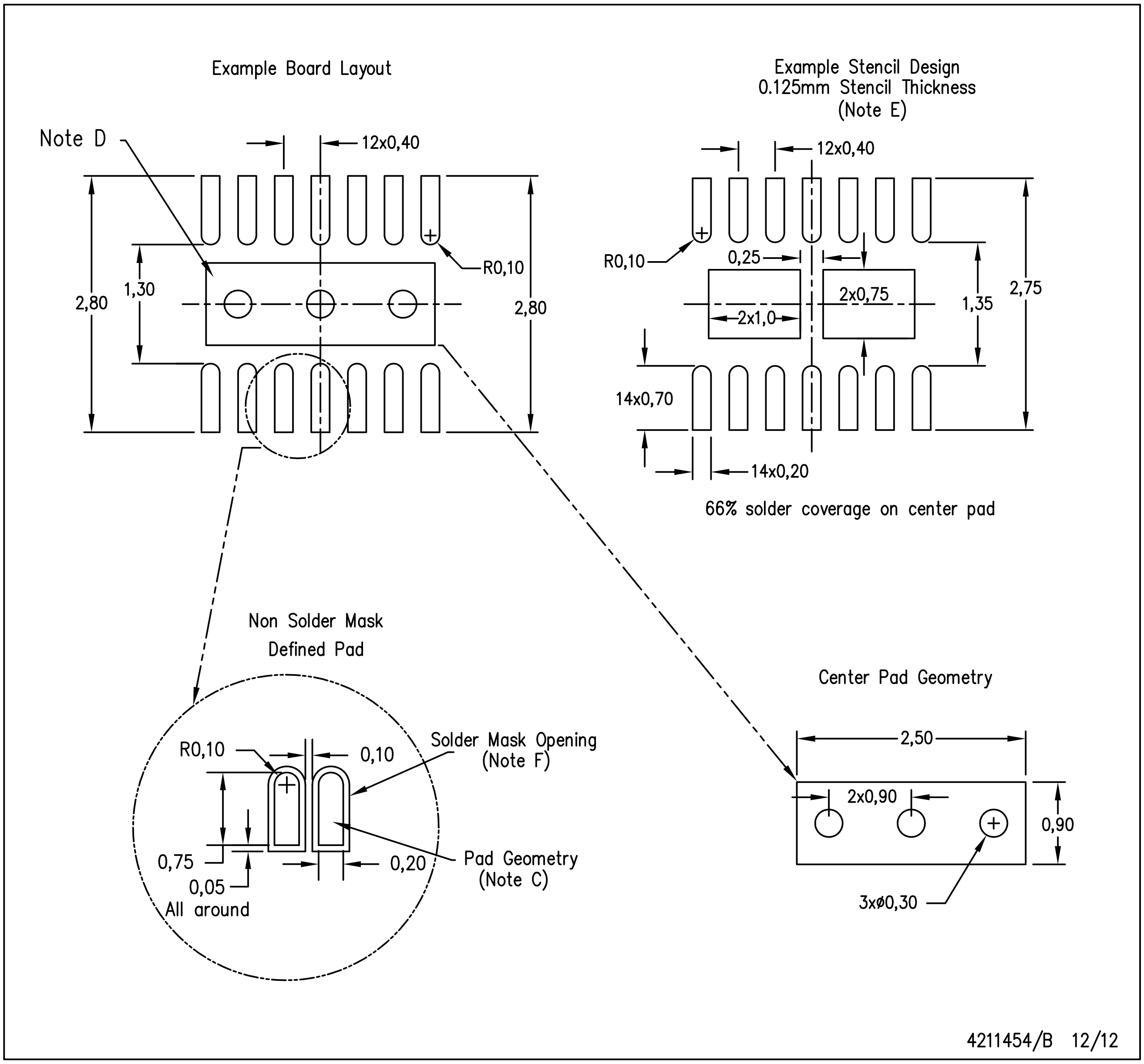
Bottom View

Exposed Thermal Pad Dimensions

4211395/B 12/12

NOTE: All linear dimensions are in millimeters

DPU (R–PWSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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