3-V to 20-V Integrated FET Hot Swap

Check for Samples: TPS2421-1, TPS2421-2

FEATURES

- **Integrated Pass MOSFET**
- **3.3-V to 20-V Bus Operation**
- **Programmable Fault Current**
- **Current Limit Proportionally Larger than Fault Current**
- **Programmable Fault Timer**
- **Internal MOSFET Power Limiting**
- **Latch-Off on Fault (-1) and Retry (-2) Versions**
- **SO-8 PowerPad™ Package**
- **–40°C to 125°C Junction Temperature Range**
- **UL Listed - File Number E169910**

APPLICATIONS

- **RAID Arrays**
- **Telecommunications**
- **Plug-In Circuit Boards**
- **Disk Drive**

DESCRIPTION

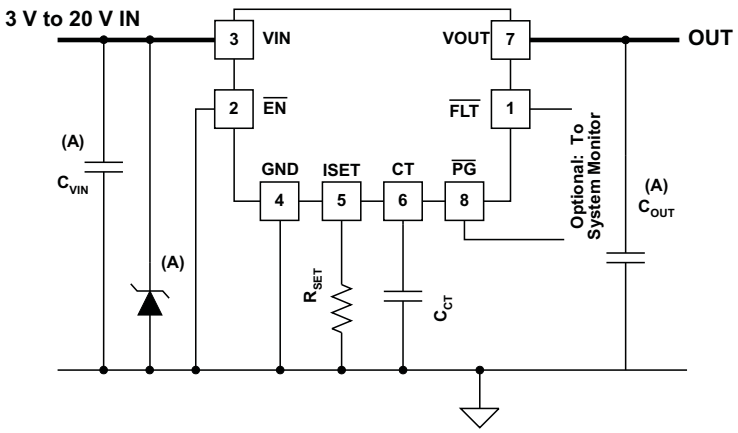
The TPS2421 provides highly integrated hot swap power management and superior protection in applications where the load is powered by voltages between 3 V and 20 V. These devices are very effective in systems where a voltage bus must be protected to prevent shorts from interrupting or damaging the unit. The TPS2421 is an easy to use devices in an 8-pin PowerPad™ SO-8 package.

The TPS2421 has multiple programmable protection features. Load protection is accomplished by a non-current limiting fault threshold, a hard current limit, and a fault timer. The current dual thresholds allow the system to draw short high current pulses, while the fault timer is running, without causing a voltage droop at the load. An example of this is a disk drive startup. This technique is ideal for loads that experience brief high demand, but benefit from protection levels in-line with their average current draw.

Hotswap MOSFET protection is provided by power limit circuitry which protects the internal MOSFET against SOA related failures.

The TPS2421 is available in latch-off on fault (-1) and retry on fault (-2).

Typical Application



A. Required only in systems with lead and/or load inductance.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPad is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PRODUCT INFORMATION(1)

DEVICE	FEATURE	PACKAGE	MARKING
TPS2421-1	Latchoff	DDA (SO8 PowerPad™)	2421-1
TPS2421-2	Auto-retry		2421-2

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

	VALUE	UNIT
Input voltage range, V_{VIN}, V_{VOUT}	–0.3 to 25	V
Voltage range, $\overline{FLT}$, $\overline{PG}$	–0.3 to 20	
Maximum continuous output current, I_{MAX}	9	A
Output sink current, $\overline{FLT}$, $\overline{PG}$	10	mA
Input voltage range, $\overline{EN}$	–0.3 to 6	V
Voltage range, CT,(3) ISET(3)	-0.3 to 3	
ESD rating, HBM	2.5	kV
ESD rating, CDM	400	V
Operating junction temperature range, T_J	Internally Limited	°C
Storage temperature range, T_{stg}	–65 to 150	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Do not apply voltage to these pins.

DISSIPATION RATINGS(1)

PACKAGE	θ_{JA} LOW K, °C/W	θ_{JA} HIGH K, °C/W	θ_{JA} BEST(2), °C/W
DDA	190(3)	45(4)	45

(1) Tested per JEDEC JESD51, natural convection. The definitions of high-k and low-k are per JESD 51-7 and JESD 51-3.
(2) The best case thermal resistance is obtained using the recommendations per SLMA002A (2 signal – 2 plane with the pad connected to the plane).
(3) Low-k (2 signal – no plane, 3 in. by 3 in. board, 0.062 in. thick, 1 oz. copper) test board with the pad soldered, and an additional 0.12 in.2 of top-side copper added to the pad.
(4) High-k is a (2 signal – 2 plane) test board with the pad soldered.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{VIN}, V_{VOUT}	Input voltage range	3		20	V
$\overline{EN}$	Voltage range	0		5	
$\overline{FLT}$, $\overline{PG}$	Voltage range	0		20	
I_{OUT}	Continuous output current	0		6	A
$\overline{FLT}$, $\overline{PG}$	Output sink current	0		1	mA
C_{CT}		0.1			nF
R_{RSET}		49.9		200	kΩ
T_J	Junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: 3 V ≤ V_{VIN} ≤ 18 V, $\overline{EN}$ = 0 V, $\overline{PG}$ = $\overline{FLT}$ = open, R_{OUT} = open, R_{RSET} = 49.9 kΩ, –40°C ≤ T_J ≤ 125°C, No external capacitor connected to VOUT

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	VIN						
	UVLO	VIN rising		2.6	2.85	2.9	V
		Hysteresis			150		mV
	Bias current	$\overline{EN}$ = 2.4V			25	100	µA
		$\overline{EN}$ = 0V			3.9	5	mA
	VIN, VOUT						
	R_{ON}	$R_{VIN-VOUT}$, I_{VOUT} < I_{LIM}, 1 A ≤ I_{VOUT} ≤ 4.5 A			33	50	mΩ
	Power limit TPS242x	V_{VIN}: 12 V, C_{OUT} = 1000 µF $\overline{EN}$: 3 V → 0 V		3	5	7.5	V
	Reverse diode voltage	V_{VOUT} > V_{VIN} , $\overline{EN}$ = 5 V, I_{VIN} = –1 A			0.77	1.0	
	ISET						
I_{SET}	Fault current threshold	I_{VOUT} ↑, I_{CT}: sinking → sourcing, pulsed test					A
		0°C ≤ T_J ≤ 85°C	R_{RSET} = 200 kΩ	0.80		1.2	
			R_{RSET} = 100 kΩ	1.80		2.2	
			R_{RSET} = 49.9 kΩ	3.60		4.40	
		-40°C ≤ T_J ≤ 125°C	R_{RSET} = 200 kΩ	0.75		1.25	
			R_{RSET} = 100 kΩ	1.75		2.25	
			R_{RSET} = 49.9 kΩ	3.60		4.40	
I_{LIM} / I_{SET}	Ratio I_{LIM} / I_{SET}	R_{RSET} = 200 kΩ		1.1	1.8	2.6	–
		R_{RSET} = 100 kΩ		1.1	1.5	2.1	
		R_{RSET} = 49.9 kΩ		1.1	1.4	1.6	
I_{LIM}	Current limit	I_{VOUT} rising, $V_{VIN-VOUT}$ = 0.3 V, pulsed test	R_{RSET} = 200 kΩ	1.1	1.8	2.4	
			R_{RSET} = 100 kΩ	2.3	3.0	3.7	A
			R_{RSET} = 49.9 kΩ	4.6	5.5	6.3	
	CT						
	Charge/discharge current	I_{CT} sourcing, V_{CT} = 1 V, In current limit		29	35	41	µA
		I_{CT} sinking (-2), V_{CT} = 1 V, drive CT to 1 V, measure current		1.0	1.4	1.8	
	Threshold voltage	V_{CT} rising		1.3	1.4	1.5	V
		V_{CT} falling, drive CT to 1 V, measure current		0.1	0.16	0.3	
	ON/OFF fault duty cycle	V_{VOUT} = 0 V		2.8%	3.7%	4.6%	

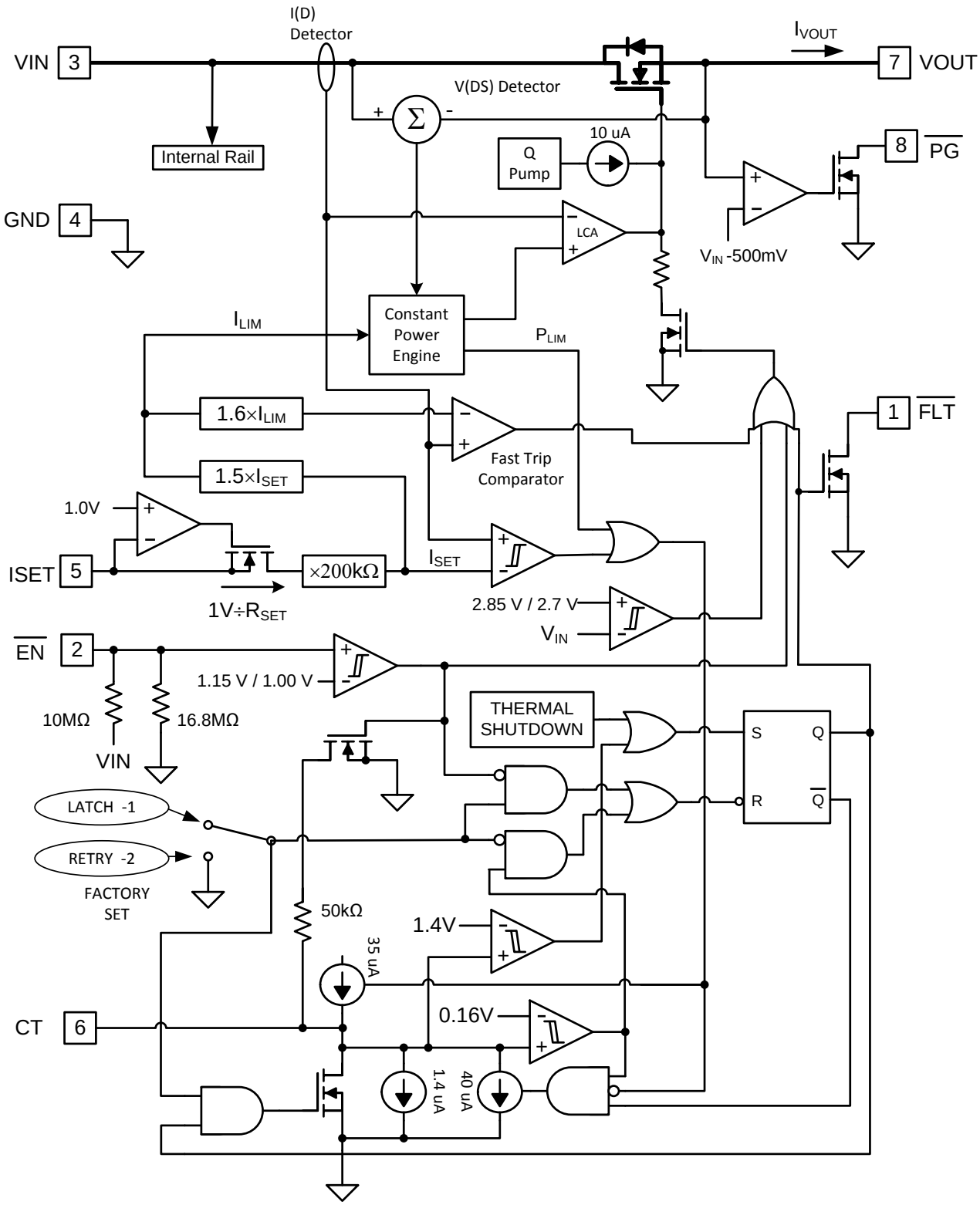
ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted: 3 V ≤ V_{VIN} ≤ 18 V, $\overline{EN}$ = 0 V, $\overline{PG}$ = $\overline{FLT}$ = open, R_{OUT} = open, R_{RSET} = 49.9 kΩ, –40°C ≤ T_J ≤ 125°C, No external capacitor connected to VOUT

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	$\overline{EN}$					
	Threshold voltage	$V_{\overline{EN}}$ falling	0.8	1.0	1.5	V
		Hysteresis	20	150	250	mV
	Input bias current	$V_{\overline{EN}}$ = 2.4 V	–2.0	0	0.5	µA
		$V_{\overline{EN}}$ = 0.2 V	–3.0	1	0.5	
	Turn on propagation delay	V_{VIN} = 3.3 V, I_{LOAD} = 1 A, $V_{\overline{EN}}$: 2.4 V → 0.2 V, V_{VOUT}: rising 90% × V_{VIN}		350	500	µs
	Turn off propagation delay	V_{VIN} = 3.3 V, I_{LOAD} = 1 A, $V_{\overline{EN}}$: 0.2 V → 2.4 V, V_{VOUT}: ↓ 10% × V_{VIN}		30	50	
	$\overline{FLT}$					
V_{OL}	Low level output voltage	V_{CT} = 1.8 V, $I_{\overline{FLT}}$ = 1 mA		0.2	0.4	V
	Leakage current	$V_{\overline{FLT}}$ = 18 V			1	µA
	$\overline{PG}$					
	PG threshold	$V_{(VIN-VOUT)}$ falling	0.4	0.5	0.75	V
		Hysteresis	0.1	0.25	0.4	
V_{OL}	Low level output voltage	$I_{\overline{PG}}$ = 1 mA		0.2	0.4	
	Leakage current	$V_{\overline{PG}}$ = 18 V			1	µA
	Thermal Shutdown					
	Thermal shutdown	Junction temperature rising		160		°C
		Hysteresis		10		

BLOCK DIAGRAM

Block Diagram



PINOUT DIAGRAM

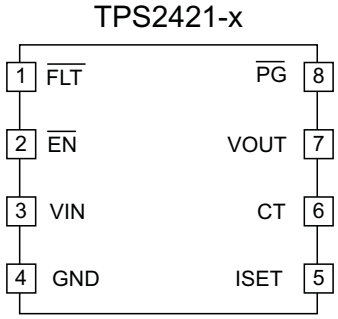


Table 1. TERMINAL FUNCTIONS

FUNCTION	PIN NO.	DESCRIPTION
$\overline{FLT}$	1	Fault low indicated the fault time has expired and the FET is switched off
$\overline{EN}$	2	Device is enabled when this pin is pulled low
VIN	3	Power In and control supply voltage
GND	4	GND
ISET	5	A resistor to ground sets the fault current, the current limit is 125% of the fault current. TPS2421 only
CT	6	A capacitor to ground sets the fault time
VOUT	7	Output to the load
$\overline{PG}$	8	Power Good low represents the output voltage is within 300 mV of the input voltage

PIN DESCRIPTION

CT: Connect a capacitor from CT to GND to set the fault time. The fault timer starts when I_{VOUT} exceeds I_{SET} or when SOA protection mode is active, charging the capacitor with 35 µA from GND towards an upper threshold of 1.4 V. If the capacitor reaches the upper threshold, the internal pass MOSFET is turned off. For TPS2421-1, the MOSFET will remain off until $\overline{EN}$ is cycled. For TPS2421-2, the capacitor will discharge at 1.4 µA to 0.16 V and then re-enable the pass MOSFET. If the upper threshold is not crossed, the capacitor will discharge at 40 µA to 0.16 V and then to 0 V at 1.4 µA. When the device is disabled, CT is pulled to GND through a 50-kΩ resistor.

The timer period must be chosen long enough to allow the external load capacitance to charge. The nominal (not including component tolerances) fault timer period is selected using Equation 1 where T_{FAULT} is the minimum timer period in seconds and C_{CT} is in Farads.

$$C_{CT} = \frac{T_{FAULT}}{40 \text{ x } 10^3} \tag{1}$$

For TPS2421-2, the second and subsequent retry timer periods will be slightly shorter than the first retry period. CT nominal (not including component tolerances) discharge time, t_{SD} from 1.4 V to 0.16 V is shown in Equation 2, where C_{CT} is in Farads and t_{SD} is in seconds.

$$T_{SD} = 885.7 \times 10^3 \times C_{CT} \tag{2}$$

The nominal ratio of on to off times represents about a 3.7% duty cycle when a hard fault is present on the output.

$\overline{FLT}$: Open-drain output that pulls low on any condition that causes the output to open. These conditions are either an overload with a fault time-out, or a thermal shutdown. $\overline{FLT}$ becomes operational before UV, when V_{VIN} is greater than 1 V. $\overline{FLT}$ will pulse low momentarily prior to the onset of V_{VOUT} ramp up during IN or $\overline{EN}$ based start up.

GND: This is the most negative voltage in the circuit and is used as reference for all voltage measurements unless otherwise specified.

ISET: A resistor from this pin to GND sets both the fault current (I_{SET}) and current limit (I_{LIM}) levels. The current limit is internally set at 150% of the fault current. The fault timer described in the CT section starts when I_{VOUT} exceeds I_{SET}.

The internal MOSFET actively limits current if I_{VIN} reaches the current limit set point. The fault timer operation is the same in this mode as described previously.

The fault current value is programmed as shown in Equation 3:

$$R_{RSET} = \frac{200\,k\Omega}{I_{SET}} \quad (3)$$

$\overline{EN}$: When this pin is pulled low, the device is enabled. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit. $\overline{EN}$ is pulled to VIN with a 10-MΩ resistor and to GND with a 16.8 MΩ resistor. Because high impedance pullup/down resistors are used to reduce current draw, any external FET controlling this pin should be low leakage.

VIN: Input voltage to the TPS2421. The recommended operating voltage range is 3 V to 20 V. Connect VIN to the power source.

VOUT: Output connection for the TPS2421. V_{VOUT} in the ON condition considering the ON resistance of the internal MOSFET, R_{ON} is shown in Equation 4:

$$V_{VOUT} = V_{VIN} - R_{ON} \times I_{VOUT} \quad (4)$$

Connect VOUT to the load.

$\overline{PG}$: Active low, Open Drain output, Power Good indicates that there is no fault condition and the output voltage is within 0.5 V of the input voltage. $\overline{PG}$ becomes operational before UV, whenever V_{VIN} is greater than 1 V.

TYPICAL CHARACTERISTICS

FAULT CURRENT vs JUNCTION TEMPERATURE

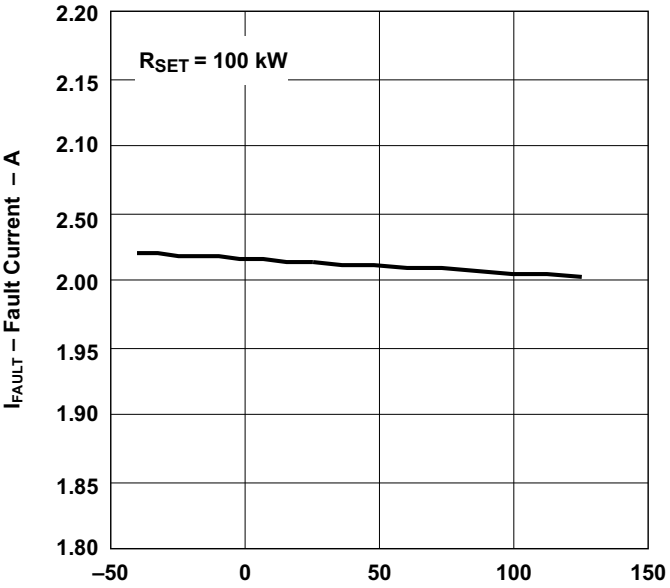


Figure 1.

FAULT TIMER THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

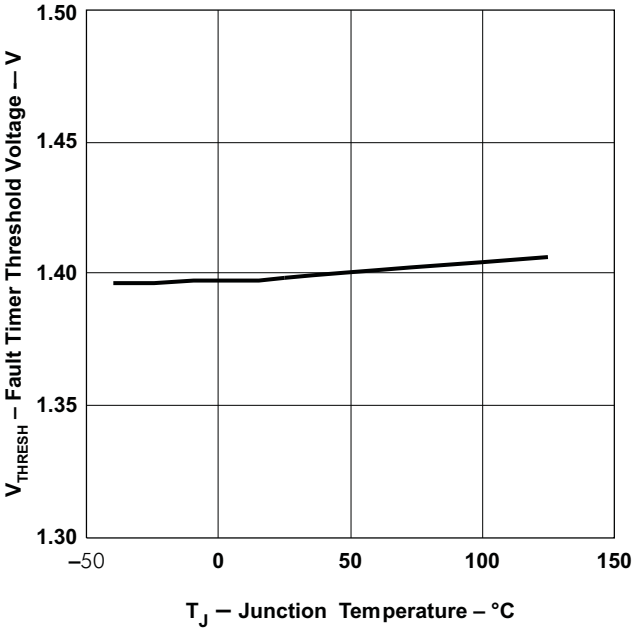


Figure 2.

POWER LIMIT vs JUNCTION TEMPERATURE

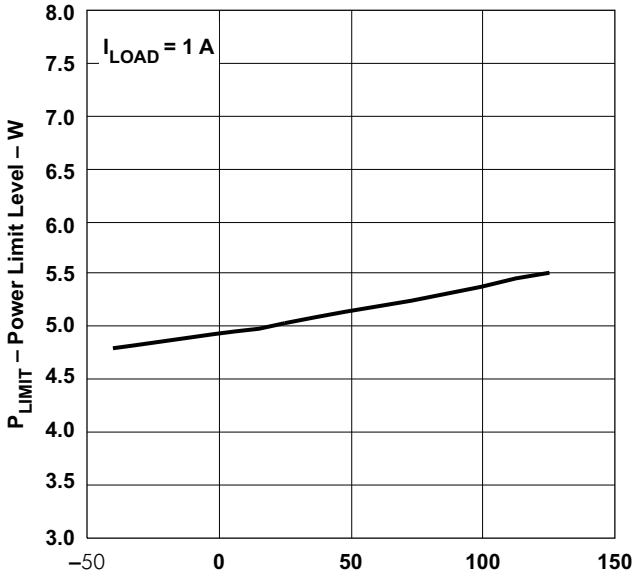


Figure 3.

SUPPLY CURRENT vs JUNCTION TEMPERATURE

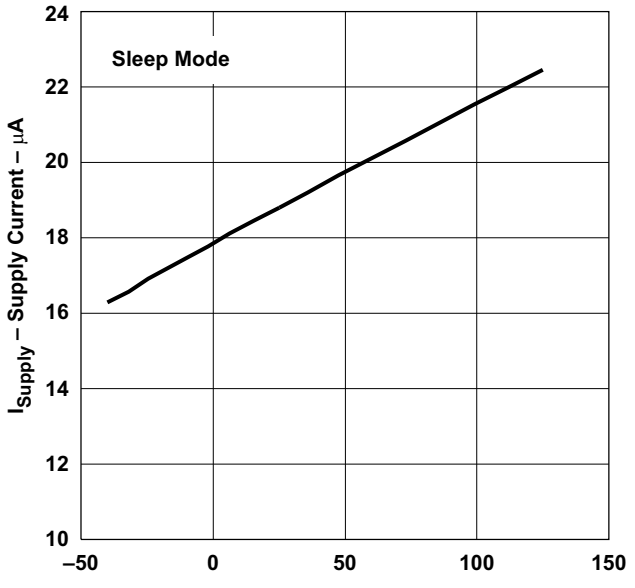


Figure 4.

TYPICAL CHARACTERISTICS (continued)

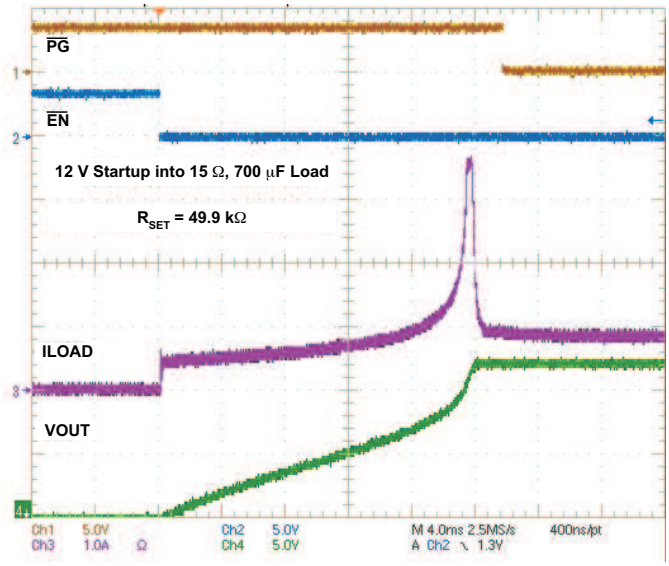


Figure 5. 12-V Startup Into 15 Ω, 700 µF Load

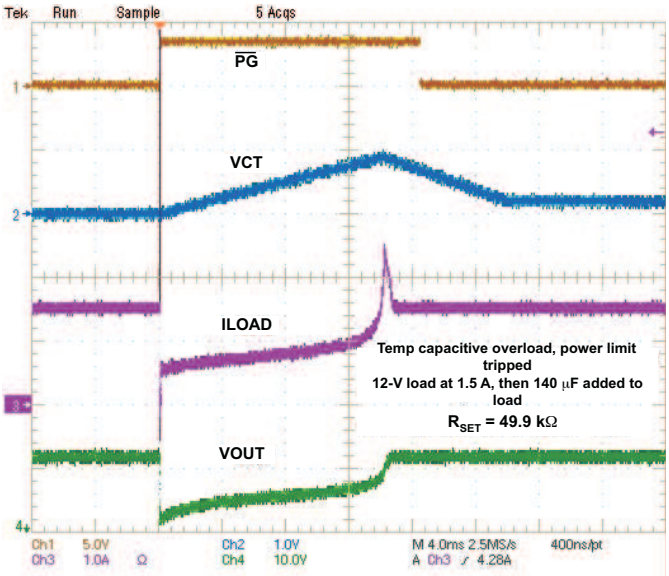


Figure 6. 12-V, 140 µF Added to 8 Ω Load

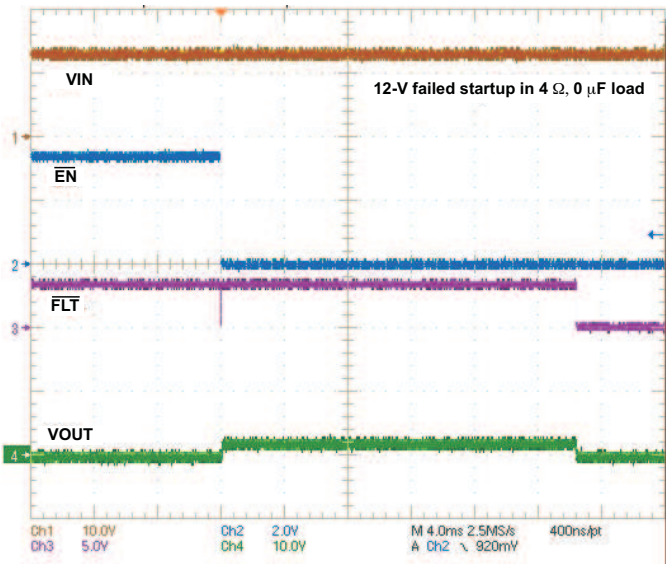


Figure 7. 12-V Faulted Startup Into 4 Ω Load

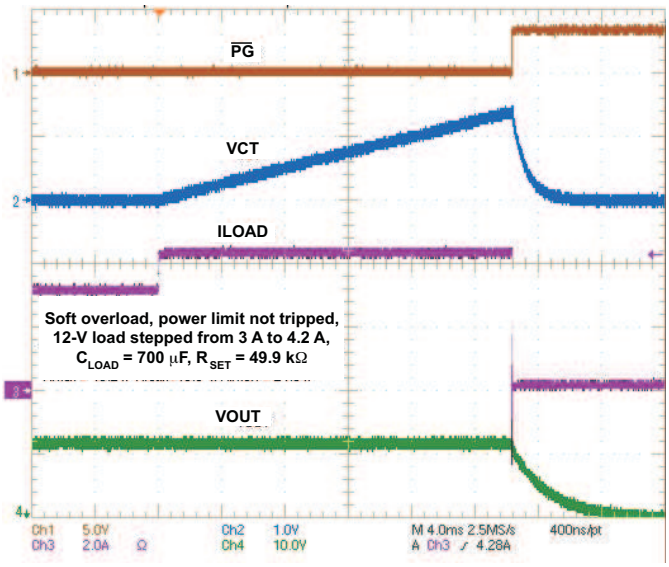


Figure 8. 12-V Soft Overload, 3 A to 4.2 A, Power Limit Not Tripped

TYPICAL CHARACTERISTICS (continued)

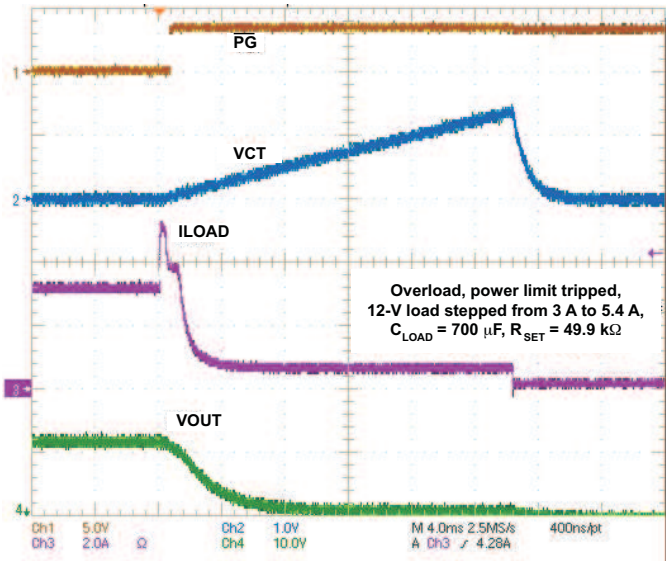


Figure 9. 12-V Firm Overload, 3 A to 5.4 A, Power Limit Tripped

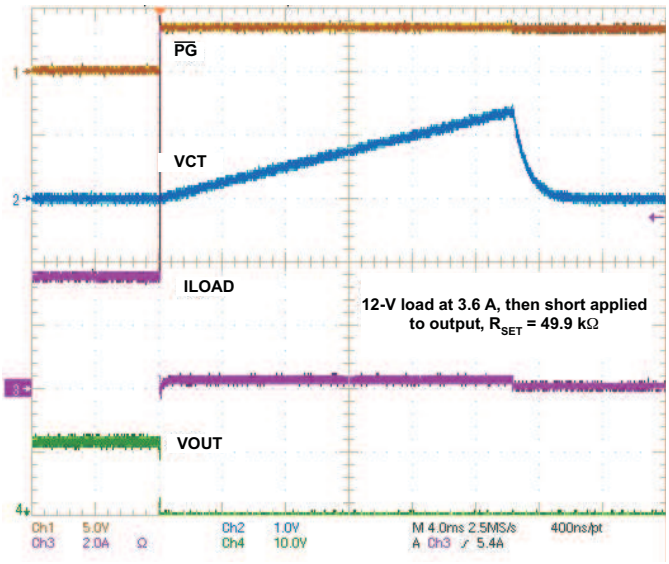


Figure 10. 12-V Hard Overload, 3.6-A Load Then Short

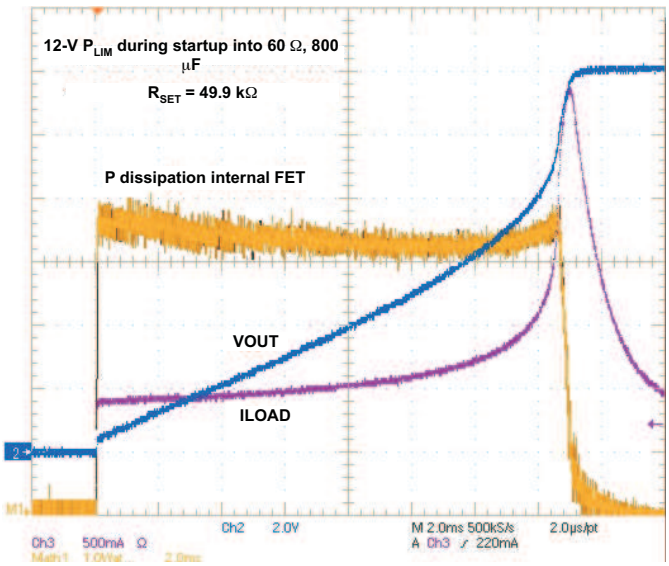


Figure 11. Power Dissipation During 12-V Startup into 60 Ω, 800 µF

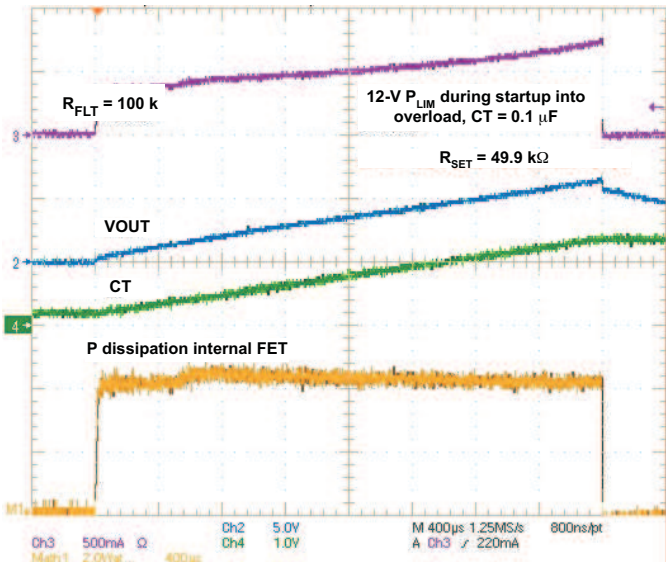


Figure 12. Power Dissipation During 12-V Startup into 15 Ω, 140 µF

TYPICAL CHARACTERISTICS (continued)

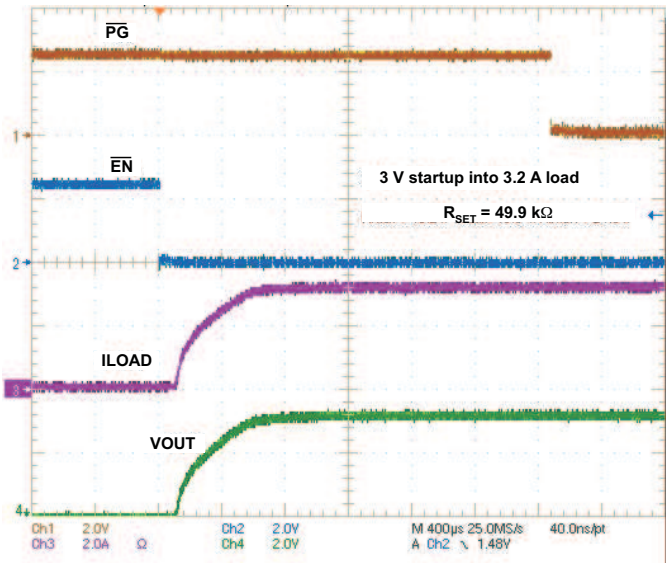


Figure 13. 3-V Startup into 1-Ω Load

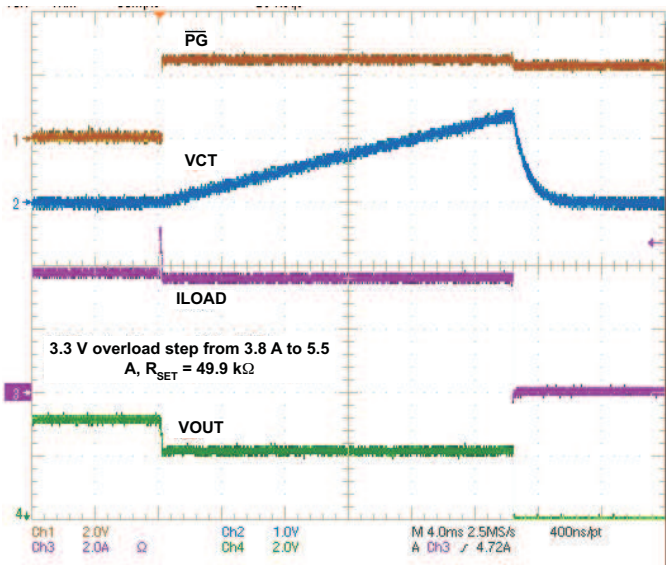


Figure 14. 3-V Firm Overload, Load Stepped From 3.8 A to 5.5 A

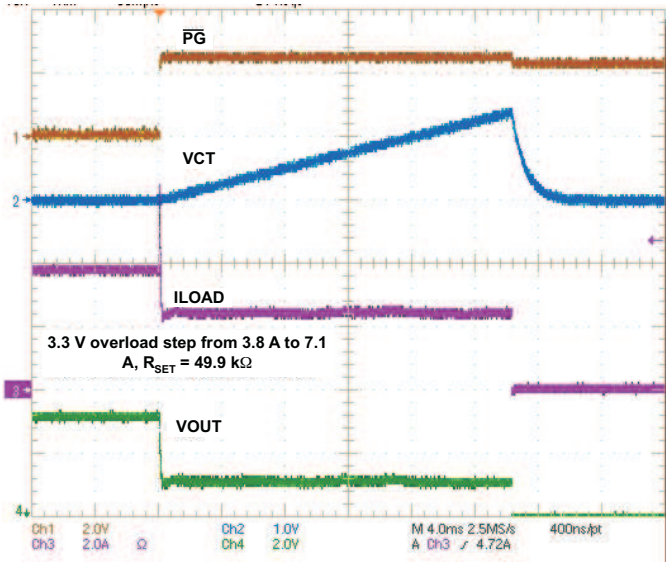


Figure 15. 3-V Hard Overload, Load Stepped From 3.8 A to 7.1 A

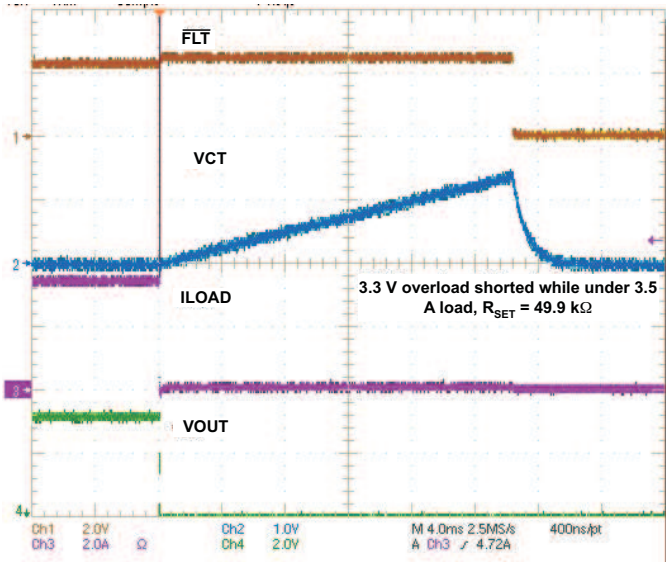


Figure 16. 3-V Output Shorted While Under 3.5-A Load

TYPICAL CHARACTERISTICS (continued)

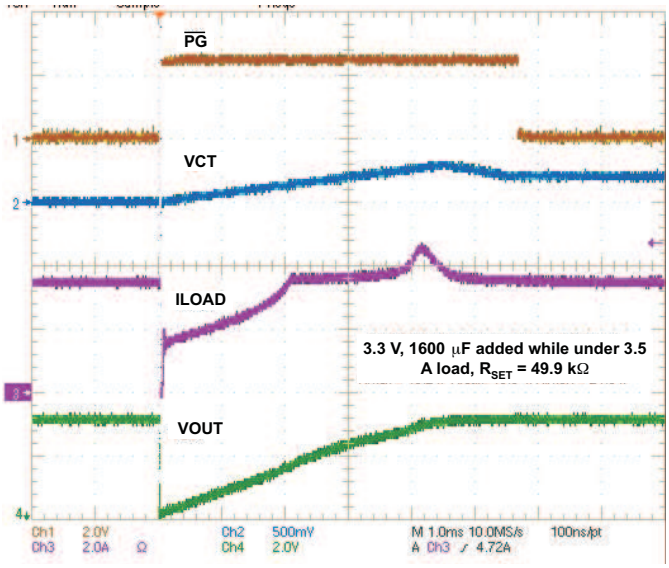


Figure 17. 3 V, 1600 µF Added To 3.5-A Load

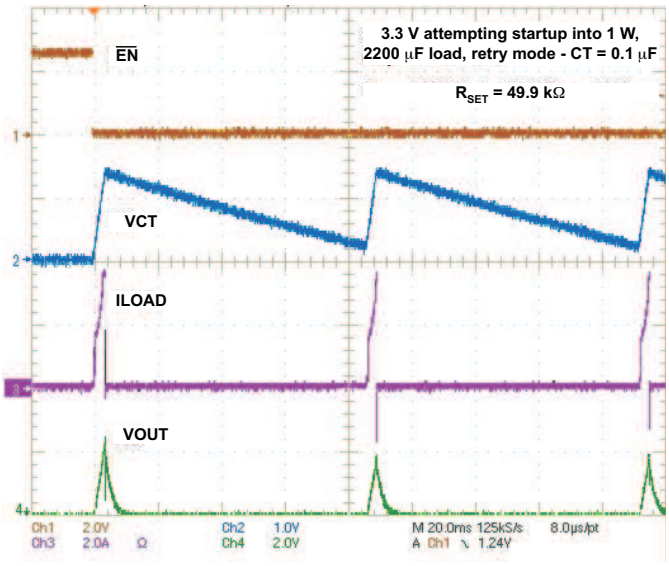


Figure 18. 3-V Retry Startup into 1 Ω, 2200-µF Load

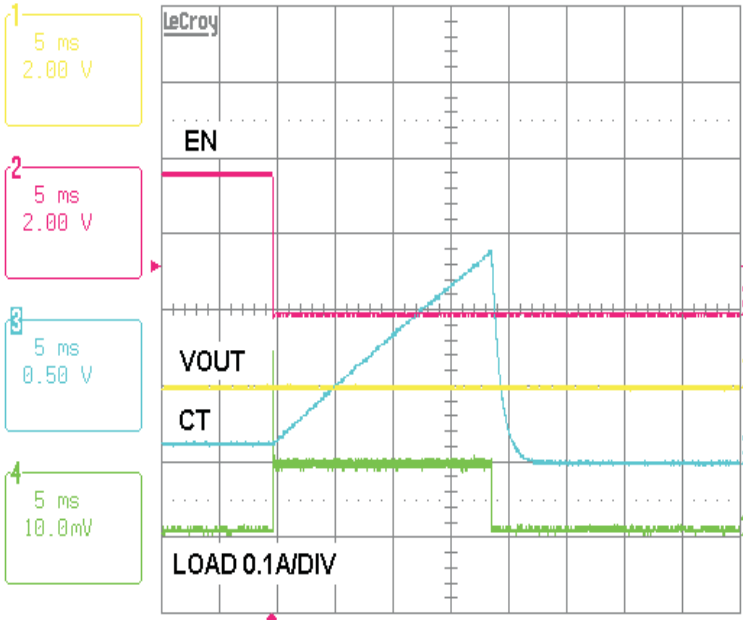


Figure 19. Startup Into a Short Circuit Output

APPLICATION INFORMATION

Startup

Large inrush current occurs when power is applied to discharged capacitors and load. During the inrush period, the TPS2421 operates in power limit (or SOA protect mode) managing the current as V_{VOUT} rises. In SOA protect mode, the internal MOSFET power dissipation ($[V_{VIN} – V_{VOUT}] \times I_{VOUT}$) is regulated at 5W typical while the fault timer starts and C_{CT} ramps up. As the charge builds on C_{LOAD}, the current increases towards I_{LIM}. When the capacitor is fully charged, I_{VOUT} drops to the dc load value, the fault timer stops, and C_{CT} ramps down. In order for the TPS2421 to start properly, the fault timer duration must exceed C_{OUT} start up time, t_{ON}. Start up time without additional dc loading can be determined using Equation 5 where P_{LIM} = 5W (typical).

$$t_{ON} = \frac{C_{OUT} \times P_{LIM}}{2 \times I_{LIM}^2} + \frac{C_{OUT} \times V_{VIN}^2}{2 \times P_{LIM}} \quad (5)$$

When the load has a resistive component in addition to C_{OUT}, the fault time must be extended because the resistive load current is unavailable to charge C_{OUT}. Table 2 and Table 3 can be used to predict start up time in the presence of resistive dc loading.

Refer to the TPS2421 Design Calculator Tool (SLUC427) for assistance with design calculations.

Table 2. Start up Time (ms) with DC Loading: V_{IN}=5V, P_{LIM}=3W, I_{LIM}=5A

R_{LOAD} (Ω)	C_{LOAD} = 100 µF	C_{LOAD} = 220 µF	C_{LOAD} = 470 µF	C_{LOAD} = 1000 µF
1000	0.43	0.95	2.03	4.33
10	0.5	1.11	2.36	5.03
5	0.61	1.34	2.87	6.1
3	0.91	2	4.28	9.11
2.5	1.31	2.88	6.14	13.07

Table 3. Start up Time (ms) with DC Loading: V_{IN}=12V, P_{LIM}=3W, I_{LIM}=5A

R_{LOAD} (Ω)	C_{LOAD} = 100 µF	C_{LOAD} = 220 µF	C_{LOAD} = 470 µF	C_{LOAD} = 1000 µF
10000	2.46	5.41	11.56	24.59
100	2.67	5.87	12.55	26.69
50	2.93	6.45	13.79	29.34
15	6.7	14.74	31.5	67.01
13	11.68	25.69	54.87	116.75

Maximum Allowable Load to Ensure Successful Start up

The power limiting function of the TPS2421 provides very effective protection for the internal FET. Expectedly, there is a supply voltage dependent maximum allowable load required for successful startup. Loads above this can cause the output to shut off due to CT timeout or thermal shutdown because V_{VOUT} hangs at an intermediate voltage below V_{IN}. The equation for maximum load (or R_{MIN} is derived using the circuit equations for V_{VOUT} as a function of V_{VIN}, R_{LOAD}, P_{LIM}, and the result is quadratic in form.

$$R_{MIN} \times I^2 - V_{IN} \times I + P_{LIM\_MIN} = 0 \quad (6)$$

$$I = \frac{V_{IN} \pm \sqrt{V_{IN}^2 - 4 \times R_{MIN} \times P_{LIM\_MIN}}}{2 \times R_{MIN}} \quad (7)$$

$$R_{MIN} \times I = V_{VOUT} = \frac{V_{VIN} \pm \sqrt{V_{VIN}^2 - 4 \times R_{MIN} \times P_{LIM\_MIN}}}{2} \quad (8)$$

When $R_{LOAD} < R_{MIN}$, the numerical result for V_{VOUT} is real ($V_{VIN}^2 – 4 \times R_{LOAD} \times P_{LIM} > 0$) and less than V_{VIN} meaning the circuit will not start (CT or thermal shutdown). When $R_{LOAD} > R_{MIN}$, the numerical result for V_{VOUT} is imaginary ($V_{VIN}^2 – 4 \times R_{LOAD} \times P_{LIM} < 0$) and the circuit will start ($V_{VOUT} = V_{VIN}$). Ensure that R_{LOAD} is > R_{MIN} per Equation 10.

$$4 \times R_{MIN} \times P_{LIM\_MIN} > V_{VIN}^2 \quad (9)$$

$$R_{LOAD} > R_{MIN} = \frac{V_{VIN}^2}{4 \times P_{LIM\_MIN}} \quad (10)$$

Enable Pin Considerations

For the case when $\overline{EN}$ is simply connected to GND, TPS2421 will start ramping the voltage on VOUT as VIN rises above UVLO (~2.85V typical). If IN does not ramp monotonically, the TPS2421 may momentarily turn off then on during startup if IN falls below ~2.70V. To avoid this problem, $\overline{EN}$ assertion can be delayed until IN is sufficiently above UVLO. A simple approach is shown in Figure 20. The 100kΩ pullup resistor will de-assert $\overline{EN}$ when VIN is above ~1.75V maximum which is well below the minimum UVLO of ~2.6V. The Zener diode ensures that $\overline{EN}$ remains below 5V. User control to enable the TPS2421 can be applied at the ON node to turn on the FET once IN has risen sufficiently above UVLO.

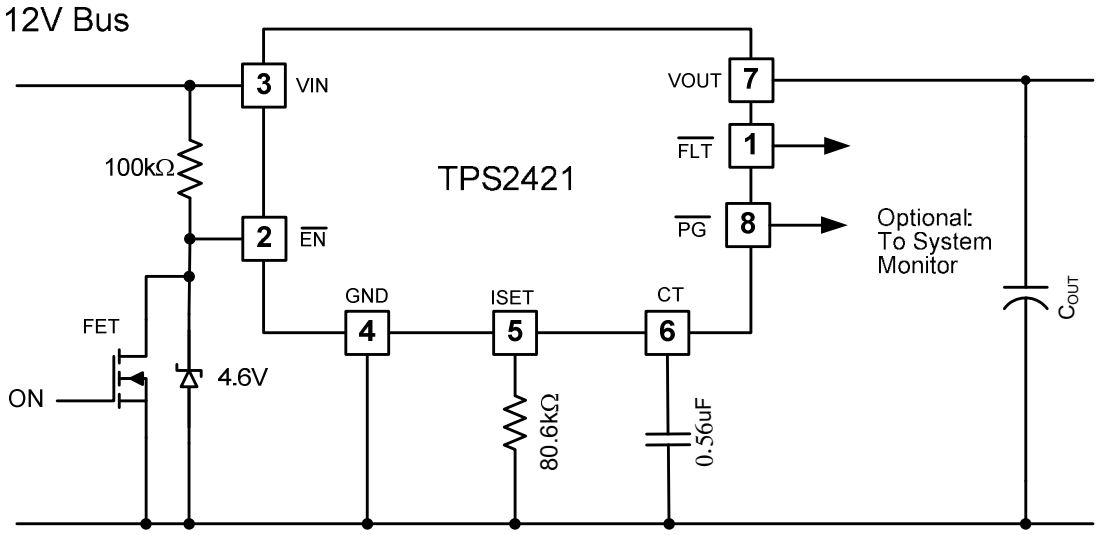


Figure 20. EN Delay Circuit

Fault Timer

The fault timer is active when the TPS2421 is in SOA protect mode or the current is above I_{SET}. Figure 21 illustrates operation during non-faulted start up (C_{OUT} =470 µF and I_{VOUT} = 1A in a 12V system). C_{CT} charges at ~35µA until TPS2421 exits SOA protect mode, discharges quickly (~40µA) to ~0.16V, and then decays slowly (~1.4µA) towards zero.

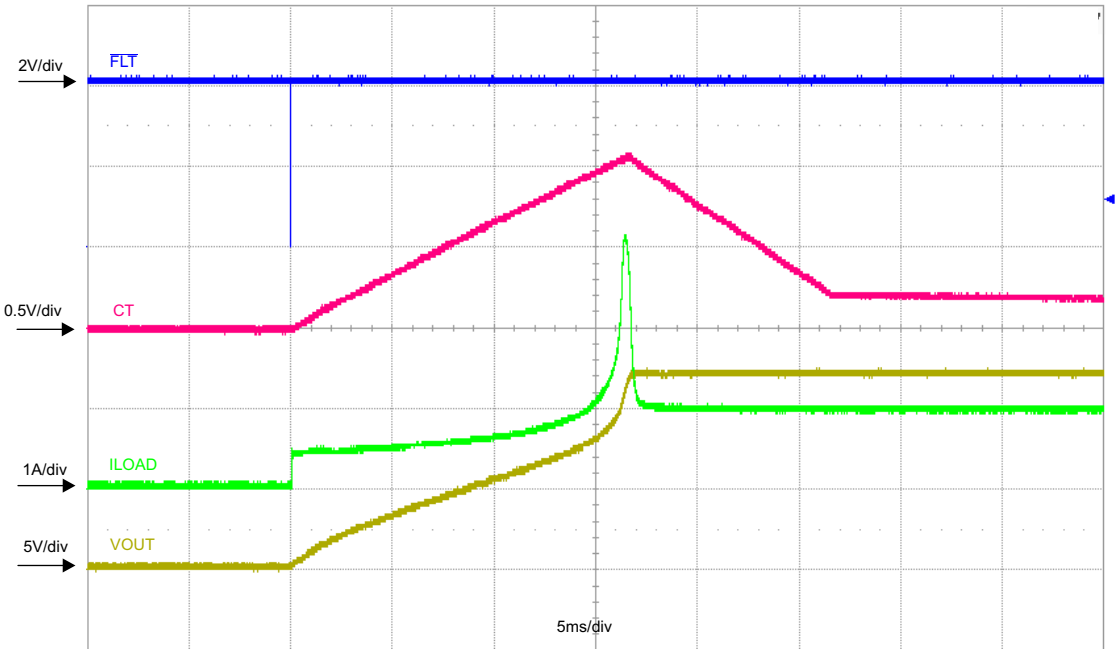


Figure 21. Fault Timer Operation During Start up

C_{CT} can be chosen for fault-free start up including expected C_{OUT} and C_{CT} capacitance tolerance as shown in Equation 11.

$$C_{CT} = \frac{(1 + C_{OUT\_TOL} + C_{CT\_TOL}) \times t_{ON}}{40000} \quad (11)$$

Normal Operation

When load current exceeds I_{SET} during normal operation the fault timer starts. If load current drops below I_{SET} before the fault timer expires, normal operation continues. If load current stays above the I_{SET} threshold the fault timer expires and a fault is declared. When a fault is declared a TPS2421-1 device turns off an can be restarted by cycling power or toggling the $\overline{EN}$ signal. A TPS2421-2 device attempts to turn on at a 3.7% duty cycle until the fault is cleared. When I_{LIM} is reached during a fault the device goes into current limit and the fault timer keeps running.

Start up into a Short

The controller attempts to power on into a short for the duration of the timer. Figure 19 shows a small current resulting from power limiting the internal MOSFET. This happens only once for TPS2421-1. For TPS2421-2, the cycle repeats at a 3.7% duty cycle as shown in Figure 18.

Shutdown Modes

Hard Overload - Fast Trip

When a hard overload causes the load current to exceed ~1.6 × I_{LIM} the TPS2421 immediately shuts off current to the load without waiting for the fault timer to expire. After such a shutoff the TPS2421 enters startup mode and attempts to apply power to the load. If the hard overload was caused by a transient, then normal startup can be expected. If the hard overload is caused by a persistent, continuous failure then the TPS2421 goes into current limit during the restart attempt and either latches off (TPS2421-1) or attempts retry (TPS2421-2).

Overcurrent Shutdown

Overcurrent shutdown occurs when the output current exceeds I_{SET} for the duration of the fault timer. Figure 8 shows a step rise in output current which exceeds the I_{SET} threshold but not the I_{LIM} threshold. The increased current is on for the duration of the timer. When the timer expires, the output is turned off.

Programming the Fault (I_{SET}) and Current-limit (I_{LIM}) Thresholds

The I_{SET} and I_{LIM} thresholds is user programmable with a single external resistor connected to ISET and the I_{LIM} threshold is internally set according to the I_{LIM}/I_{SET} ratio specified in the electrical characteristics table. The TPS2421 uses an internal regulation loop to provide a regulated voltage on the ISET pin. The fault and current-limit thresholds are proportional to the current sourced out of ISET. The recommended 1% resistor range is 49.9kΩ ≤ R_{RSET} ≤ 200kΩ to ensure the rated accuracy. Many applications require that minimum fault and current limits are known or that maximum current limit is bounded. It is important to consider the tolerance of the fault and current limit thresholds, as well as R_{RSET} when selecting values. Consult the Electrical Characteristics table for specific fault and current limit settings.

Using the data for I_{SET} and I_{LIM} from the Electrical Characteristics table, equations can be generated and used for other set points. Equation 12 and Equation 13 are used to calculate minimum and maximum I_{SET} where $R_{RSET,max}$ and $R_{RSET,min}$ include R_{RSET} tolerances. Equation 14 and Equation 15 calculate $R_{RSET,max}$ and $R_{RSET,min}$ where R_{TOL} is the 1% resistor tolerance.

$$I_{SET,min} = \frac{185.58}{R_{RSET,max}} - 0.13 \quad (12)$$

$$I_{SET,max} = \frac{213.68}{R_{RSET,min}} + 0.13 \quad (13)$$

$$R_{RSET,min} = \left(1 + R_{TOL}\right) \times \frac{213.68}{I_{SET,max} - 0.13} \quad (14)$$

$$R_{RSET,max} = \left(1 - R_{TOL}\right) \times \frac{185.58}{I_{SET,min} + 0.13} \quad (15)$$

Equation 16 and Equation 17 are used to calculate minimum and maximum I_{LIM} where $R_{RSET,max}$ and $R_{RSET,min}$ include R_{RSET} tolerances.

$$I_{LIM,min} = \frac{232.19}{R_{RSET,max}} - 0.06 \quad (16)$$

$$I_{LIM,max} = \frac{259.26}{R_{RSET,min}} + 1.11 \quad (17)$$

Design Example

A typical design is shown in Figure 22 with the following requirements:

- Nominal input voltage, V_{VIN}: 12V
- Maximum expected load current, I_{VOUT}: 2.1A
- Load capacitance, C_{OUT}: 220uF
- Expected resistive load, R_{LOAD} during start up: 15Ω
- Example calculations are shown in the TPS2421 Design Calculator Tool (SLUC427).

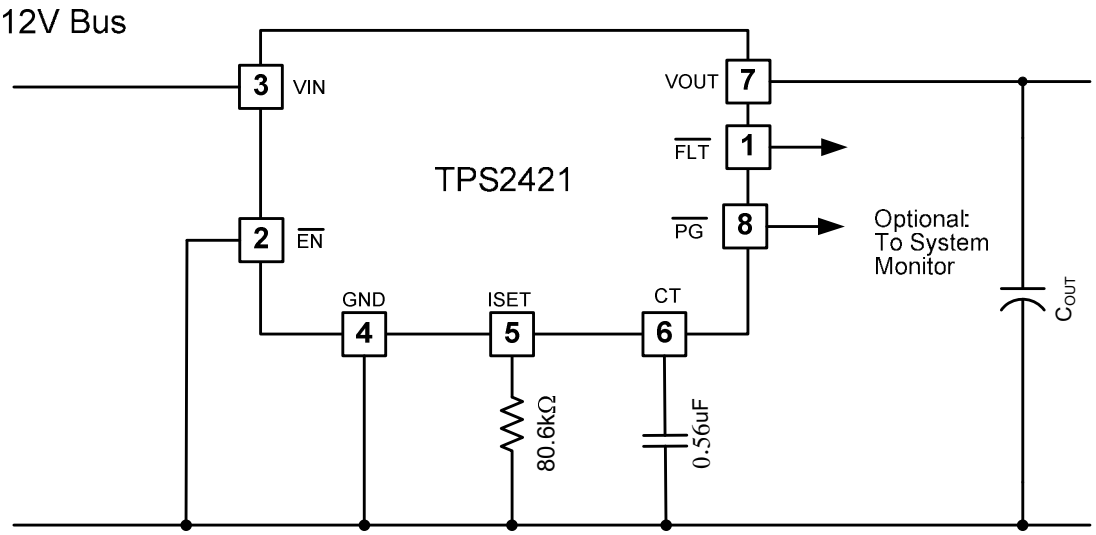


Figure 22. Design Example Schematic

1. Calculate maximum R_{RSET} to ensure that minimum I_{SET} is above maximum operating load current using Equation 15 as shown below in Equation 18.

$$R_{RSET,max} = 0.99 \times \frac{185.58}{2.1 + 0.13} = 82.39k\Omega \quad (18)$$

   - Choose a standard 1% value below $R_{RSET,max}$ for R_{RSET} = 80.6kΩ
   - $I_{SET,min}$ = 2.15A using Equation 12 and will meet the maximum operating current requirement of 2.1A without starting the fault timer during maximum steady state operation for R_{RSET} = 80.6kΩ, 1%.
   - $I_{SET,max}$ = 4.359A using Equation 13 for R_{RSET} = 80.6Ω, 1%.
2. Calculate minimum and maximum I_{LIM}.
   - $I_{LIM,min}$ = 2.792A and $I_{LIM,max}$ = 4.359A using Equation 16 and Equation 17 for R_{RSET} = 80.6kΩ, 1%.
3. Minimum R_{LOAD} at start up using Equation 10 is 12Ω. Since R_{LOAD} = 15Ω is present during circuit start up, use t_{ON} = 15ms from Table 3 for C_{OUT} = 220µF and R_{LOAD} = 15Ω.
   - Calculate C_{CT} = 0.48µF including C_{OUT} and C_{CT} tolerances (C_{OUT_TOL} = 20% and C_{CT_TOL} = 10%) using Equation 19.

$$C_{CT} = \frac{(1 + C_{OUT\_TOL} + C_{T\_TOL}) \times t_{ON}}{40000} = \frac{(1 + 0.2 + 0.1) \times 0.012}{40000} = 0.48\mu F \quad (19)$$

Transient Protection

The need for transient protection in conjunction with hot-swap controllers should always be considered. When the TPS2421 interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. Such transients can easily exceed twice the supply voltage if steps are not taken to address the issue. Typical methods for addressing transients include;

- Minimizing lead length/inductance into and out of the device
- Voltage Suppressors (TVS) on the input to absorb inductive spikes
- Shottky diode across the output to absorb negative spikes
- A combination of ceramic and electrolytic capacitors on the input and output to absorb energy
- Use PCB GND planes

The following equation estimates the magnitude of these voltage spikes:

$$V_{SPIKE(absolute)} = V_{NOM} + I_{LOAD} \times \sqrt{L/C} \quad (20)$$

where

V_{NOM} is the nominal supply voltage
I_{LOAD} is the load current
C is the capacitance present at the input or output of the TPS2421
L equals the effective inductance seen looking into the source or the load

Calculating the inductance due to a straight length of wire is shown in Equation 21.

$$L_{straightwire} \approx 0.2 \times L \times \ln\left(\frac{4 \times L}{D} - 0.75\right) (nH) \quad (21)$$

Where

L is the length of the wire
D is diameter of the wire

Some applications may require the addition of a TVS to prevent transients from exceeding the absolute ratings if sufficient capacitance cannot be included.

Layout

Support Components

Locate all TPS2421 support components, R_{RSET}, C_{CT}, or any input or output voltage clamps, close to their connection pin. Connect the other end of the component to the inner layer GND without trace length. The trace routing the R_{RSET} resistor to the TPS2421 should be as short as possible to reduce parasitic effects on fault and current-limit accuracy.

PowerPad™

When properly mounted the PowerPad package provides significantly greater cooling ability than an ordinary package. To operate at rated power the Power Pad must be soldered directly to the PC board GND plane directly under the device. The PowerPad is at GND potential and can be connected using multiple vias to inner layer GND. Other planes, such a the bottom side of the circuit board can be used to increase heat sinking in higher current applications. Refer to Technical Briefs: *PowerPad™ Thermally Enhanced Package* (TI literature Number SLMA002) and *PowerPad™ Made Easy* (TI Literature Number SLMA004) or more information on using this PowerPad™ package. These documents are available at www.ti.com (Search by Keyword).

REVISION HISTORY

Changes from Revision A (March 2009) to Revision B **Page**

- Changed MARKING 2
- Added For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com. 2

Changes from Revision B (June 2010) to Revision C **Page**

- Changed T_{SD} (ms) column in Table 3. (the table was deleted in revision F) 14

Changes from Revision C (July 2010) to Revision D **Page**

- Added Feature: UL Listed - File Number E169910 1

Changes from Revision D (August 2010) to Revision E **Page**

- Changed equation 3 from RIFLT to RISET and IFAULT to ISET 7
- Changed RFLT to RSET 8

Changes from Revision E (September 2011) to Revision F **Page**

- Changed C_{CT} values From: MIN = 100 pF/µF To 0.1 nF and MAX From: 10 pF/µF To: -- in the RECOMMENDED OPERATING CONDITIONS table 2
- Added R_{RSET} to the RECOMMENDED OPERATING CONDITIONS table 2
- Changed the conditions statement of the ELECTRICAL CHARACTERISTICS table 3
- Changed the TEST CONDITIONS for R_{ON} 3
- Changed I_{LIM} / I_{FLT} To: I_{LIM} / I_{SET} 3
- Changed the conditions statement of the ELECTRICAL CHARACTERISTICS table 4
- Changed the PIN DESCRIPTION section 6
- Changed the APPLICATION INFORMATION SECTION. 13

Changes from Revision F (April 2013) to Revision G **Page**

- Deleted I_{SET}, C_T Voltage from the ABSOLUTE MAXIMUM RATINGS table 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2421-1DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2421-1	Samples
TPS2421-1DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2421-1	Samples
TPS2421-2DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2421-2	Samples
TPS2421-2DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2421-2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

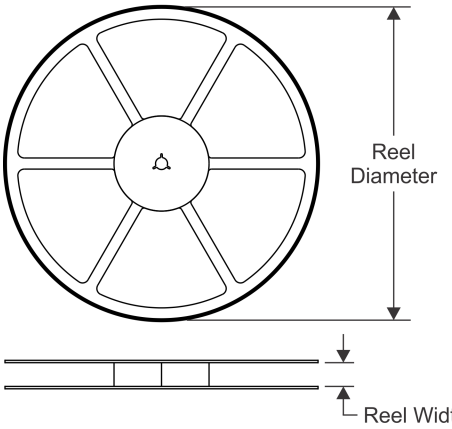
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

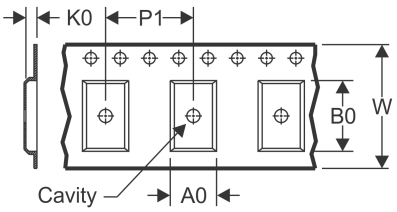
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

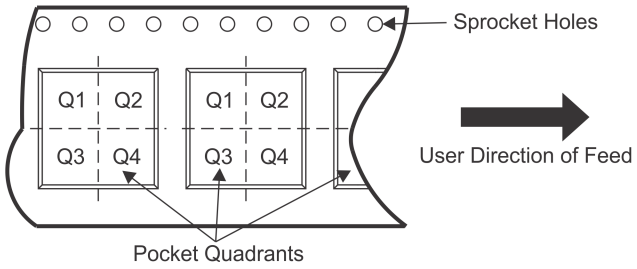


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

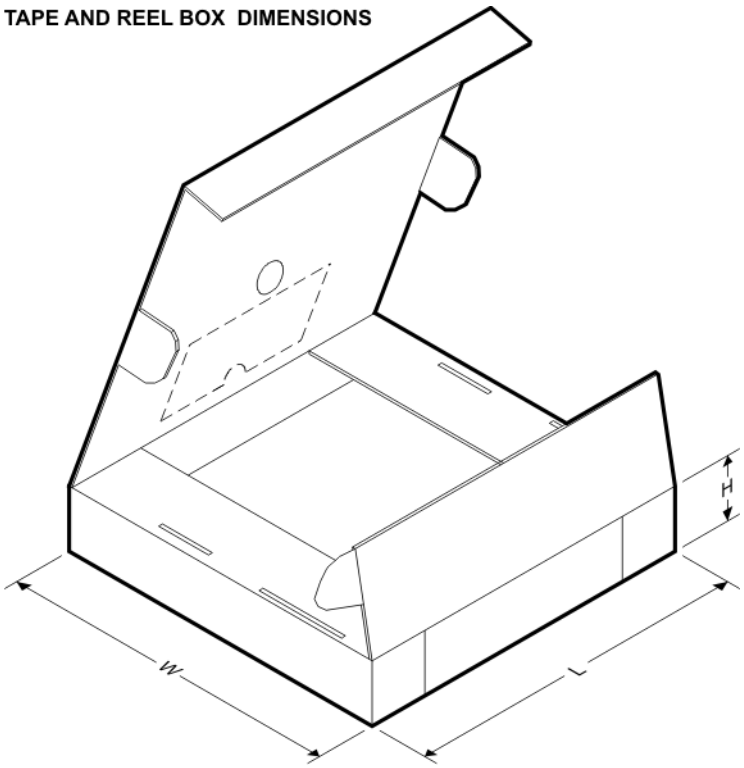
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2421-1DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS2421-2DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

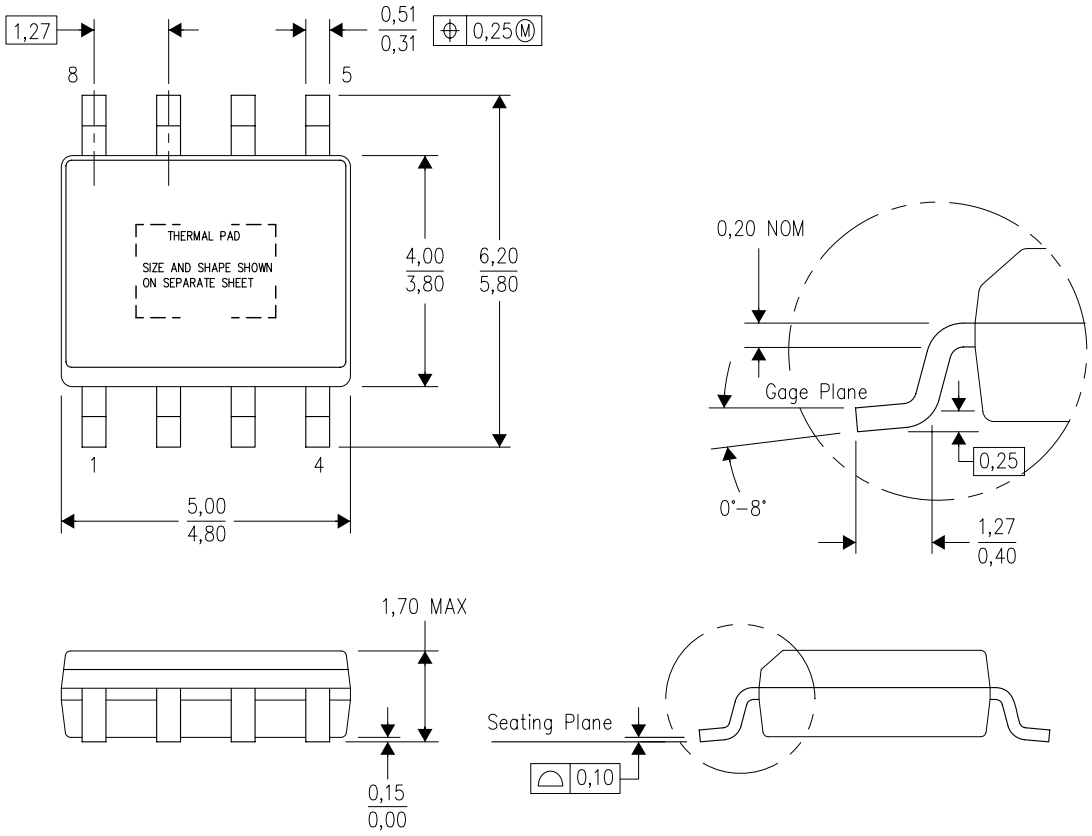
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2421-1DDAR	SO PowerPAD	DDA	8	2500	364.0	364.0	27.0
TPS2421-2DDAR	SO PowerPAD	DDA	8	2500	364.0	364.0	27.0

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

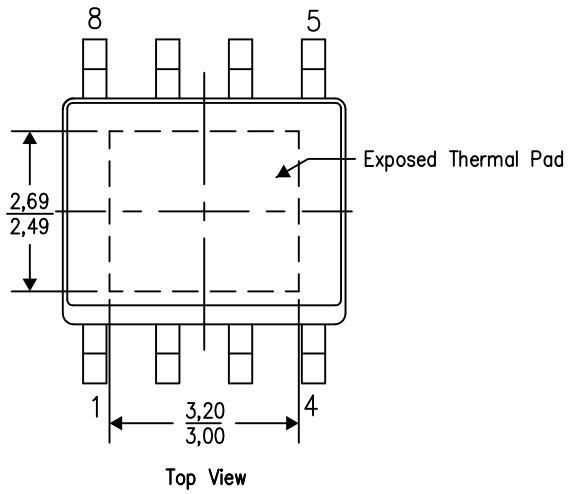
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322–7/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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