2.5-V to 18-V High-Efficiency Power-Limiting Hot-Swap Controller

Check for Samples: TPS24710, TPS24711, TPS24712, TPS24713

FEATURES

- **2.5-V to 18-V Operation**
- **Accurate Current Limiting for Startup**
- **Programmable FET SOA Protection**
- **Accurate 25-mV Current-Sense Threshold**
- **Power-Good Output**
- **Fast Breaker for Short-Circuit Protection**
- **Programmable Fault Timer**
- **Programmable UV Threshold**
- **Drop-In Upgrade for LTC4211 – No Layout Changes**
- **PG, FLT Active-High and Active-Low Versions**
- **MSOP-10 Package**

APPLICATIONS

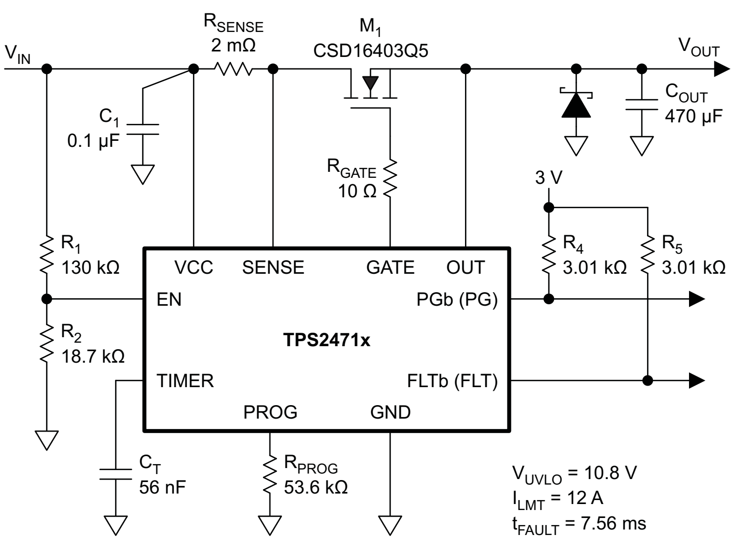
- **Server Backplanes**
- **Storage Area Networks (SAN)**
- **Medical Systems**
- **Plug-In Modules**
- **Base Stations**

DESCRIPTION

The TPS24710/11/12/13 is an easy-to-use, 2.5 V to 18 V, hot-swap controller that safely drives an external N-channel MOSFET. The programmable current limit and fault time protect the supply and load from excessive current at startup. After startup, currents above the user-selected limit will be allowed to flow until programmed timeout – except in extreme overload events when the load is immediately disconnected from source. The low, 25mV current sense threshold is highly accurate and allows use of smaller, more efficient sense resistors yielding lower power loss and smaller footprint.

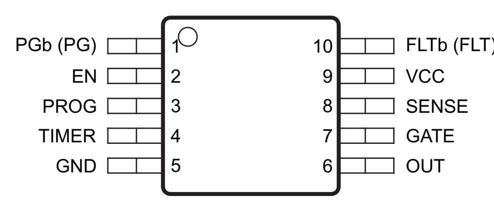
Programmable power limiting ensures the external MOSFET operates inside its safe operating area (SOA) at all times. This allows the use of smaller MOSFETS while improving system reliability. Power good and fault outputs are provided for status monitoring and downstream load control.

TYPICAL APPLICATION (12 V at 10 A)



PINOUT

DGS Package
(Top View)



	TPS24710	TPS24711	TPS24712	TPS24713
Latch Off	X		X	
Retry		X		X
PG	L	L	H	H
FLT	L	L	H	H

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION

T_A	PACKAGE	PART NUMBER[1]	FUNCTION	FLT, PG POLARITY	MARKING
–40ºC to 85ºC	MSOP-10	TPS24710	Latched	Active Low	24710
		TPS24711	Retry		24711
		TPS24712	Latched	Active High	24712
		TPS24713	Retry		24713

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range, all voltages referred to GND (unless otherwise noted)

			VALUE	UNIT
Input voltage range	EN, FLT[1][2], FLTb[1][3], GATE, OUT, PG[1][2], PGb[1][3], SENSE, VCC		–0.3 to 30	V
	PROG[1]		–0.3 to 0.3	
	SENSE to VCC		–0.3 to 0.3	
	TIMER		–0.3 to 5	
Sink current	FLT, PG, FLTb, PGb		5	mA
Source current	PROG		Internally limited	
ESD rating	Human-body model	All pins except PG and PGb	2	kV
		PG, PGb	0.5	
	Charged-device model		0.5	
Temperature	Maximum junction, T_J		Internally limited	°C

(1) Do not apply voltages directly to these pins.
(2) for TPS24712/13
(3) for TPS24710/11

THERMAL INFORMATION

THERMAL METRIC[1]		TPS24710/11/12/13	UNIT
		MSOP (10) PINS	
θ_{JA}	Junction-to-ambient thermal resistance	166.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	41.8	°C/W
θ_{JB}	Junction-to-board thermal resistance	86.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.7	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range	SENSE, VCC	2.5		18	V
	EN, FLT, FLTb, PG, PGb, OUT	0		18	
Sink current	FLT, FLTb, PG, PGb	0		2	mA
Resistance	PROG	4.99		500	kΩ
External capacitance	TIMER	1			nF
	GATE (1)			1	µF
Operating junction temperature range, T_J		–40		125	°C

(1) External capacitance tied to GATE should be in series with a resistor no less than 1 kΩ.

ELECTRICAL CHARACTERISTICS

–40°C ≤ T_J ≤ 125°C, V_{CC} = 12 V, V_{EN} = 3 V, and R_{PROG} = 50 kΩ to GND.
All voltages referenced to GND, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC					
UVLO threshold, rising		2.2	2.32	2.45	V
UVLO threshold, falling		2.1	2.22	2.35	V
UVLO hysteresis (1)			0.1		V
Supply current	Enabled — I_{OUT} + I_{VCC} + I_{SENSE}		1	1.4	mA
	Disabled (1) — EN = 0 V, I_{OUT} + I_{VCC} + I_{SENSE}		0.45		mA
EN					
Threshold voltage, falling		1.2	1.3	1.4	V
Hysteresis (1)			50		mV
Input leakage current	0 V ≤ V_{EN} ≤ 30 V	–1	0	1	µA
Turnoff time	EN ↓ to V_{GATE} < 1 V, C_{GATE} = 33 nF	20	60	150	µs
Deglitch time	EN ↑	8	14	18	µs
Disable delay	EN ↓ to GATE ↓, C_{GATE} = 0, $t_{pff50–90}$, See Figure 1	0.1	0.4	1	µs
FLT, FLTb					
Output low voltage	Sinking 2 mA		0.11	0.25	V
Input leakage current	V_{FLT} = 0 V, 30 V	–1	0	1	µA
	V_{FLTb} = 0 V, 30 V				
PG, PGb					
Threshold	$V_{(SENSE – OUT)}$ rising, PG going low	140	240	340	mV
	$V_{(SENSE – OUT)}$ rising, PGb going high				
Hysteresis (1)	Measured $V_{(SENSE – OUT)}$ falling, PG going high		70		mV
	Measured $V_{(SENSE – OUT)}$ falling, PGb going low				
Output low voltage	Sinking 2 mA		0.11	0.25	V
Input leakage current	V_{PG} = 0 V, 30 V	–1	0	1	µA
	V_{PGb} = 0 V, 30 V				
Delay (deglitch) time	Rising or falling edge	2	3.4	6	ms
PROG					
Bias voltage	Sourcing 10 µA	0.65	0.678	0.7	V
Input leakage current	V_{PROG} = 1.5 V	–0.2	0	0.2	µA
TIMER					
Sourcing current	V_{TIMER} = 0 V	8	10	12	µA

(1) Parameters are for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

ELECTRICAL CHARACTERISTICS (continued)

–40°C ≤ T_J ≤ 125°C, V_{CC} = 12 V, V_{EN} = 3 V, and R_{PROG} = 50 kΩ to GND.

All voltages referenced to GND, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Sinking current	V_{TIMER} = 2 V	8	10	12	µA
	V_{EN} = 0 V, V_{TIMER} = 2 V	2	4.5	7	mA
Upper threshold voltage		1.30	1.35	1.40	V
Lower threshold voltage		0.33	0.35	0.37	V
Timer activation voltage	Raise GATE until I_{TIMER} sinking, measure $V_{(GATE – VCC)}$, V_{CC} = 12 V	5	5.9	7	V
Bleed-down resistance	V_{ENSD} = 0 V, V_{TIMER} = 2 V	70	104	130	kΩ
OUT					
Input bias current	V_{OUT} = 12 V		16	30	µA
GATE					
Output voltage	V_{OUT} = 12 V	23.5	25.8	28	V
Clamp voltage	Inject 10 µA into GATE, measure $V_{(GATE – VCC)}$	12	13.9	15.5	V
Sourcing current	V_{GATE} = 12 V	20	30	40	µA
Sinking current	Fast turnoff, V_{GATE} = 14 V	0.5	1	1.4	A
	Sustained, V_{GATE} = 4 V to 23 V	6	11	20	mA
	In inrush current limit, V_{GATE} = 4 V to 23 V	20	30	40	µA
Pulldown resistance	Thermal shutdown	14	20	26	kΩ
Fast-turnoff duration		8	13.5	18	µs
Turn on delay	V_{CC} rising to GATE sourcing, $t_{prr50-50}$, See Figure 2		100	250	µs
SENSE					
Input bias current	V_{SENSE} = 12 V, sinking current		30	40	µA
Current limit threshold	V_{OUT} = 12 V	22.5	25	27.5	mV
Power limit threshold	V_{OUT} = 7 V, R_{PROG} = 50 kΩ	10	12.5	15	mV
	V_{OUT} = 2 V, R_{PROG} = 25 kΩ	10	12.5	15	
Fast-trip threshold		52	60	68	mV
Fast-turnoff duration		8	13.5	18	µs
Fast-turnoff delay(2)	$V_{(VCC – SENSE)}$ = 80 mV, C_{GATE} = 0 pF, $t_{prf50–50}$, See Figure 3		200		ns
OTSD					
Threshold, rising		130	140		°C
Hysteresis(2)			10		°C

(2) Parameters are for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

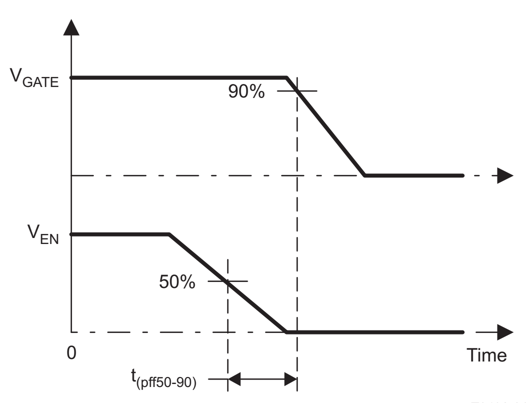


Figure 1. $t_{pff50–90}$ Timing Definition

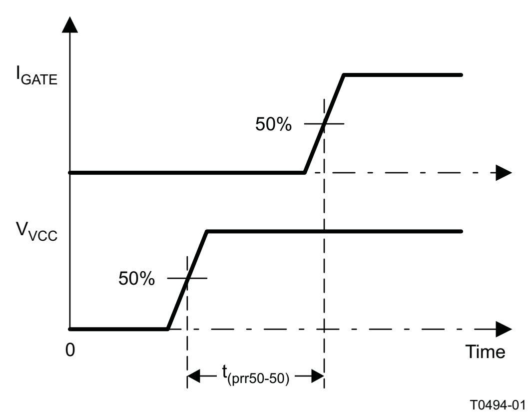


Figure 2. $t_{prr50–50}$ Timing Definition

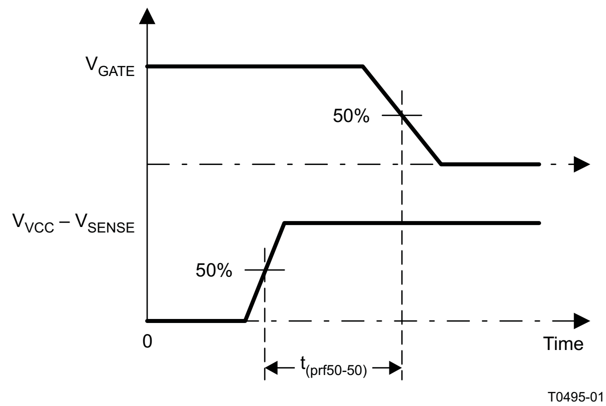
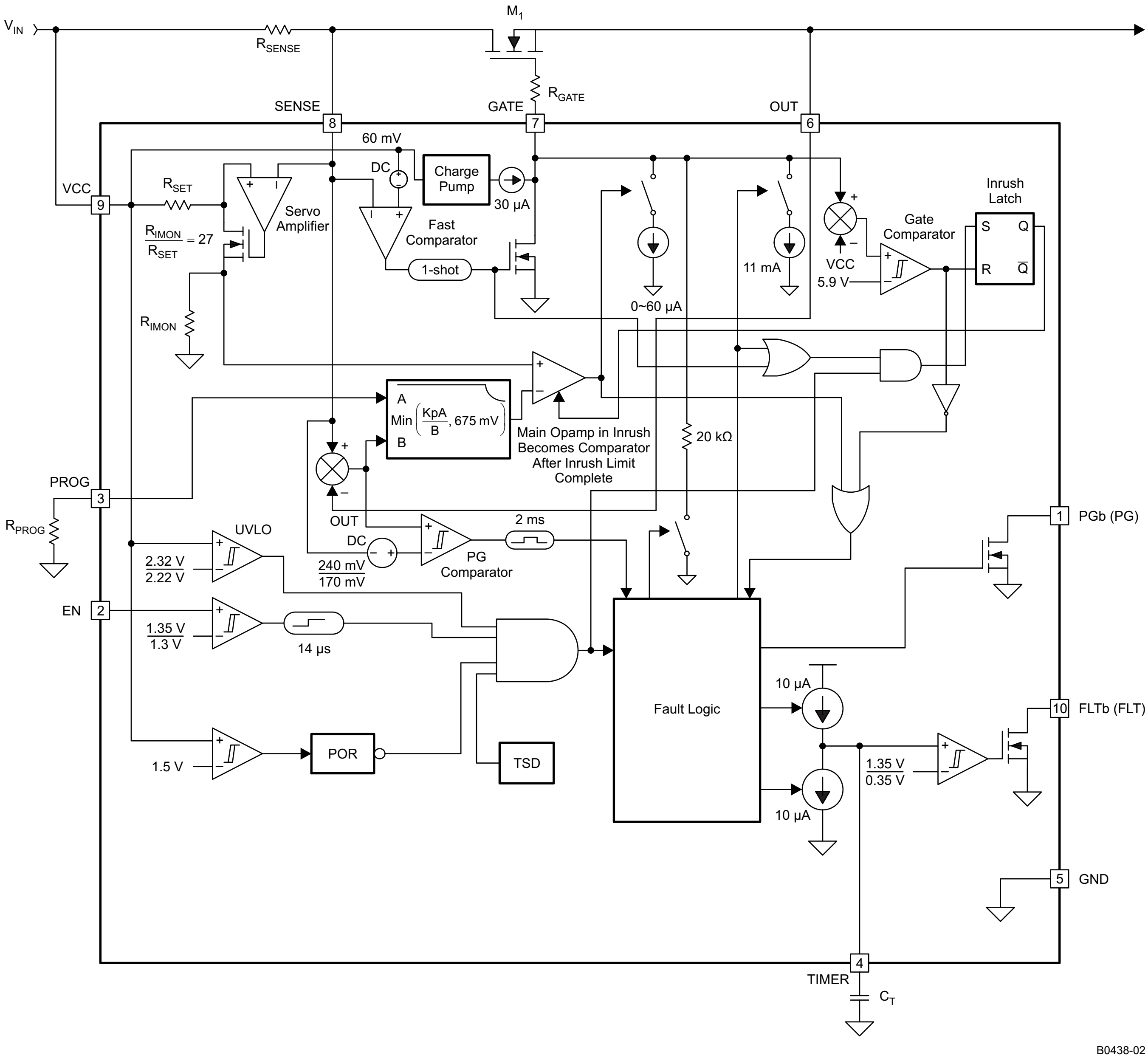


Figure 3. $t_{prf50–50}$ Timing Definition

FUNCTIONAL BLOCK DIAGRAM



NOTE: Pins 1 and 10 are PG and FLT, respectively, for TPS24712/13

Figure 4. Block Diagram of the TPS24710/11

PIN FUNCTIONS

NAME	PINS		I/O	DESCRIPTION
	TPS24710/11	TPS24712/13		
EN	2	2	I	Active-high enable input. Logic input. Connects to resistor divider.
FLT	-	10	O	Active-high, open-drain output indicates overload fault timer has turned MOSFET off.
FLTb	10	-		Active-low, open-drain output indicates overload fault timer has turned MOSFET off.
GATE	7	7	O	Gate driver output for external MOSFET
GND	5	5	–	Ground
OUT	6	6	I	Output voltage sensor for monitoring MOSFET power.

PIN FUNCTIONS (continued)

NAME	PINS		I/O	DESCRIPTION
	TPS24710/11	TPS24712/13		
PG	-	1	O	Active-high, open-drain power good indicator. Status is determined by the voltage across the MOSFET.
PGb	1	-		Active-low, open-drain power good indicator. Status is determined by the voltage across the MOSFET.
PROG	3	3	I	Power-limiting programming pin. A resistor from this pin to GND sets the maximum power dissipation for the FET.
SENSE	8	8	I	Current sensing input for resistor shunt from VCC to SENSE.
TIMER	4	4	I/O	A capacitor connected from this pin to GND provides a fault timing function.
VCC	9	9	I	Input-voltage sense and power supply

DETAILED PIN DESCRIPTIONS

The following description relies on the typical application diagram on the front page of this data sheet, as well as the functional block diagram in Figure 4.

EN: Applying a voltage of 1.35 V or more to this pin enables the gate driver. The addition of an external resistor divider allows the EN pin to serve as an undervoltage monitor. Cycling EN low and then back high resets the TPS24710/11/12/13 that has latched off due to a fault condition. This pin should not be left floating.

FLT: FLT is assigned for TPS24712/13. This active-high open-drain output assumes high-impedance when TPS24712/13 has remained in current limit long enough for the fault timer to expire. The behavior of the FLT pin depends on the version of the IC. The TPS24712 operates in latch mode and the TPS24713 operates in retry mode. In latch mode, a fault timeout disables the external MOSFET and holds FLT in open drain condition. The latched mode of operation is reset by cycling EN or VCC. In retry mode, a fault timeout first disables the external MOSFET, next waits sixteen cycles of TIMER charging and discharging, and finally attempts a restart. This process repeats as long as the fault persists. In retry mode, the FLT pin goes open-drain whenever the external MOSFET is disabled by the fault timer. In a sustained fault, the FLT waveform becomes a train of pulses. The FLT pin does not assert if the external MOSFET is disabled by EN, overtemperature shutdown, or UVLO. This pin can be left floating when not used.

FLTb: FLTb is assigned for TPS24710/11. This active-low open-drain output pulls low when TPS24710/11/12/13 has remained in current limit long enough for the fault timer to expire. The behavior of the FLTb pin depends on the version of the IC. The TPS24710 operates in latch mode and the TPS24711 operates in retry mode. In latch mode, a fault timeout disables the external MOSFET and holds FLTb low. The latched mode of operation is reset by cycling EN or VCC. In retry mode, a fault timeout first disables the external MOSFET, next waits sixteen cycles of TIMER charging and discharging, and finally attempts a restart. This process repeats as long as the fault persists. In retry mode, the FLTb pin is pulled low whenever the external MOSFET is disabled by the fault timer. In a sustained fault, the FLTb waveform becomes a train of pulses. The FLTb pin does not assert if the external MOSFET is disabled by EN, overtemperature shutdown, or UVLO. This pin can be left floating when not used.

GATE: This pin provides gate drive to the external MOSFET. A charge pump sources 30 µA to enhance the external MOSFET. A 13.9-V clamp between GATE and VCC limits the gate-to-source voltage, because V_{VCC} is very close to V_{OUT} in normal operation. During start-up, a transconductance amplifier regulates the gate voltage of M_1 to provide inrush current limiting. The TIMER pin charges timer capacitor C_T during the inrush. Inrush current limiting continues until the $V_{(GATE\,-\,VCC)}$ exceeds the Timer Activation Voltage (5.9 V for V_{VCC} = 12 V). Then the TPS24710/11/12/13 enters into circuit-breaker mode. The Timer Activation Voltage is defined as a threshold voltage. When $V_{(GATE\text{-}VCC)}$ exceeds this threshold voltage, the inrush operation is finished and the TIMER stops sourcing current and begins sinking current. In the circuit-breaker mode, the current flowing in R_{SENSE} is compared with the current-limit threshold derived from the MOSFET power-limit scheme (see PROG). If the current flowing in R_{SENSE} exceeds the current limit threshold, then MOSFET M_1 is turned off. The GATE pin is disabled by the following three conditions:

1. GATE is pulled down by an 11-mA current source when
   - The fault timer expires during an overload current fault (V_{SENSE} > 25 mV)
   - V_{EN} is below its falling threshold

   – V_{VCC} drops below the UVLO threshold
2. GATE is pulled down by a 1 A current source for 13.5 µs when a hard output short circuit occurs and $V_{(VCC\ -\ SENSE)}$ is greater than 60 mV, i.e., the fast-trip shutdown threshold. After fast-trip shutdown is complete, an 11-mA sustaining current ensures that the external MOSFET remains off.
3. GATE is discharged by a 20 kΩ resistor to GND if the chip die temperature exceeds the OTSD rising threshold.

GATE remains low in latch mode (TPS24710/12) and attempts a restart periodically in retry mode (TPS24711/13).

If used, any capacitor connecting GATE and GND should not exceed 1 µF and it should be connected in series with a resistor of no less than 1 kΩ. No external resistor should be directly connected from GATE to GND or from GATE to OUT.

GND: This pin is connected to system ground.

OUT: This pin allows the controller to measure the drain-to-source voltage across the external MOSFET M_1. The power-good indicator (PG/PGb) relies on this information, as does the power limiting engine. The OUT pin should be protected from negative voltage transients by a clamping diode or sufficient capacitors. A Schottky diode of 3 A / 40 V in a SMC package is recommended as a clamping diode for high-power applications. The OUT pin should be bypassed to GND with a low-impedance ceramic capacitor in the range of 10 nF to 1 µF.

PG: PG is assigned for TPS24712/13. This active-high, open-drain output is intended to interface to downstream dc/dc converters or monitoring circuits. PG assumes high-impedance after the drain-to-source voltage of the FET has fallen below 170 mV and a 3.4-ms deglitch delay has elapsed. It pulls low when V_{DS} exceeds 240 mV. PG assumes low-impedance status after a 3.4-ms deglitch delay once V_{DS} of M_1 rises up, resulting from GATE being pulled to GND at any of the following conditions:

- An overload current fault occurs (V_{SENSE} > 25 mV).
- A hard output short circuit occurs, leading to $V_{(VCC\ -\ SENSE)}$ greater than 60 mV, i.e., the fast-trip shutdown threshold has been exceeded.
- V_{EN} is below its falling threshold.
- V_{VCC} drops below the UVLO threshold.
- Die temperature exceeds the OTSD threshold.

This pin can be left floating when not used.

PGb: PGb is assigned for TPS24710/11. This active-low, open-drain output is intended to interface to downstream dc/dc converters or monitoring circuits. PGb pulls low after the drain-to-source voltage of the FET has fallen below 170 mV and a 3.4-ms deglitch delay has elapsed. It goes open-drain when VDS exceeds 240 mV. PGb assumes high-impedance status after a 3.4-ms deglitch delay once V_{DS} of M_1 rises up, resulting from GATE being pulled to GND at any of the following conditions:

- An overload current fault occurs (V_{SENSE} > 25 mV).
- A hard output short circuit occurs, leading to $V_{(VCC\ -\ SENSE)}$ greater than 60 mV, i.e., the fast-trip shutdown threshold has been exceeded.
- V_{EN} is below its falling threshold.
- V_{VCC} drops below the UVLO threshold.
- Die temperature exceeds the OTSD threshold.

This pin can be left floating when not used.

PROG: A resistor from this pin to GND sets the maximum power permitted in the external MOSFET M_1 during inrush. Do not apply a voltage to this pin. If the constant power limit is not desired, use a PROG resistor of 4.99 kΩ. To set the maximum power, use Equation 1,

$$P_{LIM} = \frac{3125}{R_{PROG} \times R_{SENSE}} \tag{1}$$

where P_{LIM} is the allowed power limit of MOSFET M_1. R_{SENSE} is the load-current-monitoring resistor connected between the VCC pin and the SENSE pin. R_{PROG} is the resistor connected from the PROG pin to GND. Both R_{PROG} and R_{SENSE} are in ohms and P_{LIM} is in watts. P_{LIM} is determined by the maximum allowed thermal stress of MOSFET M_1, given by Equation 2,

$$P_{LIM} < \frac{T_{J(MAX)} - T_{C(MAX)}}{R_{\theta JC(MAX)}} \tag{2}$$

where $T_{J(MAX)}$ is the maximum desired transient junction temperature and $T_{C(MAX)}$ is the maximum case temperature prior to a start or restart. $R_{\Theta JC(MAX)}$ is the junction-to-case thermal impedance of the pass MOSFET M_1 in units of °C/W. Both $T_{J(MAX)}$ and $T_{C(MAX)}$ are in °C.

SENSE: This pin connects to the negative terminal of R_{SENSE}. It provides a means of sensing the voltage across this resistor, as well as a way to monitor the drain-to-source voltage across the external FET. The current limit I_{LIM} is set by Equation 3.

$$I_{LIM} = \frac{25\ \text{mV}}{R_{SENSE}} \tag{3}$$

A fast trip shutdown occurs when $V_{(VCC - VSENSE)}$ exceeds 60 mV.

TIMER: A capacitor C_T connected from the TIMER pin to GND determines the overload fault timing. TIMER sources 10 µA when an overload is present, and discharges C_T at 10 µA otherwise. M_1 is turned off when V_{TIMER} reaches 1.35 V. In an application implementing auto-retry after a fault, this capacitor also determines the period before the external MOSFET is re-enabled. A minimum timing capacitance of 1 nF is recommended to ensure proper operation of the fault timer. The value of C_T can be calculated from the desired fault time t_{FLT}, using Equation 4.

$$C_T = \frac{10\ \mu\text{A}}{1.35\ \text{V}} \times t_{FLT} \tag{4}$$

The latch mode (TPS24710/12) or the retry mode (TPS24711/13) occurs if the load current exceeds the current limit threshold or the fast-trip shutdown threshold, While in latch mode, the TIMER pin continues to charge and discharge the attached capacitor periodically. In retry mode, the external MOSFET is disabled for sixteen cycles of TIMER charging and discharging. The TIMER pin is pulled to GND by a 2-mA current source at the end of the 16^{th} cycle of charging and discharging. The external MOSFET is then re-enabled. The TIMER pin capacitor, C_T, can also be discharged to GND during latch mode or retry mode by a 2-mA current source whenever any of the following occurs:

- V_{EN} is below its falling threshold.
- V_{VCC} drops below the UVLO threshold.

VCC: This pin performs three functions. First, it provides biasing power to the integrated circuit. Second, it serves as an input to the power-on reset (POR) and undervoltage lockout (UVLO) functions. The VCC trace from the integrated circuit should connect directly to the positive terminal of R_{SENSE} to minimize the voltage sensing error. Bypass capacitor C_1, shown in the typical application diagram on the front page, should be connected to the positive terminal of R_{SENSE}. A capacitance of at least 10 nF is recommended.

TYPICAL CHARACTERISTICS

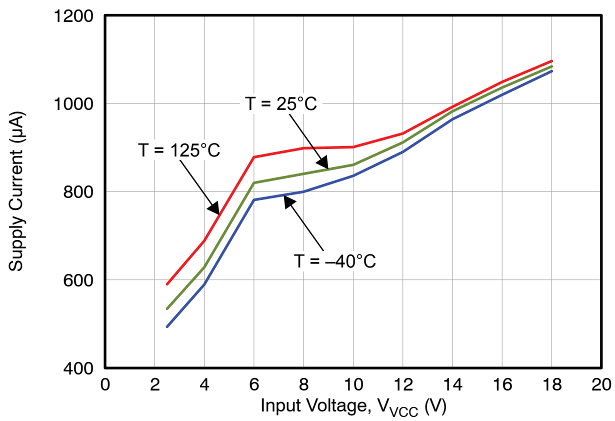


Figure 5. Supply Current vs Input Voltage at Normal Operation (EN = High)

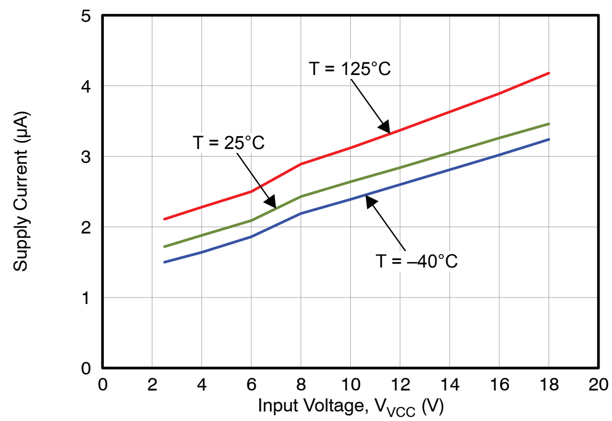


Figure 6. Supply Current vs Input Voltage at Shutdown (EN = 0 V)

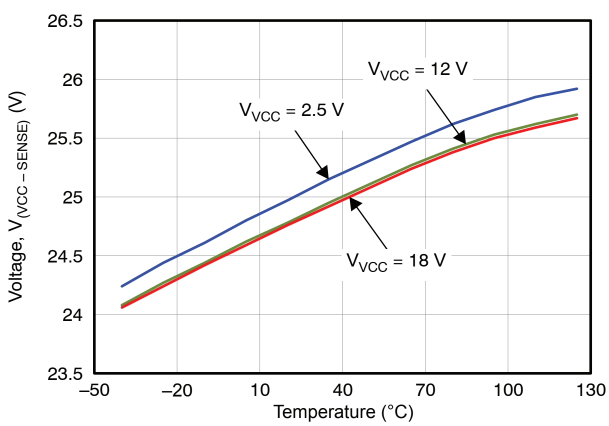


Figure 7. Voltage Across R_{SENSE} in Inrush Current Limiting vs Temperature

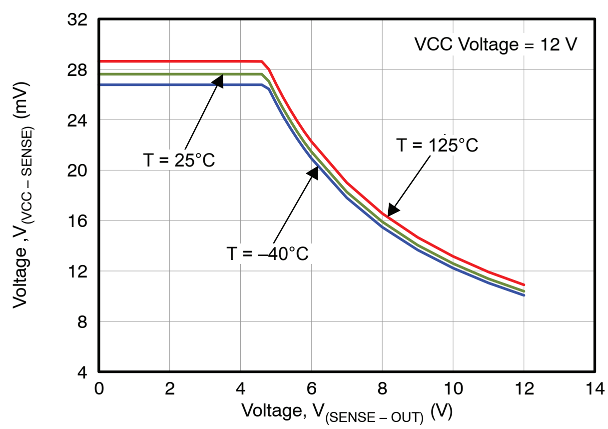


Figure 8. Voltage Across R_{SENSE} in Inrush Power Limiting vs V_{DS} of Pass MOSFET

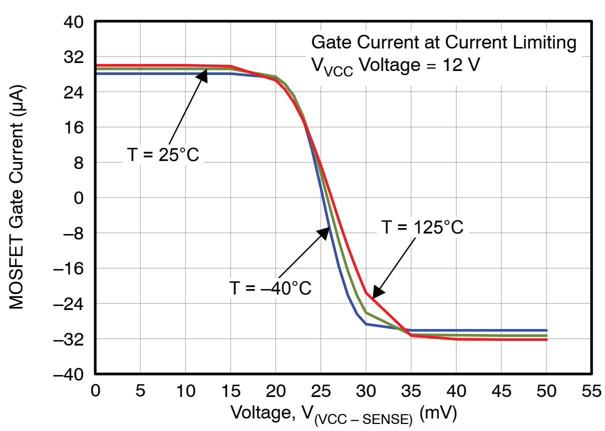


Figure 9. MOSFET Gate Current vs Voltage Across R_{SENSE} During Inrush Power Limiting

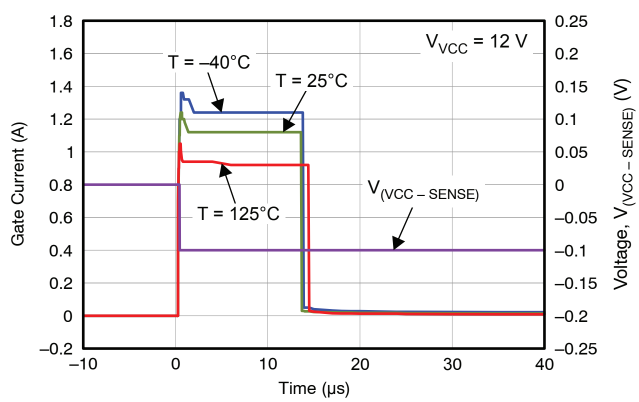


Figure 10. Gate Current During Fast Trip, V_{VCC} = V_{GATE} = 12 V

TYPICAL CHARACTERISTICS (continued)

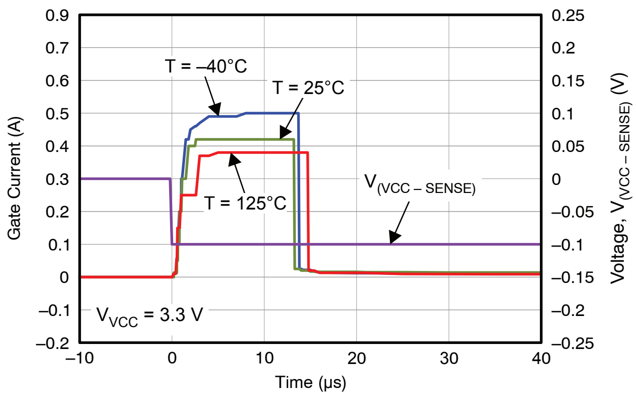


Figure 11. Gate Current During Fast Trip, V_{VCC} = V_{GATE} = 3.3 V

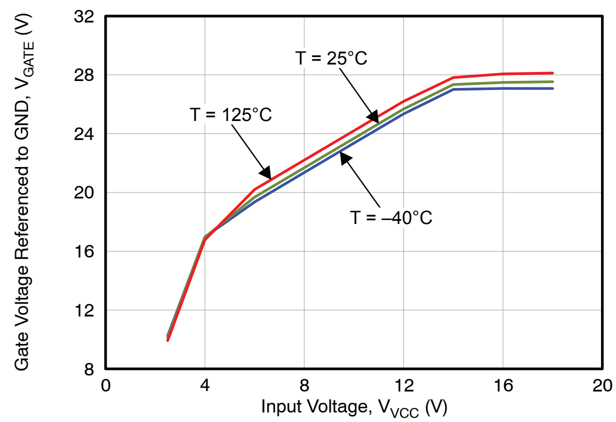


Figure 12. Gate Voltage With Zero Gate Current vs Input Voltage

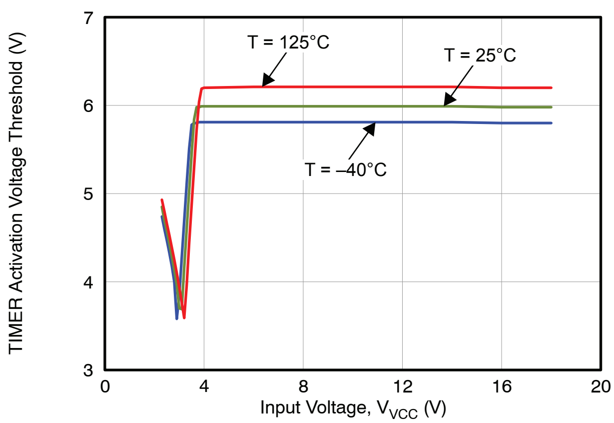


Figure 13. TIMER Activation Voltage Threshold vs Input Voltage at Various Temperatures

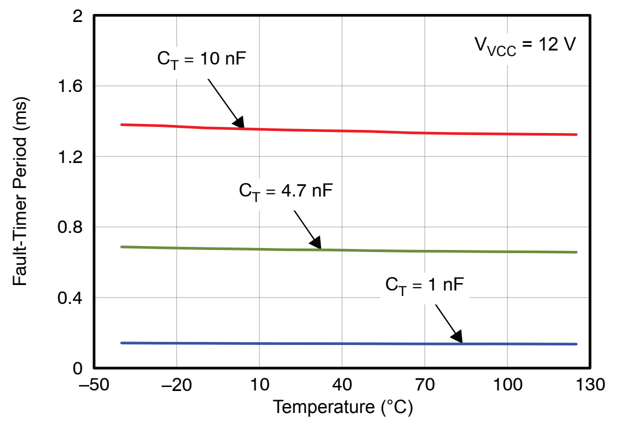


Figure 14. Fault-Timer Period vs Temperature With Various TIMER Capacitors

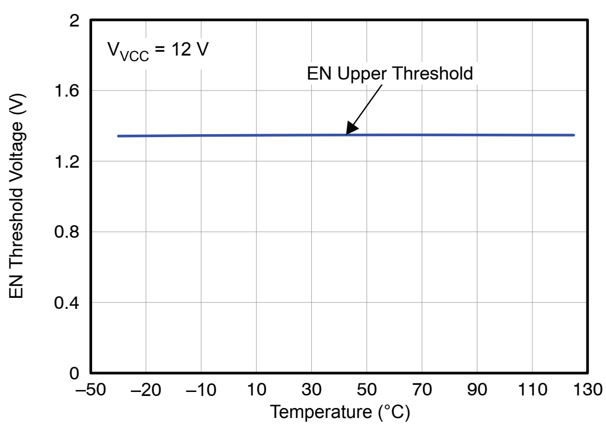


Figure 15. EN Threshold Voltage vs Temperature

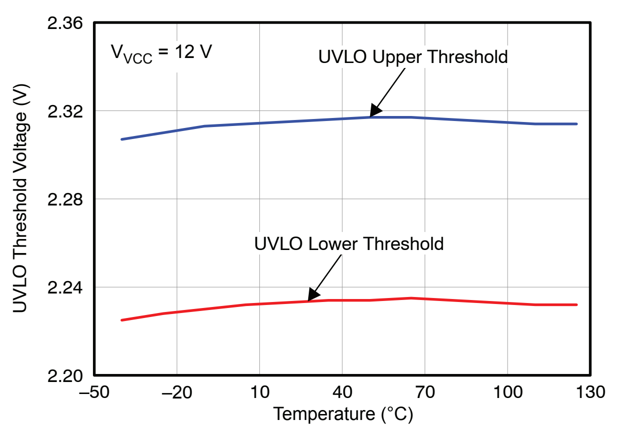


Figure 16. UVLO Threshold Voltage vs Temperature

TYPICAL CHARACTERISTICS (continued)

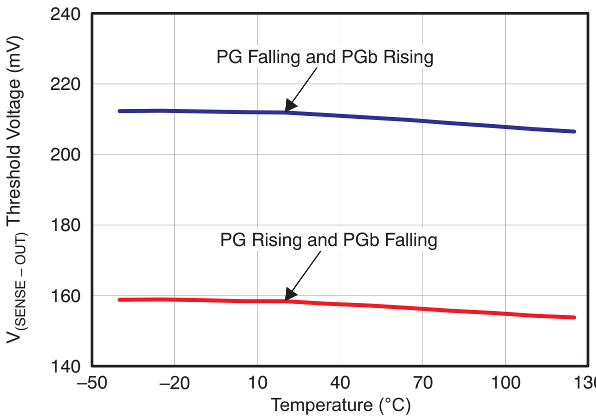


Figure 17. Threshold Voltage of V_{DS} vs Temperature, PGb and PG Rising and Falling

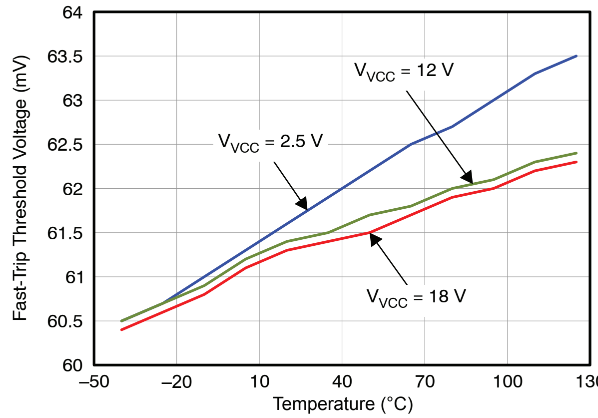


Figure 18. Fast-Trip Threshold Voltage vs Temperature

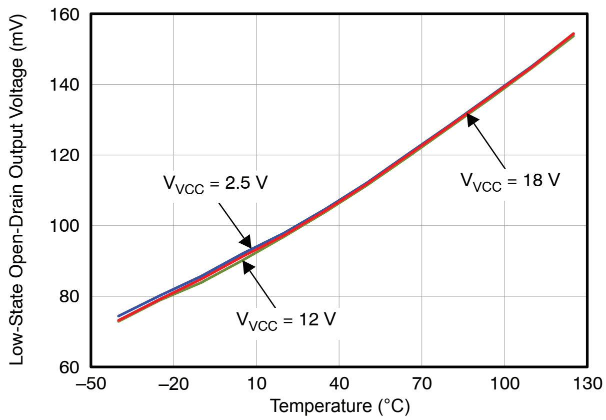


Figure 19. PG and PGb Open-Drain Output Voltage in Low State

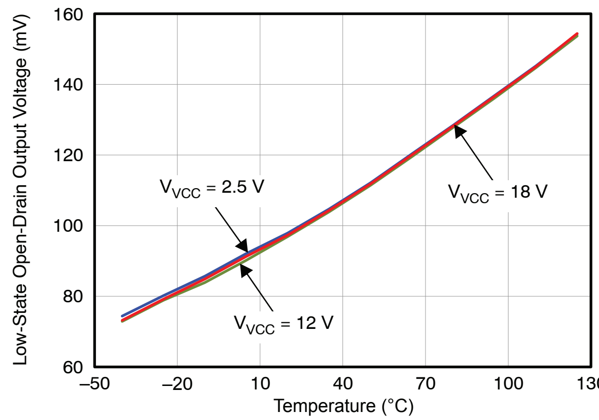


Figure 20. FLT and FLTb Open-Drain Output Voltage in Low State

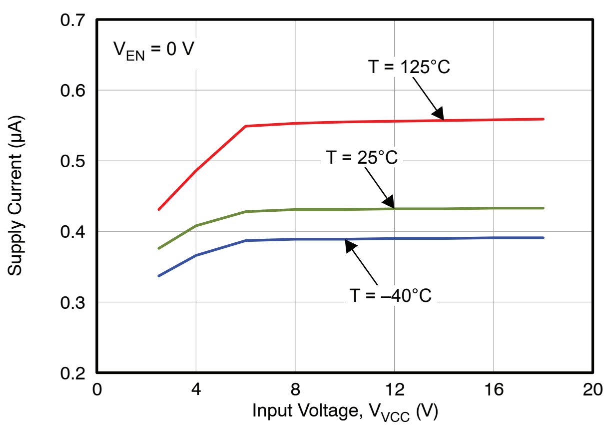


Figure 21. Supply Current vs Input Voltage at Various Temperatures When EN Pulled Low

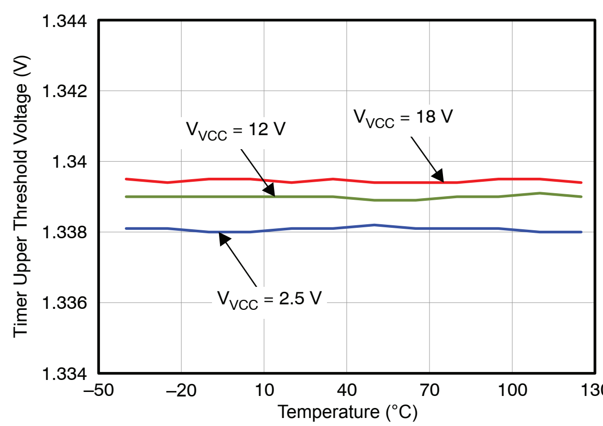


Figure 22. Timer Upper Threshold Voltage vs Temperature at Various Input Voltages

TYPICAL CHARACTERISTICS (continued)

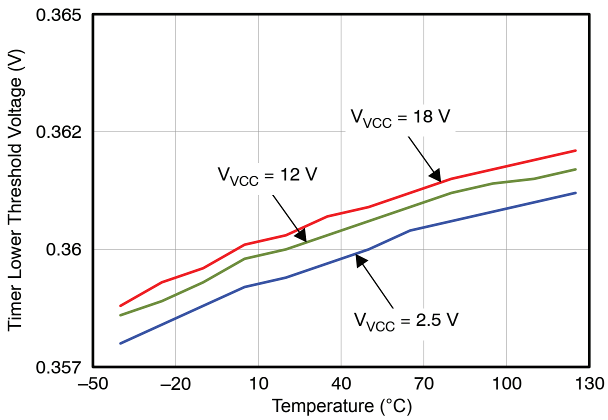


Figure 23. Timer Lower Threshold Voltage vs Temperature at Various Input Voltages

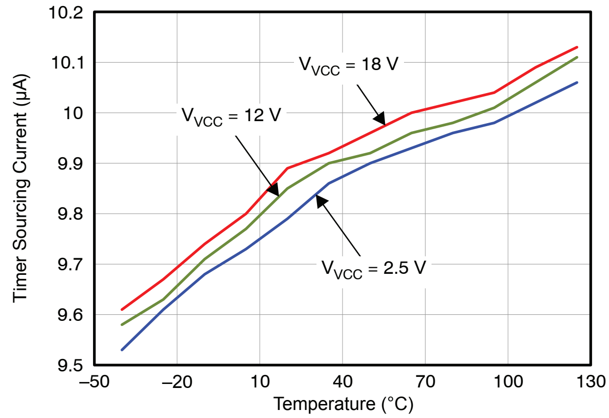


Figure 24. Timer Sourcing Current vs Temperature at Various Input Voltages

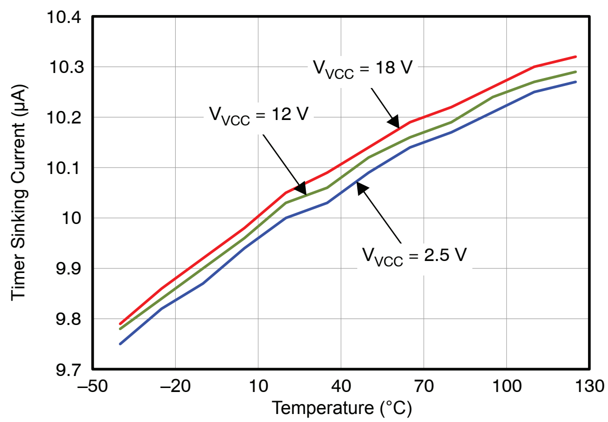


Figure 25. Timer Sinking Current vs Temperature at Various Input Voltages

SYSTEM OPERATION

INTRODUCTION

The TPS24710/11/12/13 provides all the features needed for a positive hot-swap controller. These features include:

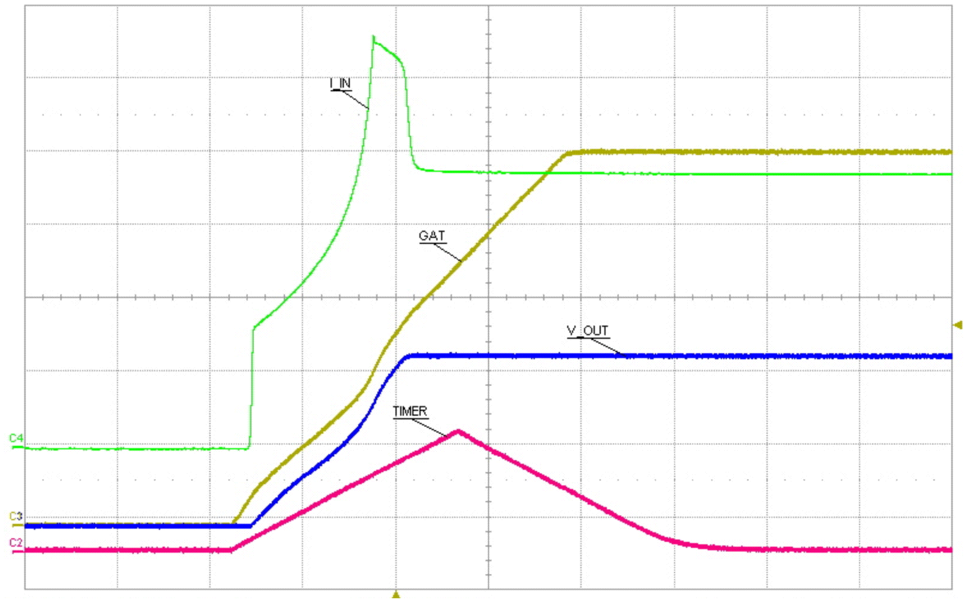
- Undervoltage lockout
- Adjustable (system-level) enable
- turn-on inrush limiting
- High-side gate drive for an external N-channel MOSFET
- MOSFET protection by power limiting
- Adjustable overload timeout — also called an electronic circuit breaker
- Charge-complete indicator for downstream converter coordination
- A choice of latch (TPS24710/12) or automatic restart mode (TPS24711/13)

The typical application diagram on the front page of this data sheet, and oscilloscope plots shown in Figure 26 through Figure 28 and Figure 30 through Figure 33, demonstrate many of the functions described previously.

BOARD PLUG IN

Figure 26 and Figure 27 illustrate the inrush current that flows when a hot swap board under the control of the TPS24710/11/12/13 is plugged into a system bus. Only the bypass capacitor charge current and small bias currents are evident when a board is first plugged in. The TPS24710/11/12/13 is held inactive, for a short period while internal voltages stabilize. During this period GATE, PROG, TIMER are held low and PG, FLT, PGb, and FLTb are held open drain. When the voltage on the internal VCC rail exceeds approximately 1.5 V, the power-on reset (POR) circuit initializes the TPS24710/11/12/13 and a start-up cycle is ready to take place.

GATE, PROG, TIMER, PG, FLT, PGb, and FLTb are released after the internal voltages have stabilized and the external EN (enable) thresholds have been exceeded. The part begins sourcing current from the GATE pin to turn on MOSFET M_1. The TPS24710/11/12/13 monitors both the drain-to-source voltage across MOSFET M_1 and the drain current passing through it. Based on these measurements, the TPS24710/11/12/13 limits the drain current by controlling the gate voltage so that the power dissipation within the MOSFET does not exceed the power limit programmed by the user. The current increases as the voltage across the MOSFET decreases until finally the current reaches the current limit I_{LIM}.



I_IN: Input Current, 2 A/div
GAT: Voltage on GATE Pin, 5 V/div
V_OUT: Voltage on OUT Pin, 5 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 2 ms/div

C001

Figure 26. Inrush Mode at Hot-Swap Circuit Insertion

INRUSH OPERATION

After TPS24710/11/12/13 initialization is complete (as described in the Board Plug-In section) and EN is active, GATE is enabled (V_{GATE} starts increasing). When V_{GATE} reaches the MOSFET M1 gate threshold, a current flows into the downstream bulk storage capacitors. When this current exceeds the limit set by the power limit engine, the gate of the MOSFET is regulated by a feedback loop to make the MOSFET current rise in a controlled manner. This not only limits the inrush current charging capacitance but it also limits the power dissipation of the MOSFET to safe levels. A more complete explanation of the power limiting scheme is given in the section entitled *Action of the Constant Power Engine*. When Gate is enabled, the TIMER pin begins to charge the timing capacitor C_T with a current of approximately 10 μA. The TIMER pin continues to charge C_T until $V_{(GATE\,-\,VCC)}$ reaches the timer activation voltage (5.9 V for V_{VCC} = 12 V). The TIMER then begins to discharge C_T with a current of approximately 10 μA. This indicates that the inrush mode is finished. If the TIMER exceeds its upper threshold of 1.35 V before $V_{(GATE\,-\,VCC)}$ reaches the timer activation voltage, the GATE pin is pulled to GND and the hot-swap circuit enters either latch mode (TPS24710/12) or auto-retry mode (TPS24711/13).

The power limit feature is disabled once the inrush operation is finished and the hotswap circuit becomes a circuit breaker. The TPS24710/11/12/13 will turn off the MOSFET, M1, after a fault timer period once the load exceeds the current limit threshold.

ACTION OF THE CONSTANT-POWER ENGINE

Figure 27 illustrates the operation of the constant-power engine during start-up. The circuit used to generate the waveforms of Figure 27 was programmed to a power limit of 29.3 W by means of the resistor connected between PROG and GND. At the moment current begins to flow through the MOSFET, a voltage of 12 V appears across it (input voltage V_{VCC} = 12 V), and the constant-power engine therefore allows a current of 2.44 A (equal to 29.3 W divided by 12 V) to flow. This current increases in inverse ratio as the drain-to-source voltage diminishes, so as to maintain a constant dissipation of 29.3 W. The constant-power engine adjusts the current by altering the reference signal fed to the current limit amplifier. The lower part of Figure 28 shows the measured power dissipated within the MOSFET, labeled *FET PWR*, remaining substantially constant during this period of operation, which ends when the current through the MOSFET reaches the current limit I_{LIM}. This behavior can be considered a form of foldback limiting, but unlike the standard linear form of foldback limiting, it allows the power device to operate near its maximum capability, thus reducing the start-up time and minimizing the size of the required MOSFET.

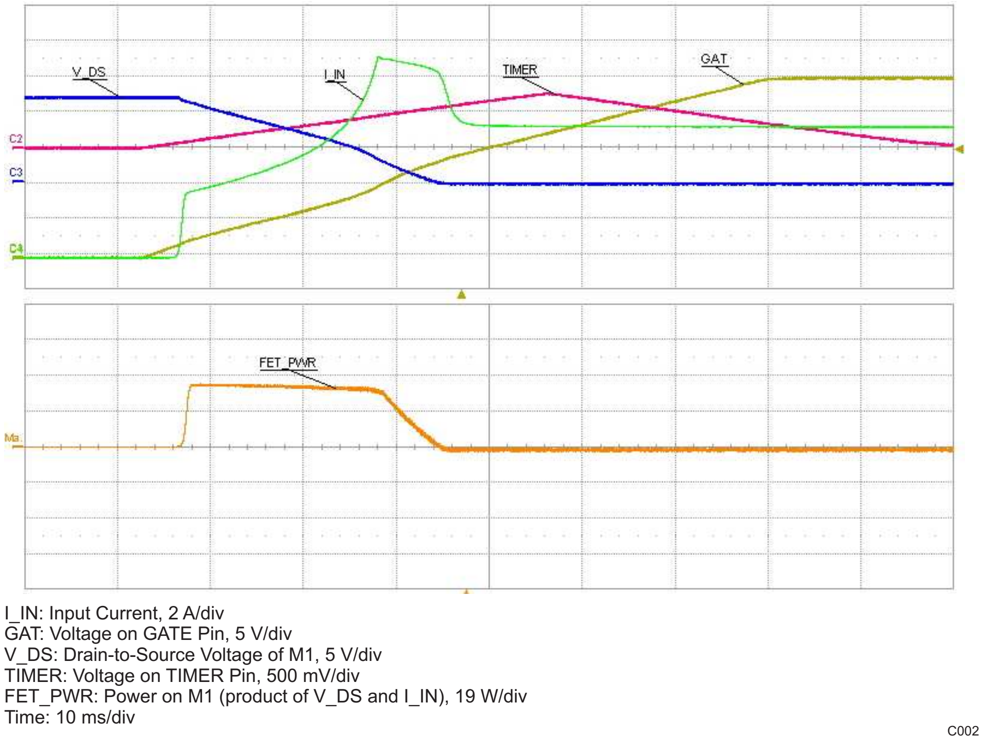


Figure 27. Computation of M_1 Power Stress During Start-Up

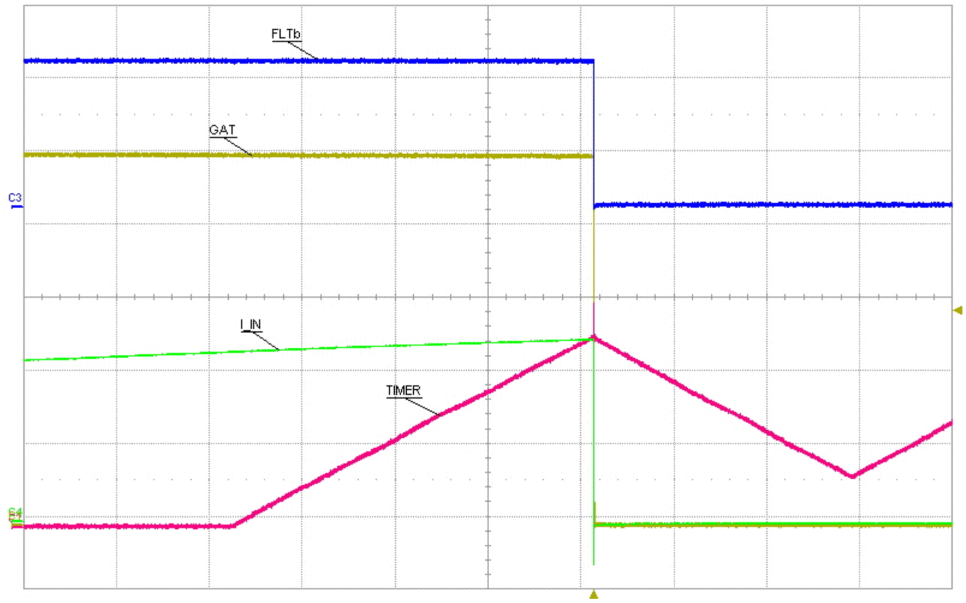
CIRCUIT BREAKER AND FAST TRIP

The TPS24710/11/12/13 monitors load current by sensing the voltage across R_{SENSE}. The TPS24710/11/12/13 incorporates two distinct thresholds: a current-limit threshold and a fast-trip threshold.

The functions of circuit breaker and fast-trip turn off are shown in Figure 28 through Figure 31.

Figure 28 shows the behavior of the TPS24710/11 when a fault in the output load causes the current passing through R_{SENSE} to increase to a value above the current limit but less than the fast-trip threshold. When the current exceeds the current-limit threshold, a current of approximately 10 µA begins to charge timing capacitor C_T. If the voltage on C_T reaches 1.35 V, then the external MOSFET is turned off. The TPS24710 latches off and the TPS24711 commences a restart cycle. In either event, fault pin FLTb pulls low to signal a fault condition. Overload between the current limit and the fast trip threshold is permitted for this period. This shutdown scheme is sometimes called an electronic circuit breaker.

The fast-trip threshold protects the system against a severe overload or a dead short circuit. When the voltage across the sense resistor R_{SENSE} exceeds the 60 mV fast-trip threshold, the GATE pin immediately pulls the external MOSFET gate to ground with approximately 1 A of current. This extremely rapid shutdown may generate disruptive transients in the system, in which case a low-value resistor inserted between the GATE pin and the MOSFET gate can be used to moderate the turn off current. The fast-trip circuit holds the MOSFET off for only a few microseconds, after which the TPS24710/11/12/13 turns back on slowly, allowing the current-limit feedback loop to take over the gate control of M_1. Then the hot-swap circuit goes into either latch mode (TPS24710/12) or auto-retry mode (TPS24711/13). Figure 30 and Figure 31 illustrate the behavior of the system implementing TPS24710/11 when the current exceeds the fast-trip threshold.



I_IN: Input Current, 5 A/div
GAT: Voltage on GATE Pin, 5 V/div
FLTb: Voltage on FLTb Pin, 2 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 2 ms/div

C003

Figure 28. Circuit Breaker Mode During Over Load Condition

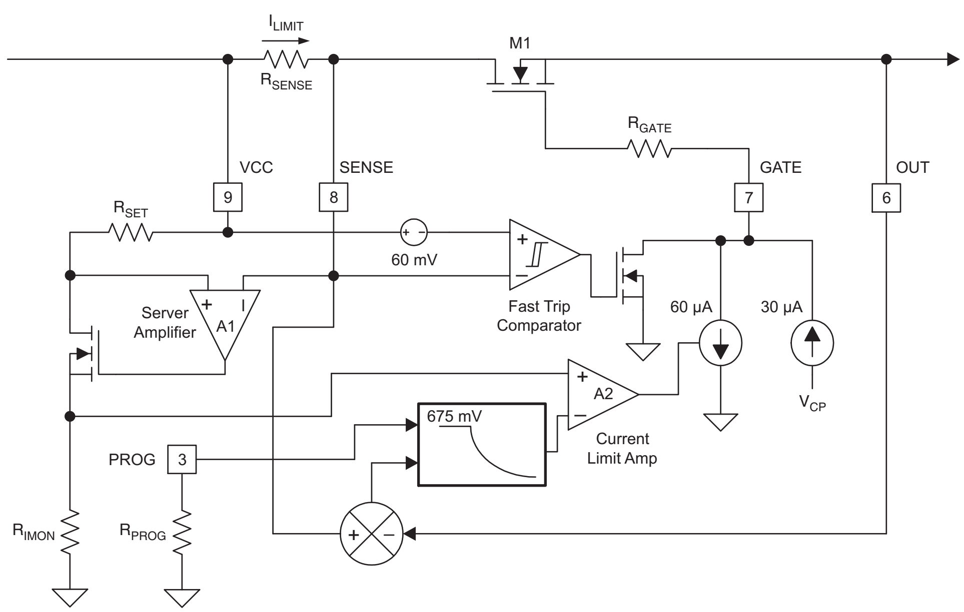


Figure 29. Partial Diagram of the TPS24710/11/12/13 With Selected External Components

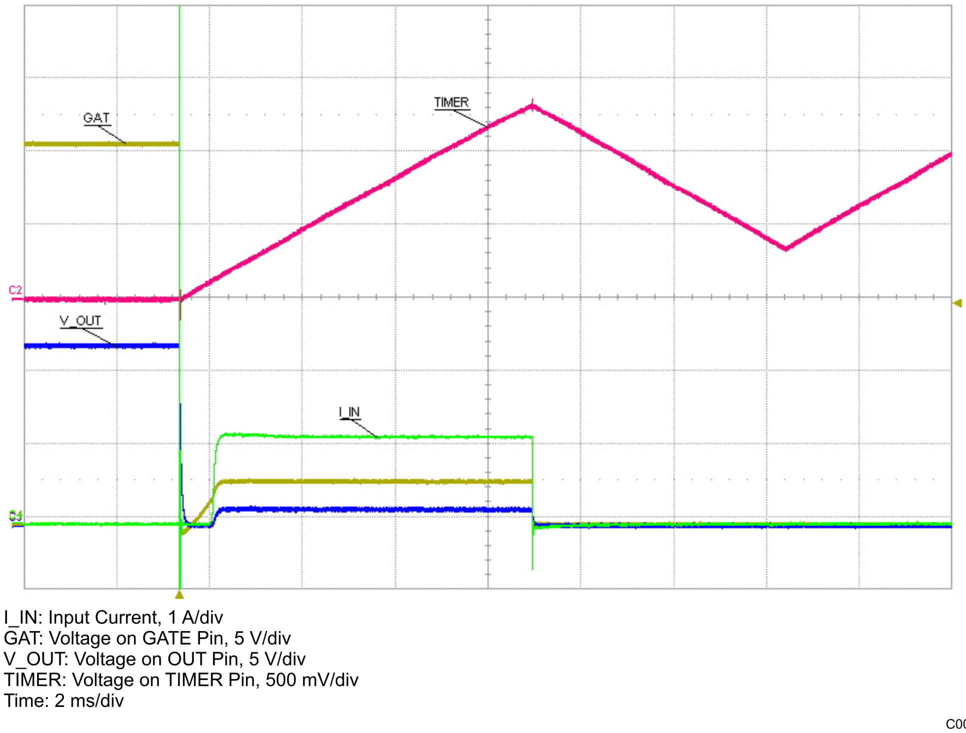


Figure 30. Current Limit During Output Load Short Circuit Condition (Overview)

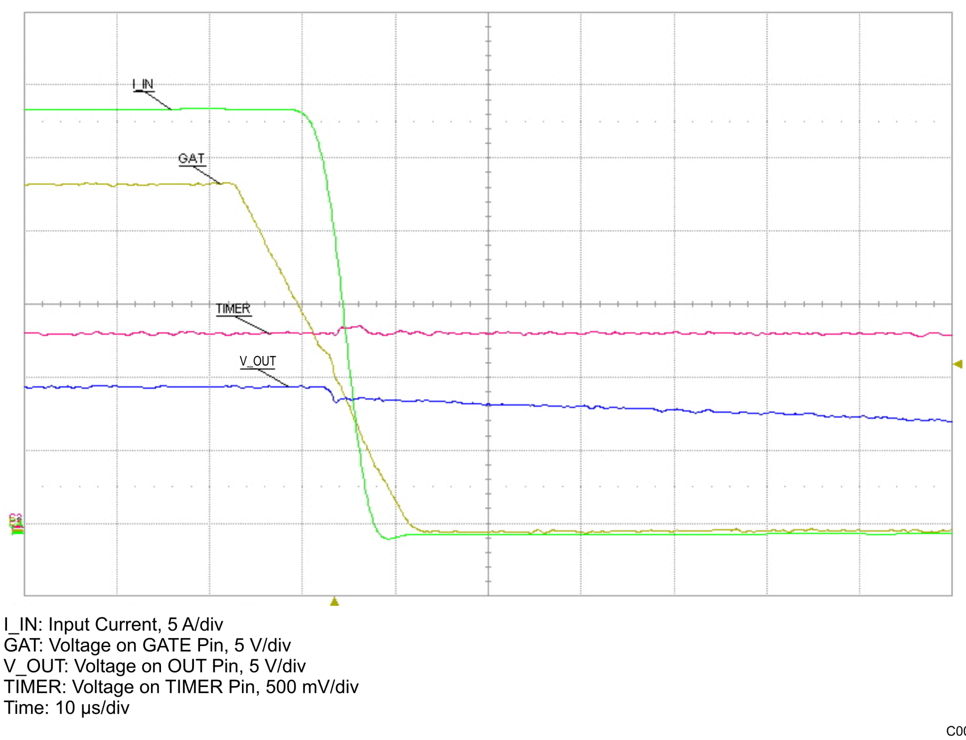
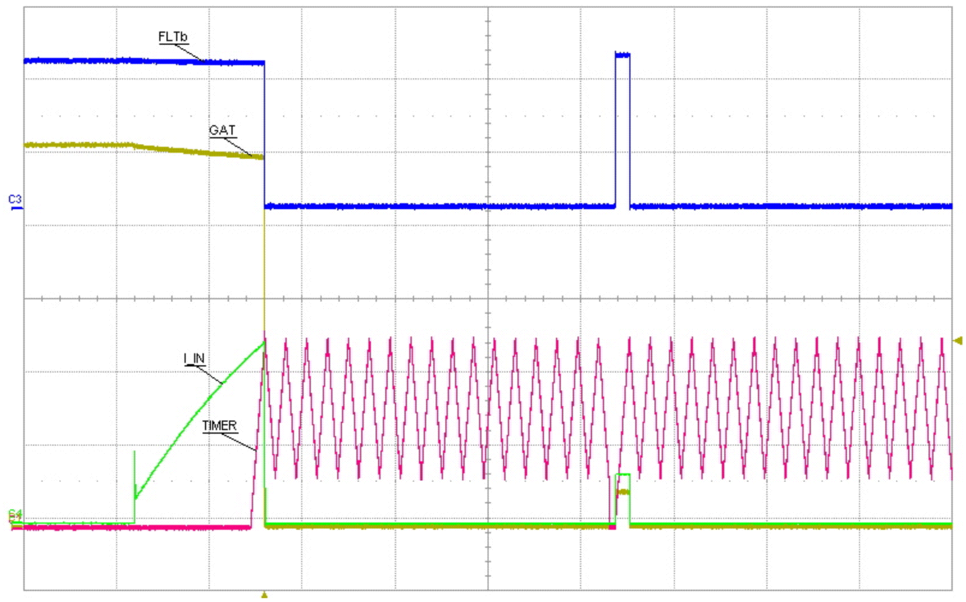


Figure 31. Current Limit During Output-Load Short-Circuit Condition (Onset)

AUTOMATIC RESTART

The TPS24711/13 automatically initiates a restart after a fault has caused it to turn off the external MOSFET M_1. Internal control circuits use C_T to count 16 cycles before re-enabling M_1 as shown in Figure 32 (TPS24711). This sequence repeats if the fault persists. The timer has a 1 : 1 charge-to-discharge current ratio. For the very first cycle, the TIMER pin starts from 0 V and rises to the upper threshold of 1.35 V and subsequently falls to 0.35 V before restarting. For the following 16 cycles, 0.35 V is used as the lower threshold. This small duty cycle often reduces the average short-circuit power dissipation to levels associated with normal operation and eliminates special thermal considerations for surviving a prolonged output short.



I_IN: Input Current, 5 A/div
GAT: Voltage on GATE Pin, 5 V/div
FLTb: Voltage on FLTb Pin, 2 V/div
TIMER: Voltage on TIMER Pin, 500 mV/div
Time: 50 ms/div

C006

Figure 32. Auto-Restart Cycle Timing

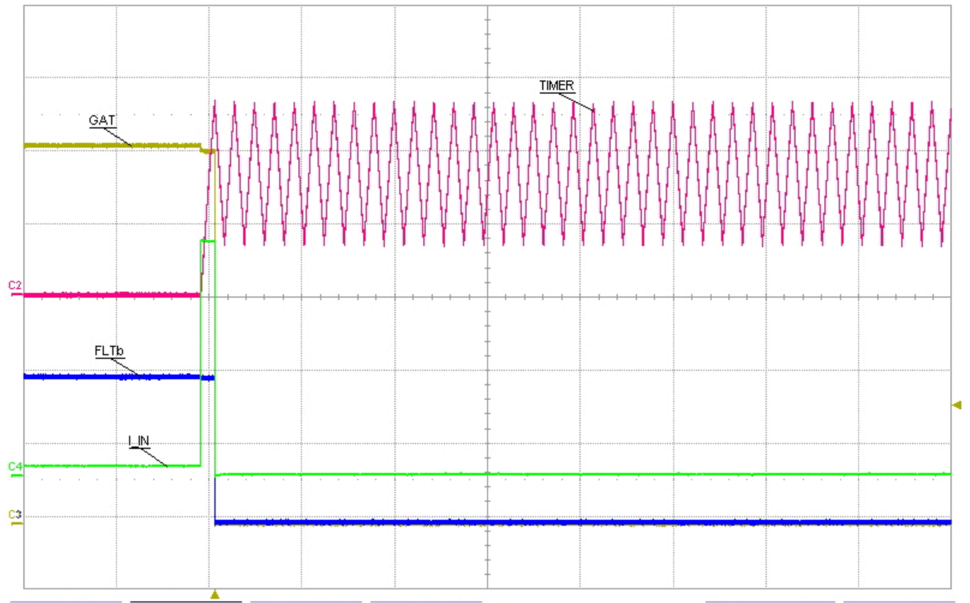


Figure 33. Latch After Overload Fault

PG, FLT, PGb, FLTb, AND TIMER OPERATIONS

The open-drain PG/PGb (PG is for TPS24712/13 and PGb is for TPS24710/11) output provides a deglitched end-of-inrush indication based on the voltage across M_1. PG/PGb is useful for preventing a downstream dc/dc converter from starting while its input capacitor C_{OUT} is still charging. PG goes active-high and PGb goes active-low about 3.4 ms after C_{OUT} is charged. This delay allows M_1 to fully turn on and any transients in the power circuits to end before the converter starts up. This type of sequencing prevents the downstream converter from demanding full current before the power-limiting engine allows the MOSFET to conduct the full current set by the current limit I_{LIM}. Failure to observe this precaution may prevent the system from starting. The pullup resistor shown on the PG/PGb pin in the typical application diagram on the front page is illustrative only; the actual connection to the converter depends on the application. The PG/PGb pin may indicate that inrush has ended before the MOSFET is fully enhanced, but the downstream capacitor will have been charged to substantially its full operating voltage. Care should be taken to ensure that the MOSFET on-resistance is sufficiently small to ensure that the voltage drop across this transistor is less than the minimum power-good threshold of 140 mV. After the hot-swap circuit successfully starts up, the PG pin can return to a low-impedance status and PGb to high-impedance status whenever the drain-to-source voltage of MOSFET M_1 exceeds its upper threshold of 340 mV, which presents the downstream converters a warning flag. This flag may occur as a result of overload fault, output short fault, input overvoltage, higher die temperature, or the GATE shutdown by UVLO and EN.

FLT/FLTb (FLT is for TPS24712/13 and FLTb is for TPS24710/11) is an indicator that the allowed fault-timer period during which the load current can exceed the programmed current limit (but not the fast-trip threshold) has expired. The fault timer starts when a current of approximately 10 µA begins to flow into the external capacitor, C_T, and ends when the voltage of C_T reaches TIMER upper threshold, i.e., 1.35 V. FLT goes high and FLTb pulls low at the end of the fault timer. Otherwise, FLT assumes a low-impedance state and FLTb a high-impedance state.

The fault-timer state requires an external capacitor C_T connected between the TIMER pin and GND pin. The length of the fault timer is the charging time of C_T from 0 V to its upper threshold of 1.35 V. The fault timer begins to count under any of the following three conditions:

1. In the inrush mode, TIMER begins to source current to the timer capacitor, C_T, when MOSFET M_1 is enabled. TIMER begins to sink current from the timer capacitor, C_T when $V_{(GATE\ -\ VCC)}$ exceeds the timer

activation voltage (see the *Inrush Operation* section). If $V_{(GATE\ -\ VCC)}$ does not reach the timer activation voltage before TIMER reaches 1.35 V, then the TPS24710/11/12/13 disables the external MOSFET M_1. After the MOSFET turns off, the timer goes into either latch mode (TPS24710/12) or retry mode (TPS24711/13).

2. In an overload fault, TIMER begins to source current to the timer capacitor, C_T, when the load current exceeds the programmed current limits. When the timer capacitor voltage reaches its upper threshold of 1.35 V, TIMER begins to sink current from the timer capacitor, C_T, and the GATE pin is pulled to ground. After the fault timer period, TIMER may go into latch mode (TPS24710/12) or retry mode (TPS24711/13).
3. In output short-circuit fault, TIMER begins to source current to the timer capacitor, C_T, when the load current exceeds the programmed current limits following a fast-trip shutdown of M_1. When the timer capacitor voltage reaches its upper threshold of 1.35 V, TIMER begins to sink current from the timer capacitor, C_T, and the GATE pin is pulled to ground. After the fault timer period, TIMER may go into latch mode (TPS24710/12) or retry mode (TPS24711/13).

If the fault current drops below the programmed current limit within the fault timer period, V_{TIMER} decreases and the pass MOSFET remains enabled.

The behaviors of TIMER are different in the latch mode (TPS24710/12) and retry mode (TPS24711/13). If the timer capacitor reaches the upper threshold of 1.35 V, then:

- In latch mode, the GATE remains low and the TIMER pin continues to charge and discharge the attached capacitor periodically until TPS24710/12 is disabled by UVLO or EN as shown in Figure 33.
- In retry mode, TIMER charges and discharges C_T between the lower threshold of 0.35 V and the upper threshold of 1.35 V for sixteen cycles before the TPS24711/13 attempts to re-start. The TIMER pin is pulled to GND at the end of the 16th cycle of charging and discharging and then ramps from 0 V to 1.35 V for the initial half-cycle in which the GATE pin sources current. This periodic pattern is stopped once the overload fault is removed or the TPS24711/13 is disabled by UVLO or EN.

OVERTEMPERATURE SHUTDOWN

The TPS24710/11/12/13 includes a built-in overtemperature shutdown circuit designed to disable the gate driver if the die temperature exceeds approximately 140°C. An overtemperature condition also causes the FLT, PG, FLTb and PGb pins to go to high-impedance states. Normal operation resumes once the die temperature has fallen approximately 10°C.

START-UP OF HOT-SWAP CIRCUIT BY VCC OR EN

The connection and disconnection between a load and the system bus are controlled by turning on and turning off the MOSFET, M_1.

The TPS24710/11/12/13 has two ways to turn on MOSFET M_1:

1. Increasing V_{VCC} above UVLO upper threshold while EN is already higher than its upper threshold sources current to the GATE pin. After an inrush period, TPS24710/11/12/13 fully turns on MOSFET M_1.
2. Increasing EN above its upper threshold while V_{VCC} is already higher than UVLO upper threshold sources current to the GATE pin. After an inrush period, TPS24710/11/12/13 fully turns on MOSFET M_1.

The EN pin can be used to start up the TPS24710/11/12/13 at a selected input voltage V_{VCC}.

To isolate the load from the system bus, the GATE pin sinks current and pulls the gate of MOSFET M_1 low. The MOSFET can be disabled by any of the following conditions: UVLO, EN, load current above current limit threshold, hard short at load, or OTSD. Three separate conditions pull down the GATE pin:

1. GATE is pulled down by an 11-mA current source when any of the following occurs.
   – The fault timer expires during an overload current fault (V_{SENSE} > 25 mV).
   – V_{EN} is below its falling threshold.
   – V_{VCC} drops below the UVLO threshold.
2. GATE is pulled down by a 1-A current source for 13.5 µs when a hard output short circuit occurs and $V_{(VCC\ -\ SENSE)}$ is greater than 60 mV, i.e., the fast-trip shutdown threshold. After fast-trip shutdown is complete, an 11-mA sustaining current ensures that the external MOSFET remains off.
3. GATE is discharged by a 20-kΩ resistor to GND if the chip die temperature exceeds the OTSD rising threshold.

DESIGN EXAMPLE: POWER-LIMITED START-UP

This design example assumes a 12-V system voltage with an operating tolerance of ±2 V. The rated load current is 10 A, corresponding to a dc load of 1.2 Ω. If the current exceeds 12 A, then the controller should shut down and then attempt to restart. Ambient temperatures may range from 20°C to 50°C. The load has a minimum input capacitance of 470 µF. Figure 34 shows a simplified system block diagram of the proposed application.

This design procedure seeks to control the junction temperature of MOSFET M_1 under both static and transient conditions by proper selection of package, cooling, $r_{DS(on)}$, current limit, fault timeout, and power limit. The design procedure further assumes that a unit running at full load and maximum ambient temperature experiences a brief input-power interruption sufficient to discharge C_{OUT}, but short enough to keep M_1 from cooling. A full C_{OUT} recharge then takes place. Adjust this procedure to fit your application and design criteria.

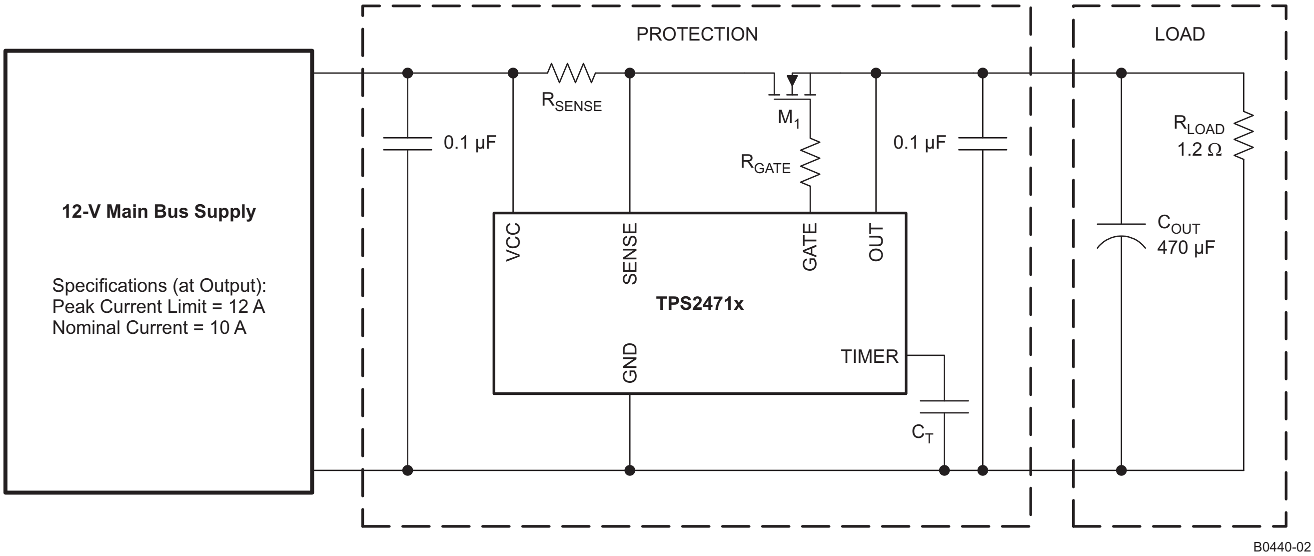


Figure 34. Simplified Block Diagram of the System Constructed in the Design Example

STEP 1. Choose R_{SENSE}

From the TPS24710/11/12/13 electrical specifications, the current-limit threshold voltage, $V_{(VCC-SENSE)}$, is around 25 mV. A resistance of 2 mΩ is selected for the peak current limit of 12 A, while dissipating only 200 mW at the rated 10-A current (see Equation 5). This represents a 0.17% power loss.

$$R_{SENSE} = \frac{V_{(VCC-SENSE)}}{I_{LIM}},$$

therefore,

$$R_{SENSE} = \frac{25\ mV}{12\ A} \approx 2\ m\Omega \tag{5}$$

STEP 2. Choose MOSFET M_1

The next design step is to select M_1. The TPS24710/11/12/13 is designed to use an N-channel MOSFET with a gate-to-source voltage rating of 20 V.

Devices with lower gate-to-source voltage ratings can be used if a Zener diode is connected so as to limit the maximum gate-to-source voltage across the transistor.

The next factor to consider is the drain-to-source voltage rating, $V_{DS(MAX)}$, of the MOSFET. Although the MOSFET only sees 12 V DC, it may experience much higher transient voltages during extreme conditions, such as the abrupt shutoff that occurs during a fast trip. A TVS may be required to limit inductive transients under such conditions. A transistor with a $V_{DS(MAX)}$ rating of at least twice the nominal input power-supply voltage is recommended regardless of whether a TVS is used or not.

Next select the on resistance of the transistor, $r_{DS(on)}$. The maximum on-resistance must not generate a voltage greater then the minimum power-good threshold voltage of 140 mV. Assuming a current limit of 12 A, a maximum $r_{DS(on)}$ of 11.67 mΩ is required. Also consider the effect of $r_{DS(on)}$ upon the maximum operating temperature $T_{J(MAX)}$ of the MOSFET. Equation 6 computes the value of $r_{DS(on)(MAX)}$ at a junction temperature of $T_{J(MAX)}$. Most manufacturers list $r_{DS(on)(MAX)}$ at 25°C and provide a derating curve from which values at other temperatures can be derived. Compute the maximum allowable on-resistance, $r_{DS(on)(MAX)}$, using Equation 6.

$$r_{DS(on)(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{I_{MAX}^{2} \times R_{\theta JA}},$$

therefore,

$$r_{DS(on)(MAX)} = \frac{150°C - 50°C}{(12\ A)^2 \times 51°C/W} = 13.6\ m\Omega \tag{6}$$

Taking these factors into consideration, the TI CSD16403Q5 was selected for this example. This transistor has a $V_{GS(MAX)}$ rating of 16 V, a $V_{DS(MAX)}$ rating of 25 V, and a maximum $r_{DS(on)}$ of 2.8 mΩ at room temperature. During normal circuit operation, the MOSFET can have up to 10 A flowing through it. The power dissipation of the MOSFET equates to 0.24 W and a 9.6°C rise in junction temperature. This is well within the data sheet limits for the MOSFET. The power dissipated during a fault (e.g., output short) is far larger than the steady-state power. The power handling capability of the MOSFET must be checked during fault conditions.

STEP 3. Choose Power-Limit Value, P_{LIM}, and R_{PROG}

MOSFET M_1 dissipates large amounts of power during inrush. The power limit P_{LIM} of the TPS24710/11/12/13 should be set to prevent the die temperature from exceeding a short-term maximum temperature, $T_{J(MAX)2}$. The short-term $T_{J(MAX)2}$ could be set as high as 130°C while still leaving ample margin to the usual manufacturer's rating of 150°C. Equation 7 is an expression for calculating P_{LIM},

$$P_{LIM} \le 0.8 \times \frac{T_{J(MAX)2} - \left[\left(I_{MAX}^{2} \times r_{DS(on)} \times R_{\theta CA}\right) + T_{A(MAX)}\right]}{R_{\theta JC}},$$

therefore,

$$P_{LIM} \le 0.8 \times \frac{130°C - \left[\left((12\ A)^2 \times 0.002\ \Omega \times (51°C/W - 1.8°C/W)\right) + 50°C\right]}{1.8°C/W} = 29.3\ W \tag{7}$$

where $R_{\theta JC}$ is the junction-to-case thermal resistance of the MOSFET, $r_{DS(on)}$ is the resistance at the maximum operating temperature, and the factor of 0.8 represents the tolerance of the constant-power engine. For an ambient temperature of 50°C, the calculated maximum P_{LIM} is 29.3 W. From Equation 1, a 53.6-kΩ, 1% resistor is selected for R_{PROG} (see Equation 8).

$$R_{PROG} = \frac{3125}{P_{LIM} + R_{SENSE}}$$

therefore,

$$R_{PROG} = \frac{3125}{29.3\ W \times 0.002\ \Omega} = 53.15\ k\Omega \tag{8}$$

$V_{SNS\text{-}PL\_MIN}$ is the minimum sense voltage during power limit operation. Due to offsets of internal amplifiers, programmed power limit (P_{LIM}) accuracy degrades at low $V_{SNS\text{-}PL\_MIN}$ and could cause start-up issues. To ensure reliable operation, verify that $V_{SNS,PL,MIN}$ > 3 mV using Equation 9.

$$V_{SNS-PL\_MIN} = \frac{P_{LIM} \times R_{SENSE}}{V_{IN\_MAX}} = \frac{29.3\ W \times 2\ m\Omega}{14\ V} = 4.19\ mV\ (> 3\ mV) \tag{9}$$

STEP 4. Choose Output Voltage Rising Time, t_{ON}, C_T

The maximum output voltage rise time, t_{ON}, set by the timer capacitor C_T must suffice to fully charge the load capacitance C_{OUT} without triggering the fault circuitry. Equation 10 defines t_{ON} for two possible inrush cases. Assuming that only the load capacitance draws current during start-up,

$$t_{ON} = \begin{cases} \dfrac{C_{OUT} \times P_{LIM}}{2 \times I_{LIM}^2} + \dfrac{C_{OUT} \times V_{VCC(MAX)}^2}{2 \times P_{LIM}} - \dfrac{C_{OUT} \times V_{VCC(MAX)}}{I_{LIM}} & \text{if} \quad P_{LIM} < I_{LIM} \times V_{VCC(MAX)} \\ \dfrac{C_{OUT} \times V_{VCC(MAX)}}{I_{LIM}} & \text{if} \quad P_{LIM} > I_{LIM} \times V_{VCC(MAX)} \end{cases}$$

therefore,

$$t_{ON} = \frac{470\ \mu F \times 29.3\ W}{2 \times (12\ A)^2} + \frac{470\ \mu F \times (12\ V)^2}{2 \times 29.3\ W} - \frac{470\ \mu F \times 12\ V}{12\ A} = 0.614\ ms \tag{10}$$

The next step is to determine the minimum fault-timer period. In Equation 10, the output rise time is t_{ON}. This is the amount of time it takes to charge the output capacitor up to the final output voltage. However, the fault timer uses the difference between the input voltage and the gate voltage to determine if the TPS24710/11/12/13 is still in inrush limit. The fault timer continues to run until V_{GS} rises 5.9 V (for V_{VCC} = 12 V) above the input voltage. Some additional time must be added to the charge time to account for this additional gate voltage rise. The minimum fault time can be calculated using Equation 11,

$$t_{FLT} = t_{ON} + \frac{5.9\ V \times C_{ISS}}{I_{GATE}},$$

therefore,

$$t_{FLT} = 0.614\ ms + \frac{5.9\ V \times 2040\ pF}{20\ \mu A} = 1.22\ ms \tag{11}$$

where C_{ISS} is the MOSFET input capacitance and I_{GATE} is the minimum gate sourcing current of TPS24710/11/12/13, or 20 μA. Using the example parameters in Equation 11 and the CSD16403Q5 data sheet (SLPS201) leads to a minimum fault time of 1.22 ms. This time is derived considering the tolerances of C_{OUT}, C_{ISS}, I_{LIM}, P_{LIM}, I_{GATE}, and $V_{VCC(MAX)}$. The fault timer must be set to a value higher than 1.22 ms to avoid turning off during start-up, but lower than any maximum fault time limit determined by the SOA curve (see Figure 35) derated for operating junction temperature.

For this example, select 7 ms to allow for variation of system parameters such as temperature, load, component tolerance, and input voltage. The timing capacitor is calculated in Equation 4 as 52 nF. Selecting the next-highest standard value, 56 nF, yields a 7.56-ms fault time (see Equation 12).

$$C_T = \frac{10\ \mu A}{1.35\ V} \times t_{FLT},$$

therefore,

$$C_T = \frac{10\ \mu A}{1.35\ V} \times 7\ ms = 52\ nF \tag{12}$$

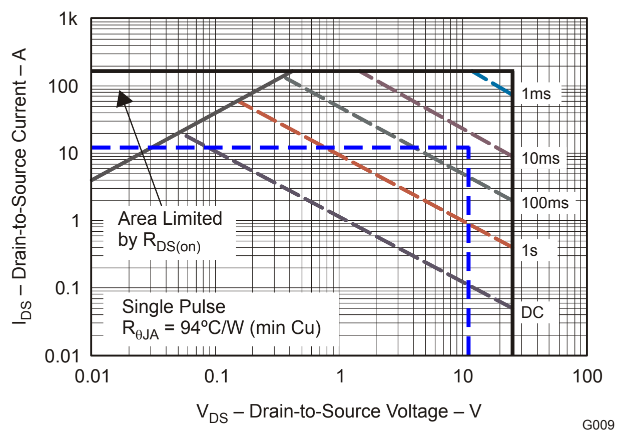


Figure 35. CSD16403Q5 SOA Curve

STEP 5. Calculate the Retry-Mode Duty Ratio

In retry mode, the TPS24711/13 is on for one charging cycle and off for 16 charge/discharge cycles, as can be seen in Figure 32. The first C_T charging cycle is from 0 V to 1.35 V, which gives 7.56 ms. The first C_T discharging cycle is from 1.35 V to 0.35 V, which gives 5.6 ms. Therefore, the total time is 7.56 ms + 33 × 5.6 ms = 192.36 ms. As a result, the retry mode duty ratio is 7.56 ms/192.36 ms = 3.93%.

STEP 6. Select R_1 and R_2 for UV

Next, select the values of the UV resistors, R_1 and R_2, as shown in the typical application diagram on the front page. From the TPS24710/11/12/13 electrical specifications, $V_{ENTHRESH}$ = 1.35 V. The V_{UV} is the undervoltage trip voltage, which for this example equals 10.7 V.

$$V_{ENTHRESH} = \frac{R_2}{R_1 + R_2} \times V_{VCC} \tag{13}$$

Assume R_1 is 130 kΩ and use Equation 13 to solve for the R_2 value of 18.7 kΩ.

STEP 7. Choose R_{GATE}, R_4, R_5 and C_1

In the typical application diagram on the front page, the gate resistor, R_{GATE}, is intended to suppress high-frequency oscillations. A resistor of 10 Ω will serve for most applications, but if M_1 has a C_{ISS} below 200 pF, then 33 Ω is recommended. Applications with larger MOSFETs and very short wiring may not require R_{GATE}. R_4 and R_5 are required only if PGb and FLTb are used; these resistors serve as pullups for the open-drain output drivers. The current sunk by each of these pins should not exceed 2 mA (see the RECOMMENDED OPERATING CONDITIONS table). C_1 is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise while in the disabled state. Where acceptable, a value in the range of 0.001 µF to 0.1 µF is recommended.

ALTERNATIVE DESIGN EXAMPLE: GATE CAPACITOR (dV/dt) CONTROL IN INRUSH MODE

The TPS24710/11/12/13 can be used in applications that expect a constant inrush current. This current is controlled by a capacitor connected from the GATE terminal to GND. A resistor of 1 kΩ placed in series with this capacitor will prevent it from slowing a fast-turnoff event. In this mode of operation, M_1 operates as a source follower, and the slew rate of the output voltage approximately equals the slew rate of the gate voltage (see Figure 36).

To implement a constant-inrush-current circuit, choose the time to charge, Δt, using Equation 14,

$$\Delta t = \frac{C_{OUT} \times V_{VCC}}{I_{CHG}} \tag{14}$$

where C_{OUT} is the output capacitance, V_{VCC} is the input voltage, and I_{CHG} is the desired charge current. Choose $I_{CHG} < P_{LIM} / V_{VCC}$ to prevent power limiting from affecting the desired current.

To select the gate capacitance, use Equation 15. I_{GATE} is the nominal gate charge current. This equation assumes that the MOSFET C_{GD} is the controlling element as the gate and output voltage rise. C_{GD} is non-linear with applied V_{DG}. An averaged estimate may be made using the MOSFET V_{GS} vs Q_G curve. Divide the charge accumulated during the plateau region by the plateau V_{GS} to get C_{RS}.

$$C_{GATE} = \left(I_{GATE} \times \frac{\Delta t}{V_{VCC}} \right) - C_{RS} \tag{15}$$

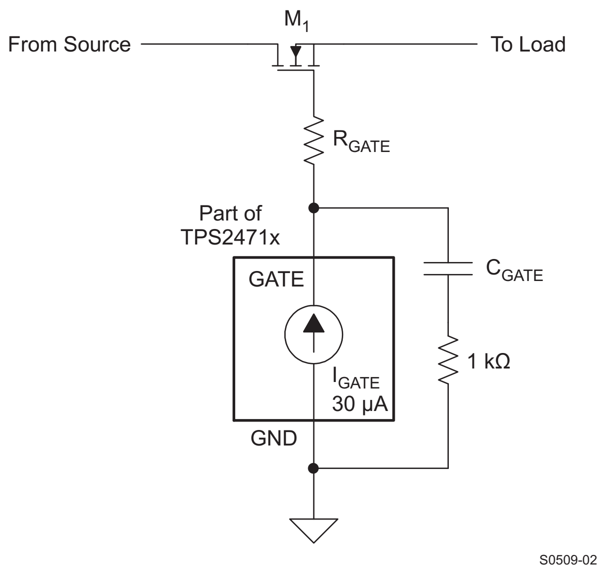


Figure 36. Gate Capacitor (dV/dt) Control Inrush Mode.

ADDITIONAL DESIGN CONSIDERATIONS

Use of PG/PGb

Use the PG/PGb pin to control and coordinate a downstream dc/dc converter. If this is not done, then a long time delay is needed to allow C_{OUT} to fully charge before the converter starts. An undesirable latch-up condition can be created between the TPS24710/11/12/13 output characteristic and the dc/dc converter input characteristic if the converter starts while C_{OUT} is still charging; the PG/PGb pin is one way to avoid this

Output Clamp Diode

Inductive loads on the output may drive the OUT pin below GND when the circuit is unplugged or during a current-limit event. The OUT pin ratings can be satisfied by connecting a diode from OUT to GND. The diode should be selected to control the negative voltage at the full short-circuit current. Schottky diodes are generally recommended for this application.

Gate Clamp Diode

The TPS24710/11/12/13 has a relatively well-regulated gate voltage of 12 V to 15.5 V with a supply voltage V_{VCC} higher than 4 V. A small clamp Zener from gate to source of M_1 is recommended if V_{GS} of M_1 is rated below 12 V. A series resistance of several hundred ohms or a series silicon diode is recommended to prevent the output capacitance from discharging through the gate driver to ground.

High-Gate-Capacitance Applications

Gate voltage overstress and abnormally large fault current spikes can be caused by large gate capacitance. An external gate clamp Zener diode is recommended to assist the internal Zener if the total gate capacitance of M_1 exceeds about 4000 pF. When gate capacitor dV/dt control is used, a 1-kΩ resistor in series with C_{GATE} is recommended (see Figure 36). If the series R-C combination is used for MOSFETs with C_{ISS} less than 3000 pF, then a Zener diode is not necessary.

Bypass Capacitors

It is a good practice to provide low-impedance ceramic capacitor bypassing of the VCC and OUT pins. Values in the range of 10 nF to 1 µF are recommended. Some system topologies are insensitive to the values of these capacitors; however, some are not and require minimization of the value of the bypass capacitor. Input capacitance on a plug-in board may cause a large inrush current as the capacitor charges through the low-impedance power bus when inserted. This stresses the connector contacts and causes a short voltage sag on the input bus. Small amounts of capacitance (e.g., 10 nF to 0.1 µF) are often tolerable in these systems.

Output Short-Circuit Measurements

Repeatable short-circuit testing results are difficult to obtain. The many details of source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet; every setup differs.

Layout Considerations

TPS24710/11/12/13 applications require careful attention to layout to ensure proper performance and to minimize susceptibility to transients and noise. In general, all traces should be as short as possible, but the following list deserves first consideration:

- Decoupling capacitors on VCC pin should have minimal trace lengths to the pin and to GND.
- Traces to VCC and SENSE must be short and run side-by-side to maximize common-mode rejection. Kelvin connections should be used at the points of contact with R_{SENSE}. (see Figure 37).
- Power path connections should be as short as possible and sized to carry at least twice the full load current, more if possible.
- Protection devices such as snubbers, TVS, capacitors, or diodes should be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, the protection Schottky diode shown in the typical application diagram on the front page of this data sheet should be physically close to the OUT pin.

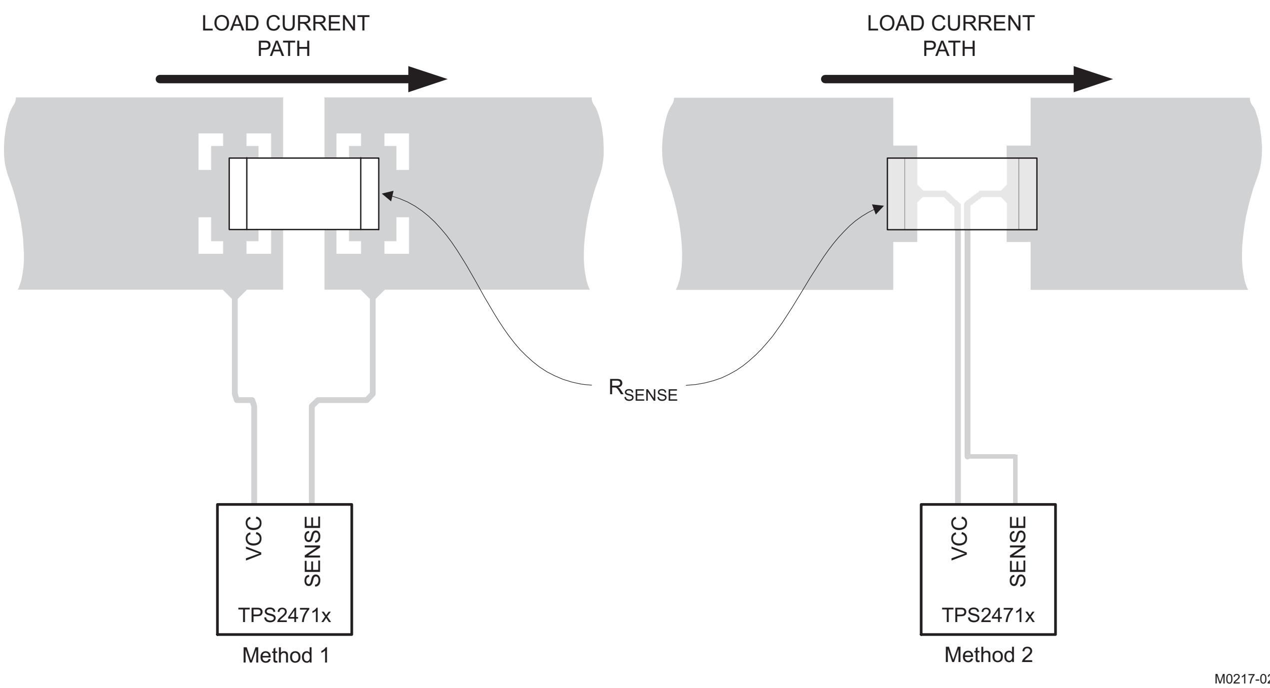


Figure 37. Recommended R_{SENSE} Layout

REVISION HISTORY

Changes from Revision A (March 2011) to Revision B **Page**

Changes from Revision B (April 2011) to Revision C **Page**

Changes from Revision C (May 2011) to Revision D **Page**

Changes from Revision D (November 2013) to Revision E **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS24710DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	24710	Samples
TPS24710DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	24710	Samples
TPS24711DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	24711	Samples
TPS24711DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	24711	Samples
TPS24712DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	24712	Samples
TPS24712DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	24712	Samples
TPS24713DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	24713	Samples
TPS24713DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	24713	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

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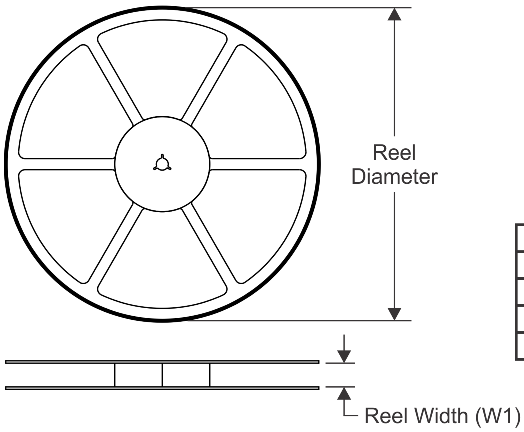
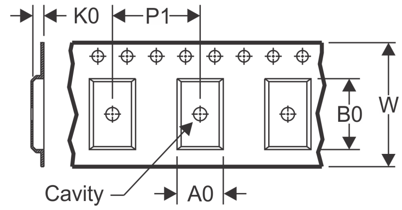
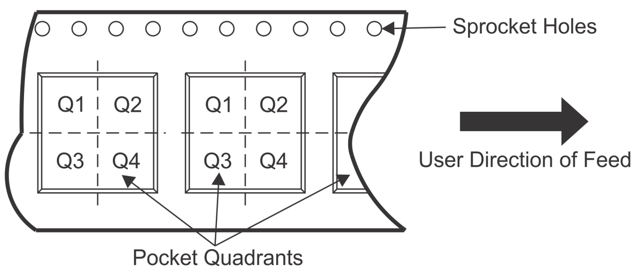


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

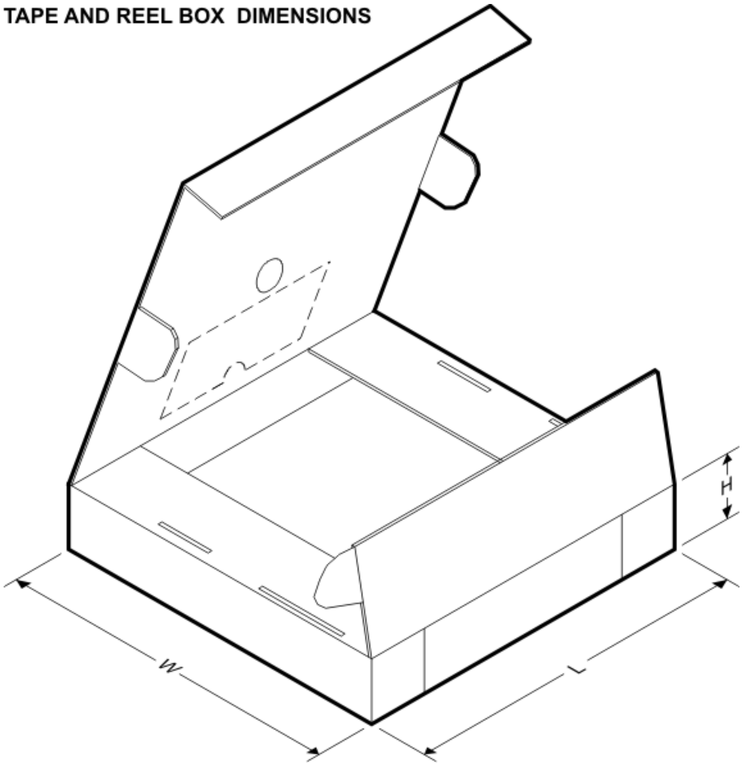
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS24710DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS24711DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS24712DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS24713DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

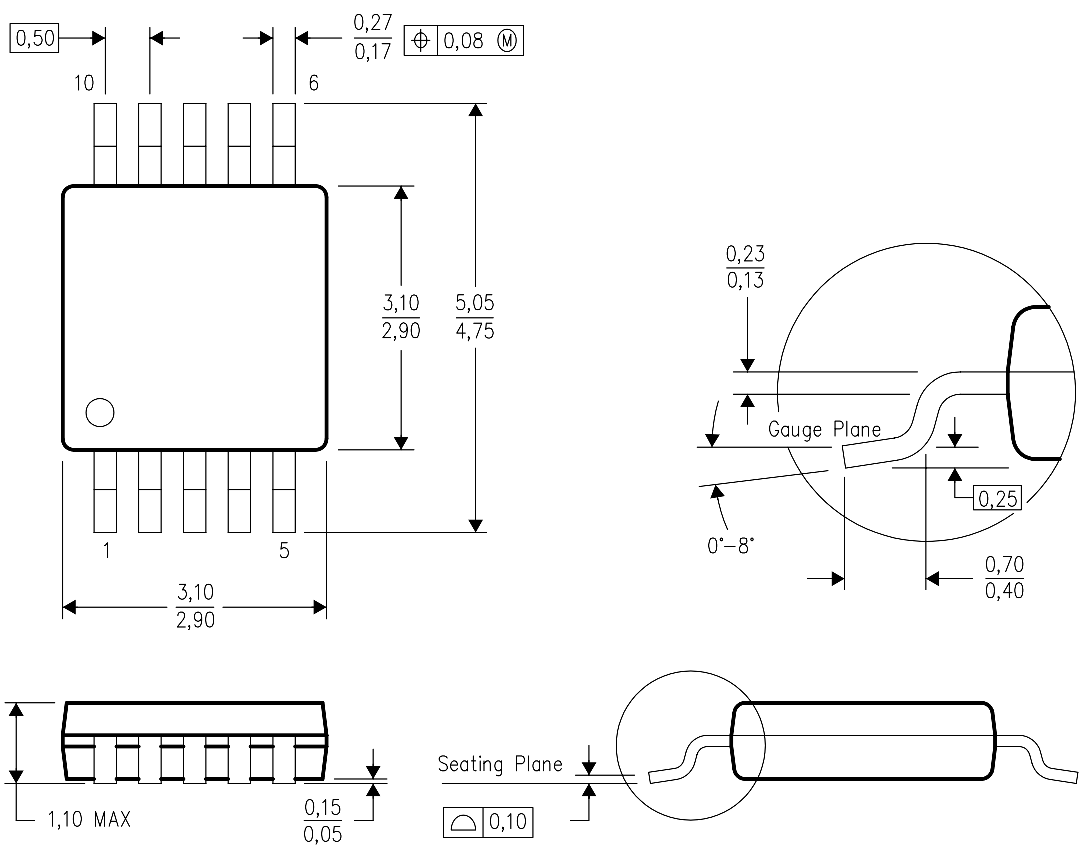
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS24710DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TPS24711DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TPS24712DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TPS24713DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0

DGS (S-PDSO-G10) PLASTIC SMALL-OUTLINE PACKAGE



4073272/C 02/04

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation BA.

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