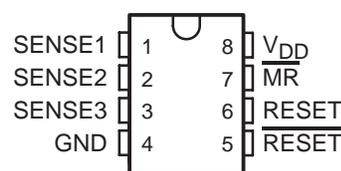


- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Triple Supervisory Circuits for DSP and Processor-Based Systems**
- **Power-On Reset Generator With Fixed Delay Time of 200 ms, No External Capacitor Needed**
- **Temperature-Compensated Voltage Reference**
- **Maximum Supply Current of 40 μA**
- **Supply Voltage Range . . . 2 V to 6 V**
- **Defined  $\overline{\text{RESET}}$  Output from  $V_{\text{DD}} \geq 1.1 \text{ V}$**
- **SO-8 and MSOP-8 Packages**

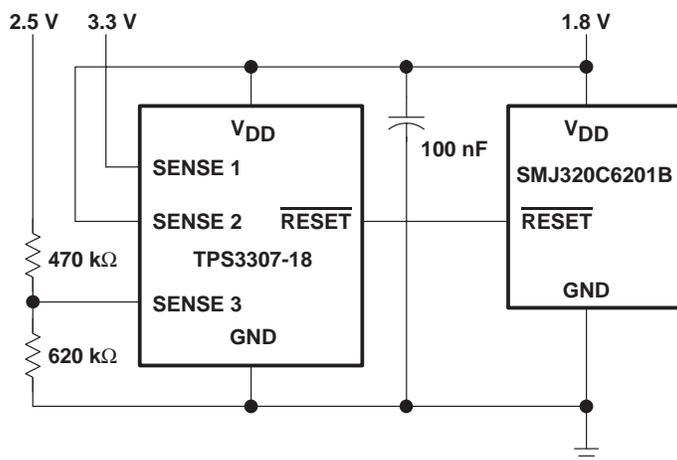
† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D or DGN PACKAGE  
(TOP VIEW)



## typical applications

Figure 1 lists some of the typical applications for the TPS3307 family, and a schematic diagram for a processor-based system application. This application uses Texas Instruments part numbers TPS3307-18 and SMJ320C6201B.



- **Military applications using DSPs, Microcontrollers or Microprocessors**
- **Industrial Equipment**
- **Programmable Controls**
- **Military Systems**

Figure 1. Applications Using the TPS3307-18

## description

The TPS3307-xx family is a series of micropower supply voltage supervisors designed for circuit initialization primarily in DSP and processor-based systems which require more than one supply voltage.

The TPS3307-18 and TPS3307-33 are designed for monitoring three independent supply voltages: 3.3 V/1.8 V/adj and 5V/3.3V/adj, respectively. The adjustable SENSE input allows the monitoring of any supply voltage >1.25 V.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# TPS3307-18-EP, TPS3307-33-EP TRIPLE PROCESSOR SUPERVISORS

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## description (continued)

The various supply voltage supervisors are designed to monitor the nominal supply voltage as shown in the following supply voltage monitoring table.

**SUPPLY VOLTAGE MONITORING**

| DEVICE     | NOMINAL SUPERVISED VOLTAGE |        |              | THRESHOLD VOLTAGE (TYP) |        |         |
|------------|----------------------------|--------|--------------|-------------------------|--------|---------|
|            | SENSE1                     | SENSE2 | SENSE3       | SENSE1                  | SENSE2 | SENSE3  |
| TPS3307-18 | 3.3 V                      | 1.8 V  | User defined | 2.93 V                  | 1.68 V | 1.25 V† |
| TPS3307-33 | 5 V                        | 3.3 V  | User defined | 4.55 V                  | 2.93 V | 1.25 V† |

† The actual sense voltage has to be adjusted by an external resistor divider according to the application requirements.

During power-on,  $\overline{\text{RESET}}$  is asserted when the supply voltage  $V_{DD}$  becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors the SENSEn inputs and keeps  $\overline{\text{RESET}}$  active as long as SENSEn remain below the threshold voltage  $V_{IT+}$ .

An internal timer delays the return of the  $\overline{\text{RESET}}$  output to the inactive state (high) to ensure proper system reset. The delay time,  $t_{dtyp} = 200$  ms, starts after all SENSEn inputs have risen above the threshold voltage  $V_{IT+}$ . When the voltage at any SENSE input drops below the threshold voltage  $V_{IT-}$ , the  $\overline{\text{RESET}}$  output becomes active (low) again.

The TPS3307-xx family of devices incorporates a manual reset input,  $\overline{\text{MR}}$ . A low level at  $\overline{\text{MR}}$  causes  $\overline{\text{RESET}}$  to become active. In addition to the active-low  $\overline{\text{RESET}}$  output, the TPS3307-xx family includes an active-high RESET output.

The devices are available in either 8-pin MSOP or a standard 8-pin SO packages and are characterized for operation over a temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

## ORDERING INFORMATION

| $T_A$  | PACKAGE‡                            |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|--|-------------------------------------|---------------|-----------------------|------------------|
| $-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$ | Small Outline (D)                   | Tape and Reel | TPS3307-18MDREP       | 30718E           |
|  | PowerPad $\mu$ -Small Outline (DGN) | Tape and Reel | TPS3307-33MDGNREP     | BNP              |

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

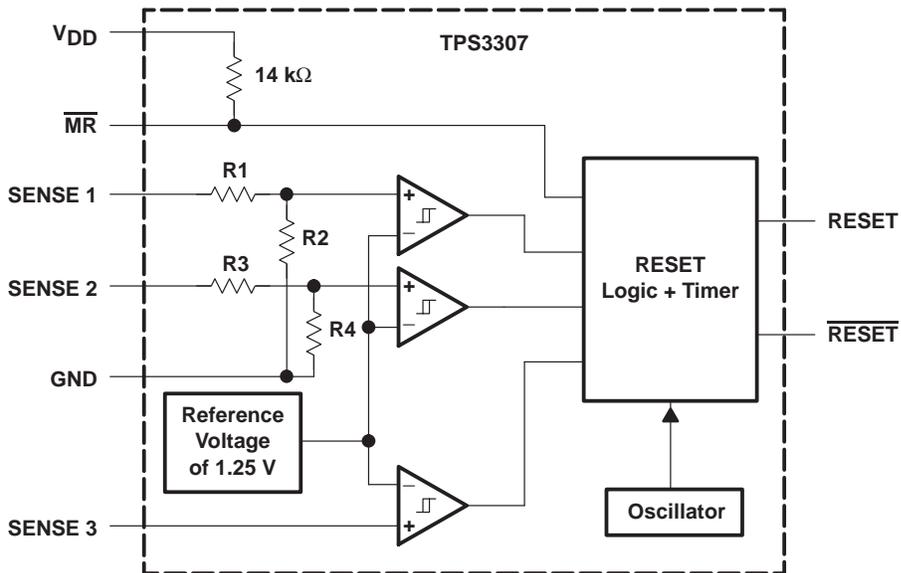
## FUNCTION/TRUTH TABLES

| $\overline{\text{MR}}$ | $\text{SENSE1} > V_{IT1}$ | $\text{SENSE2} > V_{IT2}$ | $\text{SENSE3} > V_{IT3}$ | $\overline{\text{RESET}}$ | RESET |
|------------------------|---------------------------|---------------------------|---------------------------|---------------------------|-------|
| L                      | X                         | X                         | X                         | L                         | H     |
| H                      | 0                         | 0                         | 0                         | L                         | H     |
| H                      | 0                         | 0                         | 1                         | L                         | H     |
| H                      | 0                         | 1                         | 0                         | L                         | H     |
| H                      | 0                         | 1                         | 1                         | L                         | H     |
| H                      | 1                         | 0                         | 0                         | L                         | H     |
| H                      | 1                         | 0                         | 1                         | L                         | H     |
| H                      | 1                         | 1                         | 0                         | L                         | H     |
| H                      | 1                         | 1                         | 1                         | H                         | L     |

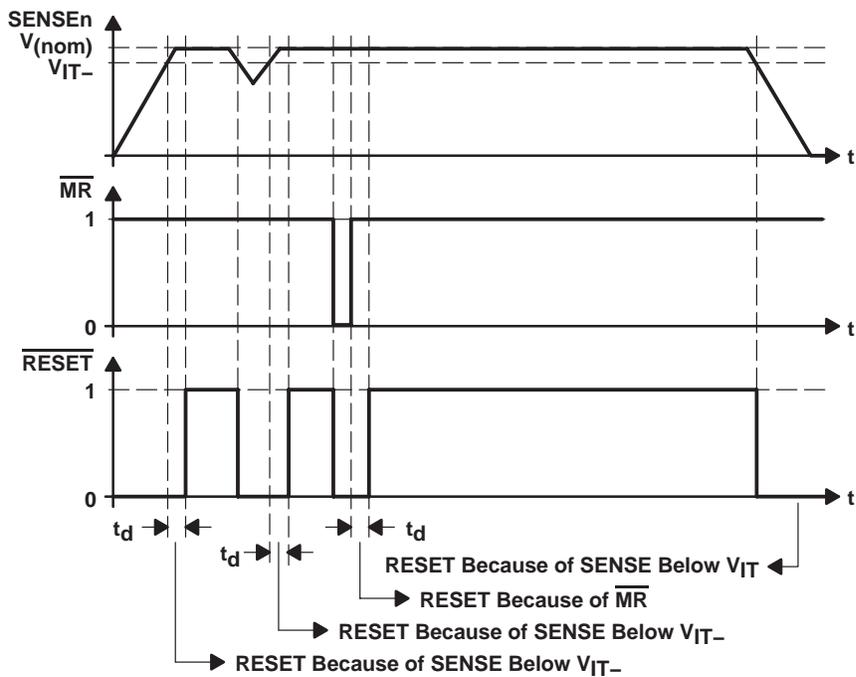
X = Don't care



functional block diagram



timing diagram



# TPS3307-18-EP, TPS3307-33-EP TRIPLE PROCESSOR SUPERVISORS

SGLS140A – NOVEMBER 2002 – REVISED AUGUST 2005

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|   |                |
|---|----------------|
| Supply voltage, $V_{DD}$ (see Note 1)                           | 7 V            |
| All other pins (see Note 1)                                     | -0.3 V to 7 V  |
| Maximum low output current, $I_{OL}$                            | 5 mA           |
| Maximum high output current, $I_{OH}$                           | -5 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ )   | $\pm 20$ mA    |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ )  | $\pm 20$ mA    |
| Maximum junction temperature, $T_J$                             | 150°C          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2) D package | 126°C/W        |
| DGN package   | 58.4°C/W       |
| Operating free-air temperature range, $T_A$                     | -55°C to 125°C |
| Storage temperature range, $T_{stg}$ (see Note 3)               | -65°C to 150°C |
| Soldering temperature   | 260°C          |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than  $t = 1000$  h continuously.

NOTE 2: The thermal impedance,  $\theta_{JA}$ , for the D package is determined for JEDEC high-K PCB (JESD51-7). The thermal impedance value for the DGN package is determined for Texas Instruments recommended assembly for PowerPAD packages. See Texas Instruments technical briefs SLMA002 and SLMA004 for more information about utilizing the PowerPAD thermally enhanced package. Thermal impedance,  $\theta_{JA}$ , values for the D and DGN packages using JEDEC low-K PCB (JESD51-3) are 215°C/W and 296°C/W, respectively.

NOTE 3: Long-term, high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See <http://www.ti.com/sc/ep> for more information.

## recommended operating conditions at specified temperature range

|  | MIN                 | MAX                         | UNIT |
|--|---------------------|-----------------------------|------|
| Supply voltage, $V_{DD}$   | 2                   | 6                           | V    |
| Input voltage at $\overline{MR}$ and SENSE3, $V_I$                           | 0                   | $V_{DD}+0.3$                | V    |
| Input voltage at SENSE1 and SENSE2, $V_I$                                    | 0                   | $(V_{DD}+0.3)V_{IT}/1.25$ V | V    |
| High-level input voltage at $\overline{MR}$ , $V_{IH}$                       | $0.7 \times V_{DD}$ |                             | V    |
| Low-level input voltage at $\overline{MR}$ , $V_{IL}$                        | $0.3 \times V_{DD}$ |                             | V    |
| Input transition rise and fall rate at $\overline{MR}$ , $\Delta t/\Delta V$ | 50                  |                             | ns/V |
| Operating free-air temperature range, $T_A$                                  | -55                 | 125                         | °C   |



# TPS3307-18-EP, TPS3307-33-EP TRIPLE PROCESSOR SUPERVISORS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                           |   | TEST CONDITIONS  | MIN   | TYP            | MAX  | UNIT |   |      |
|-------------------------------------|---|--|---|----------------|------|------|---|------|
| V <sub>OH</sub>                     | High-level output voltage                           | V <sub>DD</sub> = 2 V to 6 V, I <sub>OH</sub> = -20 μA | V <sub>DD</sub> - 0.2 V   |                |      | V    |   |      |
|                                     |   | V <sub>DD</sub> = 3.3 V, I <sub>OH</sub> = -2 mA       | V <sub>DD</sub> - 0.4 V   |                |      |      |   |      |
|                                     |   | V <sub>DD</sub> = 6 V, I <sub>OH</sub> = -3 mA         | V <sub>DD</sub> - 0.4 V   |                |      |      |   |      |
| V <sub>OL</sub>                     | Low-level output voltage                            | V <sub>DD</sub> = 2 V to 6 V, I <sub>OL</sub> = 20 μA  | 0.2   |                |      | V    |   |      |
|                                     |   | V <sub>DD</sub> = 3.3 V, I <sub>OL</sub> = 2 mA        | 0.4   |                |      |      |   |      |
|                                     |   | V <sub>DD</sub> = 6 V, I <sub>OL</sub> = 3 mA          | 0.4   |                |      |      |   |      |
| Power-up reset voltage (see Note 4) |   | V <sub>DD</sub> ≥ 1.1 V, I <sub>OL</sub> = 20 μA       | 0.4   |                |      | V    |   |      |
| V <sub>IT-</sub>                    | Negative-going input threshold voltage (see Note 5) | V <sub>DD</sub> = 2 V to 6 V                           | SENSE3  | 1.2            | 1.25 | 1.29 | V |      |
|                                     |   |  | SENSE1, SENSE2  | VSENSE = 1.8 V | 1.6  | 1.68 |   | 1.73 |
|                                     |   |  |   | VSENSE = 3.3 V | 2.8  | 2.93 |   | 3.02 |
|                                     |   |  |   | VSENSE = 5 V   | 4.4  | 4.55 |   | 4.67 |
| V <sub>hys</sub>                    | Hysteresis at VSENSE <sub>n</sub> input             | V <sub>IT-</sub> = 1.25 V                              | 2   | 10             | 30   | mV   |   |      |
|                                     |   | V <sub>IT-</sub> = 1.68 V                              | 2   | 15             | 40   |      |   |      |
|                                     |   | V <sub>IT-</sub> = 2.93 V                              | 3   | 30             | 60   |      |   |      |
|                                     |   | V <sub>IT-</sub> = 4.55 V                              | 3   | 40             | 80   |      |   |      |
| I <sub>H</sub>                      | High-level input current                            | $\overline{\text{MR}}$                                 | $\overline{\text{MR}} = 0.7 \times V_{\text{DD}}$ , V <sub>DD</sub> = 6 V | -130           | -180 | μA   |   |      |
|                                     |   | SENSE1   | VSENSE1 = V <sub>DD</sub> = 6 V   | 5              | 8    |      |   |      |
|                                     |   | SENSE2   | VSENSE2 = V <sub>DD</sub> = 6 V   | 6              | 9    |      |   |      |
|                                     |   | SENSE3   | VSENSE3 = V <sub>DD</sub>   | -1             | 1    |      |   |      |
| I <sub>L</sub>                      | Low-level input current                             | $\overline{\text{MR}}$                                 | $\overline{\text{MR}} = 0$ V, V <sub>DD</sub> = 6 V                       | -430           | -600 | μA   |   |      |
|                                     |   | SENSE <sub>n</sub>                                     | VSENSE1,2,3 = 0 V   | -1             | 1    |      |   |      |
| I <sub>DD</sub>                     | Supply current                                      |  |   |                | 40   | μA   |   |      |
| C <sub>i</sub>                      | Input capacitance                                   | V <sub>I</sub> = 0 V to V <sub>DD</sub>                |   | 10             |      | pF   |   |      |

NOTES: 4. The lowest supply voltage at which  $\overline{\text{RESET}}$  becomes active.  $t_r$ , V<sub>DD</sub> ≥ 15 μs/V  
5. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 μF) should be placed close to the supply terminals.



# TPS3307-18-EP, TPS3307-33-EP TRIPLE PROCESSOR SUPERVISORS

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timing requirements at  $V_{DD} = 2\text{ V to }6\text{ V}$ ,  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |             | TEST CONDITIONS   | MIN | TYP | MAX | UNIT          |
|-----------|-------------|---|-----|-----|-----|---------------|
| $t_w$     | Pulse width | $V_{SENSEnL} = V_{IT-} - 0.2\text{ V}$ , $V_{SENSEnH} = V_{IT+} + 0.2\text{ V}$ | 6   |     |     | $\mu\text{s}$ |
|           |             | $V_{IH} = 0.7 \times V_{DD}$ , $V_{IL} = 0.3 \times V_{DD}$                     | 100 |     |     | ns            |

switching characteristics at  $V_{DD} = 2\text{ V to }6\text{ V}$ ,  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |   | TEST CONDITIONS  | MIN | TYP | MAX | UNIT          |
|-----------|---|--|-----|-----|-----|---------------|
| $t_d$     | Delay time  | $V_I(\text{SENSEn}) \geq V_{IT+} + 0.2\text{ V}$ ,<br>$\overline{\text{MR}} \geq 0.7 \times V_{DD}$ , See timing diagram | 140 | 200 | 280 | ms            |
| $t_{PHL}$ | Propagation (delay) time,<br>high-to-low level output | $\overline{\text{MR}}$ to $\overline{\text{RESET}}$  |     | 200 | 600 | ns            |
| $t_{PLH}$ | Propagation (delay) time,<br>low-to-high level output | $\overline{\text{MR}}$ to RESET  |     |     |     |               |
| $t_{PHL}$ | Propagation (delay) time,<br>high-to-low level output | SENSEn to $\overline{\text{RESET}}$  |     | 1   | 5   | $\mu\text{s}$ |
| $t_{PLH}$ | Propagation (delay) time,<br>low-to-high level output | SENSEn to RESET  |     |     |     |               |



TYPICAL CHARACTERISTICS

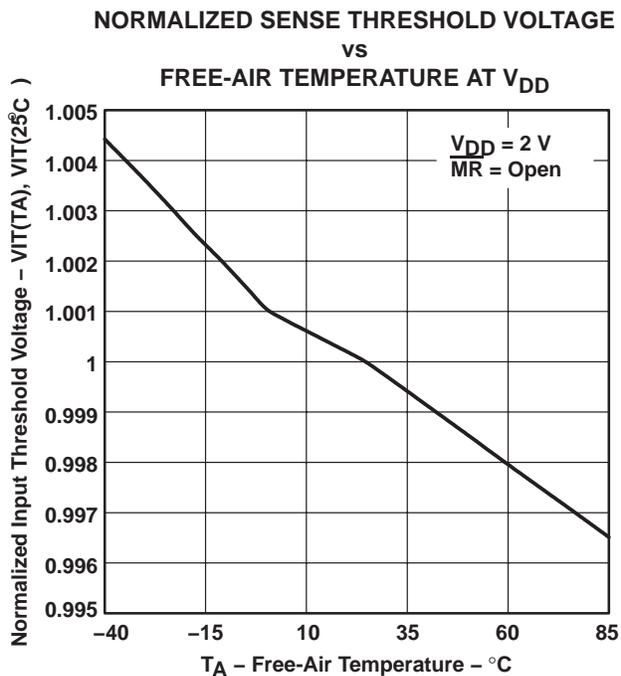


Figure 2

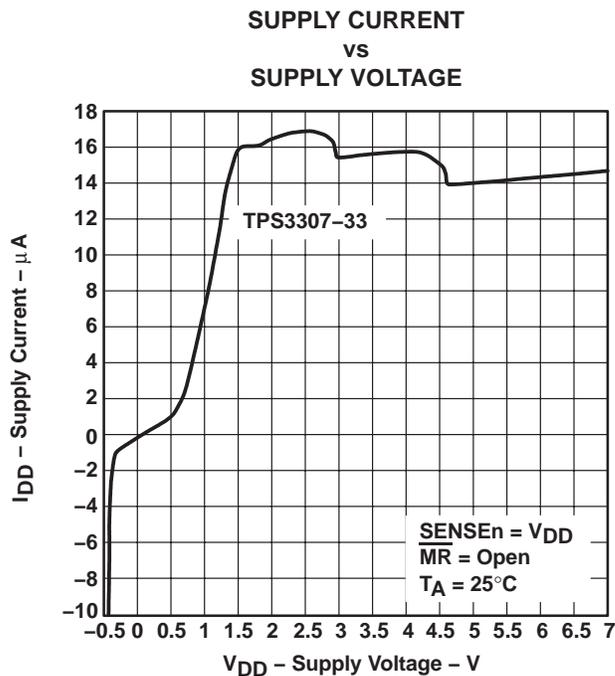


Figure 3

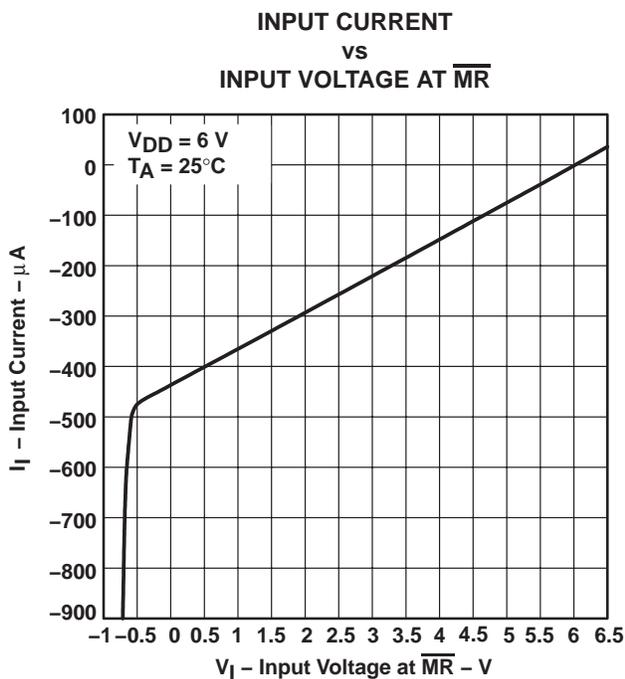


Figure 4

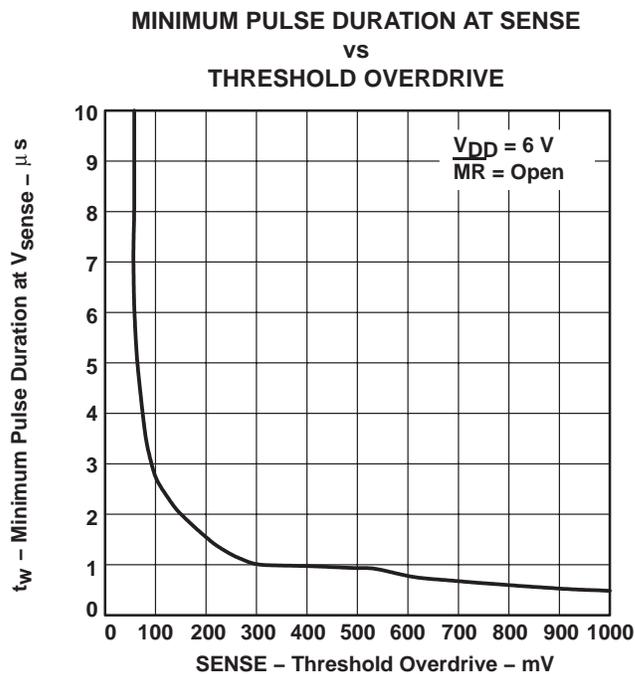
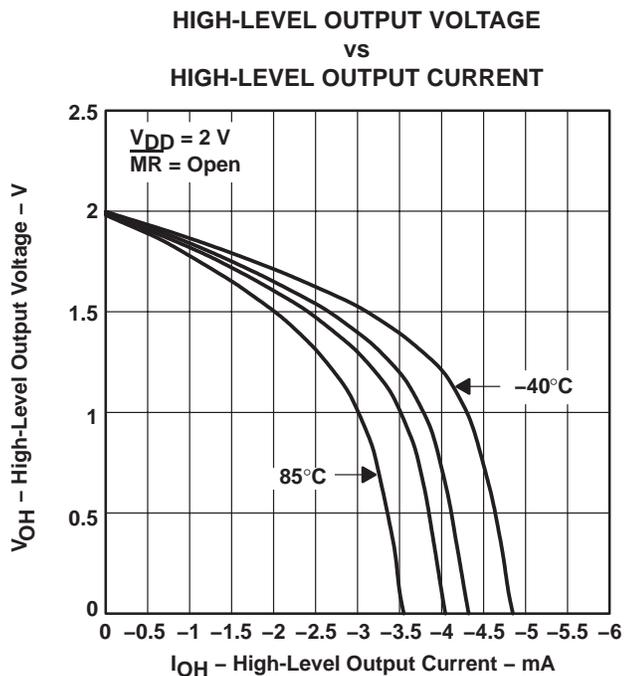
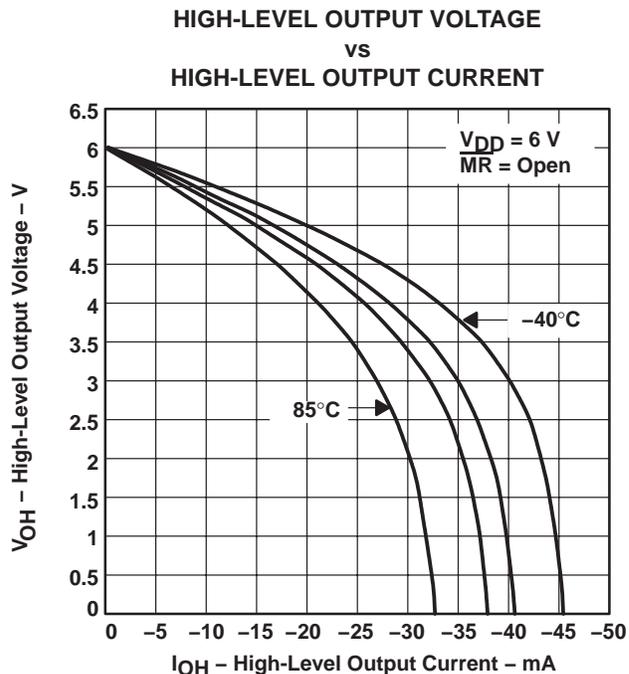


Figure 5

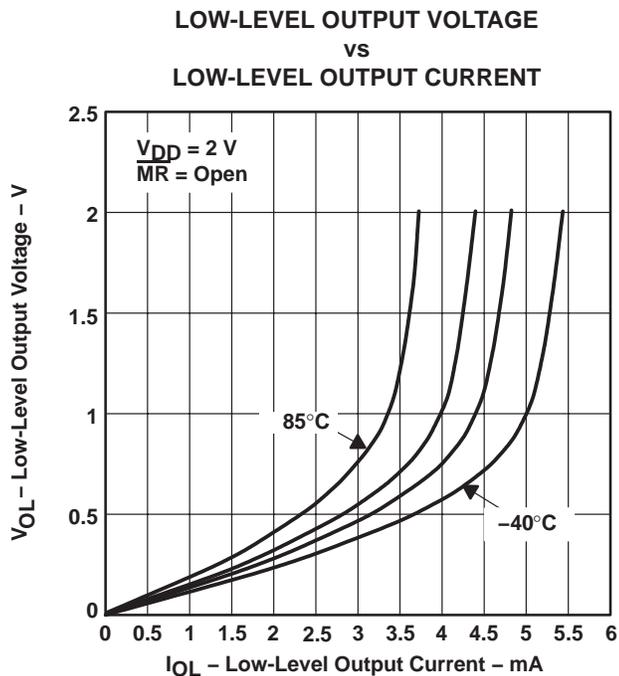
**TYPICAL CHARACTERISTICS**



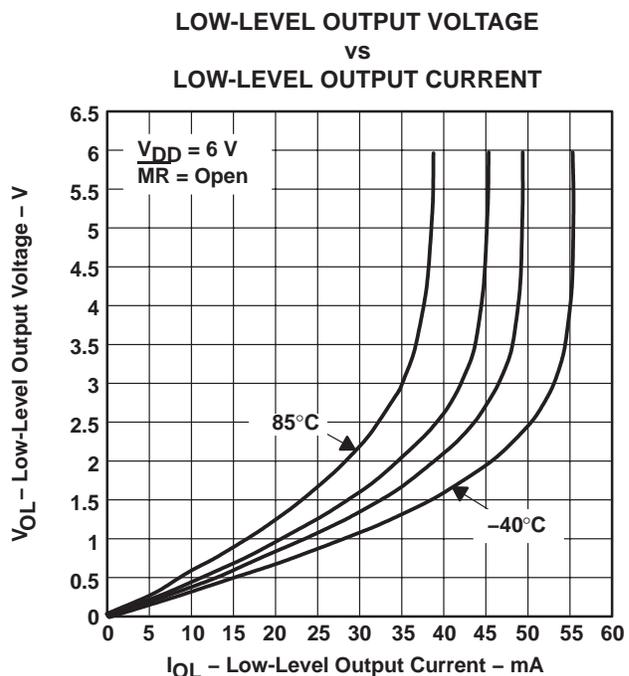
**Figure 6**



**Figure 7**



**Figure 8**



**Figure 9**

## PACKAGING INFORMATION

| Orderable Device  | Status<br>(1) | Package Type      | Package<br>Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|-------------------|---------------|-------------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| TPS3307-18MDREP   | ACTIVE        | SOIC              | D                  | 8    | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -55 to 125   | 30718E                   | <a href="#">Samples</a> |
| TPS3307-18MDREPG4 | ACTIVE        | SOIC              | D                  | 8    | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -55 to 125   | 30718E                   | <a href="#">Samples</a> |
| TPS3307-33MDGNREP | ACTIVE        | MSOP-<br>PowerPAD | DGN                | 8    | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAUAG      | Level-1-260C-UNLIM   | -55 to 125   | BNP                      | <a href="#">Samples</a> |
| V62/03629-01XE    | ACTIVE        | SOIC              | D                  | 8    | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -55 to 125   | 30718E                   | <a href="#">Samples</a> |
| V62/03629-02YE    | ACTIVE        | MSOP-<br>PowerPAD | DGN                | 8    | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAUAG      | Level-1-260C-UNLIM   | -55 to 125   | BNP                      | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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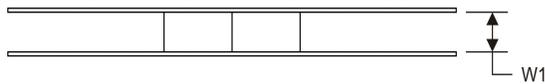
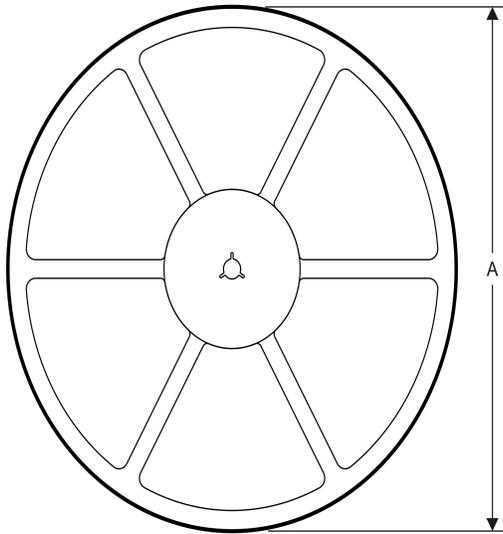
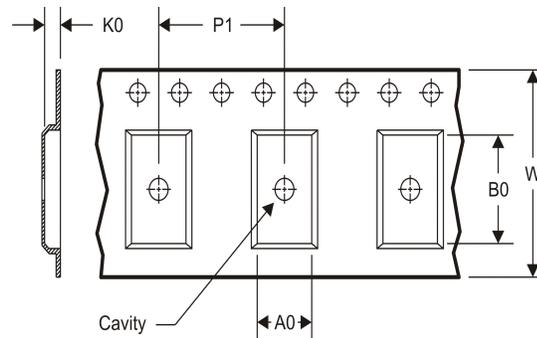
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**OTHER QUALIFIED VERSIONS OF TPS3307-18-EP, TPS3307-33-EP :**

- Catalog: [TPS3307-18](#), [TPS3307-33](#)
- Automotive: [TPS3307-18-Q1](#)
- Military: [TPS3307-18M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device            | Package Type   | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|----------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS3307-18MDREP   | SOIC           | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TPS3307-33MDGNREP | MSOP-Power PAD | DGN             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

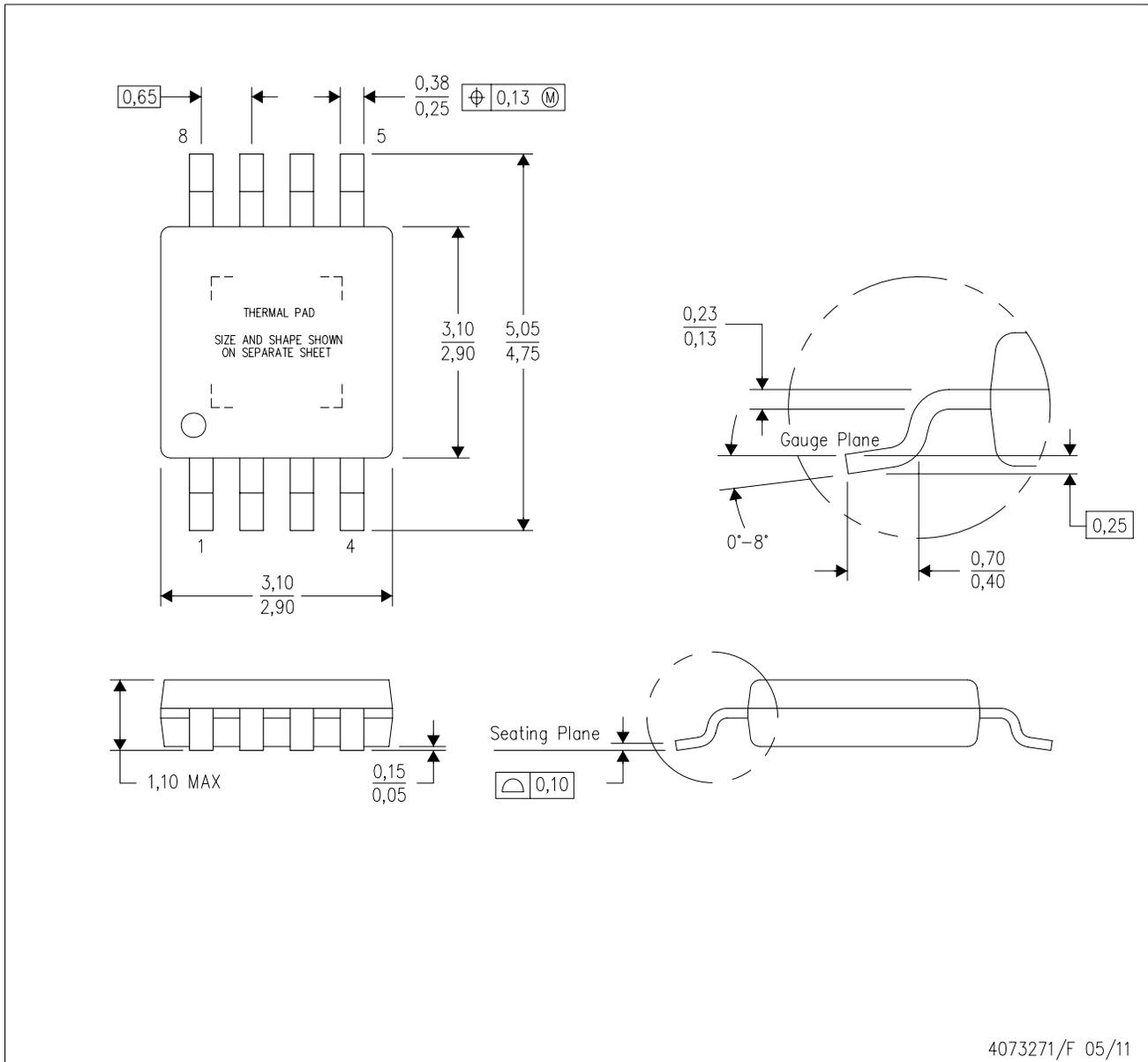


\*All dimensions are nominal

| Device            | Package Type  | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|---------------|-----------------|------|------|-------------|------------|-------------|
| TPS3307-18MDREP   | SOIC          | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| TPS3307-33MDGNREP | MSOP-PowerPAD | DGN             | 8    | 2500 | 358.0       | 335.0      | 35.0        |

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

DGN (S-PDSO-G8)

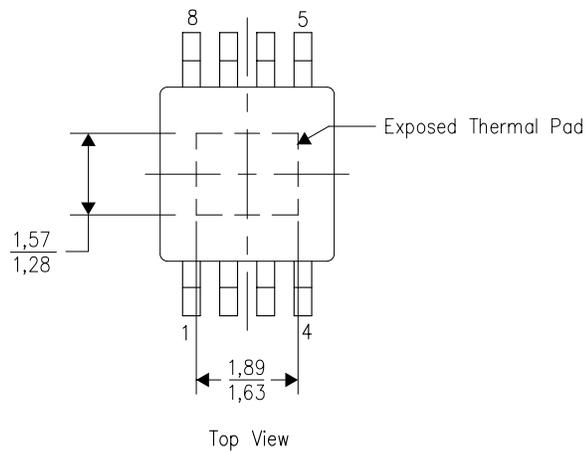
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

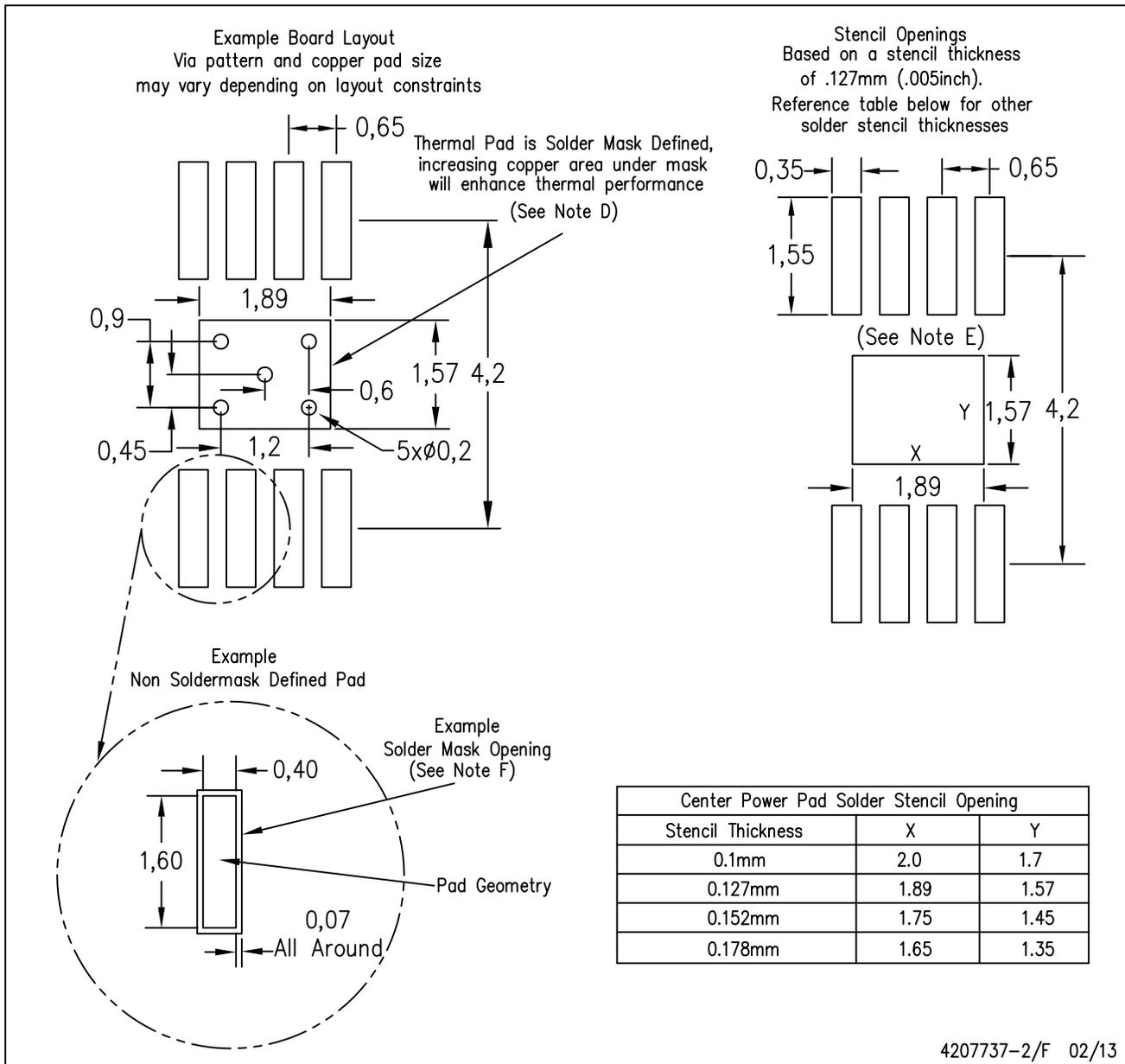


Exposed Thermal Pad Dimensions

4206323-2/1 12/11

NOTE: All linear dimensions are in millimeters

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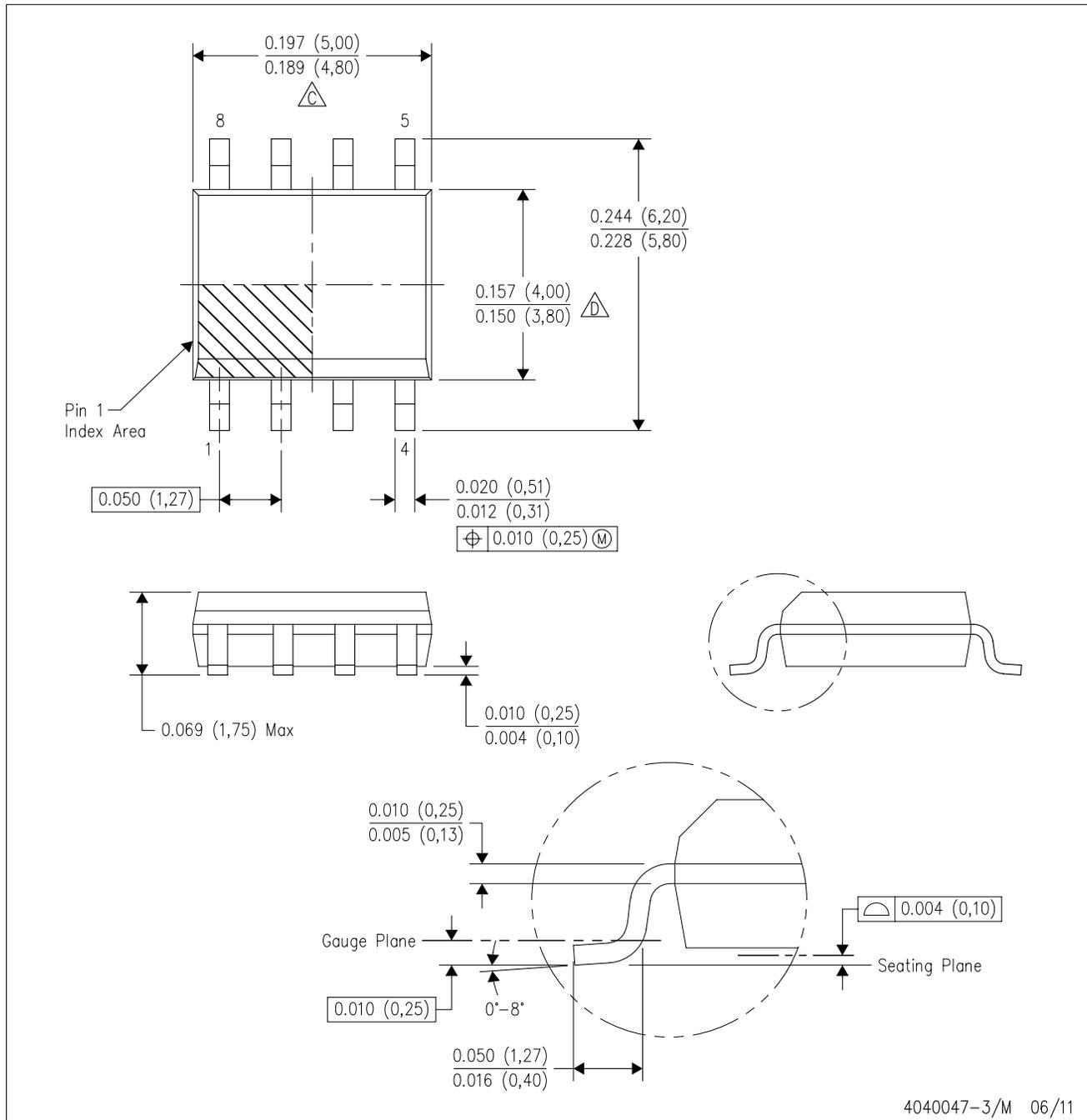


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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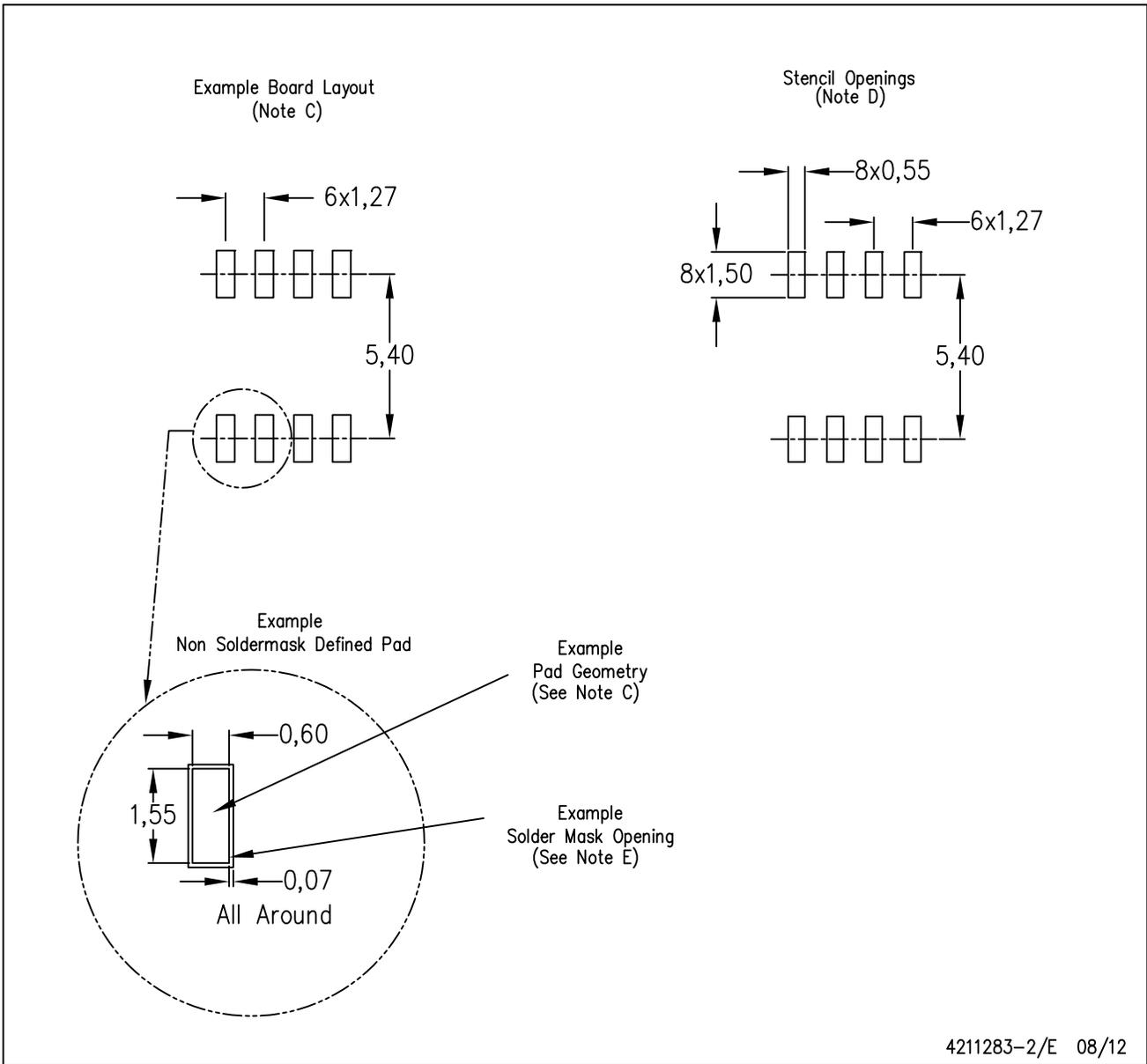
D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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