Low-Power, Push-Button Controllers with Configurable Delay

Check for Samples: TPS3420, TPS3421, TPS3422

FEATURES

- Very Small Package: 1.45-mm × 1-mm SON
- Operating Range: 1.6 V to 6.5 V
- Single (TPS3422) or Dual (TPS3420 and TPS3421) Push-Button Inputs
- Low Supply Current: 250 nA
- Two-State Logic, User-Selectable Input Delay:
  - For Example: 7.5 s and 0 s
  - Multiple Timing Options Available
- Fixed Timeout Pulse at $\overline{RST}$ (TPS3421 and TPS3422): 400 ms
  - Other Timing Options Available on Request
- Active Low, Open-Drain Output

APPLICATIONS

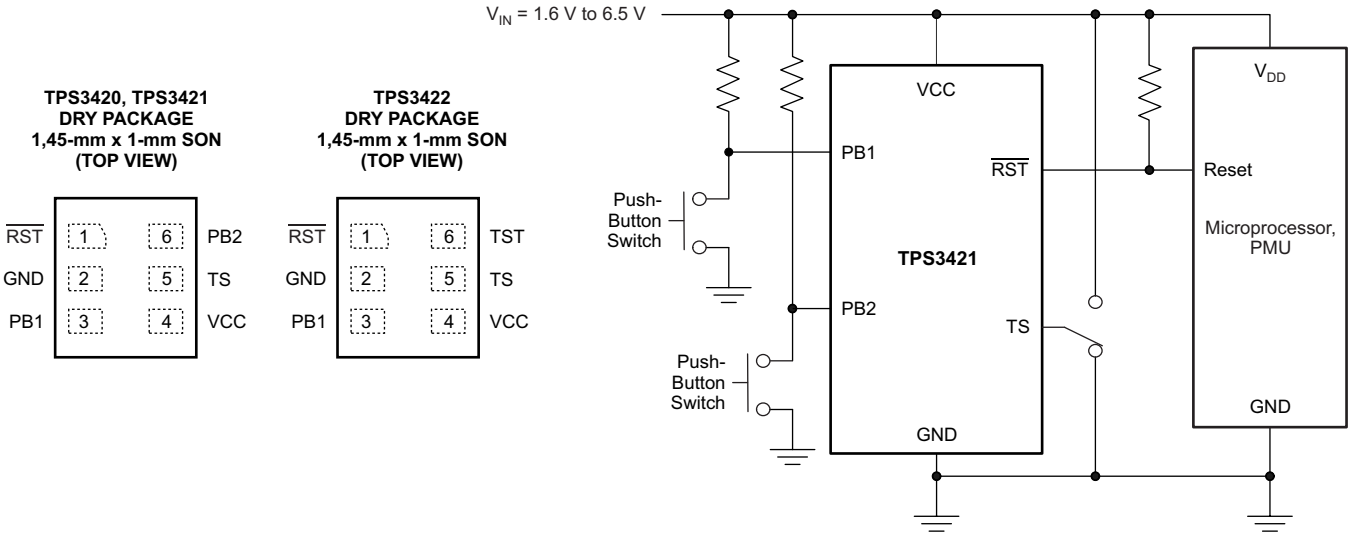
- Smart Phones
- Tablets, Ultrabooks™
- Gaming Consoles
- Portable Consumer
- Navigation Devices
- Consumer Medical
- Toys

DESCRIPTION

The TPS3420, TPS3421, and TPS3422 (TPS342x) are low-current, ultrasmall, push-button reset timers. These devices use a long timing setup delay to provide the intended system reset, and avoid resets from short push-button closures or key presses. This reset configuration also allows for differentiation between software interrupts and hard system resets.

The TPS3420 and TPS3421 monitor two inputs (PB1 and PB2) and output an active-low reset pulse signal ($\overline{RST}$) when both inputs are low for the selected time delay. For the TPS3421, $\overline{RST}$ remains low for a factory-programmed fixed time. For the TPS3420, $\overline{RST}$ remains low until one of the PBx inputs is released. The need for a dedicated reset button is eliminated because two inputs are used to ensure reset. The TPS3422 monitors one input (PB1) and outputs an active-low reset pulse signal ($\overline{RST}$) when PB1 is low for the selected time delay.

The TPS342x have an open-drain output that can be wire ORed with other open-drain devices. The TPS342x operate from 1.6 V to 6.5 V over the –40°C to +125°C temperature range, and provide a precise, space-conscious micropower solution for system resetting needs.



NOTE: Connect TS to VCC or ground for different PB time delays. Connect one PB input to ground for use as a single channel.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	DESCRIPTION
TPS3420**xzzza** TPS3421**xyzzza** TPS3422**xyzzza**	**x** is the push-button timer option. **y** is the different reset timeout pulse option. **zzz** is the package designator. **a** is the tape or reel quantity.

DEVICE FAMILY OPTIONS

DEVICE	CHANNELS	INPUT	RESET BEHAVIOR (DEASSERTION)
TPS3420	2	NMOS-based threshold	Input (PBx) dependent
TPS3421	2	External pull-up to VCC	Fixed pulse
TPS3422	1	Internal pull-up	Fixed pulse

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Voltage	VCC	–0.3 to +7	V
	$\overline{RST}$	–0.3 to +7	V
	PB1, PB2	–0.3 to +7	V
	TS	–0.3 to V_{CC} + 0.3	V
Current	$\overline{RST}$ pin	±20	mA
Temperature(2)	Operating junction, T_J	–40 to +125	°C
	Storage, T_{stg}	–65 to +150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)	2	kV
	Charge device model (CDM)	500	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute maximum- rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS3420 TPS3421 TPS3422	UNITS
		DRY (µSON)	
		6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	322.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	1185.2	
θ_{JB}	Junction-to-board thermal resistance	184.7	
ψ_{JT}	Junction-to-top characterization parameter	34.9	
ψ_{JB}	Junction-to-board characterization parameter	182.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	69.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

All specifications are over the operating temperature range of –40°C < T_J < +125°C and 1.6 V ≤ V_{CC} ≤ 6.5 V, unless otherwise noted. Typical values are at T_J = +25°C and V_{CC} = 3.3 V.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Input supply range			1.6		6.5	V
I_{CC}	Supply current (standby)	TPS3421, TPS3422	V_{CC} = 3.3 V		250		nA
			V_{CC} = 6.5 V, –40°C < T_J < +85°C			1	µA
			V_{CC} = 6.5 V			3.3	µA
		TPS3420	V_{CC} = 3.3 V		350		nA
			V_{CC} = 6.5 V, –40°C < T_J < +85°C			1.2	µA
			V_{CC} = 6.5 V			3.4	µA
	Supply current (active timer)(1)	TPS3420, TPS3421	PB1, PB2 = 0 V, V_{CC} = 6.5 V		6	12	µA
		TPS3422	PB1, PB2 = 0 V, V_{CC} = 6.5 V		106	136	µA
V_{IH}	High-level input voltage	TPS3421, TPS3422	PB1, PB2	0.7 V_{CC}			V
		TPS3420	PB1, PB2	0.85			V
V_{IL}	Low-level input voltage	TPS3421, TPS3422	PB1, PB2	0		0.3 V_{CC}	V
		TPS3420	PB1, PB2	0		0.3	V
R_{PB1}	PB1 internal pull-up resistance (TPS3422)				65		kΩ
I_{PB}	Input current (PB1, PB2)	TPS3420 TPS3421	PB1, PB2 = 0 V or V_{CC}	–50		50	nA
		TPS3422	PB1, PB2 = V_{CC}	-50		50	nA
V_{OL}	Low-level output voltage		V_{CC} ≥ 4.5 V, I_{SINK} = 8 mA			0.4	V
			V_{CC} ≥ 3.3 V, I_{SINK} = 5 mA			0.3	V
			V_{CC} ≥ 1.6 V, I_{SINK} = 3 mA			0.3	V
$I_{lkg(OD)}$	Open-drain output leakage current		High impedance, V $\overline{RST}$ = 6.5 V	–0.35		0.35	µA

(1) Includes current through pull-up resistor between input pin (PB1) and supply pin (VCC) for TPS3422.

TIMING REQUIREMENTS

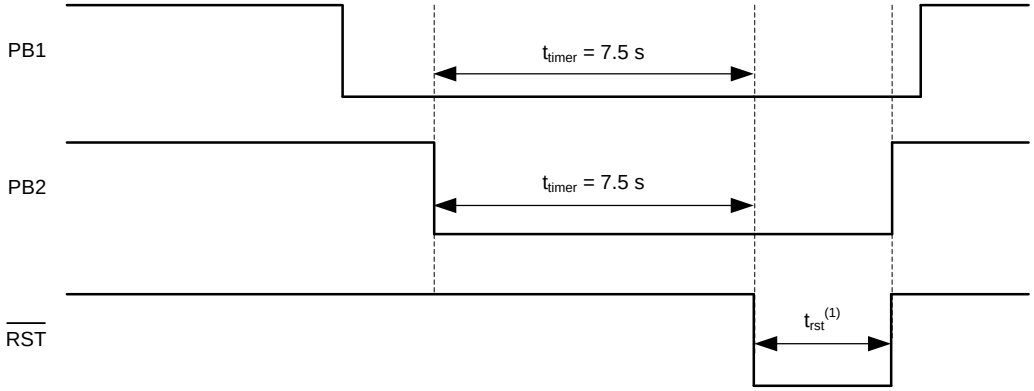
All specifications are over the operating temperature range of –40°C < T_J < +125°C and 1.6 V ≤ V_{CC} ≤ 6.5 V, unless otherwise noted. Typical values are at T_J = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{timer}	Push button timer(1)		–20%		20%	
		TPS3420D: TS = GND	6	7.5	9	s
		TPS3420D: TS = VCC	10	12.5	15	s
		TPS3421Ey, TPS3422Ey: TS = GND	6	7.5	9	s
		TPS3421Ey, TPS3422Ey: TS = VCC		0		s
t_{rst}	Reset pulse duration		–20%		20%	
		TPS3421xC	64	80	96	ms
		TPS3421xG	320	400	480	ms
		TPS3422xG	320	400	480	ms
t_{dd}	Detection delay (from input to $\overline{RST}$)(2)	For 0-s t_{timer} condition		150		µs
	Start-up time(2)	VCC rising		300		µs

(1) For devices with a 0-second delay while TS = VCC, this option is only for factory testing and is not intended for normal operation. In normal operation, the TS pin should be tied to GND.
(2) For devices with a 0-second delay when TS = VCC, reset asserts in t_{dd} time when both PB inputs go low in this configuration. During start up, if the PB inputs are low, reset asserts after a start-up time delay. This value is specified by design.

TIMING DIAGRAMS

TIMING DIAGRAM: TPS3420



(1) For the TPS3420, t_{rst} is not a fixed time, but instead depends on one of the PB pins going high.

Figure 1. TPS3420 Timing Diagram

TIMING DIAGRAM: TPS3421

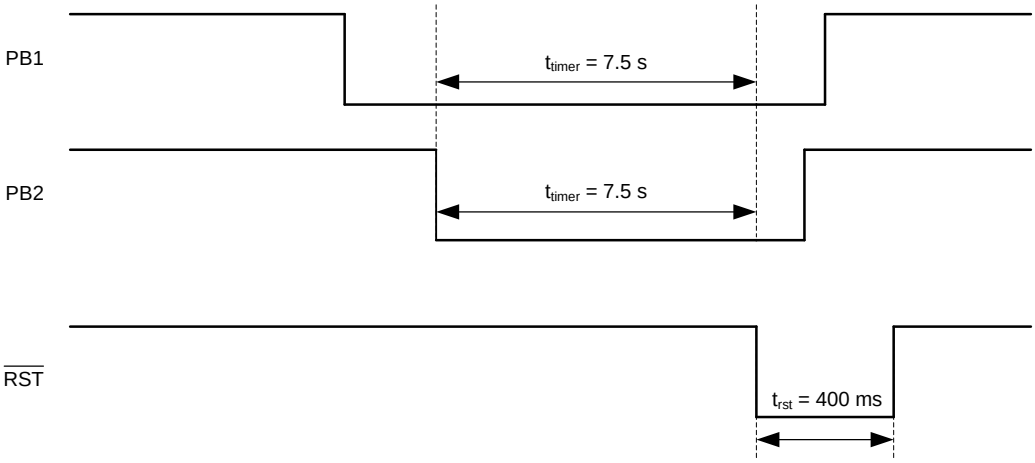


Figure 2. TPS3421 Timing Diagram

TIMING DIAGRAM: TPS3422

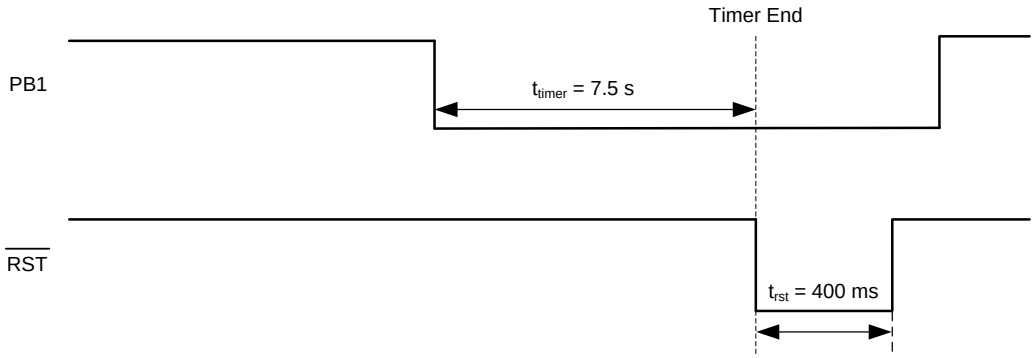
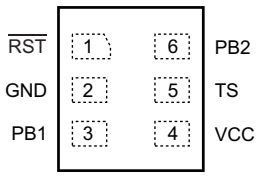


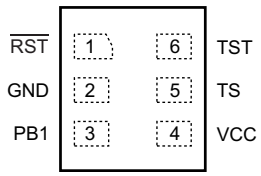
Figure 3. TPS3422 Timing Diagram

PIN CONFIGURATION

TPS3420, TPS3421: DRY PACKAGE
1.45-mm × 1-mm SON
(TOP VIEW)



TPS3422: DRY PACKAGE
1.45-mm × 1-mm SON
(TOP VIEW)



PIN DESCRIPTIONS

PIN NAME	PIN NO.		DESCRIPTION
	TPS3420/21	TPS3422	
GND	2	2	Ground
PB1	3	3	Push-button input. PB1 and PB2 must be held low for greater than t_{timer} time to assert the reset output.
PB2	6	—	Second push-button input. PB1 and PB2 must be held low for greater than t_{timer} time to assert the reset output.
$\overline{RST}$	1	1	Active low, open-drain output. Reset is asserted (goes low) when both PB1 and PB2 are held low for longer than t_{timer} time (only PB1 for TPS3422). For TPS3420: Reset is deasserted when either PBx input goes high. For TPS3421,TPS3422: Reset is deasserted after fixed time of t_{rst}.
TS	5	5	Time delay selection input. Connect to VCC or GND for different t_{timer} selections. In normal operation, the TS pin state should not be changed because it is intended to be permanently connected to either GND or VCC. If switching the TS pin is required, it should be done during power off, or when either PBx input is high.
TST	—	6	Connect this pin to GND or VCC during normal device operation.
VCC	4	4	Supply voltage input. Connect a 1.6-V to 6.5-V supply to VCC to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

FUNCTIONAL BLOCK DIAGRAMS

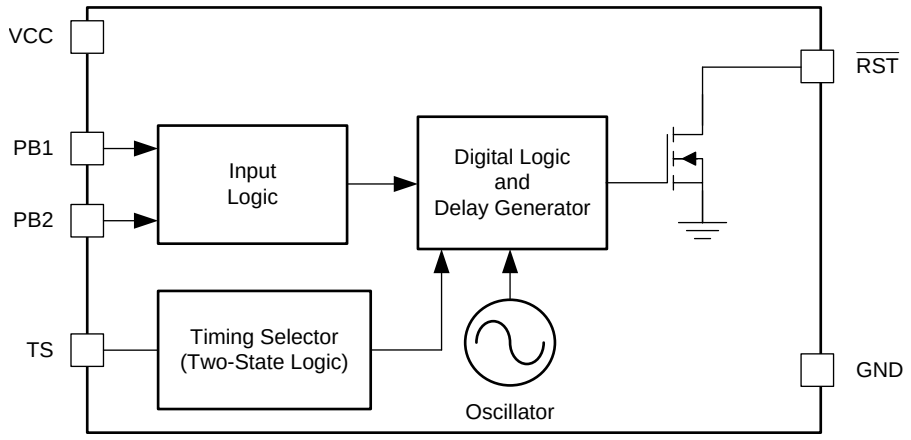


Figure 4. TPS3420 Block Diagram

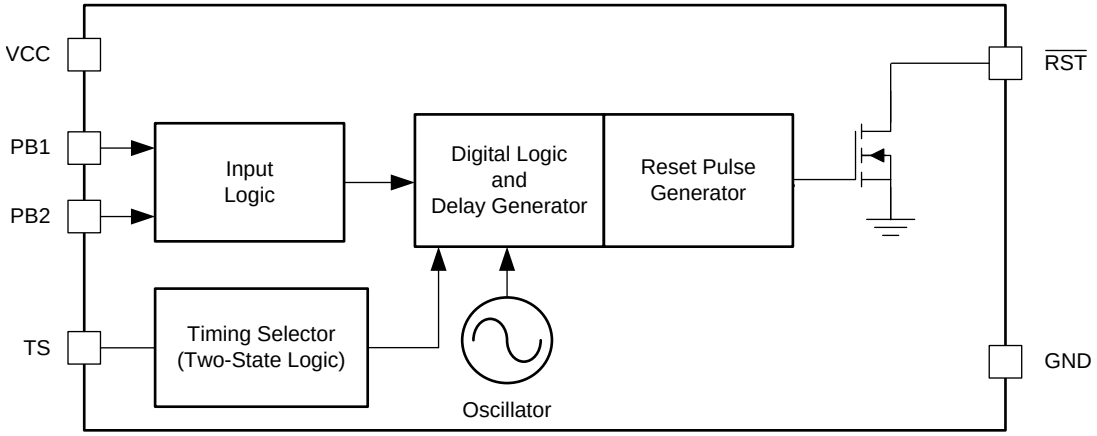


Figure 5. TPS3421 Block Diagram

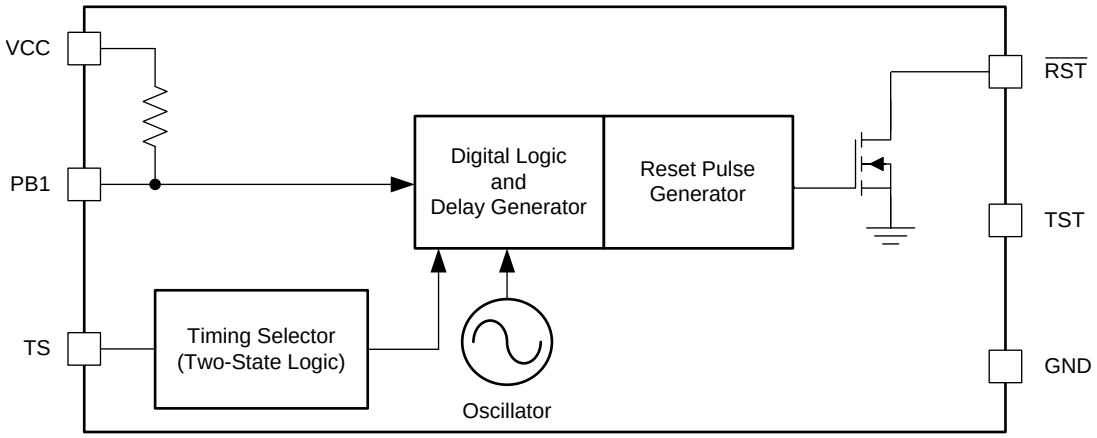


Figure 6. TPS3422 Block Diagram

TYPICAL CHARACTERISTICS

At T_J = +25°C and V_{CC} = 3.3 V, unless otherwise noted.

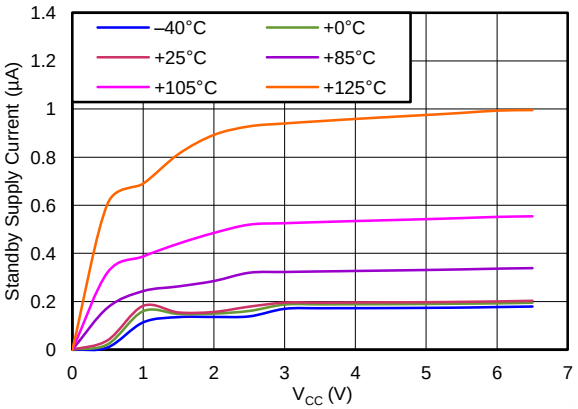


Figure 7. TPS3421: STANDBY SUPPLY CURRENT vs SUPPLY VOLTAGE

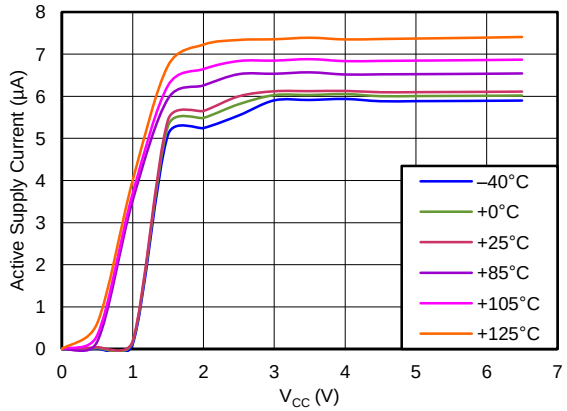


Figure 8. TPS3421: ACTIVE SUPPLY CURRENT vs SUPPLY VOLTAGE (PB1 = PB2 = GND)

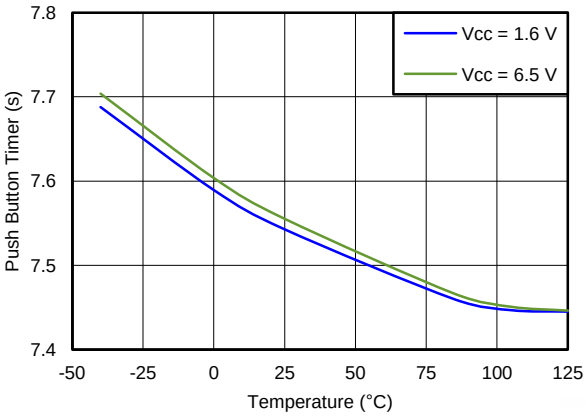


Figure 9. PUSH BUTTON TIMER vs TEMPERATURE (TS = GND)

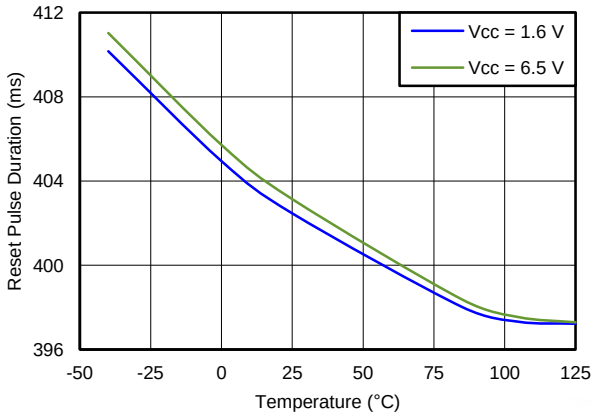


Figure 10. RESET PULSE DURATION vs TEMPERATURE

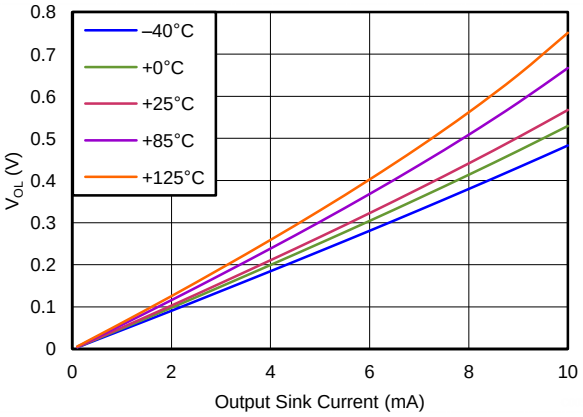


Figure 11. OUTPUT VOLTAGE LOW vs OUTPUT SINK CURRENT (V_{CC} = 1.6 V)

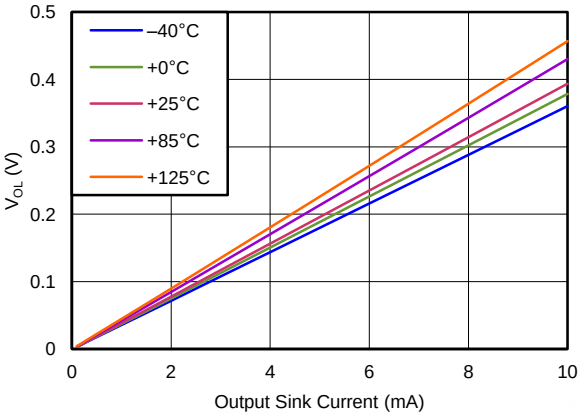


Figure 12. OUTPUT VOLTAGE LOW vs OUTPUT SINK CURRENT (V_{CC} = 3.3 V)

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C and V_{CC} = 3.3 V, unless otherwise noted.

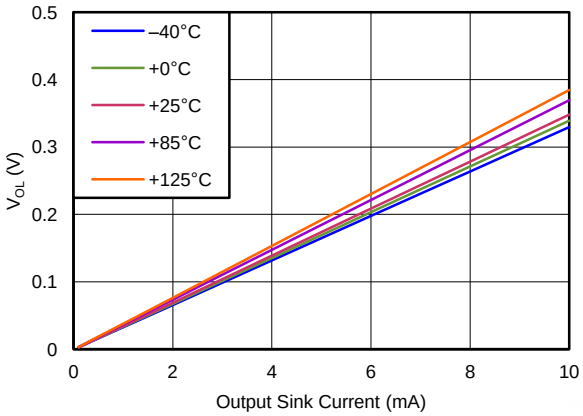


Figure 13. OUTPUT VOLTAGE LOW vs OUTPUT SINK CURRENT (V_{CC} = 6.5 V)

DETAILED DESCRIPTION

OVERVIEW

The TPS342x are a family of push-button reset devices with an extended setup period that prevents resets from occurring as a result of short-duration switch closures. See the Device Family Options table for details.

The TPS3420 is a dual-channel device with an output that asserts when both inputs (PB1 and PB2) are held low for the push-button timer duration, and deasserts when either input PBx is released.

The TPS3421 is a dual-channel device with an output that asserts when both inputs (PB1 and PB2) are held low for the push-button timer duration, and deasserts after the reset timeout duration.

TPS3422 is a single-channel device with an output that asserts when the PB1 input is held low for the push-button timer duration, and deasserts after the reset timeout duration.

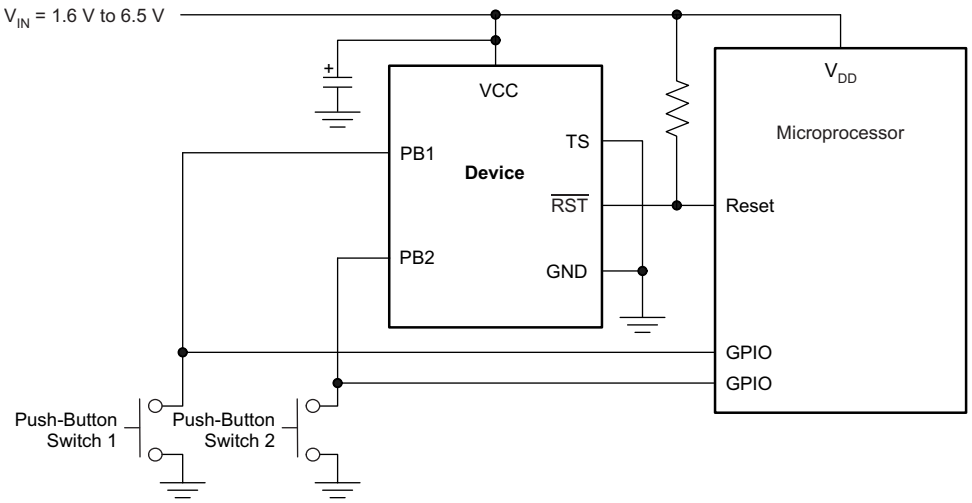
The TPS342x family also has a TS pin that selects between two different push-button timing options by connecting the pin to either GND or V_{CC}.

DEVICE INPUTS

This section describes the input of the TPS342x devices.

TPS3420 Inputs (PB1, PB2)

The TPS3420 has two NMOS-based threshold inputs (PB1, PB2) with a $V_{IH} \geq 0.85$ V, and a $V_{IL} \leq 0.3$ V. When input conditions are met (that is, when both inputs are simultaneously held low for the push-button timer period, t_{timer}), the device asserts a reset low, as shown in Figure 1. Reset deassertion occurs when either input goes high. The reset pulse occurs only one time after each valid input condition. At least one input pin must be released (goes high) and then driven low for the t_{timer} period before $\overline{RST}$ asserts again. An application diagram is shown in Figure 14.

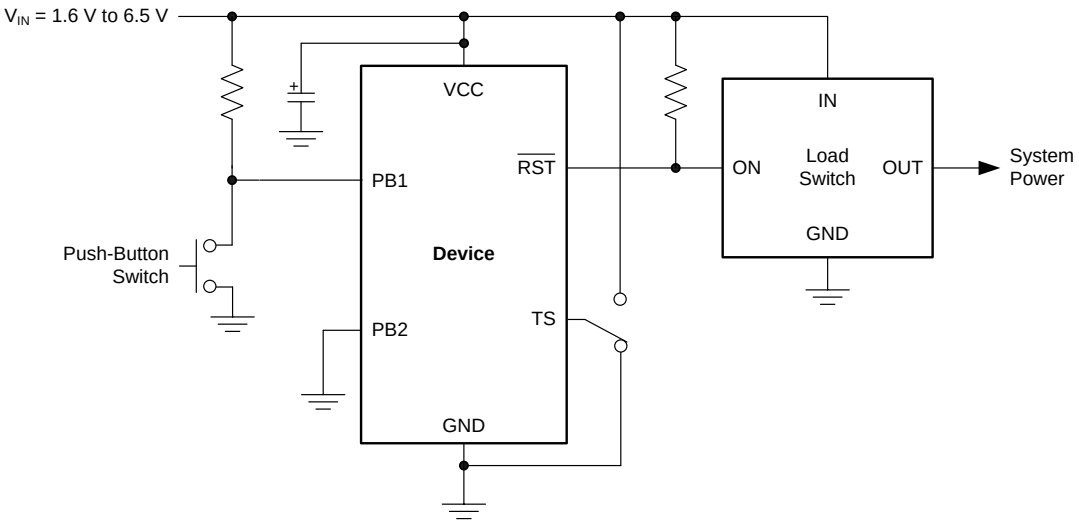


NOTE: Connect TS to VCC or ground for different PB time delays. Connect one PB input to ground for use as a single channel.

Figure 14. TPS3420 Application Diagram

TPS3421 Inputs (PB1, PB2)

The TPS3421 has two inputs: PB1 and PB2. External pull-up resistors to VCC are required to pull the input pins high, as shown in Figure 15. When input conditions are met (that is, when both inputs are held low simultaneously for the push-button timer period, t_{timer}), the device asserts a single reset pulse of a fixed time (t_{rst}); see Figure 2. Reset deassertion is independent of the inputs because t_{rst} is a fixed time pulse. A reset pulse occurs only one time after each valid input condition. At least one input pin must be released (go high) and then driven low for the t_{timer} duration before $\overline{RST}$ asserts again; see Figure 17.

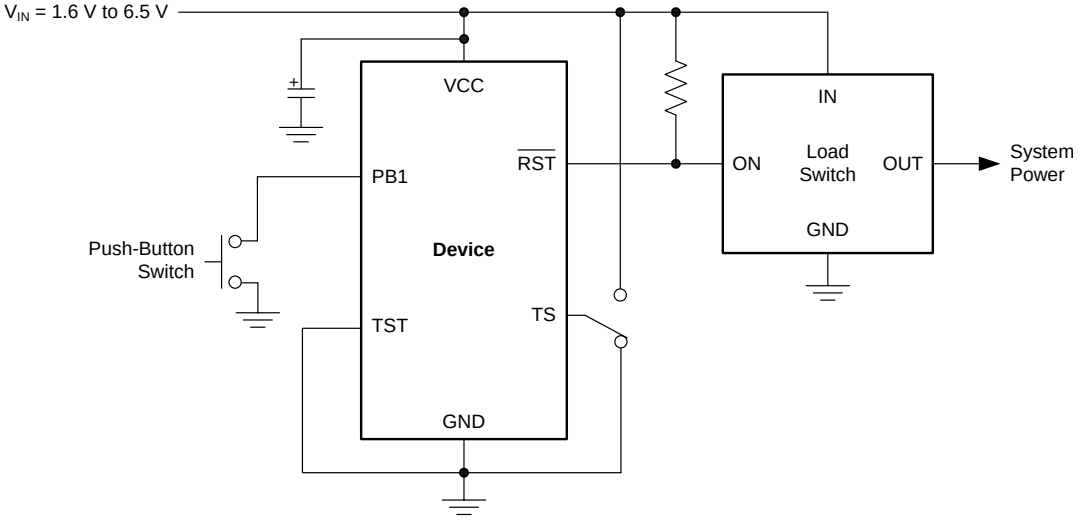


NOTE: Connect TS to VCC or ground for different PB time delays. Connect one PB input to ground for use as a single channel.

Figure 15. TPS3421 Application Diagram

TPS3422 Input (PB1)

The TPS3422 has only one input: PB1. This input has an internal pull-up resistor to V_{CC}. When input conditions are met (that is, when the input is held low for the push-button timer period, t_{timer}), the device asserts a single reset pulse of a fixed time (t_{rst}); see Figure 3. Reset deassertion is independent of the input because t_{rst} is a fixed time pulse. A reset pulse occurs only one time after each valid input condition. The input pin must be released (go high) and then driven low for the t_{timer} period before $\overline{RST}$ asserts again. An application diagram is shown in Figure 16.



NOTE: Connect TS to VCC or ground for different PB time delays.

Figure 16. TPS3422 Application Diagram

PUSH-BUTTON TIMER SELECTION (TS)

The TPS342x offer two different push-button timer options (t_{timer}) for system flexibility with the use of TS pin. Connect the TS pin to either GND or VCC for two different timing options, as shown in Table 1.

Table 1. Push-Button Timer Option Examples

PRODUCT	PUSH-BUTTON TIMER		RESET PULSE
	TS = VCC	TS = GND	
TPS3420DDRYR/T	12.5 s	7.5 s	N/A
TPS3421EGDRYR/T	0 s	7.5 s	400 ms
TPS3422EGDRYR/T	0 s	7.5 s	400 ms

During normal operation, the TS pin state should not be changed because TS is intended to be permanently connected to either ground or VCC. The state of the TS pin is checked during power-up and when either PBx input is high. Therefore, if a different timing option is desired, the state must be changed during power-off, or when either PBx input is high, in order to avoid false operation.

OUTPUT ($\overline{RST}$)

The TPS342x have an open-drain output. A pull-up resistor must be used to hold the line high when the output is in a high-impedance state (not asserted). By connecting a pull-up resistor to the proper voltage rail, the output can be connected to other devices at correct interface voltage levels. The TPS342x output can be pulled up to 6.5 V, independent of the device supply voltage. To ensure proper voltage levels, make sure to choose the correct pull-up resistor values. The pull-up resistor value is determined by V_{OL}, sink current capability, and output leakage current ($I_{lkg(OD)}$). These values are specified in the Electrical Charactersitcs table.

The *Inputs (PB1, PB2)* section describes how the output is asserted or deasserted. See Figure 1 (TPS3420), Figure 2 (TPS3421) , or Figure 3 (TPS3422) for a timing diagram that describes the relationship between the PB1 and PB2 inputs and the output. Figure 17 shows the TPS3421 reset timing.

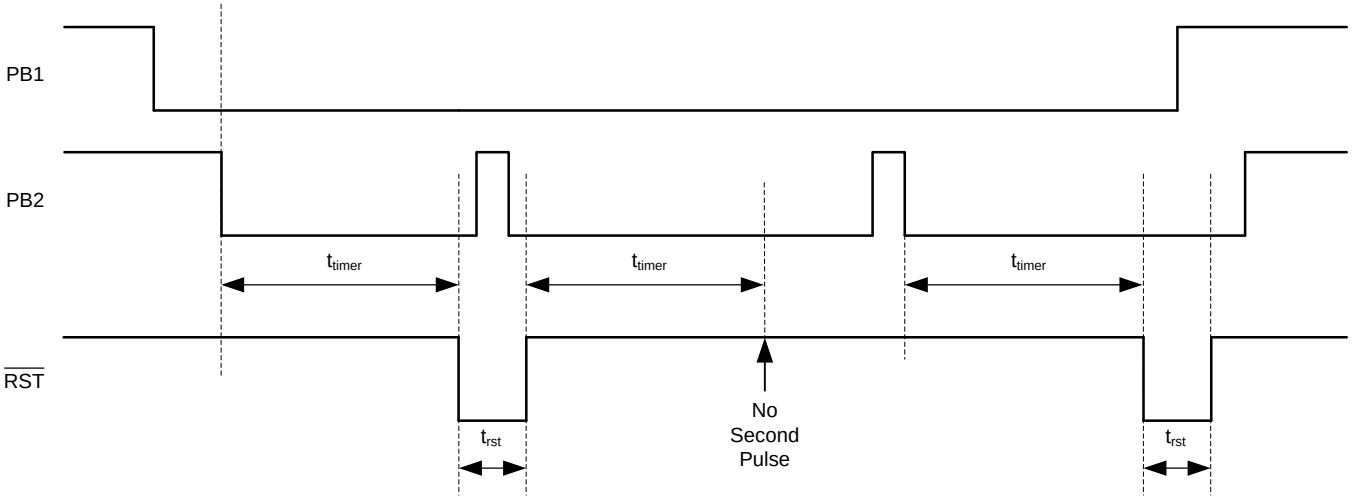


Figure 17. TPS3421 Reset Timing Diagram

Any change in input condition is detected after reset is deasserted. If input PB1 or PB2 has a pulse (low-to-high-to-low) during the t_{rst} period, the change is not recognized by the device. If input PB1 or PB2 go high during the t_{rst} period, the change is detected after reset is deasserted.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from the page numbers in the current version.

Changes from Original (August 2012) to Revision A	Page
• Changed data sheet from product preview to production data	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS3420DDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD	Samples
TPS3420DDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD	Samples
TPS3421ECDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB	Samples
TPS3421ECDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB	Samples
TPS3421EGDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC	Samples
TPS3421EGDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC	Samples
TPS3422EGDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AE	Samples
TPS3422EGDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

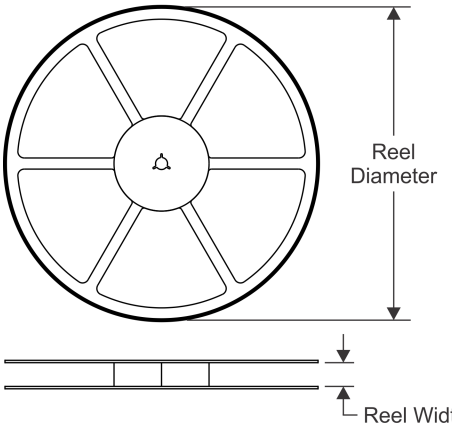
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

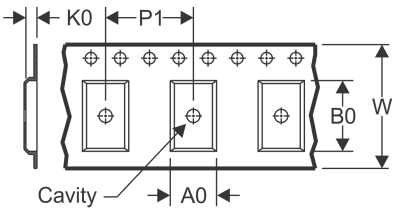
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

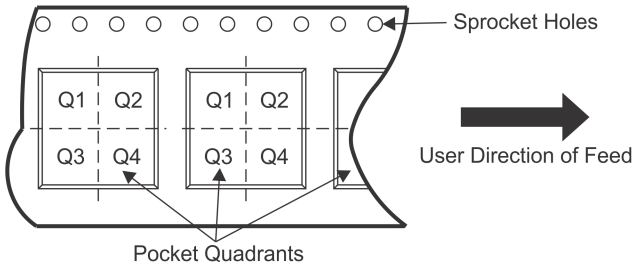


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

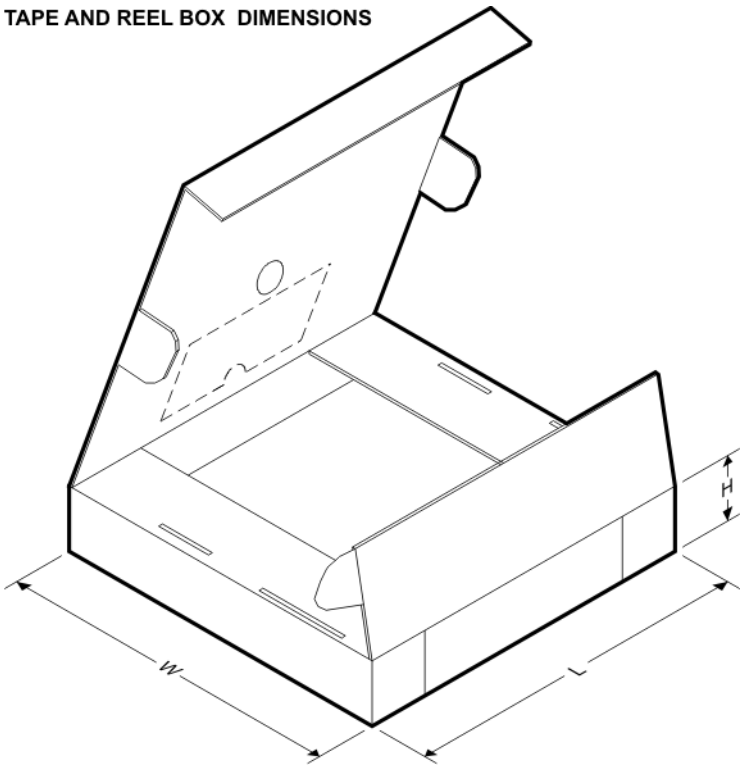
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3420DDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3420DDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3421ECDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3421ECDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3421EGDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3421EGDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3422EGDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3422EGDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1

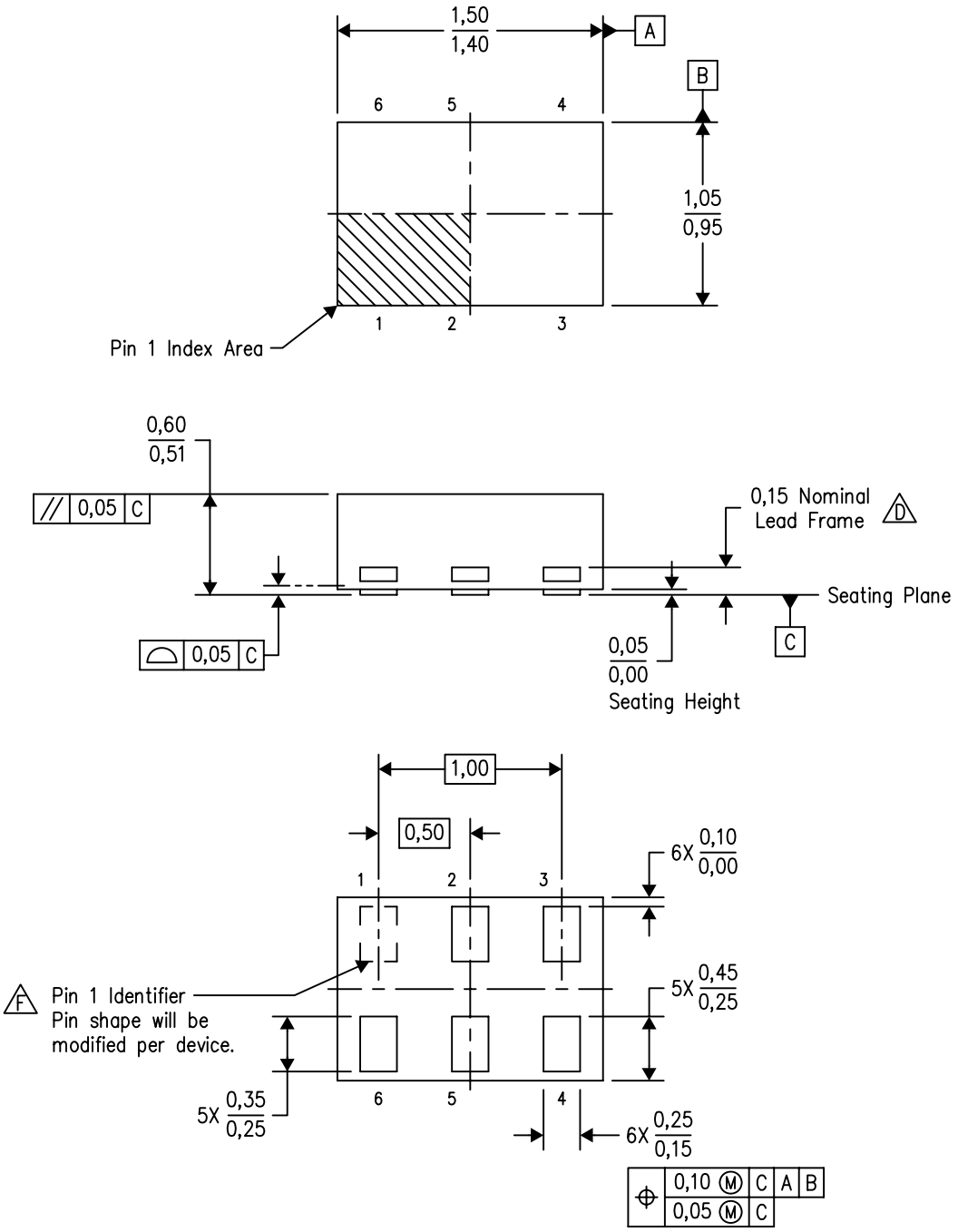
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3420DDRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3420DDRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3421ECDRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3421ECDRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3421EGDRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3421EGDRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3422EGDRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPS3422EGDRYT	SON	DRY	6	250	203.0	203.0	35.0

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



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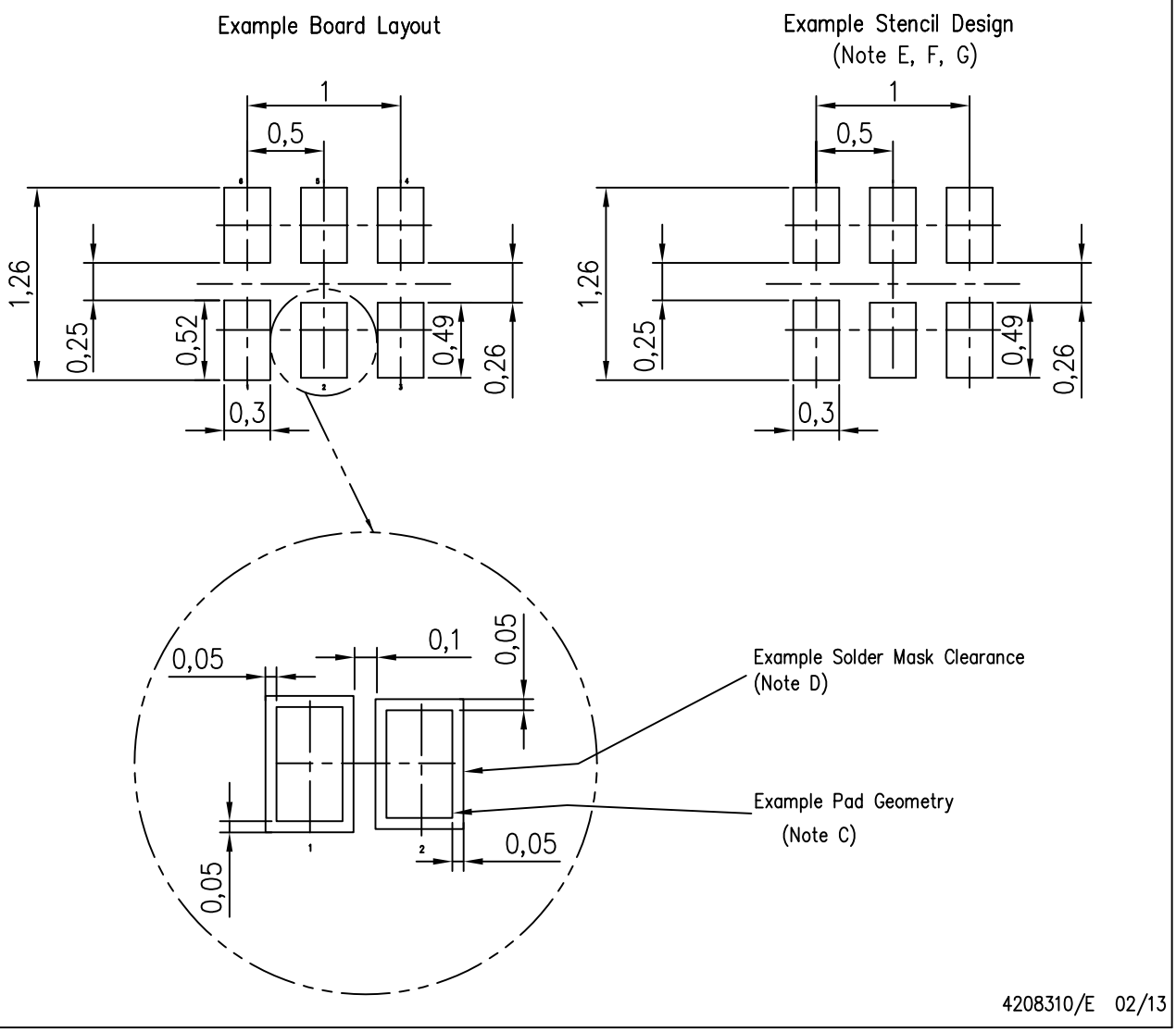
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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