LOW QUIESCENT CURRENT, PROGRAMMABLE DELAY SUPERVISORY CIRCUIT

FEATURES

- **Power-On Reset Generator With Adjustable Delay Time: 1.25 ms to 10 s**
- **Very Low Quiescent Current: 2.4 μA Typical**
- **High Threshold Accuracy: 0.5% Typical**
- **Fixed Threshold Voltages for Standard Voltage Rails from 0.9 V to 5 V and Adjustable Voltage Down to 0.4 V Are Available**
- **Manual Reset ($\overline{MR}$) Input**
- **Open-Drain $\overline{RESET}$ Output**
- **Temperature Range: –55°C to 125°C**
- **Small SOT23 Package**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

APPLICATIONS

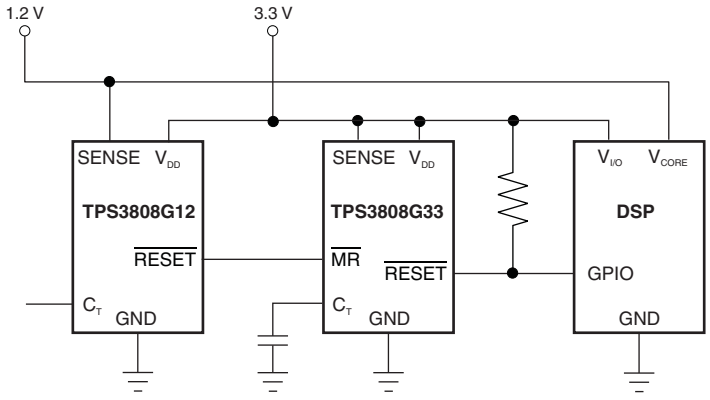
- **DSP or Microcontroller Applications**
- **Notebook/Desktop Computers**
- **PDAs/Hand-Held Products**
- **Portable/Battery Powered Products**
- **FPGA/ASIC Applications**

(1) Custom temperature ranges available

DESCRIPTION/ORDERING INFORMATION

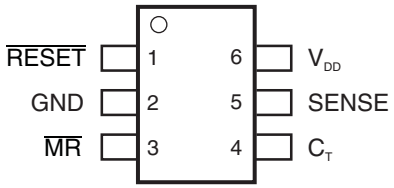
The TPS3808xxx family of microprocessor supervisory circuits monitors system voltages from 0.4 V to 5.0 V, asserting an open-drain $\overline{RESET}$ signal when the SENSE voltage drops below a preset threshold or when the manual reset ($\overline{MR}$) pin drops to a logic low. The $\overline{RESET}$ output remains low for the user-adjustable delay time after the SENSE voltage and manual reset ($\overline{MR}$) return above the respective thresholds.

The TPS3808 uses a precision reference to achieve 0.5% threshold accuracy for $V_{IT} \leq 3.3$ V. The reset delay time can be set to 20 ms by disconnecting the C_T pin, 300 ms by connecting the C_T pin to V_{DD} using a resistor, or can be user-adjusted between 1.25 ms and 10 s by connecting the C_T pin to an external capacitor. The TPS3808 has a very low typical quiescent current of 2.4 μA, so it is well-suited to battery-powered applications. It is available in a small SOT23 package, and is fully specified over a temperature range of –55°C to +125°C (T_J).



Typical Application Circuit

DBV (SOT-23) PACKAGE
(TOP VIEW)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT(2)	NOMINAL SUPPLY VOLTAGE(3)	THRESHOLD VOLTAGE (V_{IT})	TOP-SIDE MARKING
TPS3808G01MDBVTEP	Adjustable	0.405 V	NXS
TPS3808G09MDBVTEP(4)	0.9 V	0.84 V	PREVIEW
TPS3808G12MDBVTEP(4)	1.2 V	1.12 V	PREVIEW
TPS3808G125MDBVTEP(4)	1.25 V	1.16 V	PREVIEW
TPS3808G15MDBVTEP(4)	1.5 V	1.40 V	PREVIEW
TPS3808G18MDBVTEP(4)	1.8 V	1.67 V	PREVIEW
TPS3808G25MDBVTEP(4)	2.5 V	2.33 V	PREVIEW
TPS3808G30MDBVTEP(4)	3.0 V	2.79 V	PREVIEW
TPS3808G33MDBVREP	3.3 V	3.07 V	CHK
TPS3808G50MDBVTEP(4)	5.0 V	4.65 V	PREVIEW

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com. Devices are shipped on tape and reel with either 250 units per reel (part numbers ending with 'TEP') or 3000 units per reel (part numbers ending with 'REP').
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Custom threshold voltages from 0.82 V to 3.3 V, 4.4 V to 5.0 V are available through the use of factory EEPROM programming. Minimum order quantities apply. Contact factory for details and availability.
(4) Product Preview. Contact your TI sales representative for availability.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating junction temperature range, unless otherwise noted.

	TPS3808	UNIT
Input voltage range, V_{DD}	–0.3 to 7.0	V
C_T voltage range, V_{CT}	–0.3 to V_{DD} + 0.3	V
Other voltage ranges: V_{RESET}, V_{MR}, V_{SENSE}	–0.3 to 7	V
$\overline{RESET}$ pin current	5	mA
Operating junction temperature range, T_J(2)	–55 to +150	°C
Storage temperature range, T_{stg}	–65 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

ELECTRICAL CHARACTERISTICS

1.7 V ≤ V_{DD} ≤ 6.5 V, R_{LRESET} = 100 kΩ, C_{LRESET} = 50 pF, over operating temperature range (T_J = –55°C to +125°C), unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input supply range			1.7		6.5	V
I_{DD}	Supply current (current into V_{DD} pin)		V_{DD} = 3.3 V, $\overline{RESET}$ not asserted $\overline{MR}$, $\overline{RESET}$, C_T open		2.4	5.0	µA
			V_{DD} = 6.5 V, $\overline{RESET}$ not asserted $\overline{MR}$, $\overline{RESET}$, C_T open		2.7	6.0	µA
V_{OL}	Low-level output voltage		1.3 V ≤ V_{DD} < 1.8 V, I_{OL} = 0.4 mA			0.3	V
			1.8 V ≤ V_{DD} ≤ 6.5 V, I_{OL} = 1.0 mA			0.4	V
	Power-up reset voltage(1)		V_{OL} (max) = 0.2 V, $I_{\overline{RESET}}$ = 15 µA			0.8	V
V_{IT}	Negative-going input threshold accuracy	TPS3808G01		–2.0	±1.0	+2.0	%
		V_{IT} ≤ 3.3 V		–1.7	±0.5	+1.7	
		3.3 V < V_{IT} ≤ 5.0 V		–2.0	±1.0	+2.0	
V_{HYS}	Hysteresis on V_{IT} pin	TPS3808G01			1.5	3.0	%V_{IT}
		Fixed versions			1.0	2.5	
$R_{\overline{MR}}$	$\overline{MR}$ Internal pullup resistance			70	90		kΩ
I_{SENSE}	Input current at SENSE pin	TPS3808G01	V_{SENSE} = V_{IT}	–25		25	nA
		Fixed versions	V_{SENSE} = 6.5 V		1.7		µA
I_{OH}	$\overline{RESET}$ leakage current		$V_{\overline{RESET}}$ = 6.5 V, $\overline{RESET}$ not asserted			300	nA
C_{IN}	Input capacitance, any pin	C_T pin	V_{IN} = 0 V to V_{DD}		5		pF
		Other pins	V_{IN} = 0 V to 6.5 V		5		
V_{IL}	$\overline{MR}$ logic low input			0		0.3 V_{DD}	V
V_{IH}	$\overline{MR}$ logic high input			0.7 V_{DD}		V_{DD}	
t_w	Input pulse width to $\overline{RESET}$	SENSE	V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		20		µs
		$\overline{MR}$	V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		0.001		
t_d	$\overline{RESET}$ delay time	C_T = Open	See Timing Diagram	12	20	29	ms
		C_T = V_{DD}		180	300	440	ms
		C_T = 100 pF		0.75	1.25	1.8	ms
		C_T = 180 nF		0.7	1.2	1.8	s
t_{pHL}	Propagation delay	$\overline{MR}$ to $\overline{RESET}$	V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		150		ns
	High-to-low level $\overline{RESET}$ delay	SENSE to $\overline{RESET}$	V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		20		µs
θ_{JA}	Thermal resistance, junction-to-ambient				290		°C/W

(1) The lowest supply voltage (V_{DD}) at which $\overline{RESET}$ becomes active. $T_{rise(VDD)}$ ≥ 15 µs/V.

FUNCTIONAL BLOCK DIAGRAMS

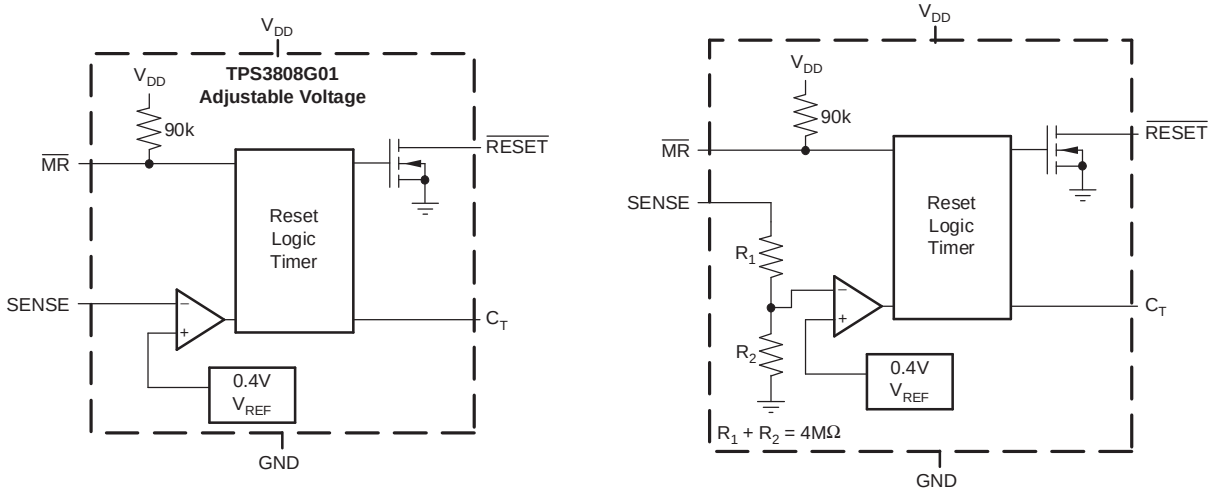


Figure 1. Adjustable and Fixed Voltage Versions

PIN ASSIGNMENTS

DBV PACKAGE
SOT23
(TOP VIEW)

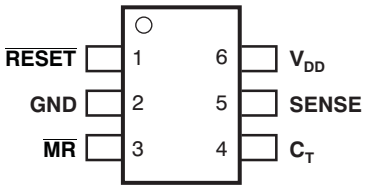


Table 1. TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	SOT23 (DBV) PIN NO.	
$\overline{\text{RESET}}$	1	$\overline{\text{RESET}}$ is an open-drain output that is driven to a low impedance state when $\overline{\text{RESET}}$ is asserted (either the SENSE input is lower than the threshold voltage (V_{IT}) or the $\overline{\text{MR}}$ pin is set to a logic low). $\overline{\text{RESET}}$ remains low (asserted) for the reset period after both SENSE is above V_{IT} and $\overline{\text{MR}}$ is set to a logic high. A pullup resistor from 10 kΩ to 1 MΩ should be used on this pin, and allows the reset pin to attain voltages higher than V_{DD}.
GND	2	Ground
$\overline{\text{MR}}$	3	Driving the manual reset pin ($\overline{\text{MR}}$) low asserts $\overline{\text{RESET}}$. $\overline{\text{MR}}$ is internally tied to V_{DD} by a 90kΩ pullup resistor.
C_T	4	Reset period programming pin. Connecting this pin to V_{DD} through a 40-kΩ to 200-kΩ resistor or leaving it open results in fixed delay times (see Electrical Characteristics). Connecting this pin to a ground referenced capacitor ≥ 100 pF gives a user-programmable delay time. See the *Selecting the Reset Delay Time* section for more information.
SENSE	5	This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage V_{IT}, then $\overline{\text{RESET}}$ is asserted.
V_{DD}	6	Supply voltage. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

TIMING DIAGRAM

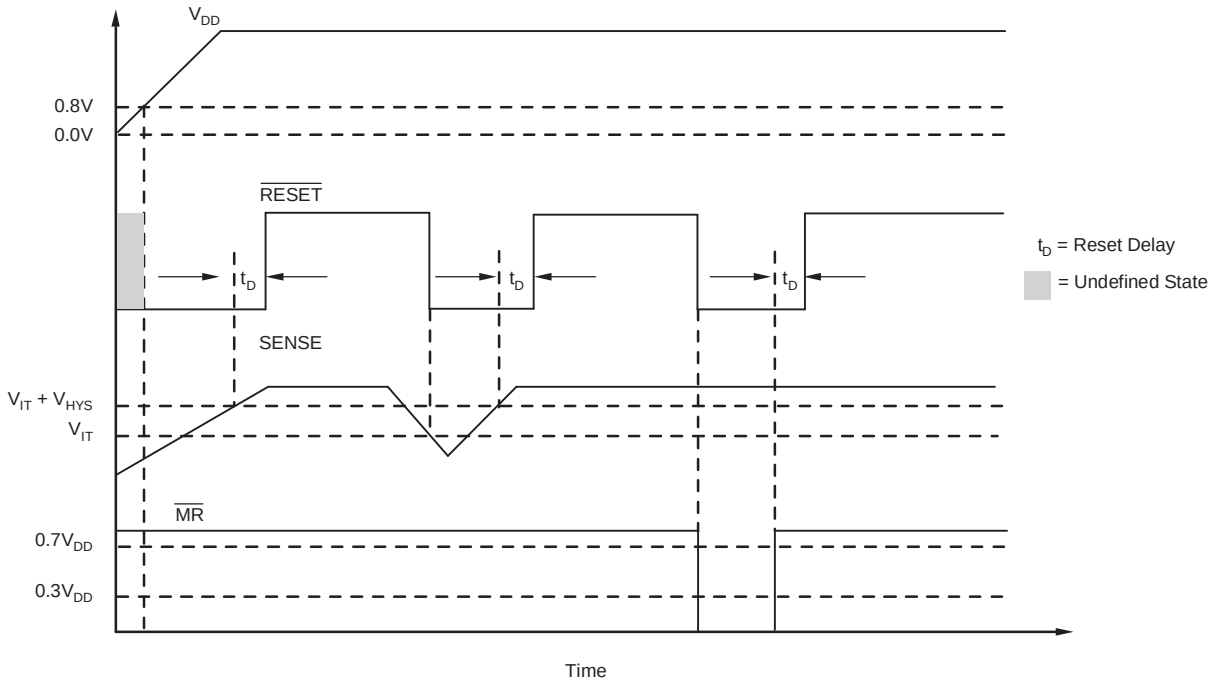


Figure 2. TPS3808 Timing Diagram Showing $\overline{MR}$ and SENSE Reset Timing

TRUTH TABLE

$\overline{MR}$	SENSE > V_{IT}	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{DD} = 3.3 V, R_{LRESET} = 100kΩ, and C_{LRESET} = 50pF, unless otherwise noted.

SUPPLY CURRENT vs SUPPLY VOLTAGE

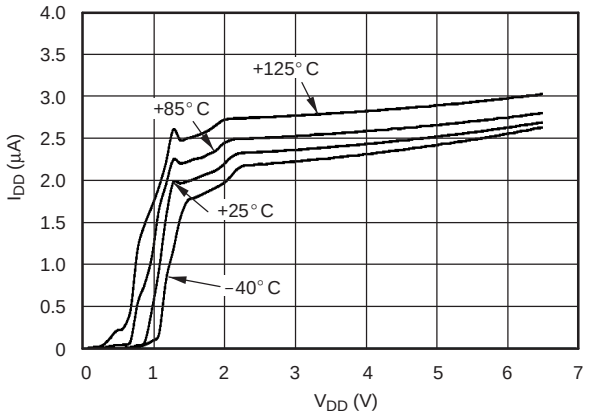


Figure 3.

RESET TIMEOUT PERIOD vs C_T

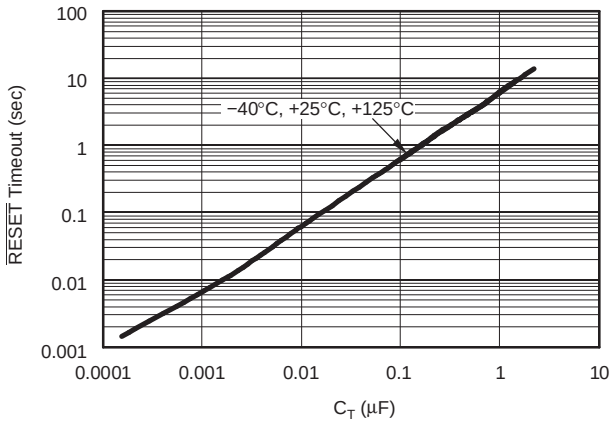


Figure 4.

NORMALIZED RESET TIMEOUT PERIOD vs TEMPERATURE (C_T = OPEN, C_T = V_{DD}, C_T = Any)

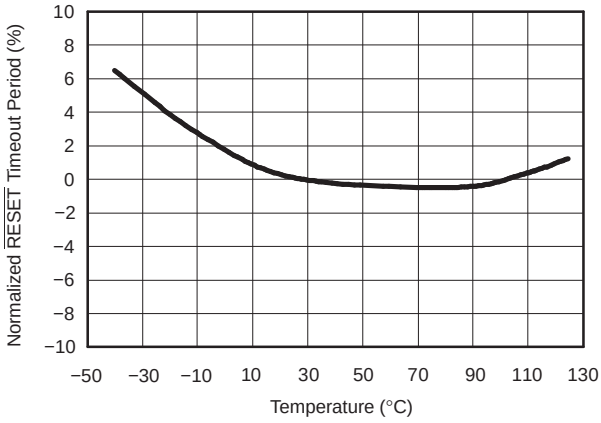


Figure 5.

MAXIMUM TRANSIENT DURATION AT SENSE vs SENSE THRESHOLD OVERDRIVE VOLTAGE

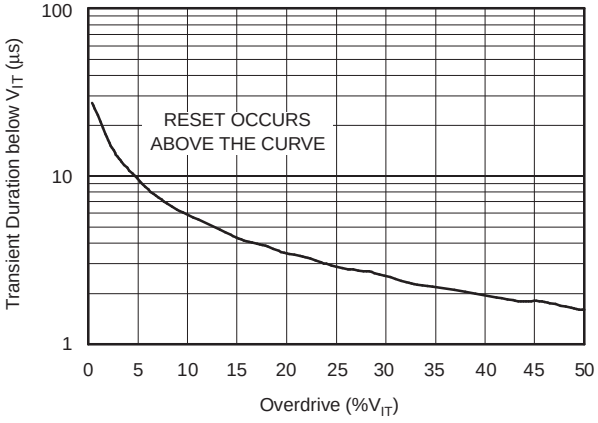


Figure 6.

NORMALIZED SENSE THRESHOLD VOLTAGE (V_{IT}) vs TEMPERATURE

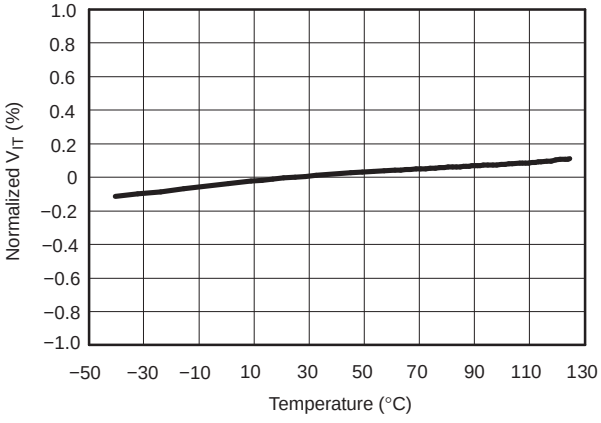


Figure 7.

LOW-LEVEL RESET VOLTAGE vs RESET CURRENT

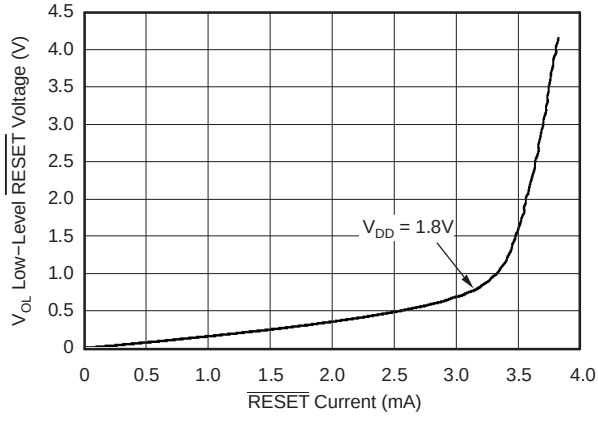


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{DD} = 3.3 V, R_{LRESET} = 100kΩ, and C_{LRESET} = 50pF, unless otherwise noted.

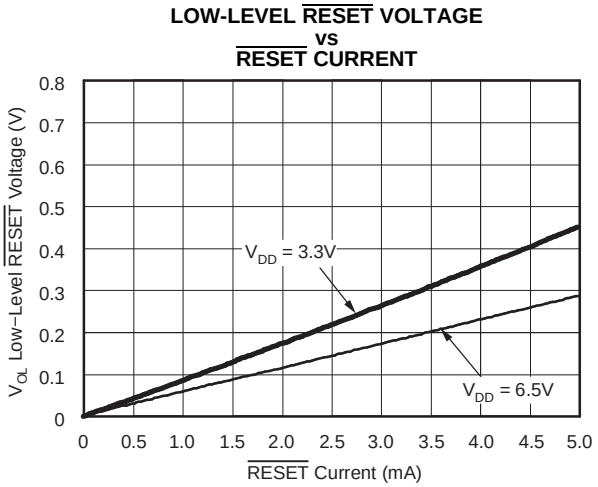


Figure 9.

DEVICE OPERATION

The TPS3808 microprocessor supervisory product family is designed to assert a RESET signal when either the SENSE pin voltage drops below V_{IT} or the manual reset (MR) is driven low. The RESET output remains asserted for a user-adjustable time after both the manual reset (MR) and SENSE voltages return above the respective thresholds. A broad range of voltage threshold and reset delay time adjustments are available, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82 V to 3.3 V or from 4.4 V to 5.0 V, while the TPS3808G01 can be set to any voltage above 0.405 V using an external resistor divider. Two preset delay times are also user-selectable: connecting the C_T pin to V_{DD} results in a 300ms reset delay, while leaving the C_T pin open yields a 20-ms reset delay. In addition, connecting a capacitor between C_T and GND allows the designer to select any reset delay period from 1.25 ms to 10 s.

RESET OUTPUT

A typical application of the TPS3808G25 used with the OMAP1510 processor is shown in Figure 10. The open-drain RESET output is typically connected to the RESET input of a microprocessor. A pullup resistor must be used to hold this line high when RESET is not asserted. The RESET output is undefined for voltage below 0.8 V, but this is normally not a problem since most microprocessors do not function below this voltage. RESET remains high (unasserted) as long as SENSE is above its threshold (V_{IT}) and the manual reset (MR) is logic high. If either SENSE falls below V_{IT} or MR is driven low, RESET is asserted, driving the RESET pin to a low impedance.

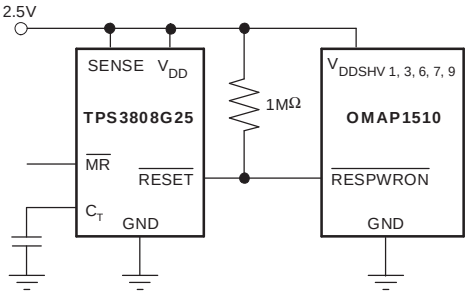


Figure 10. Typical Application of the TPS3808 with an OMAP Processor

Once MR is again logic high and SENSE is above V_{IT} + V_{HYS} (the threshold hysteresis), a delay circuit is enabled which holds RESET low for a specified reset delay period. Once the reset delay has expired, the RESET pin goes to a high impedance state. The pullup resistor from the open-drain RESET to the supply line can be used to allow the reset signal for the microprocessor to have a voltage higher than V_{DD} (up to 6.5 V). The pullup resistor should be no smaller than 10 kΩ as a result of the finite impedance of the RESET line.

SENSE INPUT

The SENSE input provides a terminal at which any system voltage can be monitored. If the voltage on this pin drops below V_{IT}, then RESET is asserted. The comparator has a built-in hysteresis to ensure smooth RESET assertions and de-assertions. It is good analog design practice to put a 1-nF to 10-nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

The TPS3808G01 can be used to monitor any voltage rail down to 0.405 V using the circuit shown in Figure 11.

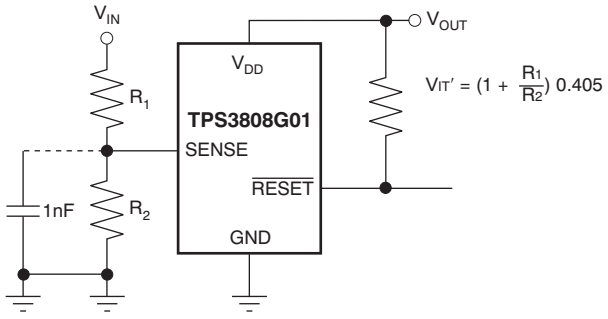


Figure 11. Using the TPS3808G01 to Monitor a User-Defined Threshold Voltage

MANUAL RESET (MR) INPUT

The manual reset (MR) input allows a processor or other logic circuits to initiate a reset. A logic low (0.3 V_{DD}) on MR causes RESET to assert. After MR returns to a logic high and SENSE is above its reset threshold, RESET is de-asserted after the user defined reset delay expires. Note that MR is internally tied to V_{DD} using a 90-kΩ resistor so this pin can be left unconnected if MR will not be used.

See Figure 12 for how MR can be used to monitor multiple system voltages. Note that if the logic signal driving MR does not go fully to V_{DD}, there will be some additional current draw into V_{DD} as a result of the internal pullup resistor on MR. To minimize current draw, a logic-level FET can be used as illustrated in Figure 13.

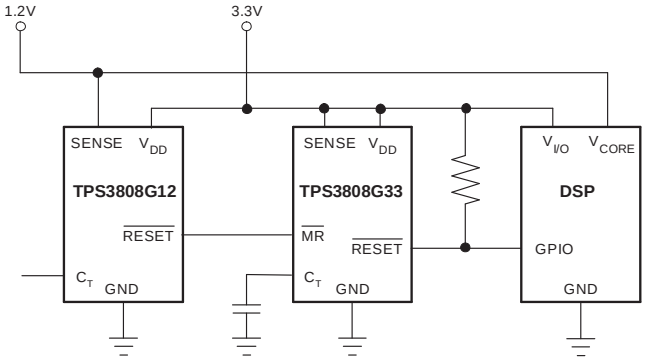


Figure 12. Using $\overline{MR}$ to Monitor Multiple System Voltages

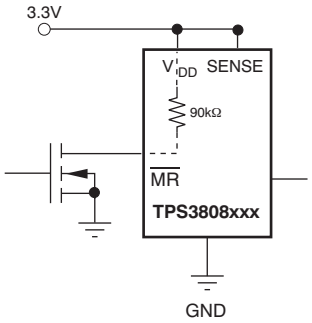


Figure 13. Using an External MOSFET to Minimize I_{DD} When $\overline{MR}$ Signal Does Not Go to V_{DD}

SELECTING THE RESET DELAY TIME

The TPS3808 has three options for setting the $\overline{RESET}$ delay time as shown in Figure 14. Figure 14a shows the configuration for a fixed 300-ms typical delay time by tying C_T to V_{DD}; a resistor from 40 kΩ to 200 kΩ must be used. Supply current is not affected by the choice of resistor. Figure 14b shows a fixed 20-ms delay time by leaving the C_T pin open. Figure 14c shows a ground referenced capacitor connected to C_T for a user-defined program time between 1.25 ms and 10 s.

The capacitor C_T should be ≥ 100 pF nominal value in order for the TPS3808xxx to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using the following equation:

$$C_T\,(nF) = \left[t_D\,(s) - 0.5 \times 10^{-3}\,(s)\right] \times 175 \quad (1)$$

The reset delay time is determined by the time it takes an on-chip precision 220-nA current source to charge the external capacitor to 1.23 V. When a $\overline{RESET}$ is asserted the capacitor is discharged. When the $\overline{RESET}$ conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23 V, $\overline{RESET}$ is deasserted. Note that a low-leakage type capacitor such as a ceramic should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

IMMUNITY TO SENSE PIN VOLTAGE TRANSIENTS

The TPS3808 is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive, as shown in the *Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage* graph (Figure 6) in the Typical Characteristics section.

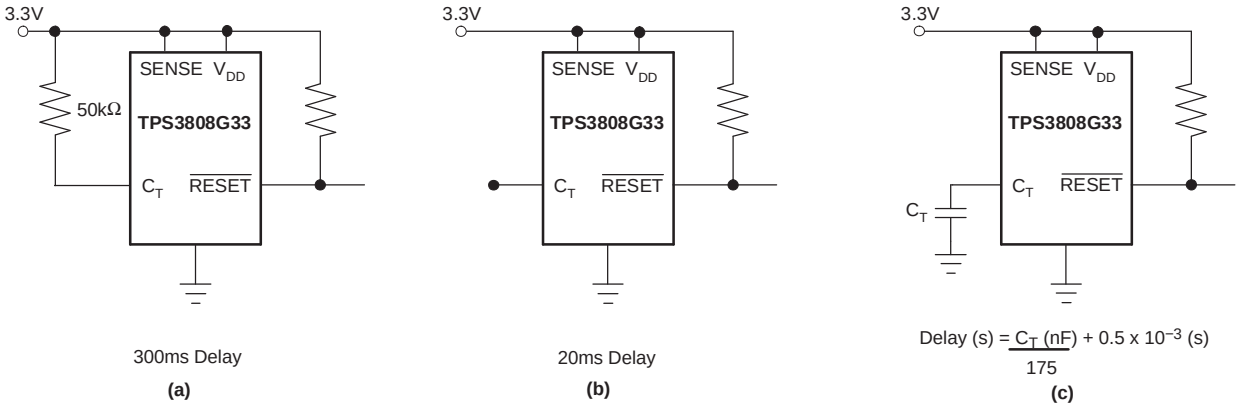


Figure 14. Configuration Used to Set the $\overline{RESET}$ Delay Time

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS3808G01MDBVTEP	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	NXS	Samples
TPS3808G33MDBVREP	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CHK	Samples
V62/08607-01XE	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	NXS	Samples
V62/08607-09XE	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CHK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

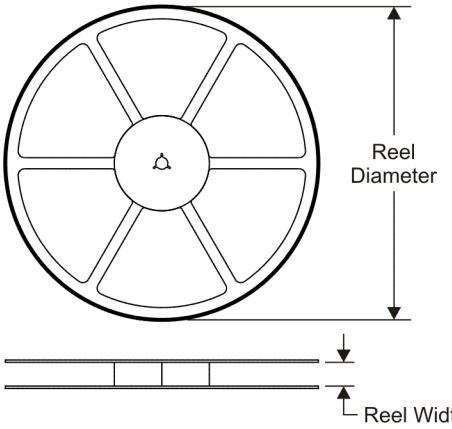
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

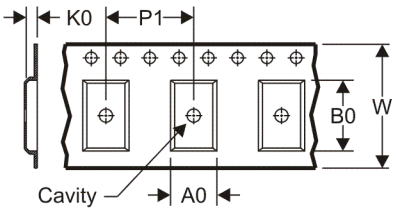
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

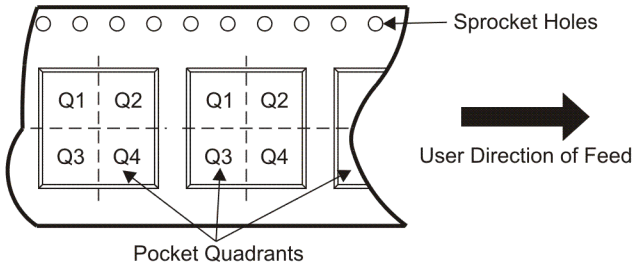


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

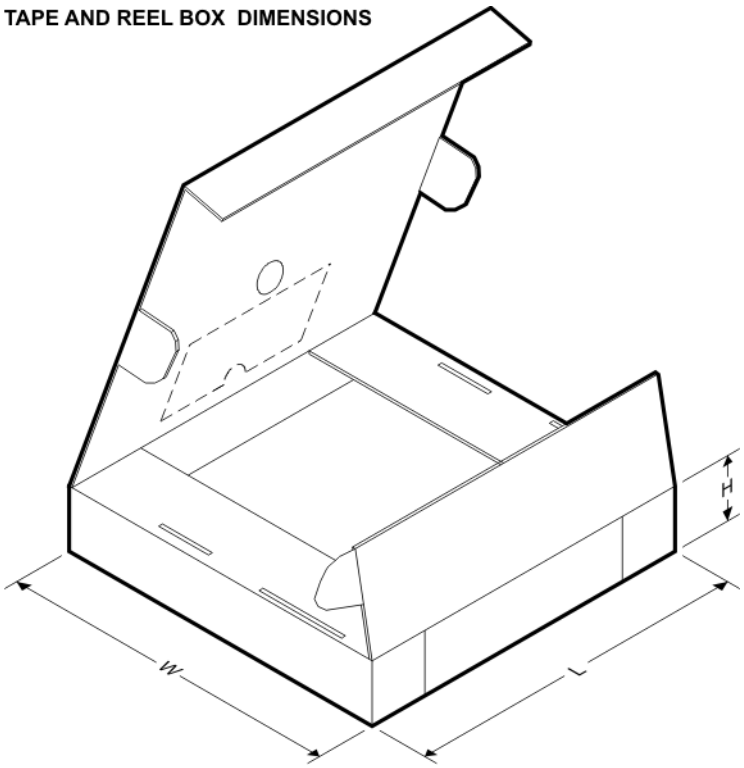
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3808G01MDBVTEP	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G33MDBVREP	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

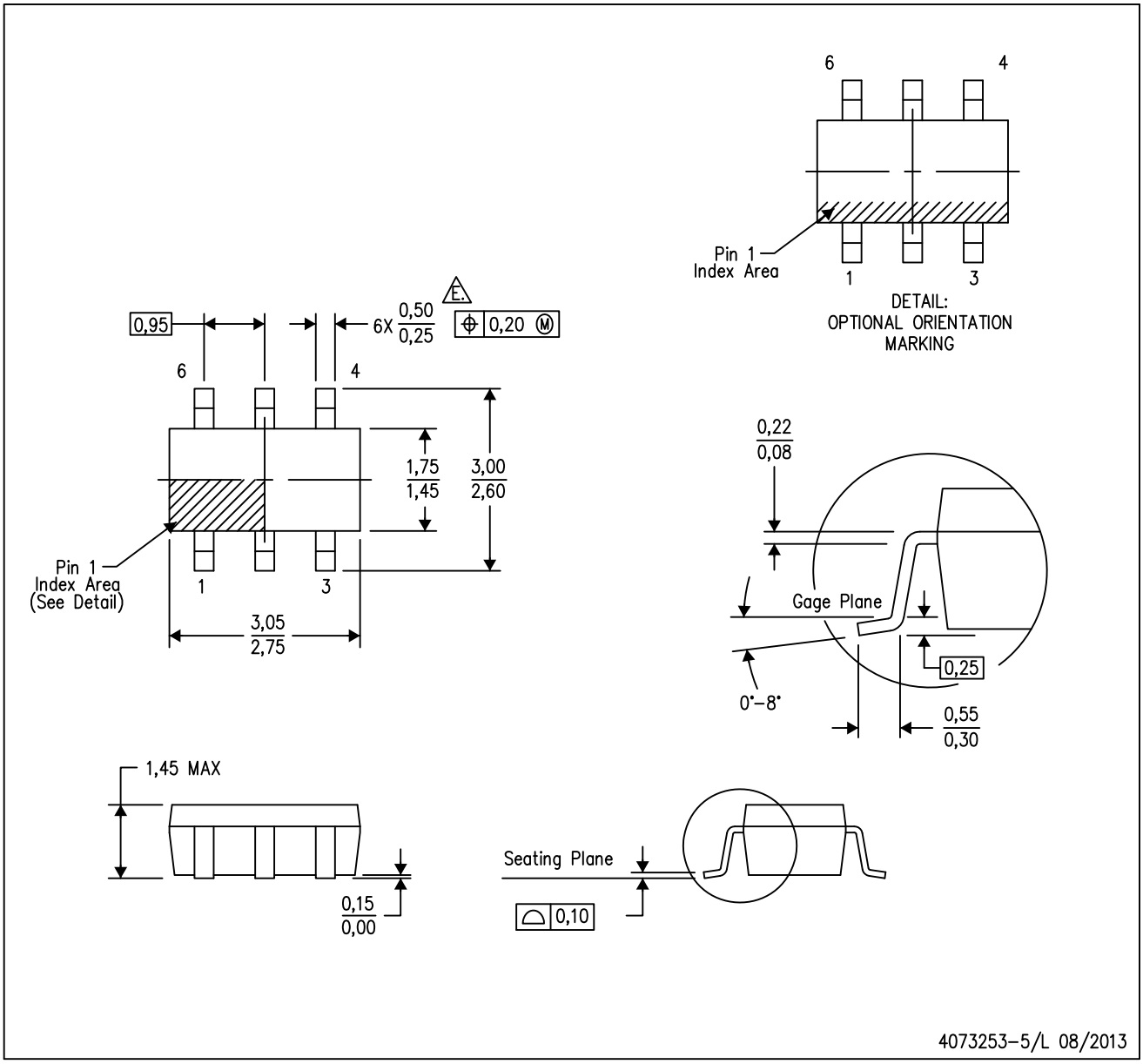
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

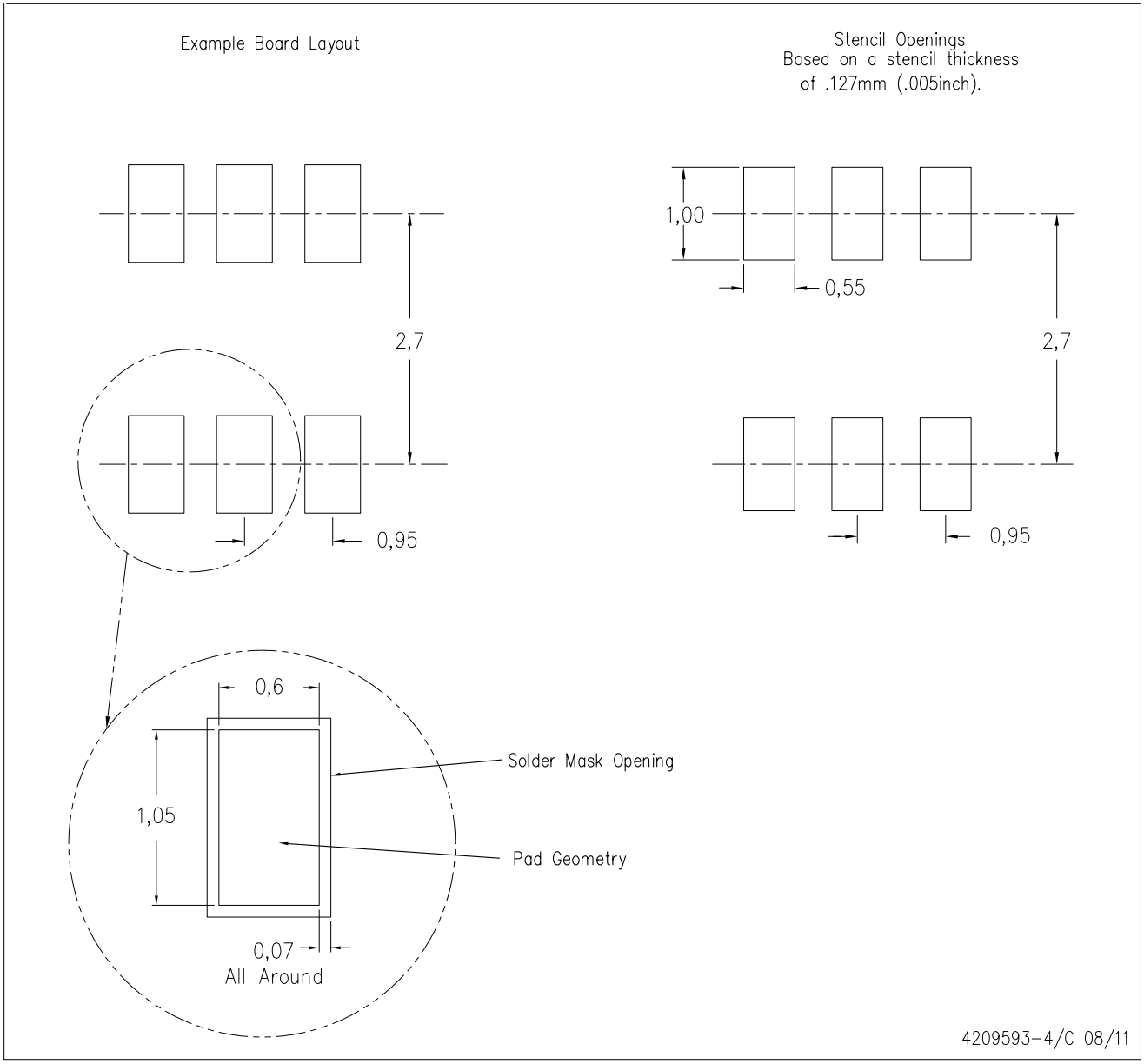
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3808G01MDBVTEP	SOT-23	DBV	6	250	203.0	203.0	35.0
TPS3808G33MDBVREP	SOT-23	DBV	6	3000	203.0	203.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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