WIDE-INPUT SYNCHRONOUS BUCK CONTROLLER

Check for Samples: TPS40055-EP

FEATURES

- **Operating Input Voltage 8 V to 40 V**
- **Input Voltage Feed-Forward Compensation**
- **< 1 % Internal 0.7-V Reference**
- **Programmable Fixed-Frequency Up to 1-MHz Voltage Mode Controller**
- **Internal Gate Drive Outputs for High-Side and Synchronous N-Channel MOSFETs**
- **16-Pin PowerPAD™ Package (θ_{JC} = 25°C/W)**
- **Thermal Shutdown**
- **Externally Synchronizable**
- **Programmable High-Side Sense Short-Circuit Protection**
- **Programmable Closed-Loop Soft-Start**
- **TPS40055 Source/Sink**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Additional temperature ranges available - contact factory

APPLICATIONS

- **Power Modules**
- **Networking/Telecom**
- **Industrial/Servers**

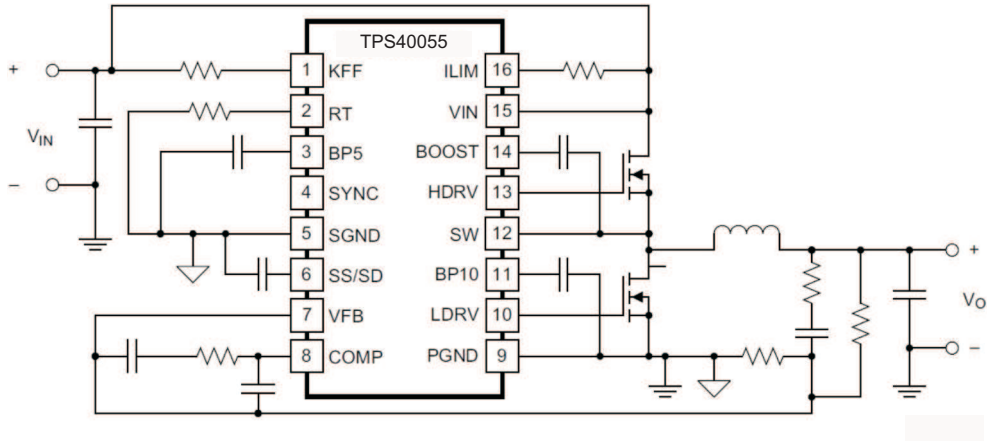
DESCRIPTION

The TPS40055 is a family of high-voltage, wide input (8 V to 40 V), synchronous, step-down converters. The TPS40055 family offers design flexibility with a variety of user programmable functions, including soft-start, UVLO, operating frequency, voltage feed-forward, high-side current limit, and loop compensation.

The TPS40055 are also synchronizable to an external supply. The TPS40055 incorporates MOSFET gate drivers for external N-channel high-side and synchronous rectifier (SR) MOSFETs. Gate drive logic incorporates anti-cross conduction circuitry to prevent simultaneous high-side and synchronous rectifier conduction.

The TPS40055 uses voltage feed-forward control techniques to provide good line regulation over the wide (4:1) input voltage range and fast response to input line transients with near constant gain with input variation which eases loop compensation. The externally programmable current limit provides pulse-by-pulse current limit, as well as a hiccup mode operation utilizing an internal fault counter for longer duration overloads.

SIMPLIFIED APPLICATION DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	APPLICATION(2)	PACKAGE(3)(4)	PART NUMBER
–55°C to 125°C	SOURCE/SINK	Plastic HTSSOP (PWP)	TPS40055MPWPREP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) See *Application Information* section.
(3) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(4) The PWP package is also available taped and reeled. Add an R suffix to the device type. See the application section of the data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE / UNIT
V_{IN}	Input voltage range	VIN	45 V
		VFB, SS, SYNC	–0.3 V to 6 V
		SW	–0.3 V to 45 V
		SW, transient < 50 ns	–2.5 V
		KFF, with $I_{IN(max)}$ = –5 mA	–0.3 V to 11 V
V_{OUT}	Output voltage range	COMP, RT, SS	–0.3 V to 6 V
I_{IN}	Input current	KFF	5 mA
I_{OUT}	Output current	RT	200 µA
T_J	Operating junction temperature range		–55°C to 140°C
T_{stg}	Storage temperature(2)		–55°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C
T_{JC}	Thermal resistance junction-to-case		26.6°C/W
T_{JA}	Thermal resistance junction-to-ambient (3) (4)		36.5°C/W
T_{JP}	Thermal resistance junction-to-bottom of thermal pad (3)		2.1°C/W
φ_{JT}	Junction-to-top thermal parameter (3) (4)		0.848°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in reduced overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.
(3) See technical brief SLMA002 - PowerPAD Thermally Enhanced Package(http://www-s.ti.com/sc/techlit/slma002).
(4) Tested in accordance with the thermal metric definitions of EIA/JESD51-5.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage	8		40	V
T_A	Operating free-air temperature	–55		125	°C

ELECTRICAL CHARACTERISTICS

T_A = –55°C to 125°C, V_{IN} = 24 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 150 µA, f_{SW} = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range, VIN		8		40	V
OPERATING CURRENT						
I_{DD}	Quiescent current	Output drivers not switching, VFB ≥ 0.75 V		1.5	3.3	mA
BP5						
V_{BP5}	Output voltage	I_{OUT} ≤ 1 mA	4.7	5	5.3	V
OSCILLATOR/RAMP GENERATOR(1)						
f_{OSC}	Accuracy	8 V ≤ V_{IN} ≤ 40 V	465	520	585	kHz
V_{RAMP}	PWM ramp voltage(2)	V_{PEAK} – V_{VAL}		2		V
V_{IH}	High-level input voltage, SYNC		2		5	V
V_{IL}	Low-level input voltage, SYNC				0.8	V
I_{SYNC}	Input current, SYNC			5	11	µA
	Pulse width, SYNC		50			ns
V_{RT}	RT voltage		2.37	2.5	2.59	V

(1) I_{KFF} increases with SYNC frequency, I_{KFF} decreases with maximum duty cycle.
(2) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –55°C to 125°C, V_{IN} = 24 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 150 µA, f_{SW} = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Maximum duty cycle	V_{FB} = 0 V, f_{SW} ≤ 500 kHz	84%		94%	
		V_{FB} = 0 V, 500 kHz ≤ f_{SW} ≤ 1 MHz(2)	80%			
	Minimum duty cycle	V_{FB} ≥ 0.75 V			0%	
V_{KFF}	Feed-forward voltage		3.35	3.48	3.7	V
I_{KFF}	Feed-forward current operating range(2)		20		1200	µA
SOFT START						
I_{SS}	Soft-start source current		1.2	2.35	3.6	µA
V_{SS}	Soft-start clamp voltage			3.7		V
t_{DSCH}	Discharge time	C_{SS} = 220 pF	1.4	2.2	3.4	µs
t_{SS}	Soft-start time	C_{SS} = 220 pF, 0 V ≤ V_{SS} ≤ 1.6 V	102	150	230	µs
BP10						
V_{BP10}	Output voltage	I_{OUT} ≤ 1 mA	8.9	9.6	10.45	V
ERROR AMPLIFIER						
V_{FB}	Feedback input voltage	8 V ≤ V_{IN} ≤ 40 V, T_A = 25°C	0.698	0.7	0.704	V
		8 V ≤ V_{IN} ≤ 40 V, 0°C ≤ T_A ≤ 125°C	0.689	0.7	0.717	
		8 V ≤ V_{IN} ≤ 40 V, –55°C ≤ T_A ≤ 125°C	0.689	0.7	0.719	
G_{BW}	Gain bandwidth(3)		2.8	5		MHz
A_{VOL}	Open loop gain		40	80		dB
I_{OH}	High-level output source current		1.85	4		mA
I_{OL}	Low-level output source current		1.95	4		
V_{OH}	High-level output voltage	I_{SOURCE} = 500 µA	3.1	3.5		V
V_{OL}	Low-level output voltage	I_{SINK} = 500 µA		0.2	0.37	
I_{BIAS}	Input bias current	V_{FB} = 0.7 V		100	220	nA
CURRENT LIMIT						
I_{SINK}	Current limit sink current		7.5	10	12.2	µA
	Propagation delay to output	V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM} – 0.5 V)		300		ns
		V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM} – 2 V)		200		
t_{ON}	Switch leading-edge blanking pulse time(3)		100			ns
t_{OFF}	Off time during a fault			7		cycles
V_{OS}	Offset voltage SW vs ILIM	V_{ILIM} = 23.6 V, T_A = 25°C	–115	–70	–50	mV
		V_{ILIM} = 23.6 V, 0°C ≤ T_A ≤ 125°C	–155		–38	
		V_{ILIM} = 23.6 V, –55°C ≤ T_A ≤ 125°C	–155		–10	
		V_{ILIM} = 11.6 V, T_A = 25°C	–118		–43	
		V_{ILIM} = 11.6 V, 0°C ≤ T_A ≤ 125°C	–160		–45	
		V_{ILIM} = 11.6 V, T_A = –55°C to 125°C	–160		–15	
OUTPUT DRIVER						
t_{LRISE}	Low-side driver rise time	C_{LOAD} = 2200 pF		48	110	ns
t_{LFALL}	Low-side driver fall time			24	58	
t_{HRISE}	High-side driver rise time	C_{LOAD} = 2200 pF, (HDRV – SW)		48	105	ns
t_{HFALL}	High-side driver fall time			36	82	
V_{OH}	High-level output voltage, HDRV	I_{HDRV} = –0.1 A (HDRV - SW)	BOOST –1.9	BOOST –1		V
V_{OL}	Low-level output voltage, HDRV	I_{HDRV} = 0.1 A (HDRV - SW)			0.85	V

(3) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –55°C to 125°C, V_{IN} = 24 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 150 µA, f_{SW} = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, LDRV	I_{LDRV} = –0.1 A	BP10 –1.8	BP10 –1		V
V_{OL}	Low-level output voltage, LDRV	I_{LDRV} = 0.1 A			0.6	V
	Minimum controllable pulse width			100	160	ns
SS/SD SHUTDOWN						
V_{SD}	Shutdown threshold voltage	Outputs off	85	125	170	mV
V_{EN}	Device active threshold voltage		180	210	260	mV
BOOST REGULATOR						
V_{BOOST}	Output voltage	V_{IN} = 24 V	30.8	32.2	33.9	V
SW NODE						
I_{LEAK}	Leakage current(4)				35	µA
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature(4)			165		°C
	Hysteresis(4)			20		
UVLO						
V_{UVLO}	KFF programmable threshold voltage	R_{KFF} = 28.7 kΩ	6.85	7.5	7.95	V
V_{DD}	UVLO, fixed		7.05	7.5	7.9	
	UVLO, hysteresis			0.46		

(4) Ensured by design. Not production tested.

TYPICAL CHARACTERISTICS

OFFSET VOLTAGE (VLim vs SW) TEMPERATURE

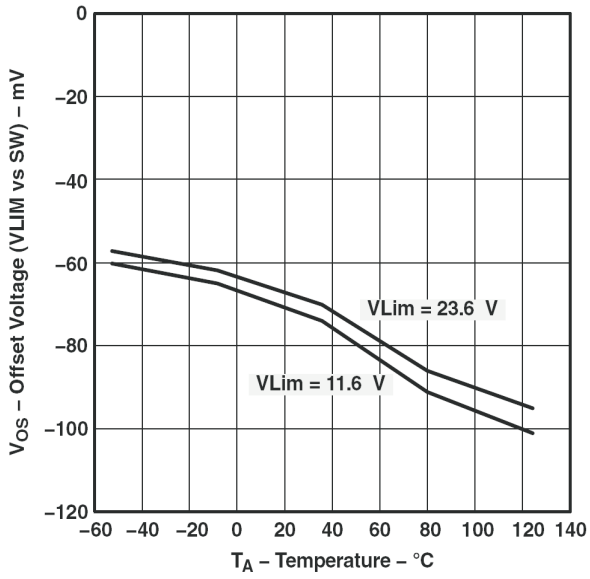
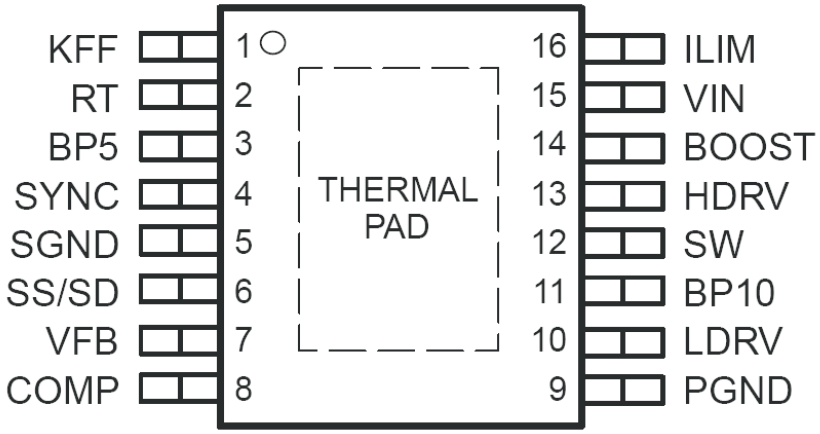


Figure 1.

DEVICE INFORMATION

PWP PACKAGE(1)(2)
(TOP VIEW)



(1) For more information on the PWP package, see the Texas Instruments Technical Brief (SLMA002)

(2) PowerPAD heat slug must be connected to SGND (pin 5) or electrically isolated from all other pins.

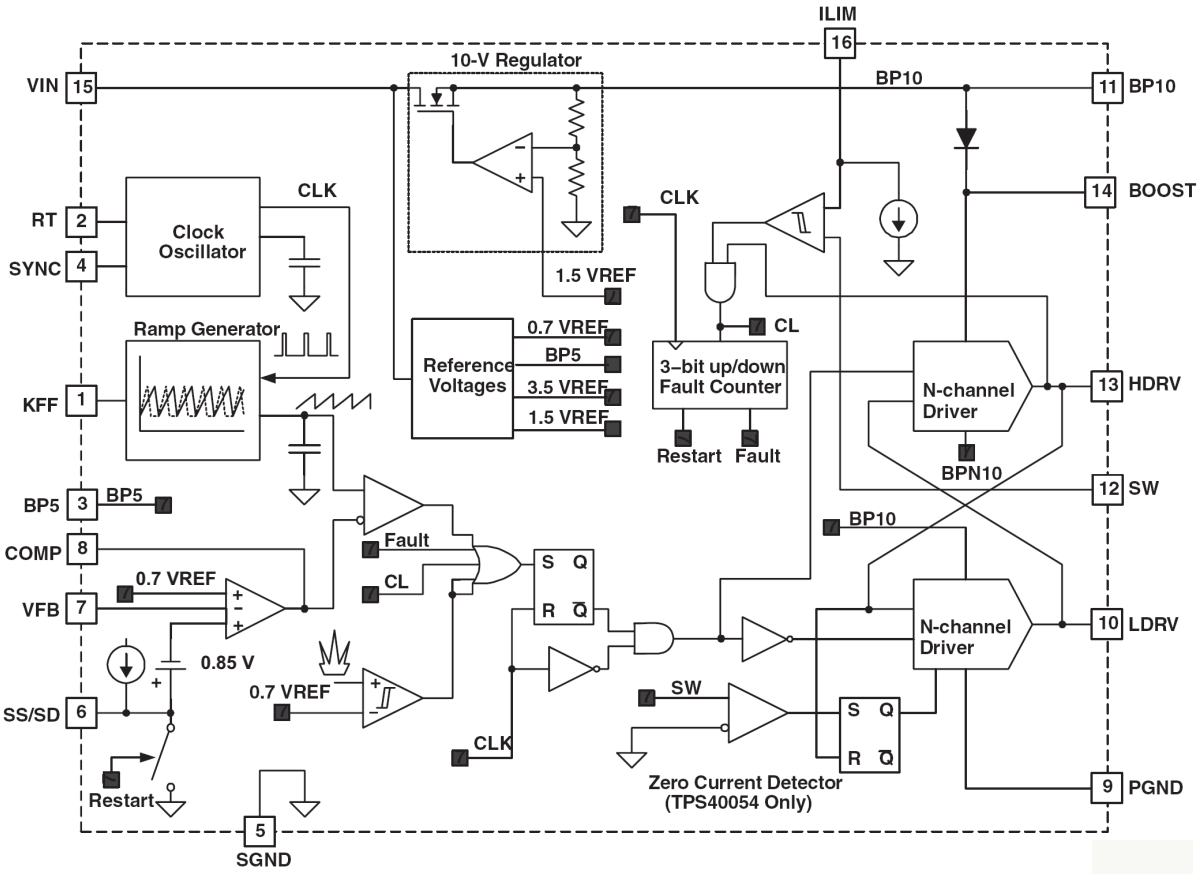
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BOOST	14	O	Gate drive voltage for the high side N-channel MOSFET. The BOOST voltage is 9 V greater than the input voltage. A 0.1-µF ceramic capacitor should be connected from this pin to the drain of the lower MOSFET.
BP5	3	O	5-V reference. This pin should be bypassed to ground with a 0.1-µF ceramic capacitor. This pin may be used with an external dc load of 1 mA or less.
BP10	11	O	10-V reference used for gate drive of the N-channel synchronous rectifier. This pin should be bypassed by a 1-µF ceramic capacitor. This pin may be used with an external dc load of 1 mA or less.
COMP	8	O	Output of the error amplifier, input to the PWM comparator. A feedback network is connected from this pin to the VFB pin to compensate the overall loop. The COMP pin is internally clamped above the peak of the ramp to improve large signal transient response.
HDRV	13	O	Floating gate drive for the high-side N-channel MOSFET. This pin switches from BOOST (MOSFET on) to SW (MOSFET off).
ILIM	16	I	Current limit pin used to set the overcurrent threshold. An internal current sink from this pin to ground sets a voltage drop across an external resistor connected from this pin to VCC. The voltage on this pin is compared to the voltage drop (VIN -SW) across the high side MOSFET during conduction.
KFF	1	I	A resistor is connected from this pin to VIN to program the amount of voltage feed-forward. The current fed into this pin is internally divided and used to control the slope of the PWM ramp.
LDRV	10	O	Gate drive for the N-channel synchronous rectifier. This pin switches from BP10 (MOSFET on) to ground (MOSFET off).
PGND	9	–	Power ground reference for the device. There should be a low-impedance path from this pin to the source(s) of the lower MOSFET(s).
RT	2	I	A resistor is connected from this pin to ground to set the internal oscillator and switching frequency.
SGND	5	–	Signal ground reference for the device
SS/SD	6	I	Soft-start programming pin. A capacitor connected from this pin to ground programs the soft-start time. The capacitor is charged with an internal current source of 2.3 µA. The resulting voltage ramp on the SS pin is used as a second non-inverting input to the error amplifier. The output voltage begins to rise when $V_{SS/SD}$ is approximately 0.85 V. The output continues to rise and reaches regulation when $V_{SS/SD}$ is approximately 1.55 V. The controller is considered shut down when VSS/SD is 125 mV or less. All internal circuitry is inactive. The internal circuitry is enabled when $V_{SS/SD}$ is 210 mV or greater. When $V_{SS/SD}$ is less than approximately 0.85 V, the outputs cease switching and the output voltage (V_{OUT}) decays while the internal circuitry remains active.
SW	12	I	This pin is connected to the switched node of the converter and used for overcurrent sensing.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
SYNC	4	I	Synchronization input for the device. This pin can be used to synchronize the oscillator to an external master frequency. If synchronization is not used, connect this pin to SGND.
VFB	7	I	Inverting input to the error amplifier. In normal operation, the voltage on this pin is equal to the internal reference voltage, 0.7 V.
VIN	15	I	Supply voltage for the device

SIMPLIFIED BLOCK DIAGRAM



APPLICATION INFORMATION

The TPS40055 allows the user to optimize the PWM controller to the specific application.

The TPS40055 is the controller of choice for synchronous buck designs, which includes most applications. It has two quadrant operations and will source or sink output current. This provides the best transient response.

SETTING THE SWITCHING FREQUENCY (PROGRAMMING THE CLOCK OSCILLATOR)

The TPS40055 has independent clock oscillator and ramp generator circuits. The clock oscillator serves as the master clock to the ramp generator circuit. The switching frequency, f_{SW} in kHz, of the clock oscillator is set by a single resistor (R_T) to ground. The clock frequency is related to R_T, in kΩ by Equation 1 and the relationship is charted in Figure 3.

$$R_T = \left(\frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 17 \right) k\Omega \quad (1)$$

PROGRAMMING THE RAMP GENERATOR CIRCUIT

The ramp generator circuit provides the actual ramp used by the PWM comparator. The ramp generator provides voltage feed-forward control by varying the PWM ramp slope with line voltage, while maintaining a constant ramp magnitude. Varying the PWM ramp directly with line voltage provides excellent response to line variations since the PWM does not have to wait for loop delays before changing the duty cycle. (See Figure 2).

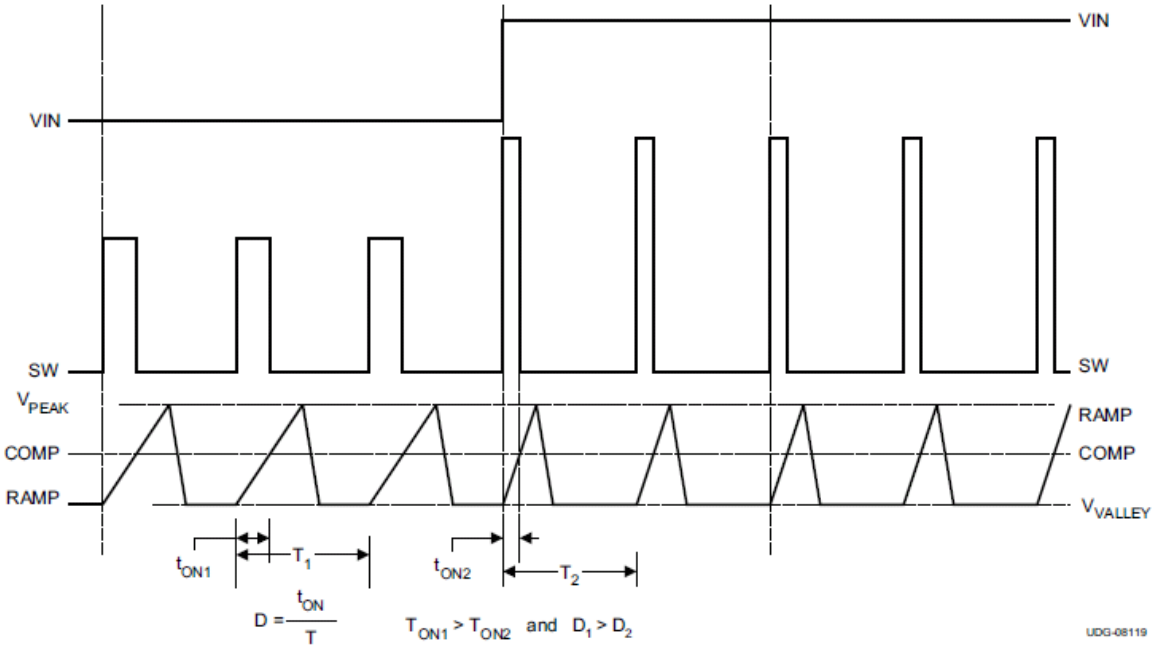


Figure 2. Voltage Feed-Forward Effect on PWM Duty Cycle

The PWM ramp must be faster than the master clock frequency or the PWM is prevented from starting. The PWM ramp time is programmed via a single resistor (R_{KFF}) pulled up to VIN. R_{KFF} is related to RT and the minimum input voltage ($V_{IN(min)}$) through the following:

$$R_{KFF} = \left(V_{IN\,(min)} - 3.5 \right) \times \left(58.14 \times R_T + 1340 \right) \Omega \quad (2)$$

where:

$V_{IN(min)}$ is the ensured minimum start-up voltage. The actual start-up voltage is nominally about 10% lower at 25°C.

R_T is the timing resistance in kΩ.

The curve showing the R_{KFF} required for a given switching frequency (f_{SW}) is shown in Figure 4.

For low input voltage and high duty cycle applications, the voltage feed-forward may limit the duty cycle prematurely. This does not occur for most applications. The voltage control loop controls the duty cycle and regulates the output voltage. For more information on large duty cycle operation, see the application note (SLUA310).

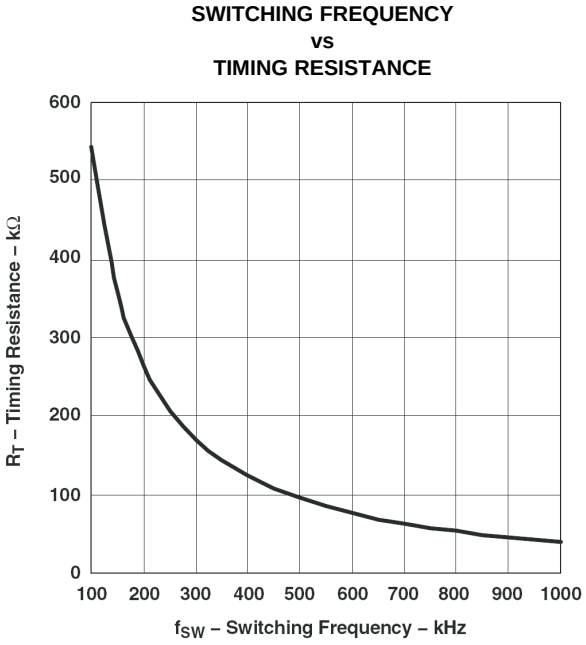


Figure 3.

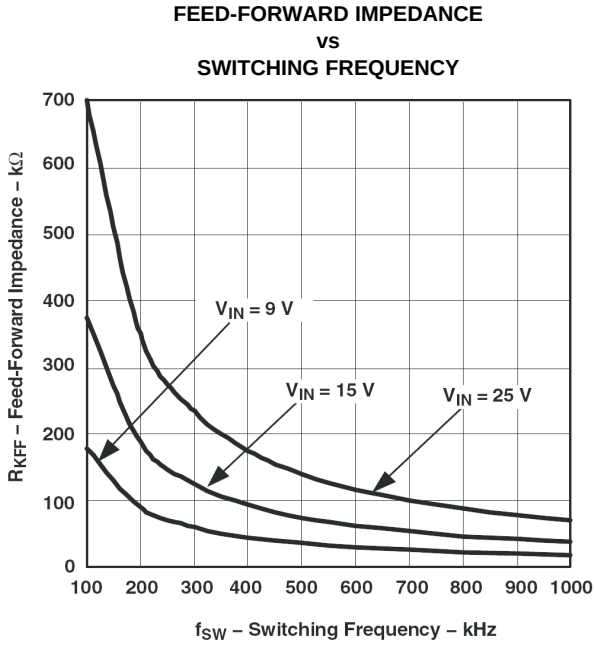


Figure 4.

UVLO OPERATION

The TPS40055 uses variable (user programmable) UVLO protection. The UVLO circuit holds the soft-start low until the input voltage has exceeded the user programmable undervoltage threshold.

The TPS40055 uses the feed-forward pin, KFF, as a user programmable low-line UVLO detection. This variable low-line TPS40055 uses variable (user programmable) UVLO protection. The UVLO circuit holds the soft-start low until the input voltage has exceeded the user programmable undervoltage threshold. UVLO threshold compares the PWM ramp duration to the oscillator clock period. An undervoltage condition exists if the TPS40055 receives a clock pulse before the ramp has reached 90% of its full amplitude. The ramp duration is a function of the ramp slope, which is directly related to the current into the KFF pin. The KFF current is a function of the input voltage and the resistance from KFF to the input voltage. The KFF resistor can be referenced to the oscillator frequency as described in Equation 3:

$$R_{KFF} = \left(V_{IN\,(min)} - 3.5\right) \times \left(58.14 \times R_T + 1340\right)\ \Omega \quad (3)$$

where:

V_{IN} is the desired start-up (UVLO) input voltage

R_T is the timing resistance in kΩ

The variable UVLO function uses a 3-bit full adder to prevent spurious shut-downs or turn-ons due to spikes or fast line transients. When the adder reaches a total of seven counts in which the ramp duration is shorter than the clock cycle a power-good signal is asserted and a soft-start initiated and the upper and lower MOSFETS are turned off.

Once the soft-start is initiated, the UVLO circuit must see a total count of seven cycles in which the ramp duration is longer than the clock cycle before an undervoltage condition is declared. (See Figure 5).

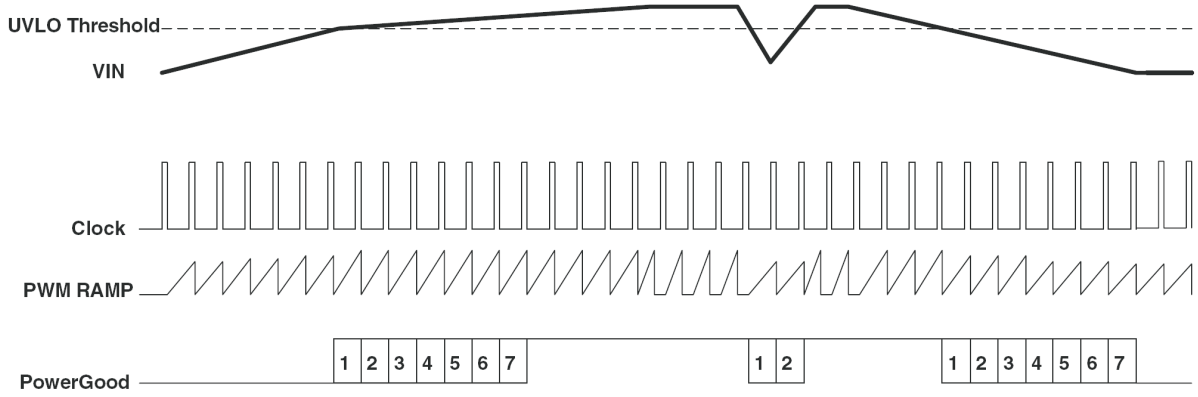


Figure 5. Undervoltage Lockout Operation

The tolerance on the UVLO set point also affects the maximum duty cycle achievable. If the UVLO starts the device at 10% below the nominal start up voltage, the maximum duty cycle is reduced approximately 10% at the nominal start up voltage.

The impedance of the input voltage can cause the input voltage, at the controller, to sag when the converter starts to operate and draw current from the input source. Therefore, there is voltage hysteresis that prevents nuisance shutdowns at the UVLO point. With R_T chosen to select the operating frequency and R_{KFF} chosen to select the start-up voltage, the approximate amount of hysteresis voltage is shown in Figure 7.

Figure 6. UNDERVOLTAGE LOCKOUT THRESHOLD vs HYSTERESIS

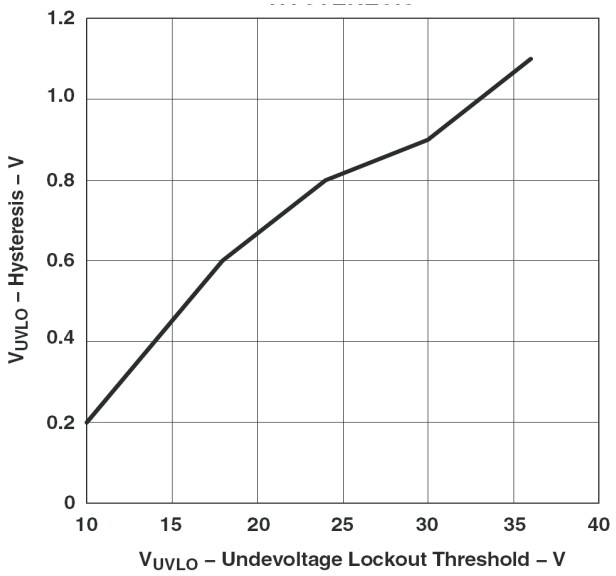


Figure 7.

BP5 AND BP10 INTERNAL VOLTAGE REGULATORS

Start-up characteristics of the BP5 and BP10 regulators over different temperature ranges are shown in Figure 8 and Figure 9. Slight variations in the BP5 occurs dependent upon the switching frequency. Variation in the BP10 regulation characteristics is also based on the load presented by switching the external MOSFETs.

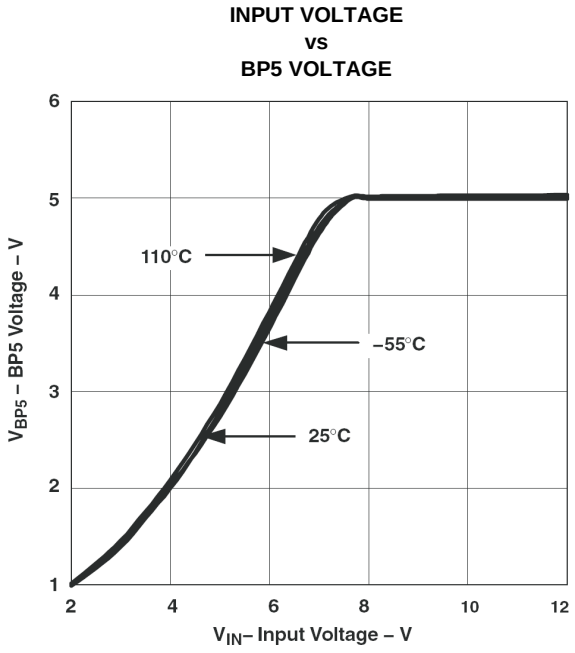


Figure 8.

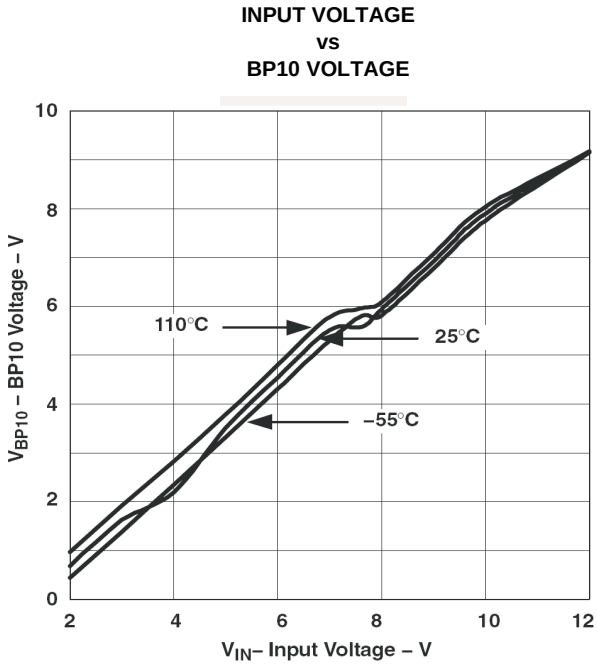


Figure 9.

SELECTING THE INDUCTOR VALUE

The inductor value determines the magnitude of ripple current in the output capacitors as well as the load current at which the converter enters discontinuous mode. Too large an inductance results in lower ripple current but is physically larger for the same load current. Too small an inductance results in larger ripple currents and a greater number of (or more expensive output capacitors for) the same output ripple voltage requirement. A good compromise is to select the inductance value such that the converter does not enter discontinuous mode until the load approximated somewhere between 10% and 30% of the rated output. The inductance value is described in Equation 4.

$$L = \frac{(V_{IN} - V_O) \times V_O}{V_{IN} \times \Delta I \times f_{SW}} \quad \text{(Henries)} \tag{4}$$

where:

V_O is the output voltage

ΔI is the peak-to-peak inductor current

CALCULATING THE OUTPUT CAPACITANCE

The output capacitance depends on the output ripple voltage requirement, output ripple current, as well as any output voltage deviation requirement during a load transient.

The output ripple voltage is a function of both the output capacitance and capacitor ESR. The worst case output ripple is described in Equation 5.

$$\Delta V = \Delta I \left[ESR + \left(\frac{1}{8 \times C_O \times f_{SW}} \right) \right] V_{P-P} \tag{5}$$

The output ripple voltage is typically between 90% and 95% due to the ESR component.

The output capacitance requirement typically increases in the presence of a load transient requirement. During a step load, the output capacitance must provide energy to the load (light-to-heavy load step) or absorb excess inductor energy (heavy-to-light load step) while maintaining the output voltage within acceptable limits. The amount of capacitance depends on the magnitude of the load step, the speed of the loop and the size of the inductor.

Stepping the load from a heavy load to a light load results in an output overshoot. Excess energy stored in the inductor must be absorbed by the output capacitance. The energy stored in the inductor is described in Equation 6.

$$E_L = \frac{1}{2} \times L \times I^2 \quad \text{(Joules)} \tag{6}$$

where:

$$I^2 = \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right] \quad \left((\text{Amperes})^2 \right) \tag{7}$$

I_{OH} is the output current under heavy load conditions

I_{OL} is the output current under light load conditions

Some applications may require an additional circuit to prevent false restarts at the UVLO voltage level. This applies to applications which have high impedance on the input voltage line or which have excessive ringing on the V_{IN} line. The input voltage impedance can cause the input voltage to sag enough at start-up to cause a UVLO shutdown and subsequent restart. Excessive ringing can also affect the voltage seen by the device and cause a UVLO shutdown and restart. A simple external circuit provides a selectable amount of hysteresis to prevent the nuisance UVLO shutdown.

Assuming a hysteresis current of 10% I_{KFF} and the peak detector charges to 8 V and $V_{IN(min)}$ = 10 V, the value of R_A is calculated by Equation 8 using a R_{KFF} = 71.5 kΩ.

$$R_A = \frac{R_{KFF} \times (8 - 3.5)}{0.1 \times \left(V_{IN(min)} - 3.5\right)} = 495\ \text{k}\Omega \cong 499\ \text{k}\Omega \tag{8}$$

C_A is chosen to maintain the peak voltage between switching cycles. To keep the capacitor charge from drooping 0.1 V, or from 8 V to 7.9 V.

$$C_A = \frac{(8 - 3.5)}{\left(R_A \times 7.9 \times f_{SW}\right)} \tag{9}$$

The value of C_A may calculate to less than 10 pF, but some standard value up to 47 pF works adequately. The diode can be a small signal switching diode or Schottky rated for more then 20 V. Figure 10 illustrates a typical implementation using a small switching diode.

The tolerance on the UVLO set point also affects the maximum duty cycle achievable. If the UVLO starts the device at 10% below the nominal start up voltage, the maximum duty cycle is reduced approximately 10% at the nominal start up voltage.

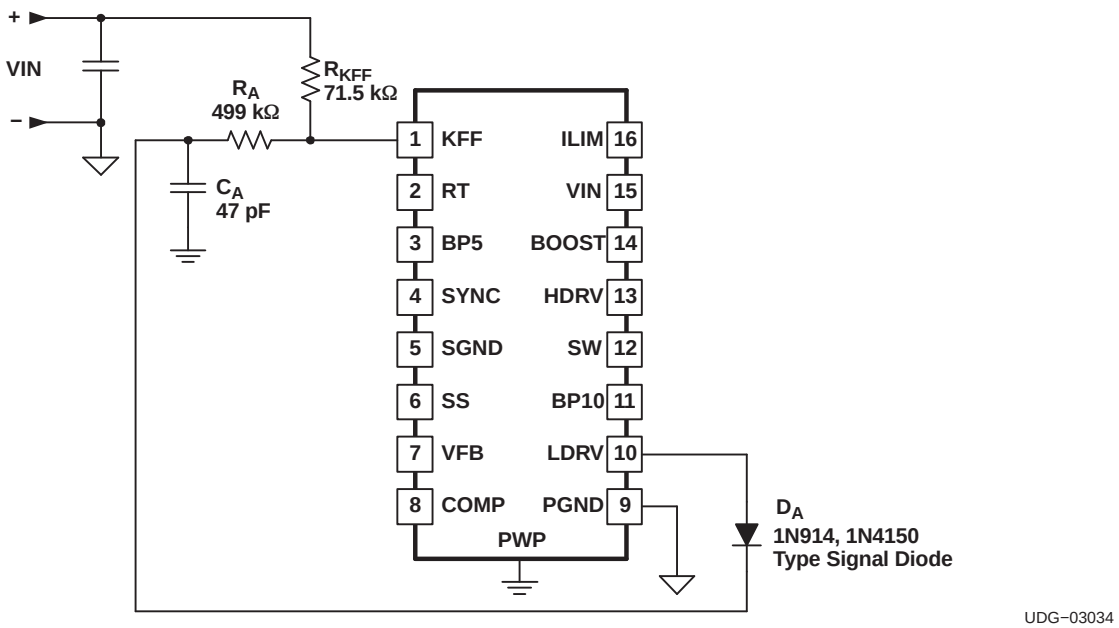


Figure 10. Hysteresis for Programmable UVLO

Energy in the capacitor is described in Equation 10.

$$E_C = \frac{1}{2} \times C \times V^2 \quad \text{(Joules)} \tag{10}$$

where:

$$V^2 = \left[\left(V_f\right)^2 - \left(V_i\right)^2 \right] \quad \left(\text{Volts}^2\right) \tag{11}$$

where:

V_f is the final peak capacitor voltage

V_I is the initial capacitor voltage

Substituting Equation 7 into Equation 6, then substituting Equation 11 into Equation 10, then setting Equation 10 equal to Equation 6, and then solving for C_O yields the capacitance described in Equation 12.

$$C_O = \frac{L \times \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right]}{\left[\left(V_f\right)^2 - \left(V_i\right)^2 \right]} \quad \text{(Farads)} \tag{12}$$

PROGRAMMING SOFT START

TPS40055 uses a closed-loop approach to ensure a controlled ramp on the output during start-up. Soft-start is programmed by charging an external capacitor (C_{SS}) via an internally generated current source. The voltage on C_{SS} minus 0.85 V is fed into a separate non-inverting input to the error amplifier (in addition to FB and 0.7-V VREF). The loop is closed on the lower of the (C_{SS} – 0.85 V) voltage or the internal reference voltage (0.7-V VREF). Once the (C_{SS} – 0.85 V) voltage rises above the internal reference voltage, regulation is based on the internal reference. To ensure a controlled ramp-up of the output voltage the soft-start time should be greater than the L-C_O time constant as described in Equation 13.

$$t_{START} \geq 2\pi \times \sqrt{L \times C_O} \quad \text{(seconds)} \tag{13}$$

There is a direct correlation between t_{START} and the input current required during start-up. The faster t_{START}, the higher the input current required during start-up. This relationship is describe in more detail in the section titled, *Programming the Current Limit* which follows. The soft-start capacitance, C_{SS}, is described in Equation 14.

$$C_{SS} = \frac{2.3\ \mu A}{0.7\ V} \times t_{START} \quad \text{(Farads)} \tag{14}$$

For applications in which the V_{IN} supply ramps up slowly, (typically between 50 ms and 100 ms) it may be necessary to increase the soft-start time to between approximately 2 ms and 5 ms to prevent nuisance UVLO tripping. The soft-start time should be longer than the time that the V_{IN} supply transitions between 6 V and 7 V.

PROGRAMMING CURRENT LIMIT

The TPS40055 uses a two-tier approach for overcurrent protection. The first tier is a pulse-by-pulse protection scheme. Current limit is implemented on the high-side MOSFET by sensing the voltage drop across the MOSFET when the gate is driven high. The MOSFET voltage is compared to the voltage dropped across a resistor connected from VIN pin to the ILIM pin when driven by a constant current sink. If the voltage drop across the MOSFET exceeds the voltage drop across the ILIM resistor, the switching pulse is immediately terminated. The MOSFET remains off until the next switching cycle is initiated.

The second tier consists of a fault counter. The fault counter is incremented on an overcurrent pulse and decremented on a clock cycle without an overcurrent pulse. When the counter reaches seven, a restart is issued and seven soft-start cycles are initiated. Both the upper and lower MOSFETs are turned off during this period. The counter is decremented on each soft-start cycle. When the counter is decremented to zero, the PWM is re-enabled. If the fault has been removed the output starts up normally. If the output is still present, the counter counts seven overcurrent pulses and re-enters the second-tier fault mode. See Figure 11 for typical overcurrent protection waveforms.

The minimum current limit setpoint (I_{LIM}) depends on t_{START}, C_O, V_O, and the load current at turn-on (I_L).

$$I_{LIM} = \left[\frac{(C_O \times V_O)}{t_{START}}\right] + I_L \quad \text{(Amperes)} \tag{15}$$

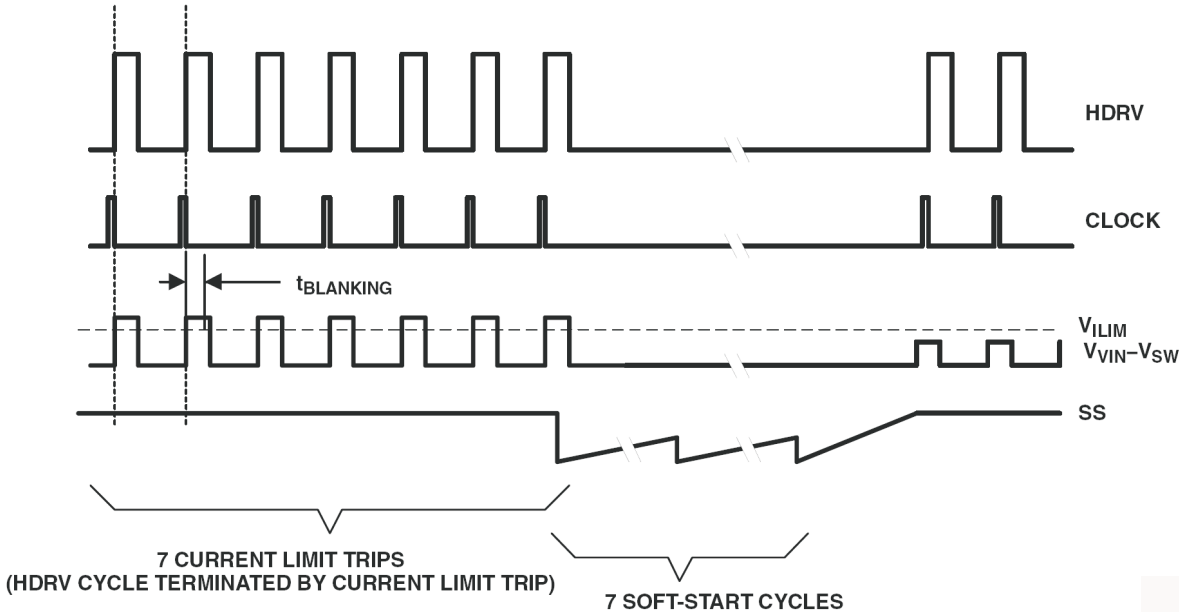


Figure 11. Typical Current Limit Protection Waveforms

The current limit programming resistor (R_{ILIM}) is calculated using Equation 16. Care must be taken in choosing the values used for V_{OS} and I_{SINK} in the equation. In order to assure the output current at the overcurrent level, the minimum value of I_{SINK} and the maximum value of V_{OS} must be used.

$$R_{ILIM} = \frac{I_{OC} \times R_{DS(on)[max]} + V_{OS}}{1.12 \times I_{SINK}} + \frac{42.86 \times 10^{-3}}{I_{SINK}} (\Omega) \quad (16)$$

where:

I_{SINK} is the current into the ILIM pin and is 7.5 µA, minimum

I_{OC} is the overcurrent setpoint which is the dc output current plus one-half of the peak inductor current

V_{OS} is the overcurrent comparator offset and is –20 mV, maximum

SYNCHRONIZING TO AN EXTERNAL SUPPLY

The TPS40055 can be synchronized to an external clock through the SYNC pin. Synchronization occurs on the falling edge of the SYNC signal. The synchronization frequency should be in the range of 20% to 30% higher than its programmed free-run frequency. The clock frequency at the SYNC pin replaces the master clock generated by the oscillator circuit. Pulling the SYNC pin low programs the TPS40055 to freely run at the frequency programmed by R_T.

The higher synchronization must be factored in when programming the PWM ramp generator circuit. If the PWM ramp is interrupted by the SYNC pulse, a UVLO condition is declared and the PWM becomes disabled. Typically this is of concern under low-line conditions only. In any case, R_{KFF} needs to be adjusted for the higher switching frequency. In order to specify the correct value for R_{KFF} at the synchronizing frequency, calculate a *dummy* value for RT that would cause the oscillator to run at the synchronizing frequency. Do not use this value of RT in the design.

$$R_{T(dummy)} = \left(\frac{1}{f_{SYNC} \times 17.82 \times 10^{-6}} - 17 \right) k\Omega \quad (17)$$

Use the value of $R_{T(dummy)}$ to calculate the value for R_{KFF}.

$$R_{KFF} = \left(V_{IN(min)} - 3.5\ V \right) \times \left(58.14 \times R_{T(dummy)} + 1340 \right) \Omega \quad (18)$$

This value of R_{KFF} ensures that UVLO is not engaged when operating at the synchronization frequency.

$R_{T(dummy)}$ is in kΩ

Loop Compensation

Voltage-mode buck-type converters are typically compensated using Type III networks. Since the TPS40055 uses voltage feedforward control, the gain of the PWM modulator with voltage feedforward circuit must be included. The modulator gain is described in Figure 11, with V_{IN} being the minimum input voltage required to cause the ramp excursion to cover the entire switching period as described in Equation 19.

$$A_{MOD} = \frac{V_{IN}}{V_S} \quad \text{or} \quad A_{MOD(dB)} = 20 \times \log \left(\frac{V_{IN}}{V_S} \right) \quad (19)$$

Duty cycle (D) varies from 0 to 1 as the control voltage (V_C) varies from the minimum ramp voltage to the maximum ramp voltage (V_S). Also, for a synchronous buck converter, $D = V_O / V_{IN}$. To get the control voltage to output voltage modulator gain in terms of the input voltage and ramp voltage:

$$D = \frac{V_O}{V_{IN}} = \frac{V_C}{V_S} \quad \text{or} \quad \frac{V_O}{V_C} = \frac{V_{IN}}{V_S} \quad (20)$$

Calculate the Poles and Zeros

For a buck converter using voltage mode control, there is a double pole due to the output L-C_O. The double pole is located at the frequency calculated in Equation 21.

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_O}} \quad \text{(Hertz)} \tag{21}$$

There is also a zero created by the output capacitance (C_O) and its associated ESR. The ESR zero is located at the frequency calculated in Equation 22.

$$f_Z = \frac{1}{2\pi \times ESR \times C_O} \quad \text{(Hertz)} \tag{22}$$

Calculate the value of R_{BIAS} to set the output voltage (V_{OUT}).

$$R_{BIAS} = \frac{0.7 \times R1}{V_{OUT} - 0.7} \ \Omega \tag{23}$$

The maximum crossover frequency (0 dB loop gain) is calculated in Equation 24.

$$f_C = \frac{f_{SW}}{4} \quad \text{(Hertz)} \tag{24}$$

Typically, f_C is selected to be close to the midpoint between the L-C_O double pole and the ESR zero. At this frequency, the control to output gain has a -2 slope (–40 dB/decade), while the Type III topology has a +1 slope (20 dB/decade), resulting in an overall closed loop –1 slope (–20 dB/decade). Figure 13 shows the modulator gain, L-C filter, output capacitor ESR zero, and the resulting response to be compensated.

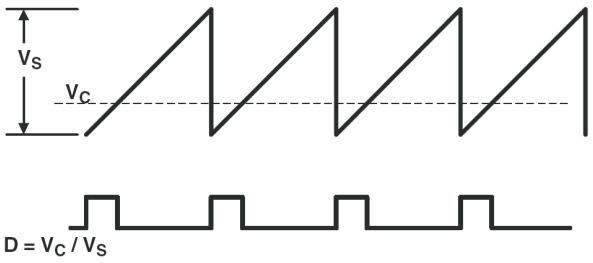


Figure 12. PWM Modulator Relationships

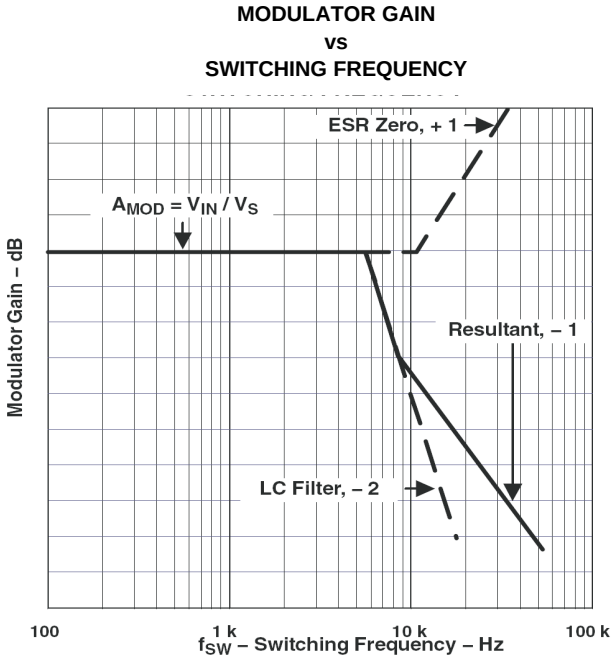


Figure 13.

A Type III topology, shown in Figure 14, has 2 zero-pole pairs in addition to a pole at the origin. The gain and phase boost of a Type III topology is shown in Figure 15. The two zeros are used to compensate the L-C_O double pole and provide phase boost. The double pole is used to compensate for the ESR zero and provide controlled gain roll-off. In many cases, the second pole can be eliminated and the amplifier's gain roll-off used to roll-off the overall gain at higher frequencies. Figure 14.

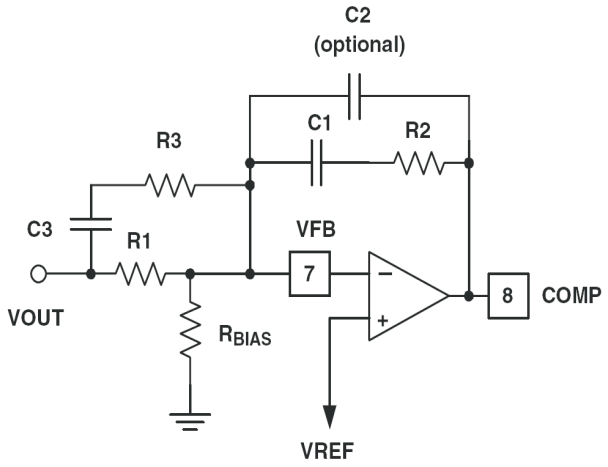


Figure 14. Type III Compensation Configuration

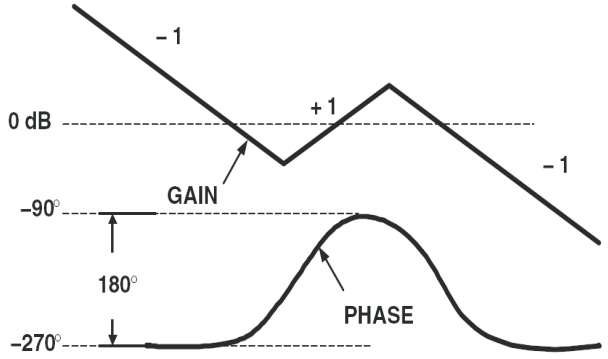


Figure 15. Type III Compensation Gain and Phase

The poles and zeros for a Type III network are described in Equation 25.

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \text{ (Hertz)} \qquad f_{Z2} = \frac{1}{2\pi \times R1 \times C3} \text{ (Hertz)}$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} \text{ (Hertz)} \qquad f_{P2} = \frac{1}{2\pi \times R3 \times C3} \text{ (Hertz)} \tag{25}$$

The value of R1 is somewhat arbitrary, but influences other component values. A value between 50 kΩ and 100 kΩ usually yields reasonable values.

The unity gain frequency is described in Equation 26.

$$f_C = \frac{1}{2\pi \times R1 \times C2 \times G} \text{ (Hertz)} \tag{26}$$

where G is the reciprocal of the modulator gain at f_C.

The modulator gain as a function of frequency at f_C, is described in Equation 27.

$$AMOD(f) = AMOD \times \left(\frac{f_{LC}}{f_C}\right)^2 \text{ and } G = \frac{1}{AMOD(f)} \tag{27}$$

Minimum Load Resistance

Care must be taken not to load down the output of the error amplifier with the feedback resistor, R2, that is too small. The error amplifier has a finite output source and sink current, which must be considered when sizing R2. Too small a value does not allow the output to swing over its full range.

$$R2_{(MIN)} = \frac{V_{C\,(max)}}{I_{SOURCE\,(min)}} = \frac{3.5\text{ V}}{2\text{ mA}} = 1750\ \Omega \tag{28}$$

CALCULATING THE BOOST AN BP10 BYPASS CAPACITOR

The BOOST capacitance provides a local, low impedance source for the high-side driver. The BOOST capacitor should be a good quality, high-frequency capacitor. The size of the bypass capacitor depends on the total gate charge of the MOSFET and the amount of droop allowed on the bypass capacitor. The BOOST capacitance is described in Equation 29.

$$C_{BOOST} = \frac{Q_g}{\Delta V} \text{ (Farads)} \tag{29}$$

The 10-V reference pin, BP10V provides energy for both the synchronous MOSFET and the high-side MOSFET via the BOOST capacitor. Neglecting any efficiency penalty, the BP10V capacitance is described in Equation 30.

$$C_{BP10} = \frac{\left(Q_{gHS} + Q_{gSR}\right)}{\Delta V} \quad \text{(Farads)} \tag{30}$$

dv/dt INDUCED TURN-ON

MOSFETs are susceptible to dv/dt turn-on particularly in high-voltage (V_{DS}) applications. The turn-on is caused by the capacitor divider that is formed by C_{GD} and C_{GS}. High dv/dt conditions and drain-to-source voltage, on the MOSFET causes current flow through C_{GD} and causes the gate-to-source voltage to rise. If the gate-to-source voltage rises above the MOSFET threshold voltage, the MOSFET turns on, resulting in large shoot-through currents. Therefore, the SR MOSFET should be chosen so that the C_{GD} capacitance is smaller than the C_{GS} capacitance.

HIGH SIDE MOSFET POWER DISSIPATION

The power dissipated in the external high-side MOSFET is comprised of conduction and switching losses. The conduction losses are a function of the I_{RMS} current through the MOSFET and the $R_{DS(on)}$ of the MOSFET. The high-side MOSFET conduction losses are defined by Equation 31.

$$P_{COND} = \left(I_{RMS}\right)^2 \times R_{DS(on)} \times \left(1 + TC_R \times \left[T_J - 25^{\circ}C\right]\right) \quad \text{(Watts)} \tag{31}$$

where:

TC_R is the temperature coefficient of the MOSFET $R_{DS(on)}$

The TC_R varies depending on MOSFET technology and manufacturer, but typically ranges between 3500 ppm/°C and 10000 ppm/°C.

The I_{RMS} current for the high side MOSFET is described in Equation 32.

$$I_{RMS} = I_{OUT} \times \sqrt{d} \quad \left(A_{RMS}\right) \tag{32}$$

The switching losses for the high-side MOSFET are described in Equation 33.

$$P_{SW(fsw)} = \left(V_{IN} \times I_{OUT} \times t_{SW}\right) \times f_{SW} \quad \text{(Watts)} \tag{33}$$

where:

I_O is the dc-output current

t_{SW} is the switching rise time, typically < 20 ns

f_{SW} is the switching frequency

Typical switching waveforms are shown in Figure 16.

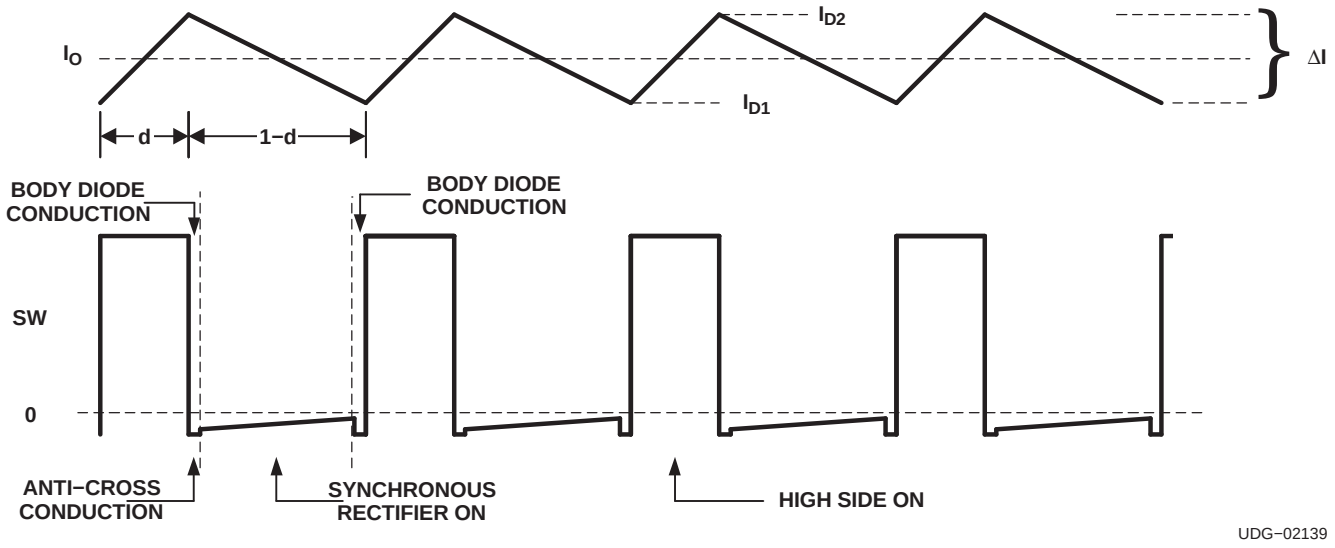


Figure 16. Inductor Current and SW Node Waveforms

The maximum allowable power dissipation in the MOSFET is determined by Equation 34.

$$P_T = \frac{(T_J - T_A)}{\theta_{JA}} \quad \text{(Watts)} \tag{34}$$

where:

$$P_T = P_{COND} + P_{SW(fsw)} \quad \text{(Watts)} \tag{35}$$

and θ_{JA} is the package thermal impedance.

SYNCHRONOUS RECTIFIER MOSFET POWER DISSIPATION

The power dissipated in the synchronous rectifier MOSFET is comprised of three components: $R_{DS(on)}$ conduction losses, body diode conduction losses, and reverse recovery losses. $R_{DS(on)}$ conduction losses can be found using Equation 31 and the RMS current through the synchronous rectifier MOSFET is described in Equation 36.

$$I_{RMS} = I_O \times \sqrt{1 - d} \quad (\text{Amperes}_{RMS}) \tag{36}$$

The body-diode conduction losses are due to forward conduction of the body diode during the anti-cross conduction delay time. The body diode conduction losses are described by Equation 37.

$$P_{DC} = 2 \times I_O \times V_F \times t_{DELAY} \times f_{SW} \quad \text{(Watts)} \tag{37}$$

where:

V_F is the body diode forward voltage

t_{DELAY} is the delay time just before the SW node rises

The 2-multiplier is used because the body diode conducts twice during each cycle (once on the rising edge and once on the falling edge). The reverse recovery losses are due to the time it takes for the body diode to recovery from a forward bias to a reverse blocking state. The reverse recovery losses are described in Equation 38.

$$P_{RR} = 0.5 \times Q_{RR} \times V_{IN} \times f_{SW} \quad \text{(Watts)} \tag{38}$$

where:

Q_{RR} is the reverse recovery charge of the body diode.

The Q_{RR} is not always described in a MOSFET's data sheet, but may be obtained from the MOSFET vendor. The total synchronous rectifier MOSFET power dissipation is described in Equation 39.

$$P_{SR} = P_{DC} + P_{RR} + P_{COND} \quad (\text{Watts}) \tag{39}$$

TPS40055 POWER DISSIPATION

The power dissipation in the TPS40055 is largely dependent on the MOSFET driver currents and the input voltage. The driver current is proportional to the total gate charge, Q_g, of the external MOSFETs. Driver power (neglecting external gate resistance)[2] can be calculated from Equation 40.

$$P_D = Q_g \times V_{DR} \times f_{SW} \quad (\text{Watts/driver}) \tag{40}$$

And the total power dissipation in the TPS40055, assuming the same MOSFET is selected for both the high-side and synchronous rectifier is described in Equation 41.

$$P_T = \left(\frac{2 \times P_D}{V_{DR}} + I_Q \right) \times V_{IN} \quad (\text{Watts}) \tag{41}$$

or

$$P_T = \left(2 \times Q_g \times f_{SW} + I_Q \right) \times V_{IN} \quad (\text{Watts}) \tag{42}$$

where:

I_Q is the quiescent operating current (neglecting drivers)

The maximum power capability of the device's PowerPad package is dependent on the layout as well as air flow. The thermal impedance from junction to air, assuming 2 oz. copper trace and thermal pad with solder and no air flow.

$$\theta_{JA} = 36.515^{\circ}\text{C/W} \tag{43}$$

The maximum allowable package power dissipation is related to ambient temperature by Equation 44.

$$P_T = \frac{T_J - T_A}{\theta_{JA}} \quad (\text{Watts}) \tag{44}$$

Substituting Equation 45 into Equation 41 and solving for f_{SW} yields the maximum operating frequency for the TPS40055. The result is described in Equation 45.

$$f_{SW} = \frac{\left(\left[\frac{(T_J - T_A)}{(\theta_{JA} \times V_{DD})} \right] - I_Q \right)}{(2 \times Q_g)} \quad (\text{Hz}) \tag{45}$$

LAYOUT CONSIDERATIONS

PowerPAD™ PACKAGE

The PowerPAD package provides low thermal impedance for heat removal from the device. The PowerPAD derives its name and low thermal impedance from the large bonding pad on the bottom of the device. For maximum thermal performance, the circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depends on the size of the PowerPAD package. For a 16-pin TSSOP (PWP) package, dimensions of the circuit board pad area are 5 mm x 3,4 mm [2]. The dimensions of the package pad are shown in Figure 17.

Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0,33 mm (13 mils) works well when 1-oz copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter of 0,1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. See the *PowerPAD Thermally Enhanced Package* and the mechanical illustration at the end of this document for more information on the PowerPAD package.

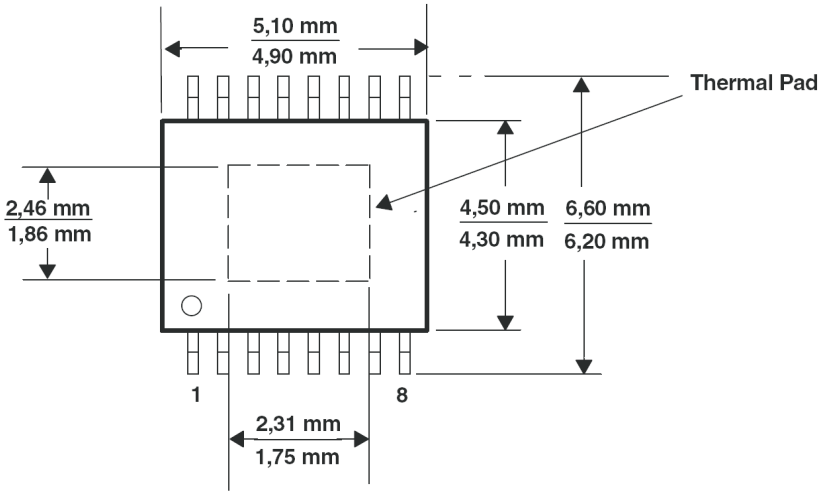


Figure 17. PowerPAD Dimensions

MOSFET PACKAGING

MOSFET package selection depends on MOSFET power dissipation and the projected operating conditions. In general, for a surface-mount applications, the DPAK style package provides the lowest thermal impedance (θ_{JA}) and, therefore, the highest power dissipation capability. However, the effectiveness of the DPAK depends on proper layout and thermal management. The θ_{JA} specified in the MOSFET data sheet refers to a given copper area and thickness. In most cases, a lowest thermal impedance of 40°C/W requires one square inch of 2-ounce copper on a G-10/FR-4 board. Lower thermal impedances can be achieved at the expense of board area. See the selected MOSFET's data sheet for more information regarding proper mounting.

GROUNDING AND CIRCUIT LAYOUT CONSIDERATIONS

The TPS40055 provides separate signal ground (SGND) and power ground (PGND) pins. It is important that circuit grounds are properly separated. Each ground should consist of a plane to minimize its impedance if possible. The high power noisy circuits such as the output, synchronous rectifier, MOSFET driver decoupling capacitor (BP10), and the input capacitor should be connected to PGND plane at the input capacitor.

Sensitive nodes such as the FB resistor divider, R_T, and ILIM should be connected to the SGND plane. The SGND plane should only make a single point connection to the PGND plane.

Component placement should ensure that bypass capacitors (BP10 and BP5) are located as close as possible to their respective power and ground pins. Also, sensitive circuits such as FB, RT, and ILIM should not be located near high dv/dt nodes such as HDRV, LDRV, BOOST, and the switch node (SW).

DESIGN EXAMPLE

- Input Voltage: 10 Vdc to 24 Vdc
- Output voltage: 3.3 V +2% ($3.234 \le V_O \le 3.366$)
- Output current: 8 A (maximum, steady state), 10 A (surge, 10-ms duration, 10% duty cycle maximum)
- Output ripple: 33 mVP-P at 8 A
- Output load response: 0.3 V => 10% to 90% step load change, from 1 A to 7 A
- Operating temperature: -40°C to 85°C
- f_{SW} = 300 kHz

1. Calculate maximum and minimum duty cycles

$$d_{MIN} = \frac{V_{O(min)}}{V_{IN(max)}} = \frac{3.324}{24} = 0.135 \qquad d_{MAX} = \frac{V_{O(max)}}{V_{IN(min)}} = \frac{3.366}{10} = 0.337 \tag{46}$$

2. Select switching frequency

The switching frequency is based on the minimum duty cycle ratio and the propagation delay of the current limit comparator. In order to maintain current limit capability, the on time of the upper MOSFET (t_{ON}) must be greater than 300 ns (see the Electrical Characteristics table). Therefore,

$$\frac{V_{O(min)}}{V_{IN(max)}} = \frac{t_{ON}}{T_{SW}} \quad \text{or} \tag{47}$$

$$\frac{1}{T_{SW}} = f_{SW} = \left[\frac{\left(\frac{V_{O(min)}}{V_{IN(max)}}\right)}{T_{ON}}\right] \tag{48}$$

Using 400 ns to provide margin,

$$f_{SW} = \frac{0.135}{400\ ns} = 337\ kHz \tag{49}$$

Since the oscillator can vary by 10%, decrease f_{SW} by 10%

$$f_{SW} = 0.9 \times 337\ kHz = 303\ kHz \tag{50}$$

and therefore choose a frequency of 300 kHz.

3. Select ΔI

In this case ΔI is chosen so that the converter enters discontinuous mode at 20% of nominal load.

$$\Delta I = I_O \times 2 \times 0.2 = 8 \times 2 \times 0.2 = 3.2\ A \tag{51}$$

4. Calculate the power losses

Power losses in the high-side MOSFET (Si7860DP) at 24-V_{IN} where switching losses dominate can be calculated from Equation 52.

$$I_{RMS} = I_O \times \sqrt{d} = 8 \times \sqrt{0.135} = 2.93\ A \tag{52}$$

substituting Equation 34 into Equation 33 yields

$$P_{COND} = 2.93^2 \times 0.008 \times (1 + 0.007 \times (150 - 25)) = 0.129\ W \tag{53}$$

and from Equation 33, the switching losses can be determined.

$$P_{SW(fsw)} = \left(V_{IN} \times I_O \times t_{SW}\right) \times f_{SW} = 24\ V \times 8\ A \times 20\ ns \times 300\ kHz = 1.152\ W \quad (54)$$

The MOSFET junction temperature can be found by substituting Equation 35 into Equation 34

$$T_J = \left(P_{COND} + P_{SW}\right) \times \theta_{JA} + T_A = (0.129 + 1.152) \times 40 + 85 = 136^{\circ}C \quad (55)$$

5. Calculate synchronous rectifier losses

The synchronous rectifier MOSFET has two loss components: conduction and diode reverse recovery losses. The conduction losses are due to IRMS losses, as well as body diode conduction losses during the dead time associated with the anti-cross conduction delay.

The IRMS current through the synchronous rectifier from Equation 38

$$I_{RMS} = I_O \times \sqrt{1 - d} = 8 \times \sqrt{1 - 0.135} = 7.44\ A_{RMS} \quad (56)$$

The synchronous MOSFET conduction loss from Equation 33 is:

$$P_{COND} = {I_{RMS}}^2 \times R_{DS(on)} = 7.44^2 \times 0.008 \times (1 + 0.007(150 - 25)) = 0.83\ W \quad (57)$$

The body diode conduction loss from Equation 39 is:

$$P_{DC} = 2 \times I_O \times V_{FD} \times t_{DELAY} \times f_{SW} = 2 \times 8.0\ A \times 0.8\ V \times 100\ ns \times 300\ kHz = 0.384\ W \quad (58)$$

The body diode reverse recovery loss from Equation 40 is:

$$P_{RR} = 0.5 \times Q_{RR} \times V_{IN} \times f_{SW} = 0.5 \times 30\ nC \times 24\ V \times 300\ kHz = 0.108\ W \quad (59)$$

The total power dissipated in the synchronous rectifier MOSFET from Equation 41 is:

$$P_{SR} = P_{RR} + P_{COND} + P_{DC} = 0.108 + 0.83 + 0.384 = 1.322\ W \quad (60)$$

The junction temperature of the synchronous rectifier at 85°C is:

$$T_J = P_{SR} \times \theta_{JA} + T_A = (1.322) \times 40 + 85 = 139^{\circ}C \quad (61)$$

In typical applications, paralleling the synchronous rectifier MOSFET with a Schottky rectifier increases the overall converter efficiency by approximately 2% due to the lower power dissipation during the body diode conduction and reverse recovery periods.

6. Calculate the inductor value

The inductor value is calculated from Equation 62.

$$L = \frac{(24 - 3.3\ V) \times 3.3\ V}{24\ V \times 3.2\ A \times 300\ kHz} = 2.96\ \mu H \quad (62)$$

A 2.9-µH Coev DXM1306-2R9 or 2.6-µH Panasonic ETQ-P6F2R9LFA can be used.

7. Setting the switching frequency

The clock frequency is set with a resistor (R_T) from the RT pin to ground. The value of R_T can be found from Equation 63, with f_{SW} in kHz.

$$R_T = \left(\frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 17\right) k\Omega = 170\ k\Omega \quad \therefore \text{ use } 169\ k\Omega \quad (63)$$

8. Programming the ramp generator circuit

The PWM ramp is programmed through a resistor (R_{KFF}) from the KFF pin to V_{IN}. The ramp generator also controls the input UVLO voltage. For an undervoltage level of 10 V, R_{KFF} can be calculated from Equation 64.

$$R_{KFF} = \left(V_{IN(min)} - 3.5\right)\left(58.14 \times R_T + 1340\right)\ \Omega\ = 72.5\ k\Omega \quad \therefore \text{ use } 71.5\ k\Omega \tag{64}$$

9. Calculating the output capacitance (C_O)

In this example the output capacitance is determined by the load response requirement of ΔV = 0.3 V for a 1-A to 8-A step load. C_O can be calculated using Equation 65.

$$C_O = \frac{2.9\ \mu \times \left((8\ A)^2 - (1\ A)^2\right)}{\left((3.3)^2 - (3.0)^2\right)} = 97\ \mu F \tag{65}$$

Using Equation 66, we can calculate the ESR required to meet the output ripple requirements.

$$33\ mV = 3.2\ A\left(ESR + \frac{1}{8 \times 97\ \mu F \times 300\ kHz}\right) \tag{66}$$

$$ESR = 10.3\ m\Omega - 3.33\ m\Omega = 6.97\ m\Omega \tag{67}$$

For this design example, two Panasonic SP EEFUEOJ1B1R capacitors, (6.3 V, 180 µF, 12 mΩ) are used.

10. Calculate the soft-start capacitor (C_{SS})

This design requires a soft-start time (t_{START}) of 1 ms. C_{SS} can be calculated on Equation 68

$$C_{SS} = \frac{2.3\ \mu A}{0.7\ V} \times 1\ ms = 3.29\ nF = 3300\ pF \tag{68}$$

11. Calculate the current limit resistor (R_{ILIM})

The current limit set point depends on t_{START}, V_O, C_O, and I_{LOAD} at start-up as shown in Equation 69. For this design,

$$I_{LIM} > \frac{360\ \mu F \times 3.3\ V}{1\ ms} + 8.0\ A = 9.2\ A \tag{69}$$

For this design, set I_{LIM} for 11 A_{DC} minimum. From Equation 70, with I_{OC} equal to the dc-output surge current plus one-half the ripple current of 3.2 A and $R_{DS(on)}$ is increased 30% (1.3 × 0.008) to allow for MOSFET heating.

$$R_{ILIM} = \frac{12.6\ A \times 0.0104\Omega}{8.6\ \mu A} + \frac{(-0.02)}{8.6\ \mu A} = 15.2\ k\Omega - 2.3\ k\Omega = 12.9\ k\Omega \cong 13\ k\Omega \tag{70}$$

12. Calculate loop compensation values

Calculate the dc modulator gain (A_{MOD}) from Equation 71

$$A_{MOD} = \frac{10}{2} = 5.0 \qquad A_{MOD(dB)} = 20 \times \log(5) = 14\ dB \tag{71}$$

Calculate the output filter L-C_O poles and C_O ESR zeros from Equation 72 and Equation 73

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C_O}} = \frac{1}{2\pi\sqrt{2.9\ \mu H \times 360\ \mu F}} = 4.93\ kHz \tag{72}$$

and

$$f_Z = \frac{1}{2\pi \times ESR \times C_O} = \frac{1}{2\pi \times 0.006 \times 360\ \mu F} = 73.7\ kHz \quad (73)$$

Select the close-loop 0 dB crossover frequency (f_C). For this example, f_C = 20 kHz.

Select the double zero location for the Type III compensation network at the output filter double pole at 4.93 kHz.

Select the double pole location for the Type III compensation network at the output capacitor ESR zero at 73.7 kHz.

The amplifier gain at the crossover frequency of 20 kHz is determined by the reciprocal of the modulator gain AMOD at the crossover frequency from Equation 74.

$$A_{MOD(f)} = A_{MOD} \times \left(\frac{f_{LC}}{f_C}\right)^2 = 5 \times \left(\frac{4.93\ kHz}{20\ kHz}\right)^2 = 0.304 \quad (74)$$

And also from Equation 75.

$$G = \frac{1}{A_{MOD(f)}} = \frac{1}{0.304} = 3.29 \quad (75)$$

Choose R1 = 100 kΩ

The poles and zeros for a type III network are described in Equation 25 and Equation 26.

$$f_{Z2} = \frac{1}{2\pi \times R1 \times C3} \therefore C3 = \frac{1}{2\pi \times 100\ k\Omega \times 4.93\ kHz} = 323\ pF,\ \text{choose } 330\ pF \quad (76)$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C3} \therefore R3 = \frac{1}{2\pi \times 330\ pF \times 73.3\ kHz} = 6.55\ k\Omega,\ \text{choose } 6.49\ k\Omega \quad (77)$$

$$f_C = \frac{1}{2\pi \times R1 \times C2 \times G} \therefore C2 = \frac{1}{2\pi \times 100\ k\Omega \times 3.29 \times 20\ kHz} = 24.2\ pF,\ \text{choose } 22\ pF \quad (78)$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} \therefore R2 = \frac{1}{2\pi \times 22\ pF \times 73.3\ kHz} = 98.2\ k\Omega,\ \text{choose } 97.6\ k\Omega \quad (79)$$

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \therefore C1 = \frac{1}{2\pi \times 97.6\ k\Omega \times 4.93\ kHz} = 331\ pF,\ \text{choose } 330\ pF \quad (80)$$

Calculate the value of R_{BIAS} from Equation 81 with R1 = 100 kΩ.

$$R_{BIAS} = \frac{0.7\ V \times R1}{V_O - 0.7\ V} = \frac{0.7\ V \times 100k\Omega}{3.3\ V - 0.7\ V} = 26.9\ k\Omega,\ \text{choose } 26.7\ k\Omega \quad (81)$$

CALCULATING THE BOOST AND BP10V BYPASS CAPACITANCE

The size of the bypass capacitor depends on the total gate charge of the MOSFET being used and the amount of droop allowed on the bypass cap. The BOOST capacitance for the Si7860DP, allowing for a 0.5-V droop on the BOOST pin from Equation 29 is:

$$C_{BOOST} = \frac{Q_g}{\Delta V} = \frac{18\ nC}{0.5\ V} = 36\ nF \quad (82)$$

and the BP10V capacitance from Equation 32 is

$$C_{BP(10\ V)} = \frac{Q_{gHS} + Q_{gSR}}{\Delta V} = \frac{2 \times Q_g}{\Delta V} = \frac{36\ nC}{0.5\ V} = 72\ nF \quad (83)$$

For this application, a 0.1-µF capacitor is used for the BOOST bypass capacitor and a 1-µF capacitor is used for the BP10V bypass.

DESIGN EXAMPLE SUMMARY

Figure 18 shows component selection for the 10-V to 24-V to 3.3-V at 8 A dc-to-dc converter specified in the design example. For an 8-V input application, it may be necessary to add a Schottky diode from BP10 to BOOST to get sufficient gate drive for the upper MOSFET. As seen in Figure 9, the BP10 output is about 6 V with the input at 8 V, so the upper MOSFET gate drive may be less than 5 V.

A Schottky diode is shown connected across the synchronous rectifier MOSFET as an optional device that may be required if the layout causes excessive negative SW node voltage, greater than or equal to 2 V.

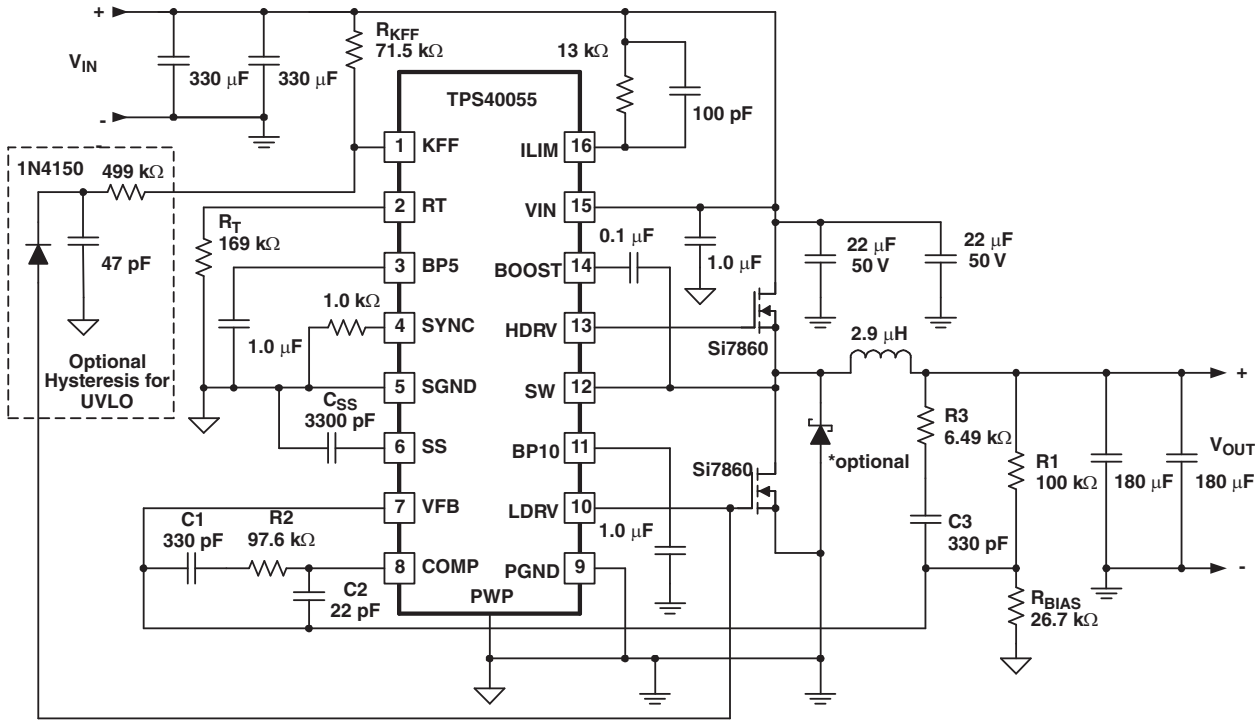


Figure 18. 24 V to 3.3 V at 8-A DC-to-DC Converter Design Example

REFERENCES

1. Balogh, Laszlo, *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, Texas Instruments/Unitrode Corporation, Power Supply Design Seminar, SEM-1400 Topic 2.
2. *PowerPAD Thermally Enhanced Package* Texas Instruments, Semiconductor Group, Technical Brief (SLMA002)

REVISION HISTORY

Changes from Revision C (February 2012) to Revision D	Page
• Changed I_{SINK} current minimum from 8.5 µA to 7.5 µA for equation 16	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS40055MPWPREP	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	40055M	Samples
TPS40055MPWPREPG4	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	40055M	Samples
V62/05617-01XE	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	40055M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF TPS40055-EP :

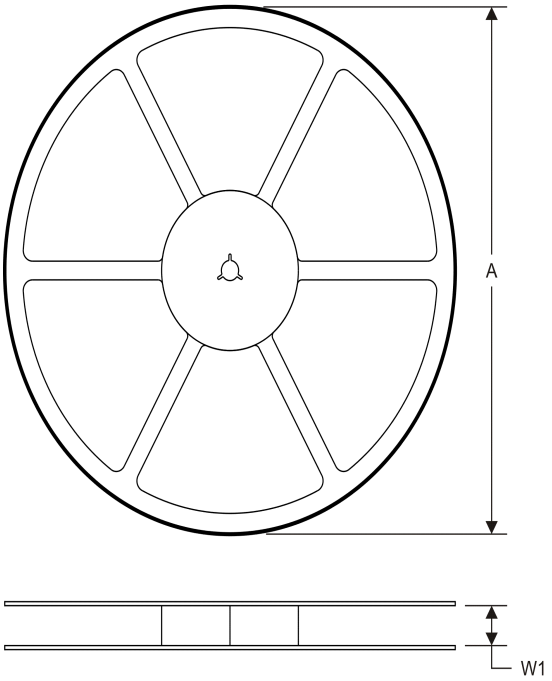
- Catalog: TPS40055

NOTE: Qualified Version Definitions:

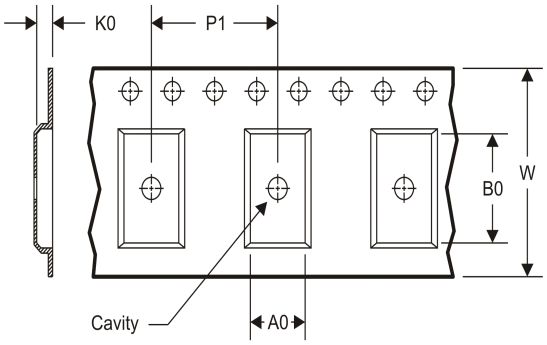
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



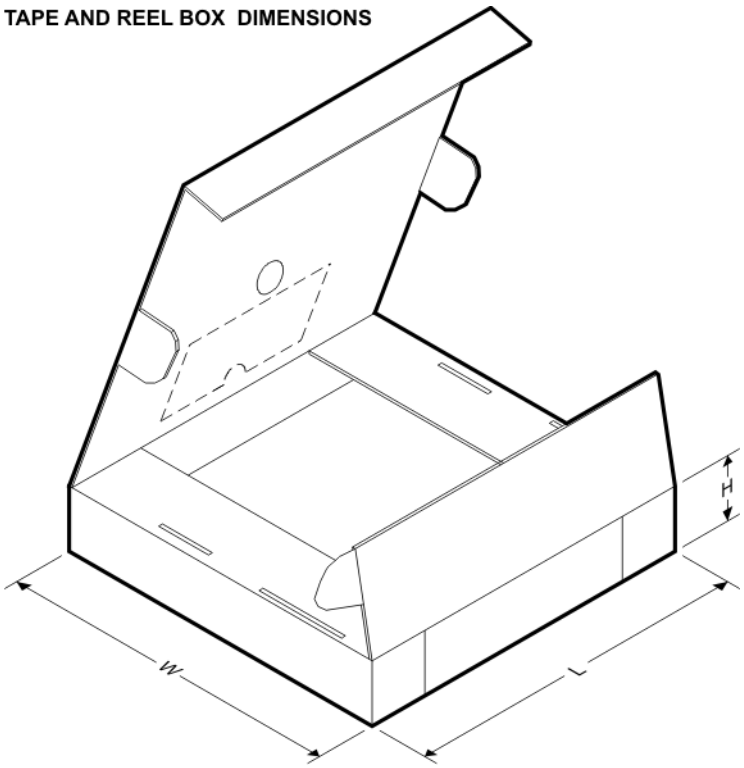
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40055MPWPREP	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

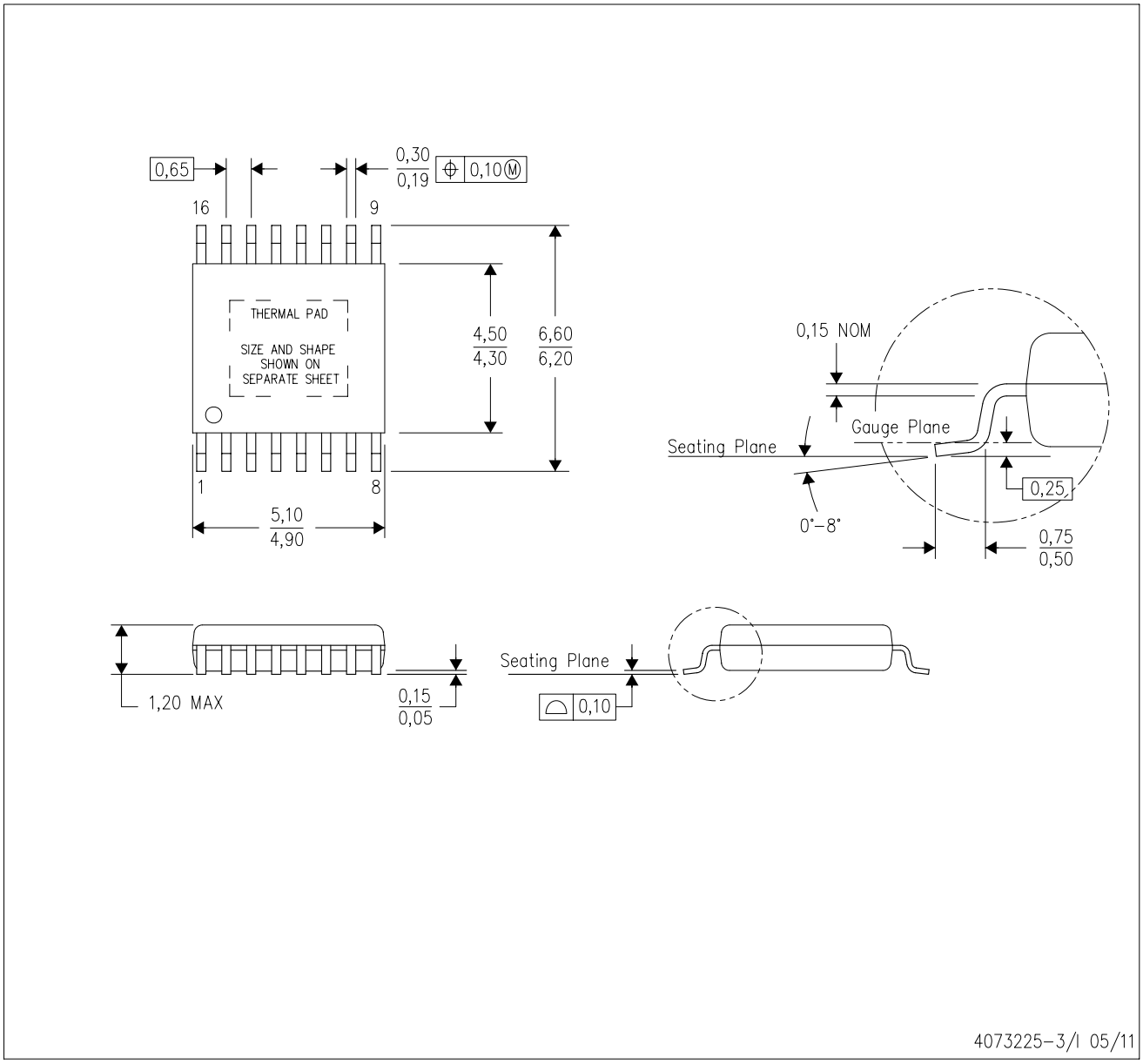
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40055MPWPREP	HTSSOP	PWP	16	2000	367.0	367.0	35.0

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

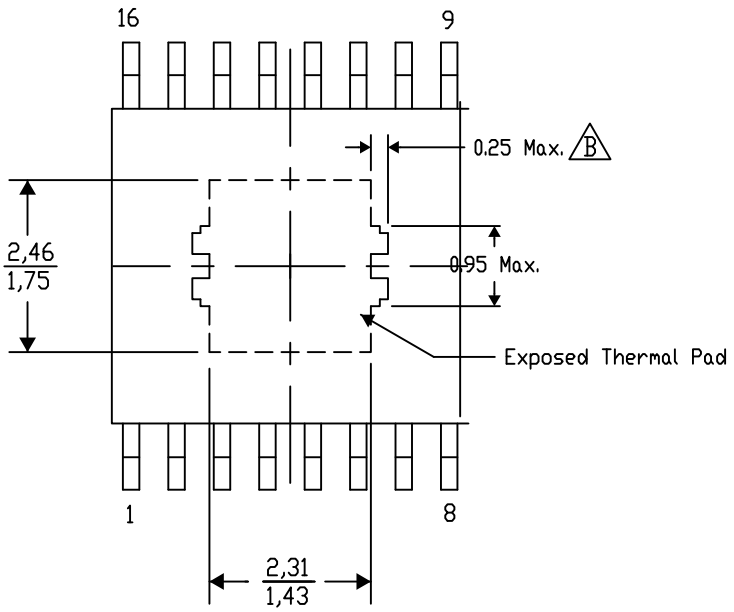
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–6/AG 08/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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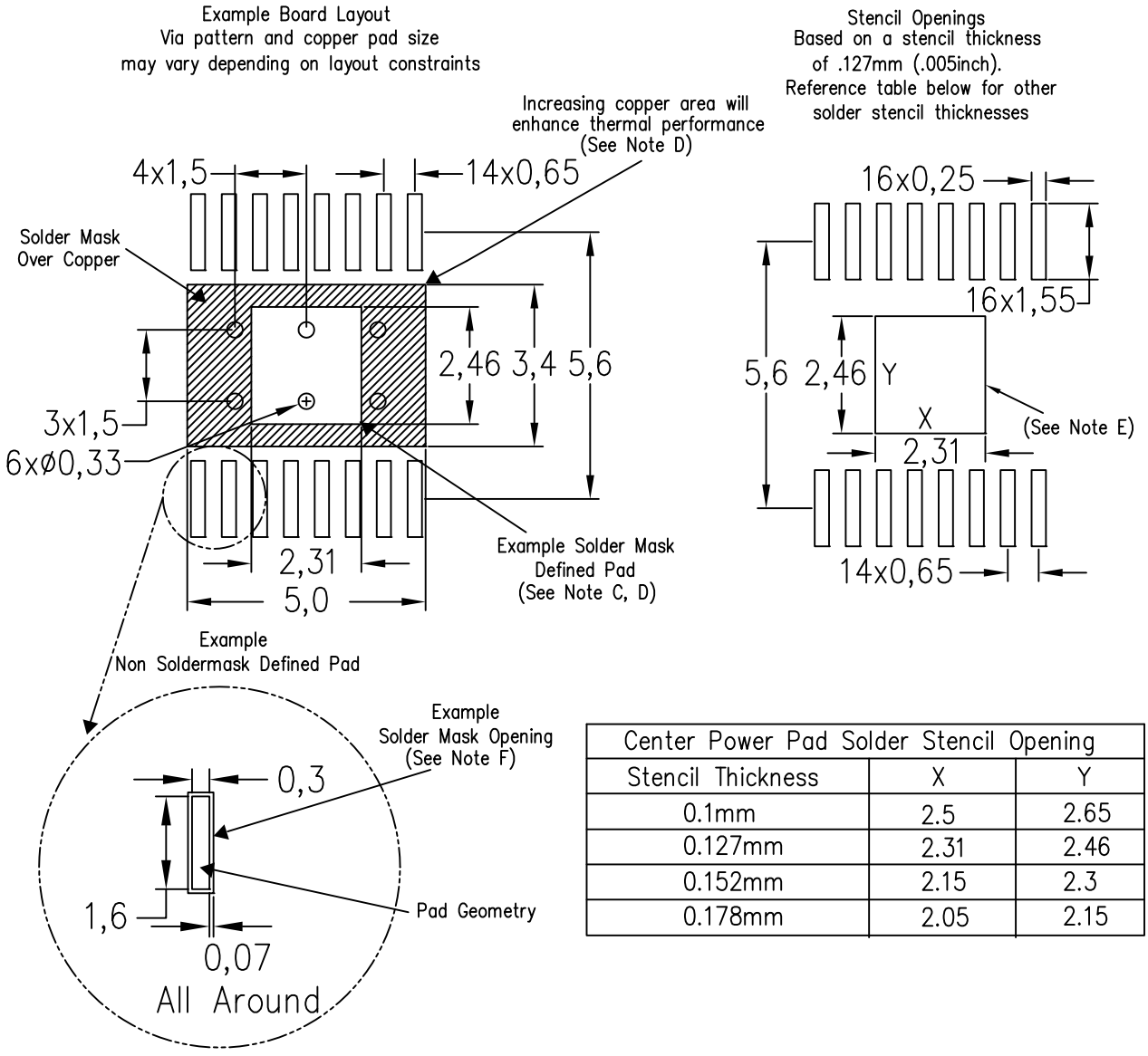
PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–3/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

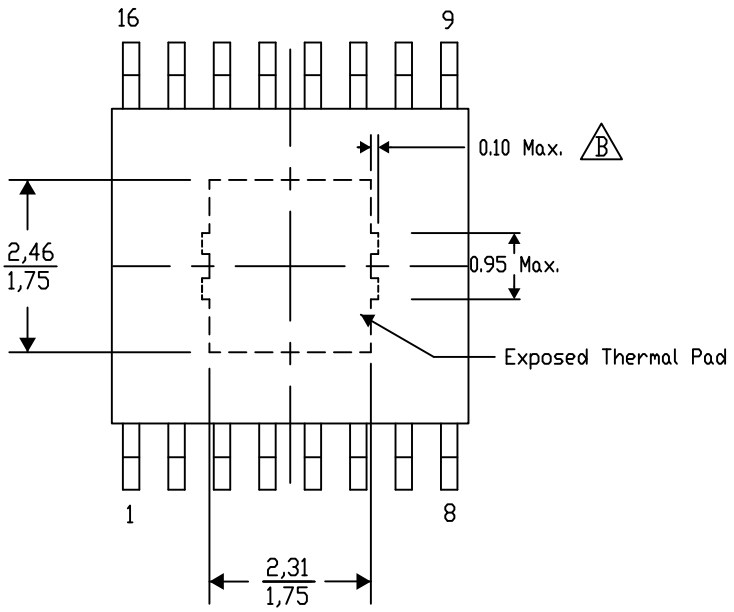
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–45/AG 08/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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