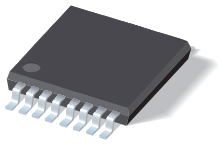

SLVS612 – APRIL 2006

WIDE-INPUT SYNCHRONOUS, TRACKING BUCK CONTROLLER

FEATURES

- Operating Input Voltage 10 V to 40 V
- Output Voltage Tracks External Reference
- Programmable Fixed-Frequency Up to 100 kHz to 1 MHz Voltage Mode Controller
- Internal Gate Drive Outputs for High-Side and Synchronous N-Channel MOSFETs
- Externally Synchronizable
- Programmable Short-Circuit Protection
- Thermal Shutdown
- 16-Pin PowerPAD™ Package (θ_{JC} = 2°C/W)
- Programmable Closed-Loop Soft-Start

APPLICATIONS

- DDR Tracking Regulators
- Power Modules
- Networking Equipment
- Industrial Servers

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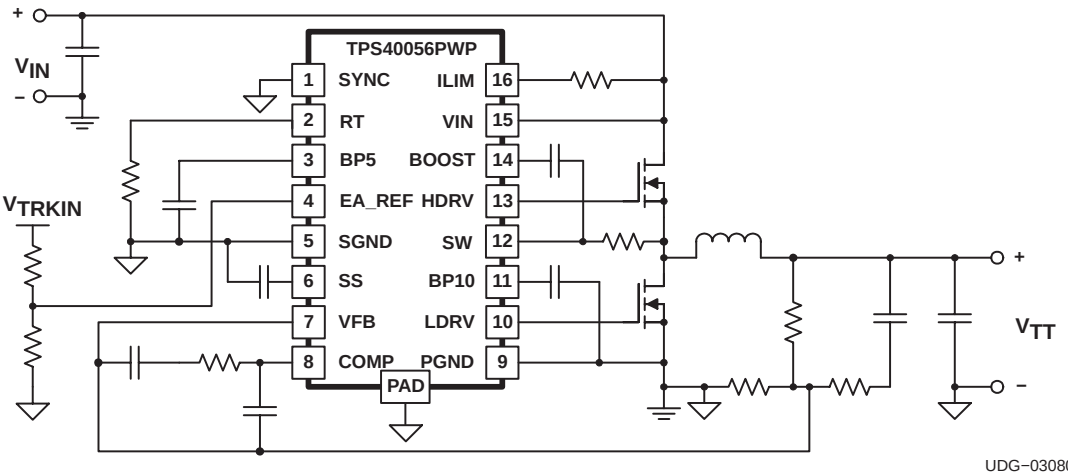
DESCRIPTION

The TPS40056 is part of a family of high-voltage, wide input, synchronous, step-down converters. The TPS40056 offers design flexibility with a variety of user programmable functions, including soft-start, operating frequency, high-side current limit, and loop compensation. The TPS40056 is also synchronizable to an external supply. It incorporates MOSFET gate drivers for external N-channel high-side and synchronous rectifier (SR) MOSFETs. Gate drive logic incorporates anti-cross conduction circuitry to prevent simultaneous high-side and synchronous rectifier conduction. The externally programmable short circuit protection provides pulse-by-pulse current limit, as well as hiccup mode operation utilizing an internal fault counter for longer duration overloads.

SIMPLIFIED APPLICATION DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	PART NUMBER
−40°C to 85°C	Plastic HTSSOP(PWP)(1)	TPS40056PWP

(1) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS40056PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(2)

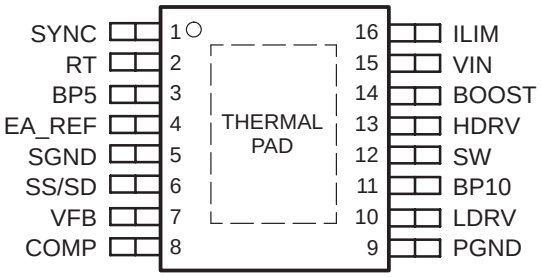
		TPS40056	UNIT
Input voltage range, V_{IN}	VIN	45	V
	VFB, SS, SYNC, EA_REF	−0.3 to 6	
	SW	−0.3 to 45	
	SW, transient < 50 ns	−2.5	
Output voltage range, V_O	COMP, RT, SS	−0.3 to 6	
Output current, I_{OUT}	RT	200	µA
Operating junction temperature range, T_J		−40 to 125	°C
Storage temperature, T_{stg}		−55 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	

(2) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V_I	10		40	V
Operating free-air temperature, T_A	−40		85	°C

PWP PACKAGE(3)(4)
(TOP VIEW)



(3) For more information on the PWP package, refer to TI Technical Brief, Literature No. SLMA002.
(4) PowerPAD™ heat slug must be connected to SGND (pin 5) or electrically isolated from all other pins.

ELECTRICAL CHARACTERISTICS

T_A = −40°C to 85°C, V_{IN} = 12 V_{dc}, R_T = 90.9 kΩ, f_{SW} = 500 kHz, V_{EA_REF} = 1.25 V, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range, VIN		10		40	V
OPERATING CURRENT						
I_{DD}	Quiescent current	Output drivers not switching, V_{FB} = 1.3 V		1.5	3.0	mA
BP5						
V_{BP5}	Ouput voltage	I_{LOAD} = 1 mA	4.5	5.0	5.5	V
OSCILLATOR/RAMP GENERATOR						
f_{OSC}	Accuracy	9 V ≤ V_{IN} ≤ 40 V	520	580	640	kHz
V_{RAMP}	PWM ramp voltage(1)	V_{PEAK}−V_{VAL}		2.0		V
V_{IH}	High-level input voltage, SYNC		2		5	
V_{IL}	Low-level input voltage, SYNC				0.8	V
I_{SYNC}	Input current, SYNC			5	10	µA
	Pulse width, SYNC		50			ns
V_{RT}	RT voltage		2.38	2.50	2.58	V
	Maximum duty cycle	V_{FB} = 0 V, f_{SW} ≤ 600 kHz	90%			
		V_{FB} = 0 V, 600 kHz ≤ f_{SW} ≤ 1 MHz	85%			
	Minumum duty cycle	V_{FB} ≥ EA_REF + 0.05 V			0%	
SOFT START						
I_{SS}	Soft-start source current		1.65	2.35	3.05	µA
V_{SS}	Soft-start clamp voltage			3.7		V
t_{DSCH}	Discharge time	C_{SS} = 220 pF	1.6	2.2	2.8	µs
t_{SS}	Soft-start time	C_{SS} = 220 pF, 0 V ≤ V_{SS} ≤ 1.6 V	100	155	205	
BP10						
V_{BP10}	Ouput voltage		9.0	9.6	10.3	V
ERROR AMPLIFIER						
V_{EA_REF}	Error amplifier reference input voltage(1)(2)	10 V ≤ V_{IN} ≤ 40 V	0.2		2.5	V
	Input offset voltage	0.5 V ≤ V_{FB} ≤ 2.25 V	−6		6	mV
	Input offset voltage	0.2 V ≤ V_{FB} ≤ 0.5 V	−10	0	10	MV
G_{BW}	Gain bandwidth	0.2 V ≤ V_{FB} ≤ 0.5 V	1.5	3.5		MHz
G_{BW}	Gain bandwidth	0.5 V ≤ V_{FB} ≤ 2.25 V	2.5	5.0		MHz
A_{VOL}	Open loop gain		60	80		dB
I_{OH}	High-level output source current		1.5	4.0		mA
I_{OL}	Low-level output sink current		2.0	4.0		
V_{OH}	High-level output voltage	I_{SOURCE} = 500 µA	3.2	3.5		V
V_{OL}	Low-level output voltage	I_{SINK} = 500 µA		0.20	0.35	
I_{BIAS}	Input bias current	V_{FB} = 1.2 V		100	200	nA

(1) Ensured by design. Not production tested.
(2) Common mode range extends to ground, but not tested below 200 mV.

ELECTRICAL CHARACTERISTICS

T_A = −40°C to 85°C, V_{IN} = 12 V_{dc}, R_T = 90.9 kΩ, f_{SW} = 500 kHz, V_{EA_REF} = 1.25 V all parameters at zero power dissipation (unless otherwise noted)

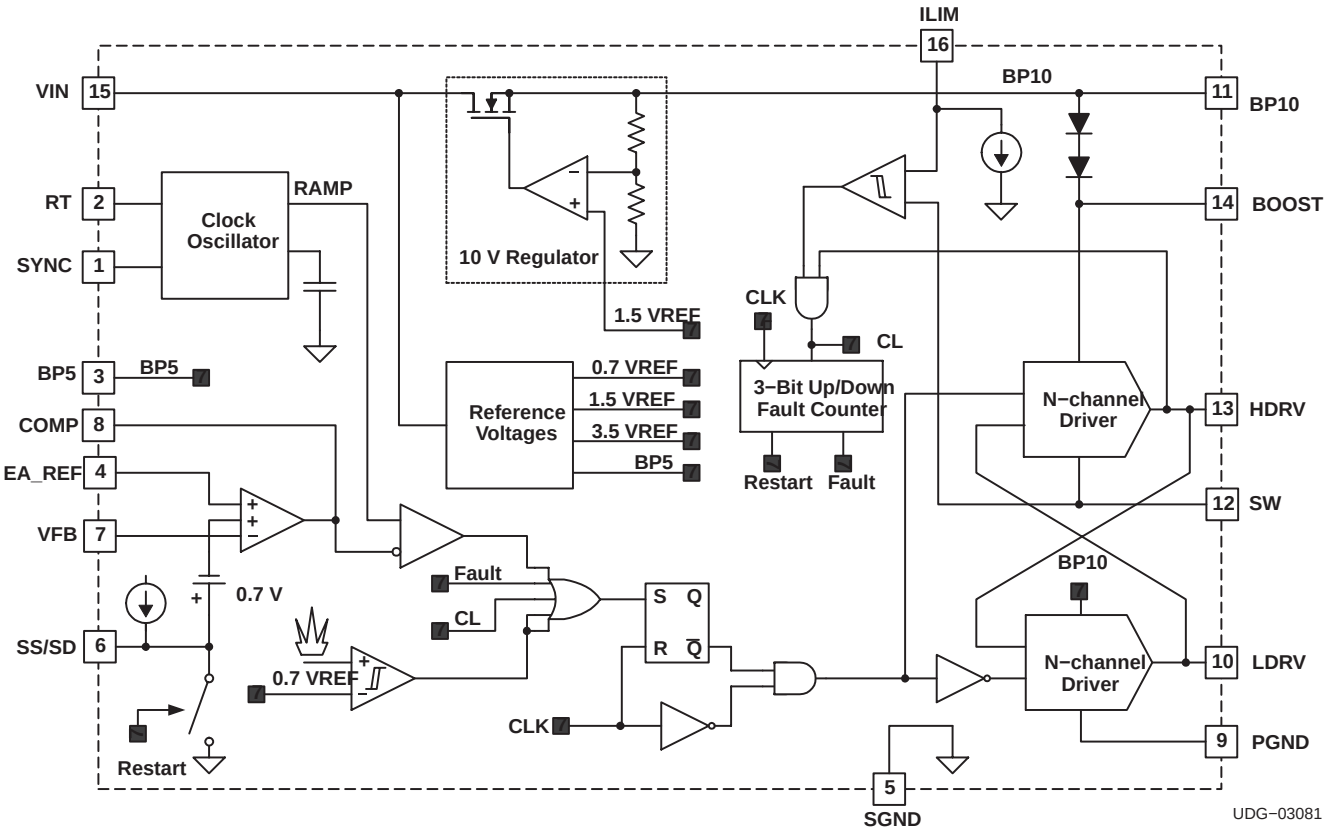
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{SINK}	Current limit sink current		8	10	12	µA
	Propagation delay to output	V_{ILIM} = 11.7 V, V_{SW} = (V_{ILIM} − 0.5 V)		300		ns
		V_{ILIM} = 11.7 V, V_{SW} = (V_{ILIM} − 2 V)		250		
t_{ON}	Switch leading-edge blanking pulse time(1)		100			
t_{OFF}	Off time during a fault			7		cycles
V_{OS}	Offset voltage SW vs. ILIM	V_{ILIM} = 11.6 V, T_A = 25°C	−100	−70	−40	mV
		V_{ILIM} = 11.6 V, 0°C ≤ T_A ≤ 85°C	−125		−30	
		V_{ILIM} = 11.6 V, −40°C ≤ T_A ≤ 85°C	−125		−15	
OUTPUT DRIVER						
t_{LRISE}	Low-side driver rise time	C_{LOAD} = 2200 pF		48	96	ns
t_{LFALL}	Low-side driver fall time			24	48	
t_{HRISE}	High-side driver rise time	C_{LOAD} = 2200 pF, (HDRV − SW)		48	96	
t_{HFALL}	High-side driver fall time			36	72	
V_{OH}	High-level ouput voltage, HDRV	I_{HDRV} = −0.1 A (HDRV − SW)	BOOST −1.5 V	BOOST −1.0 V		V
V_{OL}	Low-level ouput voltage, HDRV	I_{HDRV} = 0.1 A (HDRV − SW)			0.75	
V_{OH}	High-level ouput voltage, LDRV	I_{LDRV} = −0.1 A	BP10 −1.4 V	BP10 − 1.0 V		
V_{OL}	Low-level ouput voltage, LDRV	I_{LDRV} = 0.1 A			0.5	
	Minimum controllable pulse width(1)			100	150	ns
SS/SD SHUTDOWN						
V_{SD}	Shutdown threshold voltage	Outputs off	90	125	165	mV
V_{EN}	Device active threshold voltage		165	210	260	
BOOST REGULATOR						
V_{BOOST}	Output voltage	V_{IN} = 12.0 V	19	20	21	V
SW NODE						
I_{LEAK}	Leakage current(1)				25	µA
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature(1)			165		°C
	Hysteresis(1)			20		
UVLO						
	Input voltage UVLO threshold		8.20	8.75	9.25	V
	Input voltage UVLO hysteresis			1.0		

(1) Ensured by design. Not production tested.

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BOOST	14	O	Gate drive voltage for the high side N-channel MOSFET. The BOOST voltage is 9 V greater than the input voltage. A 0.1-µF ceramic capacitor should be connected from this pin to the SW pin.
BP5	3	O	5-V reference. This pin should be bypassed to ground with a 0.1-µF ceramic capacitor. This pin may be used with an external dc load of 1 mA or less.
BP10	11	O	10-V reference used for gate drive of the N-channel synchronous rectifier. This pin should be bypassed by a 1-µF ceramic capacitor. This pin may be used with an external dc load of 1 mA or less.
COMP	8	O	Output of the error amplifier, input to the PWM comparator. A feedback network is connected from this pin to the VFB pin to compensate the overall loop. The comp pin is internally clamped above the peak of the ramp to improve large signal transient response.
HDRV	13	O	Floating gate drive for the high-side N-channel MOSFET. This pin switches from BOOST (MOSFET on) to SW (MOSFET off).
ILIM	16	I	Current limit pin, used to set the overcurrent threshold. An internal current sink from this pin to ground sets a voltage drop across an external resistor connected from this pin to VCC. The voltage on this pin is compared to the voltage drop (VIN −SW) across the high side MOSFET during conduction.
EA_REF	4	I	Non-inverting input to the error amplifier and used as the reference for the feedback loop.
LDRV	10	O	Gate drive for the N-channel synchronous rectifier. This pin switches from BP10 (MOSFET on) to ground (MOSFET off).
PGND	9	−	Power ground reference for the device. There should be a low-impedance path from this pin to the source(s) of the lower MOSFET(s).
RT	2	I	A resistor is connected from this pin to ground to set the internal oscillator and switching frequency.
SGND	5	−	Signal ground reference for the device.
SS/SD	6	I	Soft-start programming pin. A capacitor connected from this pin to ground programs the soft-start time. The capacitor is charged with an internal current source of 2.3 µA. The resulting voltage ramp on the SS pin is used as a second non-inverting input to the error amplifier. Output voltage regulation is controlled by the SS voltage ramp until the voltage on the SS pin reaches the internal reference voltage , EA_REF V. Pulling this pin low disables the controller.
SW	12	I	This pin is connected to the switched node of the converter and used for overcurrent sensing.
SYNC	1	I	Syncronization input for the device. This pin can be used to synchronize the oscillator to an external master frequency. If synchronization is not used, connect this pin to SGND.
VFB	7	I	Inverting input to the error amplifier. In normal operation the voltage on this pin is equal to the EA_REF reference voltage.
VIN	15	I	Supply voltage for the device.

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The TPS40056 allows the user to optimize the PWM controller to the specific application.

The TPS40056 is the controller of choice for synchronous buck designs, the output of which is required to track another voltage. It has two quadrant operation and can source or sink output current, providing the best transient response.

SW NODE RESISTOR AND DIODE

The SW node of the converter will be negative during the *dead time* when both the upper and lower MOSFETs are off. The magnitude of this negative voltage is dependent on the lower MOSFET body diode and the output current which flows during this dead time. This negative voltage could affect the operation of the controller, especially at low input voltages.

Therefore, a resistor (3.3 Ω to 4.7 Ω) and Schottky diode must be placed between the lower MOSFET drain and pin 12, SW, of the controller as shown in Figure 10. The Schottky diode must have a voltage rating to accommodate the input voltage and ringing on the SW node of the converter. A 30-V Schottky such as a BAT54 or a 40-V Schottky such as a Zetex ZHCS400 or Vishay SD103AWS are adequate. These components are shown in Figure 10 as R_{SW} and D2.

SETTING THE SWITCHING FREQUENCY (PROGRAMMING THE CLOCK OSCILLATOR)

The TPS40056 has independent clock oscillator and ramp generator circuits. The clock oscillator serves as the master clock to the ramp generator circuit. The switching frequency, f_{SW} in kHz, of the clock oscillator is set by a single resistor (R_T) to ground. The clock frequency is related to R_T, in kΩ by Equation (1).

$$R_T = \left(\frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 23 \right) k\Omega \quad (1)$$

UVLO OPERATION

The TPS40056 uses fixed UVLO protection. The fixed UVLO monitors the input voltage. The UVLO circuit holds the soft-start low until the input voltage has exceeded the undervoltage threshold.

TRACKING CONFIGURATION (V_{OUT} TRACKING V_{IN})

Setting the output, V_{OUT} to track another voltage, V_{TRKIN}, is simply a matter of selecting the proper voltage divider(s) R4,R5,R1 and R6 as shown in Figure 1. The voltage on the EA_REF input should be in the range of 0.2 V to 2.5 V. If the output voltage is less than 2.5 V, resistor R6 can be omitted. For example in the DDR case, if the voltage V_{TRKIN} ramps up to 2.5 V and it is desired to have V_{OUT} to track it and come up to 1.25 V, set R4=R5 and omit R6. In general, the output voltage, V_{OUT}, in terms of VTRKIN and the two voltage dividers is shown in Equation (2).

$$V_{OUT} = V_{TRKIN} \times \left(\frac{R5}{R4 + R5} \right) \times \left(\frac{R6 + R1}{R6} \right) V \quad (2)$$

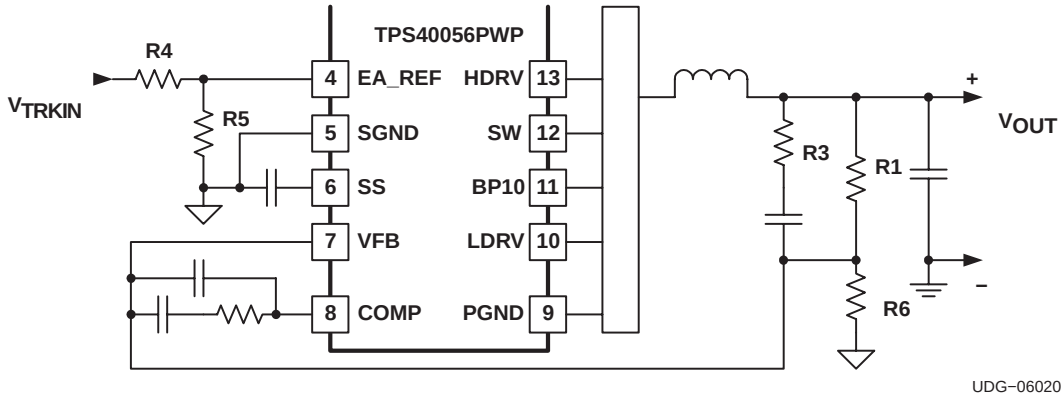


Figure 1. Tracking Configuration, V_{OUT} Tracks V_{TRKIN}

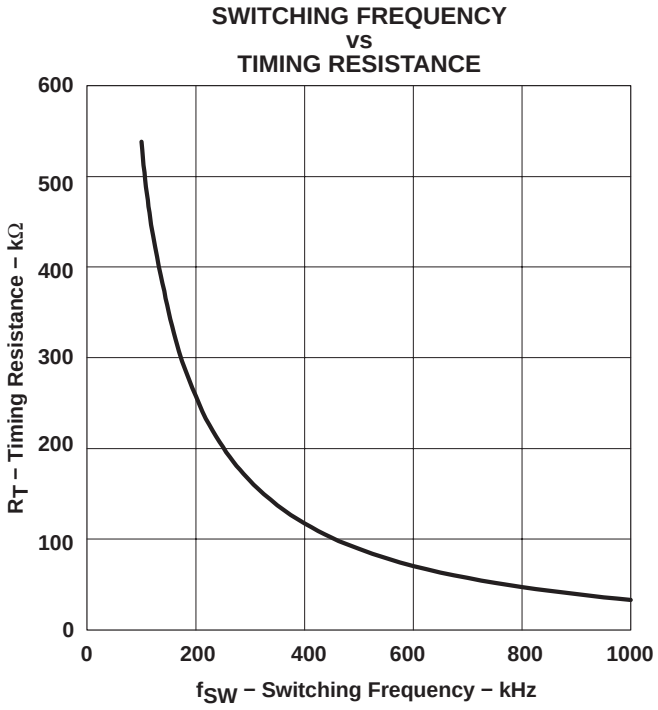


Figure 2

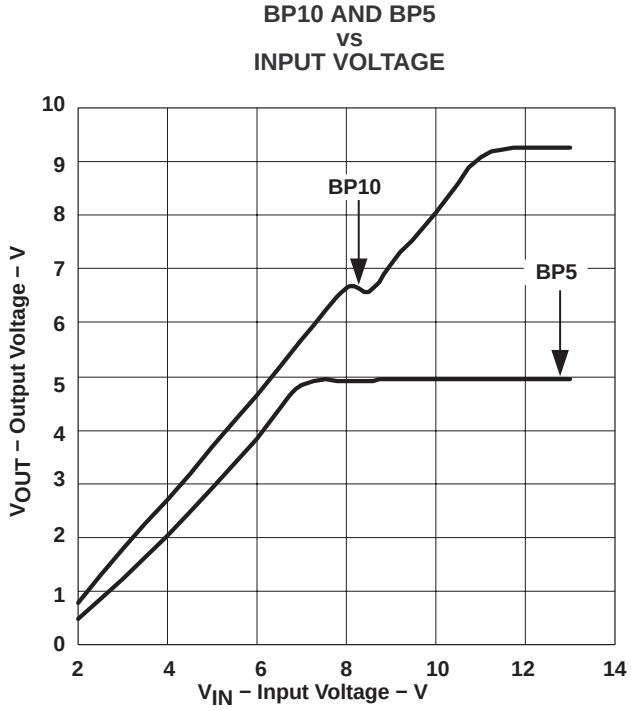


Figure 3

APPLICATION INFORMATION

BP5 AND BP10 INTERNAL VOLTAGE REGULATORS

Start-up characteristics of the BP5 and BP10 regulators are shown in Figure 2. Slight variations in the BP5 occurs dependent upon the switching frequency. Variation in the BP10 regulation characteristics is also based on the load presented by switching the external MOSFETs.

SELECTING THE INDUCTOR VALUE

The inductor value determines the magnitude of ripple current in the output capacitors as well as the load current at which the converter enters discontinuous mode. Too large an inductance results in lower ripple current but is physically larger for the same load current. Too small an inductance results in larger ripple currents and a greater number of (or more expensive output capacitors for) the same output ripple voltage requirement. A good compromise is to select the inductance value such that the converter doesn't enter discontinuous mode until the load approximated somewhere between 10% and 30% of the rated output. The inductance value is described in equation (3).

$$L = \frac{\left(V_{IN} - V_O\right) \times V_O}{V_{IN} \times \Delta I \times f_{SW}} \quad \text{(Henries)} \tag{3}$$

where:.

- V_O is the output voltage
- ΔI is the peak-to-peak inductor current

CALCULATING THE OUTPUT CAPACITANCE

The output capacitance depends on the output ripple voltage requirement, output ripple current, as well as any output voltage deviation requirement during a load transient.

The output ripple voltage is a function of both the output capacitance and capacitor ESR. The worst case output ripple is described in equation (4).

$$\Delta V = \Delta I \left[ESR + \left(\frac{1}{8 \times C_O \times f_{SW}} \right) \right] \quad V_{P-P} \tag{4}$$

The output ripple voltage is typically between 90% and 95% due to the ESR component.

The output capacitance requirement typically increases in the presence of a load transient requirement. During a step load, the output capacitance must provide energy to the load (light to heavy load step) or absorb excess inductor energy (heavy to light load step) while maintaining the output voltage within acceptable limits. The amount of capacitance depends on the magnitude of the load step, the speed of the loop and the size of the inductor.

APPLICATION INFORMATION

Stepping the load from a heavy load to a light load results in an output overshoot. Excess energy stored in the inductor must be absorbed by the output capacitance. The energy stored in the inductor is described in equation (5).

$$E_L = \frac{1}{2} \times L \times I^2 \quad \text{(Joules)} \tag{5}$$

where:

$$I^2 = \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right] \quad \left((\text{Amperes})^2 \right) \tag{6}$$

where:

- I_{OH} is the output current under heavy load conditions
- I_{OL} is the output current under light load conditions

Energy in the capacitor is described in equation (7).

$$E_C = \frac{1}{2} \times C \times V^2 \quad \text{(Joules)} \tag{7}$$

where:

$$V^2 = \left[\left(V_f\right)^2 - \left(V_i\right)^2 \right] \quad \left(\text{Volts}^2 \right) \tag{8}$$

where:

- V_f is the final peak capacitor voltage
- V_i is the initial capacitor voltage

Substituting equation (6) into equation (5), then substituting equation (8) into equation (7), then setting equation (7) equal to equation (5), and then solving for C_O yields the capacitance described in equation (9).

$$C_O = \frac{L \times \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right]}{\left[\left(V_f\right)^2 - \left(V_i\right)^2 \right]} \quad \text{(Farads)} \tag{9}$$

APPLICATION INFORMATION

PROGRAMMING SOFT START

TPS40056 uses a closed-loop approach to ensure a controlled ramp on the output during start-up. Soft-start is programmed by charging an external capacitor (C_{SS}) via an internally generated current source. The voltage on C_{SS} is fed into a separate non-inverting input to the error amplifier (in addition to FB and EA_REF). The loop is closed on the lower of the C_{SS} voltage or the the external reference voltage EA_REF. Once the C_{SS} voltage rises above the external reference voltage, regulation is based on the external reference. To ensure a controlled ramp-up of the output voltage the soft-start time should be greater than the L-C_O time constant as described in equation (10).

$$t_{START} \geq 2\pi \times \sqrt{L \times C_O} \quad \text{(seconds)} \tag{10}$$

There is a direct correlation between t_{START} and the input current required during start-up. The faster t_{START}, the higher the input current required during start-up. This relationship is describe in more detail in the section titled, *Programming the Current Limit* which follows. The soft-start capacitance, C_{SS}, is described in equation (11).

For applications in which the V_{IN} supply ramps up slowly, (typically between 50 ms and 100 ms) it may be necessary to increase the soft-start time to between approximately 2 ms and 5 ms to prevent nuisance UVLO tripping. The soft-start time should be longer than the time that the V_{IN} supply transitions between 8 V and 9 V.

$$C_{SS} = \frac{2.3\ \mu A}{0.7\ V} \times t_{START} \quad \text{(Farads)} \tag{11}$$

PROGRAMMING CURRENT LIMIT

The TPS40056 uses a two-tier approach for overcurrent protection. The first tier is a pulse-by-pulse protection scheme. Current limit is implemented on the high-side MOSFET by sensing the voltage drop across the MOSFET when the gate is driven high. The MOSFET voltage is compared to the voltage dropped across a resistor connected from VIN pin to the ILIM pin when driven by a constant current sink. If the voltage drop across the MOSFET exceeds the voltage drop across the ILIM resistor, the switching pulse is immediately terminated. The MOSFET remains off until the next switching cycle is initiated.

The second tier consists of a fault counter. The fault counter is incremented on an overcurrent pulse and decremented on a clock cycle without an overcurrent pulse. When the counter reaches seven (7) a restart is issued and seven soft-start cycles are initiated. Both the upper and lower MOSFETs are turned off during this period. The counter is decremented on each soft-start cycle. When the counter is decremented to zero, the PWM is re-enabled. If the fault has been removed the output starts up normally. If the output is still present the counter counts seven overcurrent pulses and re-enters the second-tier fault mode. See Figure 3 for typical overcurrent protection waveforms.

The minimum current limit setpoint (I_{LIM}) depends on t_{START}, C_O, V_O, and the load current at turn-on (I_L).

$$I_{LIM} = \left[\frac{\left(C_O \times V_O\right)}{t_{START}} \right] + I_L \quad \text{(Amperes)} \tag{12}$$

APPLICATION INFORMATION

The current limit programming resistor (R_{ILIM}) is calculated using equation (13). Care must be taken in choosing the values used for V_{OS} and I_{SINK} in the equation. In order to ensure the output current at the overcurrent level, the minimum value of I_{SINK} and the maximum value of V_{OS} must be used.

$$R_{ILIM} = \frac{I_{OC} \times R_{DS(on)[max]}}{I_{SINK}} + \frac{V_{OS}}{I_{SINK}} \quad (\Omega) \tag{13}$$

where:

- I_{SINK} is the current into the ILIM pin and is 8.6 μA, minimum
- I_{OC} is the overcurrent setpoint which is the DC output current plus one-half of the peak inductor current
- V_{OS} is the overcurrent comparator offset and is 30 mV, maximum

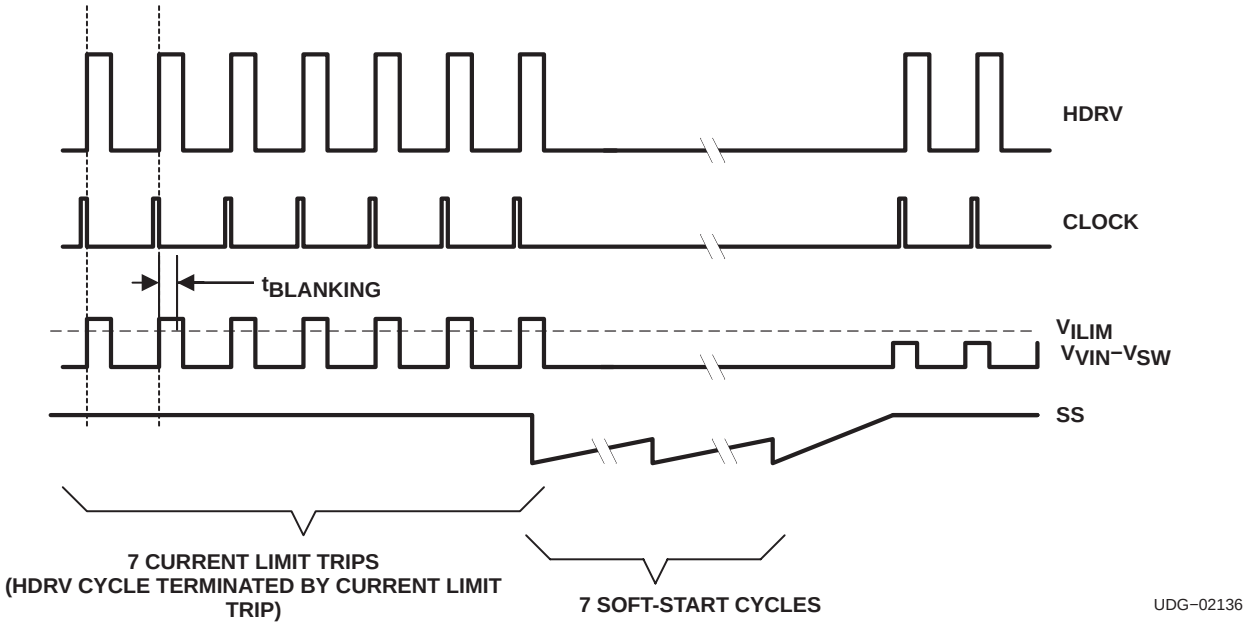


Figure 4. Typical Current Limit Protection Waveforms

SYNCHRONIZING TO AN EXTERNAL SUPPLY

The TPS40056 can be synchronized to an external clock through the SYNC pin. Synchronization occurs on the falling edge of the SYNC signal. The synchronization frequency should be in the range of 20% to 30% higher than its programmed free-run frequency. The clock frequency at the SYNC pin replaces the master clock generated by the oscillator circuit. Pulling the SYNC pin low programs the TPS40056 to freely run at the frequency programmed by R_T.

APPLICATION INFORMATION

LOOP COMPENSATION

Voltage-mode buck-type converters are typically compensated using Type III networks. Since the TPS40056 includes no voltage feedforward control, the gain of the PWM modulator must be included. The modulator gain is described in Figure 5.

$$A_{MOD} = \frac{V_{IN}}{V_S} \quad \text{or} \quad A_{MOD(dB)} = 20 \times \log\left(\frac{V_{IN}}{V_S}\right) \tag{14}$$

Duty dycle, D, varies from 0 to 1 as the control voltage, V_C, varies from the minimum ramp voltage to the maximum ramp voltage, V_S. Also, for a synchronous buck converter, $D = V_O / V_{IN}$. To get the control voltage to output voltage modulator gain in terms of the input voltage and ramp voltage,

$$D = \frac{V_O}{V_{IN}} = \frac{V_C}{V_S} \quad \text{or} \quad \frac{V_O}{V_C} = \frac{V_{IN}}{V_S} \tag{15}$$

Calculate the Poles and Zeros

For a buck converter using voltage mode control there is a double pole due to the output L-C_O. The double pole is located at the frequency calculated in equation (16).

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_O}} \quad \text{(Hertz)} \tag{16}$$

There is also a zero created by the output capacitance, C_O, and its associated ESR. The ESR zero is located at the frequency calculated in equation (17).

$$f_Z = \frac{1}{2\pi \times ESR \times C_O} \quad \text{(Hertz)} \tag{17}$$

Calculate the value of R_{BIAS} to set the output voltage, V_{OUT}.

$$R_{BIAS} = \frac{V_{EA\_REF} \times R1}{V_{OUT} - V_{EA\_REF}} \ \Omega \tag{18}$$

The maximum crossover frequency (0 dB loop gain) is calculated in equation (19).

$$f_C = \frac{f_{SW}}{4} \quad \text{(Hertz)} \tag{19}$$

Typically, f_C is selected to be close to the midpoint between the L-C_O double pole and the ESR zero. At this frequency, the control to output gain has a –2 slope (−40 dB/decade), while the Type III topology has a +1 slope (20 dB/decade), resulting in an overall closed loop –1 slope (−20 dB/decade).

Figure 5 shows the modulator gain, L-C filter, output capacitor ESR zero, and the resulting response to be compensated.

APPLICATION INFORMATION

PWM MODULATOR RELATIONSHIPS

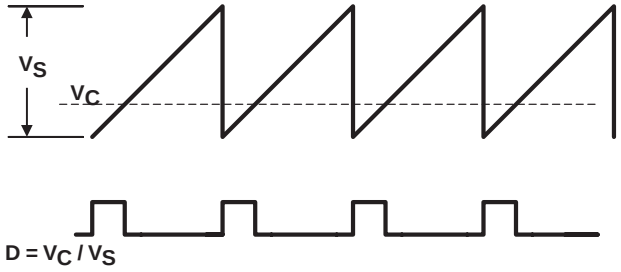


Figure 5

MODULATOR GAIN vs SWITCHING FREQUENCY

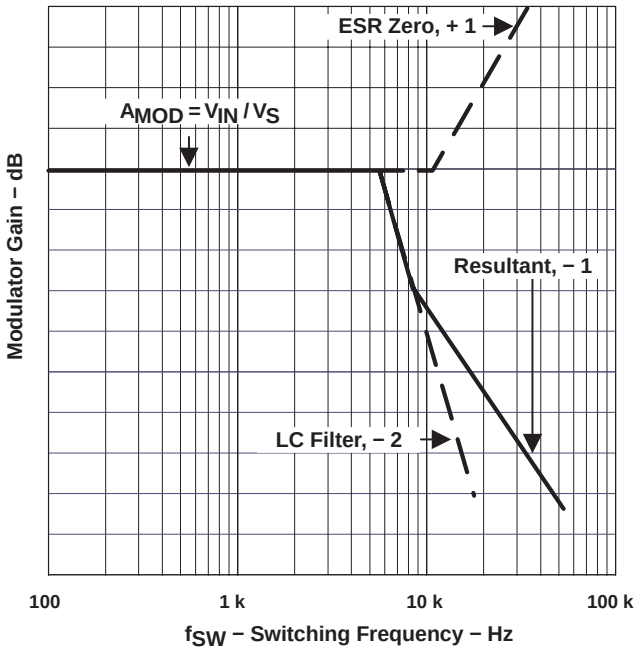


Figure 6

A Type III topology, shown in Figure 7, has two zero-pole pairs in addition to a pole at the origin. The gain and phase boost of a Type III topology is shown in Figure 8. The two zeros are used to compensate the L-C_O double pole and provide phase boost. The double pole is used to compensate for the ESR zero and provide controlled gain roll-off. In many cases the second pole can be eliminated and the amplifier's gain roll-off used to roll-off the overall gain at higher frequencies.

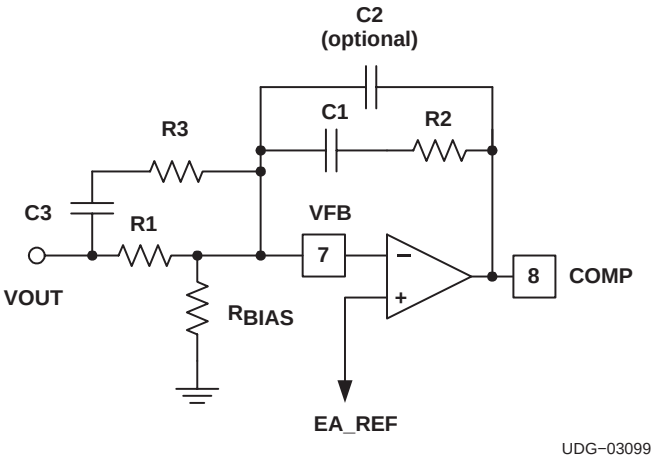


Figure 7. Type III Compensation Configuration

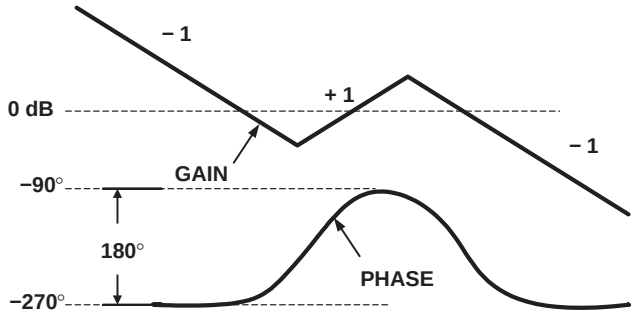


Figure 8. Type III Compensation Gain and Phase

APPLICATION INFORMATION

The poles and zeros for a type III network are described in equations (20).

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \text{ (Hertz)} \qquad f_{Z2} = \frac{1}{2\pi \times R1 \times C3} \text{ (Hertz)}$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} \text{ (Hertz)} \qquad f_{P2} = \frac{1}{2\pi \times R3 \times C3} \text{ (Hertz)} \tag{20}$$

The value of R1 is somewhat arbitraty, but influences other component values. A value between 50 kΩ and 100 kΩ usually yields reasonable values.

The unity gain frequency is described in equation (21)

$$f_C = \frac{1}{2\pi \times R1 \times C2 \times G} \text{ (Hertz)} \tag{21}$$

where G is the reciprocal of the modulator gain at f_C.

The modulator gain as a function of frequency at f_C, is described in equation (22).

$$AMOD(f) = AMOD \times \left(\frac{f_{LC}}{f_C}\right)^2 \text{ and } G = \frac{1}{AMOD(f)} \tag{22}$$

Minimum Load Resistance

Care must be taken not to load down the output of the error amplifier with the feedback resistor, R2, that is too small. The error amplifier has a finite output source and sink current which must be considered when sizing R2. Too small a value does not allow the output to swing over its full range.

$$R2_{(MIN)} = \frac{V_{C\ (max)}}{I_{SOURCE\ (min)}} = \frac{3.45\ V}{2\ mA} = 1725\ \Omega \tag{23}$$

CALCULATING THE BOOST AN BP10 BYPASS CAPACITOR

The BOOST capacitance provides a local, low impedance source for the high-side driver. The BOOST capacitor should be a good quality, high-frequency capacitor. The size of the bypass capacitor depends on the total gate charge of the MOSFET and the amount of droop allowed on the bypass capacitor. The BOOST capacitance is described in equation (24).

$$C_{BOOST} = \frac{Q_g}{\Delta V} \text{ (Farads)} \tag{24}$$

The 10-V reference pin, BP10V needs to provide energy for both the synchronous MOSFET and the high-side MOSFET via the BOOST capacitor. Neglecting any efficiency penalty, the BP10V capacitance is described in equation (25).

$$C_{BP10} = \frac{\left(Q_{gHS} + Q_{gSR}\right)}{\Delta V} \text{ (Farads)} \tag{25}$$

APPLICATION INFORMATION

dv/dt Induced Turn−On

MOSFETs are susceptible to dv/dt turn-on particularly in high-voltage (V_{DS}) applications. The turn-on is caused by the capacitor divider that is formed by C_{GD} and C_{GS}. High dv/dt conditions and drain-to-source voltage, on the MOSFET causes current flow through C_{GD} and causes the gate-to-source voltage to rise. If the gate-to-source voltage rises above the MOSFET threshold voltage, the MOSFET turns on, resulting in large shoot-through currents. Therefore, the SR MOSFET should be chosen so that the C_{GD} capacitance is smaller than the C_{GS} capacitance.

High Side MOSFET Power Dissipation

The power dissipated in the external high-side MOSFET is comprised of conduction and switching losses. The conduction losses are a function of the I_{RMS} current through the MOSFET and the $R_{DS(on)}$ of the MOSFET. The high-side MOSFET conduction losses are defined by equation (26).

$$P_{COND} = \left(I_{RMS}\right)^2 \times R_{DS(on)} \times \left(1 + TC_R \times \left[T_J - 25\right]\right) \text{ (Watts)} \quad (26)$$

where:

- TC_R is the temperature coefficient of the MOSFET $R_{DS(on)}$

The TC_R varies depending on MOSFET technology and manufacturer but is typically ranges between .0035 ppm/°C and .010 ppm/°C.

The I_{RMS} current for the high side MOSFET is described in equation (27).

$$I_{RMS} = I_O \times \sqrt{d} \quad \left(\text{Amperes}_{RMS}\right) \quad (27)$$

The switching losses for the high-side MOSFET are descibed in equation (28).

$$P_{SW(fsw)} = \left(V_{IN} \times I_{OUT} \times t_{SW}\right) \times f_{SW} \text{ (Watts)} \quad (28)$$

where:

- I_O is the DC output current
- t_{SW} is the switching rise time, typically < 20 ns
- f_{SW} is the switching frequency

Typical switching waveforms are shown in Figure 8.

APPLICATION INFORMATION

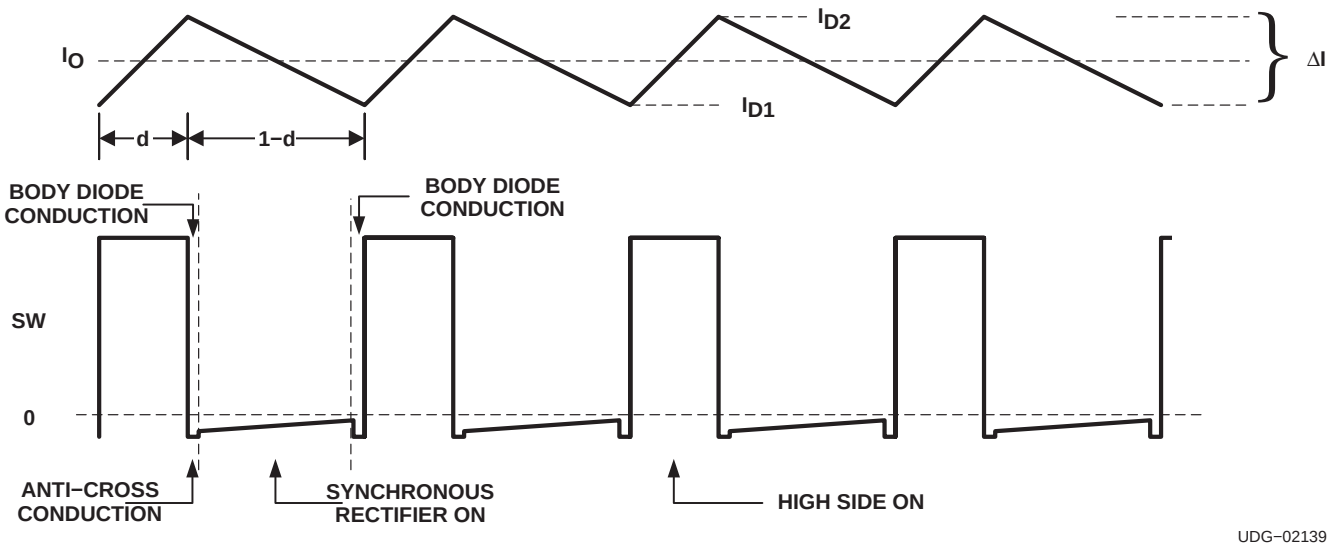


Figure 9. Inductor Current and SW Node Waveforms

The maximum allowable power dissipation in the MOSFET is determined by equation (29).

$$P_T = \frac{\left(T_J - T_A\right)}{\theta_{JA}} \quad \text{(Watts)} \tag{29}$$

where:

$$P_T = P_{COND} + P_{SW(fsw)} \quad \text{(Watts)} \tag{30}$$

and θ_{JA} is the package thermal impedance.

Synchronous Rectifier MOSFET Power Dissipation

The power dissipated in the synchronous rectifier MOSFET is comprised of three components: $R_{DS(on)}$ conduction losses, body diode conduction losses, and reverse recovery losses. $R_{DS(on)}$ conduction losses can be found using equation (32) and the RMS current through the synchronous rectifier MOSFET is described in equation (31).

$$I_{RMS} = I_O \times \sqrt{1 - d} \quad \left(\text{Amperes}_{RMS}\right) \tag{31}$$

The body-diode conduction losses are due to forward conduction of the body diode during the anti−cross conduction delay time. The body diode conduction losses are described by equation (32).

$$P_{DC} = 2 \times I_O \times V_F \times t_{DELAY} \times f_{SW} \quad \text{(Watts)} \tag{32}$$

where:

- V_F is the body diode forward voltage
- t_{DELAY} is the total delay time just before the SW node rises.

APPLICATION INFORMATION

The 2-multiplier is used because the body-diode conducts twice each cycle (once on the rising edge and once on the falling edge). The reverse recovery losses are due to the time it takes for the body diode to recovery from a forward bias to a reverse blocking state. The reverse recovery losses are described in equation (33).

$$P_{RR} = 0.5 \times Q_{RR} \times V_{IN} \times f_{SW} \quad \text{(Watts)} \tag{33}$$

where:

- Q_{RR} is the reverse recovery charge of the body diode

The total synchronous rectifier MOSFET power dissipation is described in equation (34).

$$P_{SR} = P_{DC} + P_{RR} + P_{COND} \quad \text{(Watts)} \tag{34}$$

TPS40056 POWER DISSIPATION

The power dissipation in the TPS40056 is largely dependent on the MOSFET driver currents and the input voltage. The driver current is proportional to the total gate charge, Qg, of the external MOSFETs. Driver power (neglecting external gate resistance, refer to [2] can be calculated from equation (35).

$$P_D = Q_g \times V_{DR} \times f_{SW} \quad \text{(Watts)} \tag{35}$$

And the total power dissipation in the TPS40056, assuming the same MOSFET is selected for both the high-side and synchronous rectifier is described in equation (36).

$$P_T = \left(\frac{2 \times P_D}{V_{DR}} + I_Q\right) \times V_{IN} \quad \text{(Watts)} \tag{36}$$

or

$$P_T = \left(2 \times Q_g \times f_{SW} + I_Q\right) \times V_{IN} \quad \text{(Watts)} \tag{37}$$

where:

- I_Q is the quiescent operating current (neglecting drivers)

The maximum power capability of the device's PowerPad package is dependent on the layout as well as air flow. The thermal impedance from junction to air, assuming 2 oz. copper trace and thermal pad with solder and no air flow.

θ_{JA} = 36.51°C/W

The maximum allowable package power dissipation is related to ambient temperature by equation (29). Substituting equation (29) into equation (37) and solving for f_{SW} yields the maximum operating frequency for the TPS4005x. The result is described in equation (38).

$$f_{SW} = \frac{\left(\left[\frac{(T_J - T_A)}{(\theta_{JA} \times V_{DD})}\right] - I_Q\right)}{\left(2 \times Q_g\right)} \quad \text{(Hz)} \tag{38}$$

LAYOUT CONSIDERATIONS

The PowerPAD™ package

The PowerPAD package provides low thermal impedance for heat removal from the device. The PowerPAD derives its name and low thermal impedance from the large bonding pad on the bottom of the device. For maximum thermal performance, the circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depends on the size of the PowerPAD package. For a 16-pin TSSOP (PWP) package the area is 5 mm x 3.4 mm [3].

Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) works well when 1-oz copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter of 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. Refer to *PowerPAD Thermally Enhanced Package*[3] and the mechanical illustration at the end of this document for more information on the PowerPAD package.

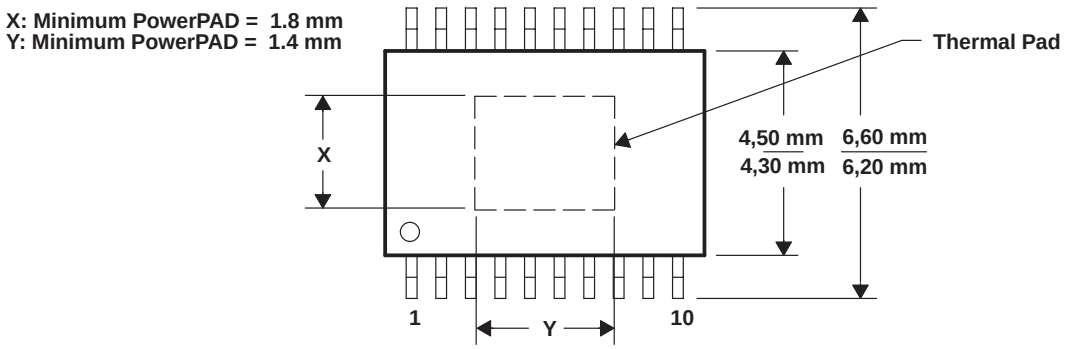


Figure 10. PowerPAD Dimensions

MOSFET Packaging

MOSFET package selection depends on MOSFET power dissipation and the projected operating conditions. In general, for a surface-mount applications, the DPAK style package provides the lowest thermal impedance (θ_{JA}) and, therefore, the highest power dissipation capability. However, the effectiveness of the DPAK depends on proper layout and thermal management. The θ_{JA} specified in the MOSFET data sheet refers to a given copper area and thickness. In most cases, a lowest thermal impedance of 40°C/W requires one square inch of 2-ounce copper on a G−10/FR−4 board. Lower thermal impedances can be achieved at the expense of board area. Please refer to the selected MOSFET's data sheet for more information regarding proper mounting.

LAYOUT CONSIDERATIONS

Grounding and Circuit Layout Considerations

The TPS4005x provides separate signal ground (SGND) and power ground (PGND) pins. It is important that circuit grounds are properly separated. Each ground should consist of a plane to minimize its impedance if possible. The high power *noisy* circuits such as the output, synchronous rectifier, MOSFET driver decoupling capacitor (BP10), and the input capacitor should be connected to PGND plane at the input capacitor.

Sensitive nodes such as the FB resistor divider, R_T, and ILIM should be connected to the SGND plane. The SGND plane should only make a single point connection to the PGND plane.

Component placement should ensure that bypass capacitors (BP10 and BP5) are located as close as possible to their respective power and ground pins. Also, sensitive circuits such as FB, RT and ILIM should not be located near high dv/dt nodes such as HDRV, LDRV, BOOST, and the switch node (SW).

The SW pin Schottky diode, D2 in Figure 10, should be placed close to the TPS40056 with short, wide traces to pins 9 and 12.

DESIGN EXAMPLE

- Input Voltage: 10 Vdc to 14.4 Vdc
- Output voltage: 1.25 V ±1% ($1.2375 \le V_O \le 1.2625$)
- Output current: 8 A (maximum, steady state), 10 A (surge, 10ms duration, 10% duty cycle maximum)
- Output ripple: 33 mV_{P-P} at 8 A
- Output load response: 0.1 V => 10% to 90% step load change, from 1 A to 7 A
- Operating temperature: −40°C to 85°C
- f_{SW}=170 kHz

1. Calculate maximum and minimum duty cycles

$$d_{MIN} = \frac{V_{O(min)}}{V_{IN(max)}} = \frac{1.2375}{14.4} = 0.086 \quad d_{MAX} = \frac{V_{O(max)}}{V_{IN(min)}} = \frac{1.2625}{10} = 0.126 \tag{39}$$

2. Select switching frequency

The switching frequency is based on the minimum duty cycle ratio and the propagation delay of the current limit comparator. In order to maintain current limit capability, the on time of the upper MOSFET, t_{ON}, must be greater than 400 ns (see Electrical Characteristics table). Therefore

$$\frac{V_{O(min)}}{V_{IN(max)}} = \frac{t_{ON}}{T_{SW}} \quad \text{or} \tag{40}$$

$$\frac{1}{T_{SW}} = f_{SW} = \left[\frac{\left(\frac{V_{O(min)}}{V_{IN(max)}} \right)}{T_{ON}} \right] \tag{41}$$

Using 450 ns to provide margin,

$$f_{SW} = \frac{0.086}{450\ ns} = 191\ kHz \tag{42}$$

Since the oscillator can vary by 10%, decrease f_{SW}, by 10%

$$f_{SW} = 0.9 \times 191\ kHz = 172\ kHz$$

and therefore choose a frequency of 170 kHz.

3. Select ΔI

In this case ΔI is chosen so that the converter enters discontinuous mode at 20% of nominal load.

$$\Delta I = I_O \times 2 \times 0.2 = 8 \times 2 \times 0.2 = 3.2\ A \tag{43}$$

DESIGN EXAMPLE

4. Calculate the power losses

Power losses in the high-side MOSFET (Si7860DP) at 14.4-V_{IN} where switching losses dominate can be calculated from equation (27).

$$I_{RMS} = I_O \times \sqrt{d} = 8 \times \sqrt{0.086} = 2.35\ A \tag{44}$$

substituting (27) into (26) yields

$$P_{COND} = 2.35^2 \times 0.008 \times (1 + 0.007 \times (150 - 25)) = 0.083\ W \tag{45}$$

and from equation (28), the switching losses can be determined.

$$P_{SW(fsw)} = \left(V_{IN} \times I_O \times t_{SW}\right) \times f_{SW} = 14.4\ V \times 8\ A \times 20\ ns \times 170\ kHz = 0.39\ W \tag{46}$$

The MOSFET junction temperature can be found by substituting equation (30) into equation (29)

$$T_J = \left(P_{COND} + P_{SW}\right) \times \theta_{JA} + T_A = (0.083 + 0.39) \times 40 + 85 = 90^{\circ}C \tag{47}$$

5. Calculate synchronous rectifier losses

The synchronous rectifier MOSFET has two loss components, conduction, and diode reverse recovery losses. The conduction losses are due to I_{RMS} losses as well as body diode conduction losses during the dead time associated with the anti-cross conduction delay.

The I_{RMS} current through the synchronous rectifier from (31)

$$I_{RMS} = I_O \times \sqrt{1 - d} = 8 \times \sqrt{1 - 0.126} = 7.48\ A_{RMS} \tag{48}$$

The synchronous MOSFET conduction loss from (26) is:

$$P_{COND} = 7.48^2 \times 0.008 \times (1 + 0.007(150 - 25)) = 0.83\ W \tag{49}$$

The body diode conduction loss from (32) is:

$$P_{DC} = 2 \times I_O \times V_{FD} \times t_{DELAY} \times f_{SW} = 2 \times 8.0\ A \times 0.8\ V \times 100\ ns \times 170\ kHz = 0.218 \tag{50}$$

The body diode reverse recovery loss from (33) is:

$$P_{RR} = 0.5 \times Q_{RR} \times V_{IN} \times f_{SW} = 0.5 \times 30\ nC \times 14.4\ V \times 170\ kHz = 0.037\ W \tag{51}$$

The total power dissipated in the synchronous rectifier MOSFET from (34) is:

$$P_{SR} = P_{RR} + P_{COND} + P_{DC} = 0.037 + 0.83 + 0.218 = 1.085\ W \tag{52}$$

The junction temperature of the synchronous rectifier at 85°C is:

$$T_J = P_{SR} \times \theta_{JA} + T_A = (1.085) \times 40 + 85 = 128^{o}C \tag{53}$$

In typical applications, paralleling the synchronous rectifier MOSFET with a Schottky rectifier increases the overall converter efficiency by approximately 2% due to the lower power dissipation during the body diode conduction and reverse recovery periods.

DESIGN EXAMPLE

6. Calculate the inductor value

The inductor value is calculated from equation (3).

$$L = \frac{(14.4 - 1.25\ V) \times 1.25\ V}{14.4\ V \times 3.2\ A \times 170\ kHz} = 2.1\ \mu H \quad (54)$$

A 2.9-µH Coev DXM1306−2R9 or 2.6-µH Panasonic ETQ−P6F2R9LFA can be used.

7. Setting the switching frequency

The clock frequency is set with a resistor (R_T) from the RT pin to ground. The value of R_T can be found from equation (1), with f_{SW} in kHz.

$$R_T = \left(\frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 23\right) k\Omega = 307\ k\Omega \quad \therefore \text{ use } 309\ k\Omega \quad (55)$$

8. Calculating the output capacitance (C_O)

In this example the output capacitance is determined by the load response requirement of ΔV = 0.1 V for a 1 A to 7 A step load. C_O can be calculated using (9)

$$C_O = \frac{2.9\ \mu \times \left((8\ A)^2 - (1\ A)^2\right)}{\left((1.25)^2 - (1.15)^2\right)} = 761\ \mu F \quad (56)$$

Using (4) we can calculate the ESR required to meet the output ripple requirements.

$$33\ mV = 3.2\ A\left(ESR + \frac{1}{8 \times 761\ \mu F \times 170\ kHz}\right) \quad (57)$$

$$ESR = 10.3\ m\Omega - 1.0\ m\Omega = 9.3\ m\Omega \quad (58)$$

For this design example two (2) Panasonic SP EEFUEOD471R capacitors, (2.0 V, 470 µF, 12 mΩ) are used.

9. Calculate the soft-start capacitor (C_{SS})

This design requires a soft−start time (t_{START}) of 1 ms. C_{SS} can be calculated on (11)

$$C_{SS} = \frac{2.3\ \mu A}{0.7\ V} \times 1\ ms = 3.29\ nF = 3300\ pF \quad (59)$$

DESIGN EXAMPLE

10. Calculate the current limit resistor (R_{ILIM})

The current limit set point depends on t_{START}, V_O,C_O and I_{LOAD} at start-up as shown in equation (12). For this design,

$$I_{LIM} > \frac{940\ \mu F \times 1.25\ V}{1\ ms} + 8.0\ A = 9.2\ A \tag{60}$$

For this design, set I_{LIM} for 11.0 A_{DC} minimum. From equation (13), with I_{OC} equal to the DC output surge current plus one-half the ripple current of 3.2 A and $R_{DS(on)}$ is increased 30% (1.3 * 0.008) to allow for MOSFET heating.

$$R_{ILIM} = \frac{12.6\ A \times 0.0104\Omega}{8.6\ \mu A} + \frac{(0.03)}{8.6\ \mu A} = 15.24\ k\Omega - 3.5\ k\Omega = 11.74\ k\Omega \cong 11.8\ \Omega \tag{61}$$

11. Calculate loop compensation values

Calculate the DC modulator gain (A_{MOD}) from equation (14)

$$A_{MOD} = \frac{12}{2} = 6.0 \qquad A_{MOD(dB)} = 20 \times \log(6) = 15.6\ dB \tag{62}$$

Calculate the output filter L-C_O poles and C_O ESR zeros from (16) and (17)

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C_O}} = \frac{1}{2\pi\sqrt{2.9\ \mu H \times 940\ \mu F}} = 3.05\ kHz \tag{63}$$

and

$$f_Z = \frac{1}{2\pi \times ESR \times C_O} = \frac{1}{2\pi \times 0.006 \times 940\ \mu F} = 28.2\ kHz \tag{64}$$

Select the close-loop 0 dB crossover frequency, f_C. For this example f_C = 20 kHz.

Select the double zero location for the Type III compensation network at the output filter double pole at 3.05 kHz.

Select the double pole location for the Type III compensation network at the output capacitor ESR zero at 28.2 kHz.

The amplifier gain at the crossover frequency of 20 kHz is determined by the reciprocal of the modulator gain AMOD at the crossover frequency from equation (22).

$$A_{MOD(f)} = A_{MOD} \times \left(\frac{f_{LC}}{f_C}\right)^2 = 6 \times \left(\frac{3.05\ kHz}{20\ kHz}\right)^2 = 0.14 \tag{65}$$

And also from equation (22).

$$G = \frac{1}{A_{MOD(f)}} = \frac{1}{0.14} = 7.14 \tag{66}$$

Choose R1 = 100 kΩ

DESIGN EXAMPLE

The poles and zeros for a type III network are described in equations (20) and (21).

$$f_{Z2} = \frac{1}{2\pi \times R1 \times C3} \therefore C3 = \frac{1}{2\pi \times 100\ k\Omega \times 3.05\ kHz} = 522\ pF,\ \text{choose } 560\ pF \quad (67)$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C3} \therefore R3 = \frac{1}{2\pi \times 560\ pF \times 28.2\ kHz} = 10.08\ k\Omega,\ \text{choose } 10\ k\Omega \quad (68)$$

$$f_{C} = \frac{1}{2\pi \times R1 \times C2 \times G} \therefore C2 = \frac{1}{2\pi \times 100\ k\Omega \times 7.14 \times 20\ kHz} = 11.1\ pF,\ \text{choose } 10\ pF \quad (69)$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} \therefore R2 = \frac{1}{2\pi \times 10\ pF \times 28.2\ kHz} = 564\ k\Omega,\ \text{choose } 562\ k\Omega \quad (70)$$

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \therefore C1 = \frac{1}{2\pi \times 562\ k\Omega \times 3.05\ kHz} = 92.9\ pF,\ \text{choose } 100\ pF \quad (71)$$

Calculate the value of R_{BIAS} from equation (17) with R1 = 100 kΩ. Since the output of 1.25-V is within the EA_REF input specification of 0.5 V to 1.5 V, an R_{BIAS} resistor is not required.

CALCULATING THE BOOST AND BP10V BYPASS CAPACITANCE

The size of the bypass capacitor depends on the total gate charge of the MOSFET being used and the amount of droop allowed on the bypass cap. The BOOST capacitance for the Si7860DP, allowing for a 0.5 voltage droop on the BOOST pin from equation (24) is:

$$C_{BOOST} = \frac{Q_g}{\Delta V} = \frac{18\ nC}{0.5\ V} = 36\ nF \quad (72)$$

and the BP10V capacitance from (25) is

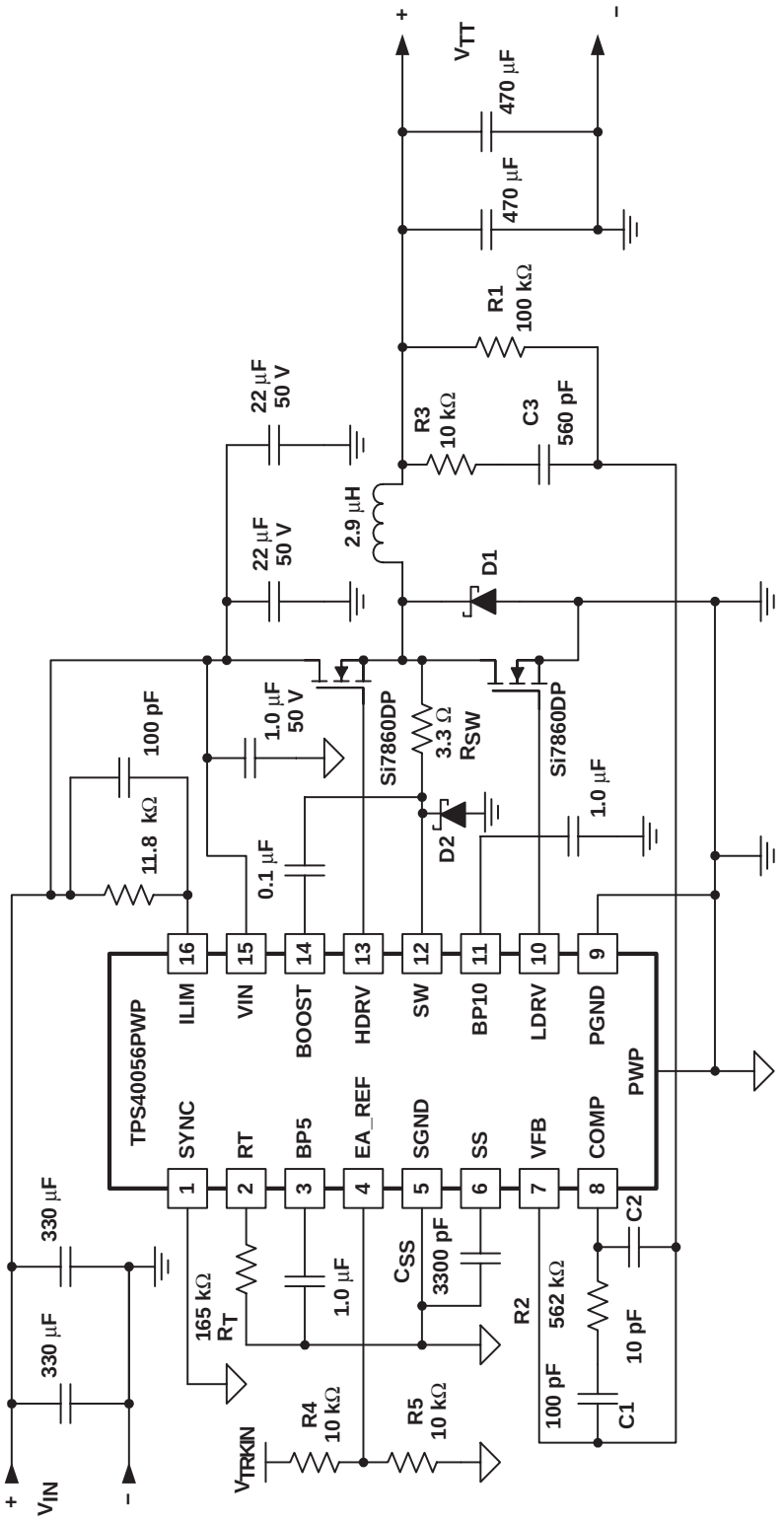
$$C_{BP(10\ V)} = \frac{Q_{gHS} + Q_{gSR}}{\Delta V} = \frac{2 \times Q_g}{\Delta V} = \frac{36\ nC}{0.5\ V} = 72\ nF \quad (73)$$

For this application, a 0.1-µF capacitor is used for the BOOST bypass capacitor and a 1.0-µF capacitor is used for the BP10V bypass.

Figure 10 shows component selection for the 10-V to 14.4-V to 1.25-V at 8 A dc-to-dc converter specified in the design example.

REFERENCES

1. Balogh, Laszlo, *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, Texas Instruments/Unitrode Corporation, Power Supply Design Seminar, SEM−1400 Topic 2.
2. *PowerPAD Thermally Enhanced Package* Texas Instruments, Semiconductor Group, Technical Brief: TI Literature No. SLMA002

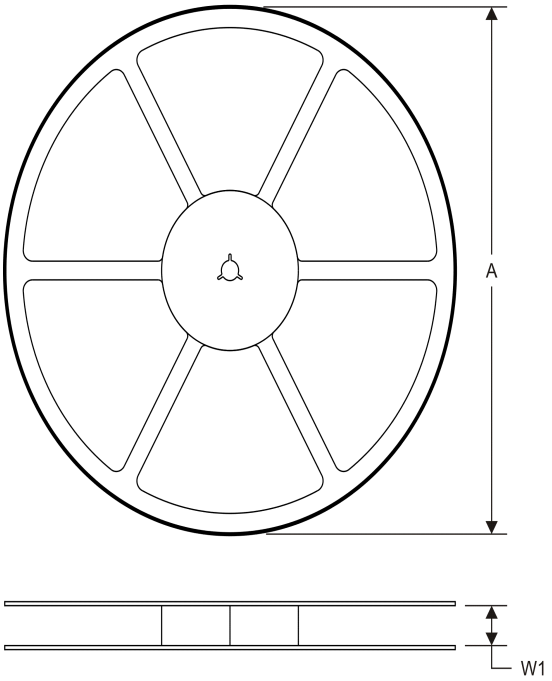


UDG−03100

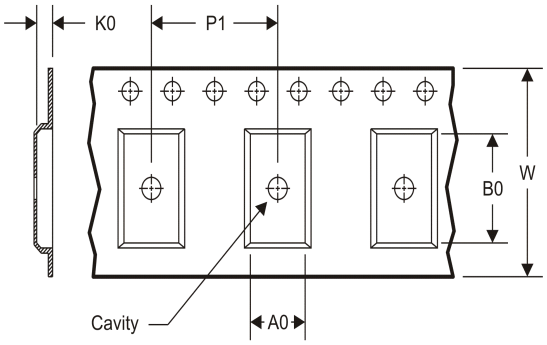
Figure 11. 12-V to 1.25-V at 8-A DC-to-DC Converter (DDR) Design Example

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



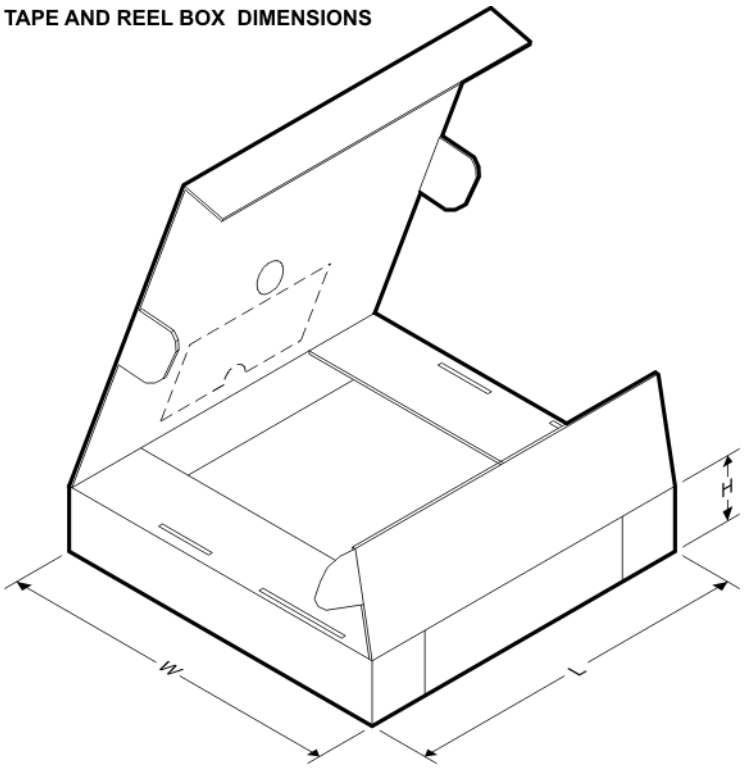
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40056PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

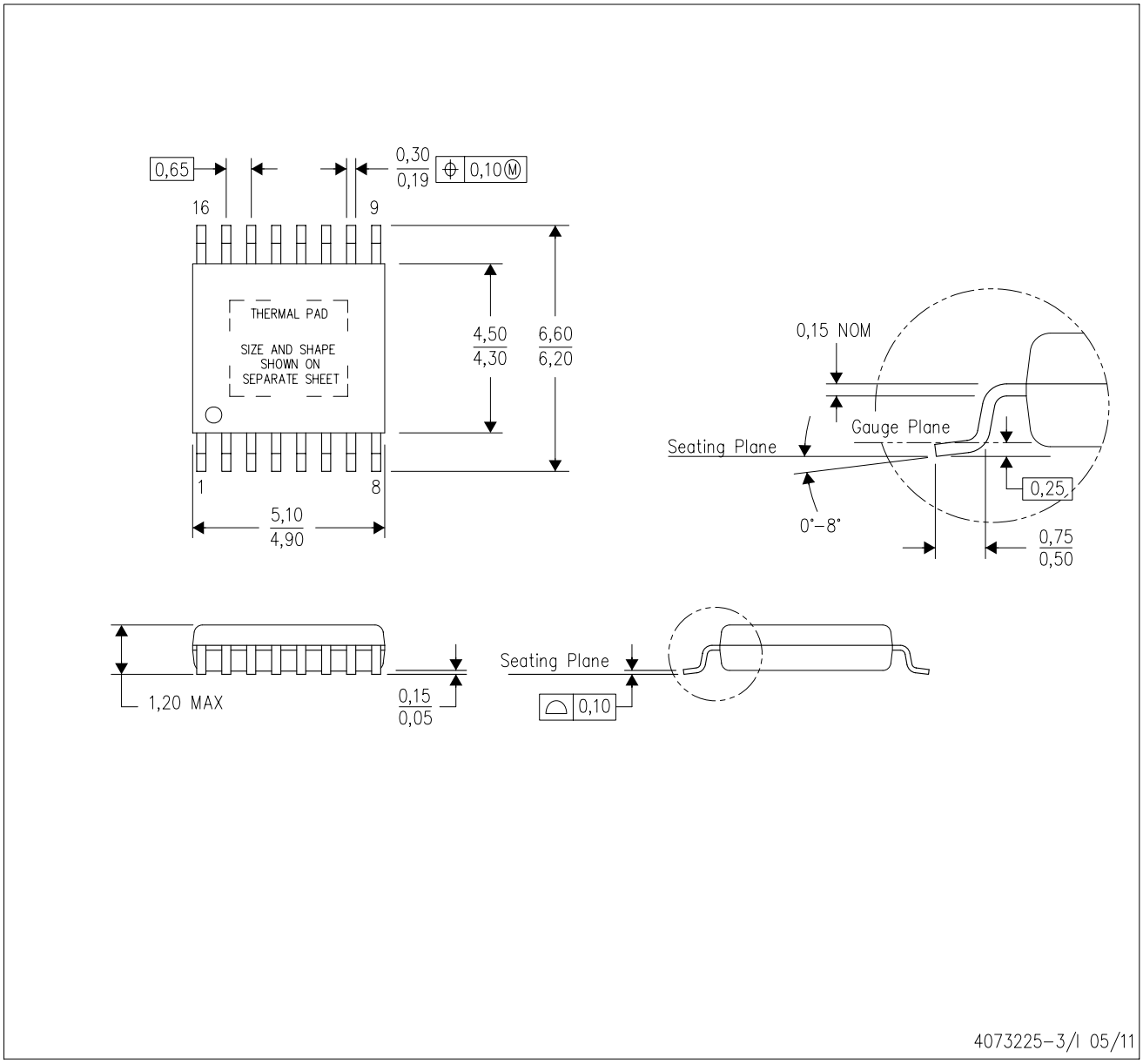
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40056PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

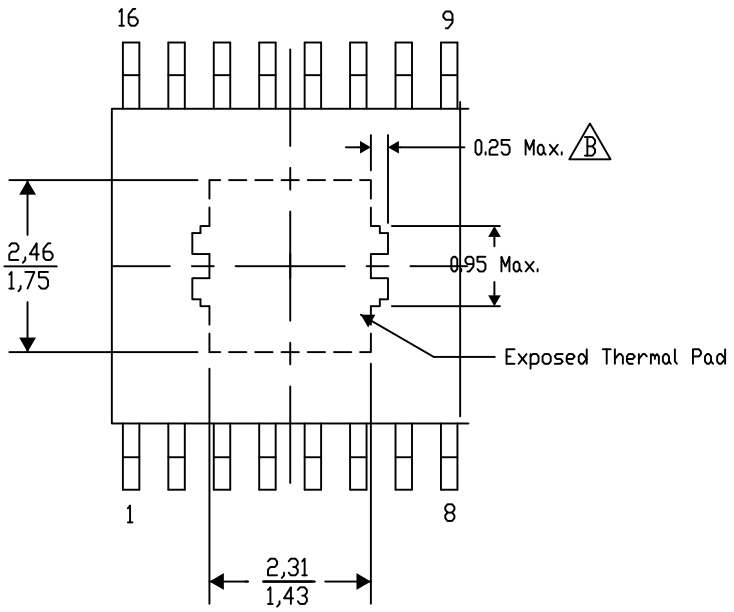
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

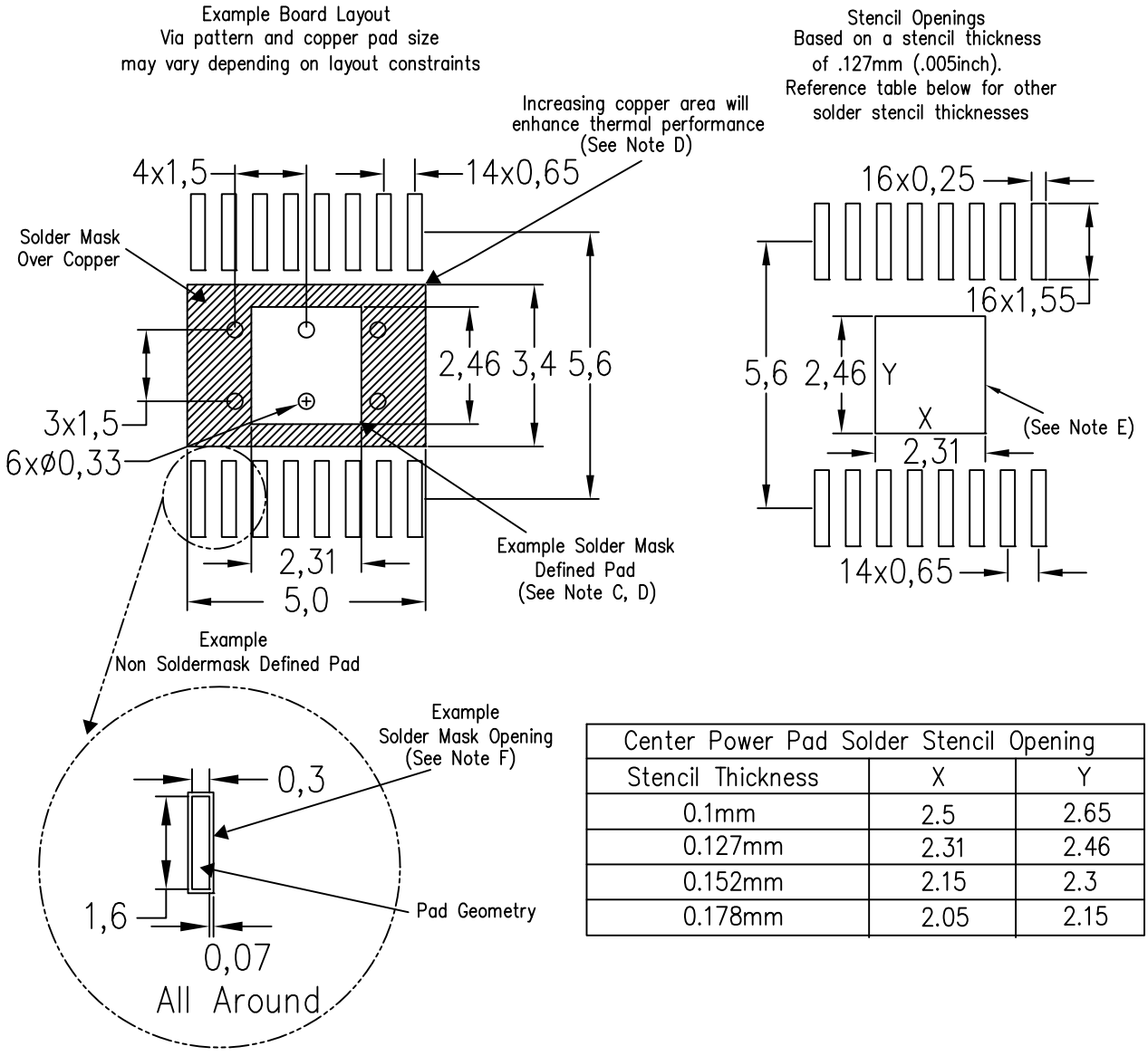
4206332–6/AG 08/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–3/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

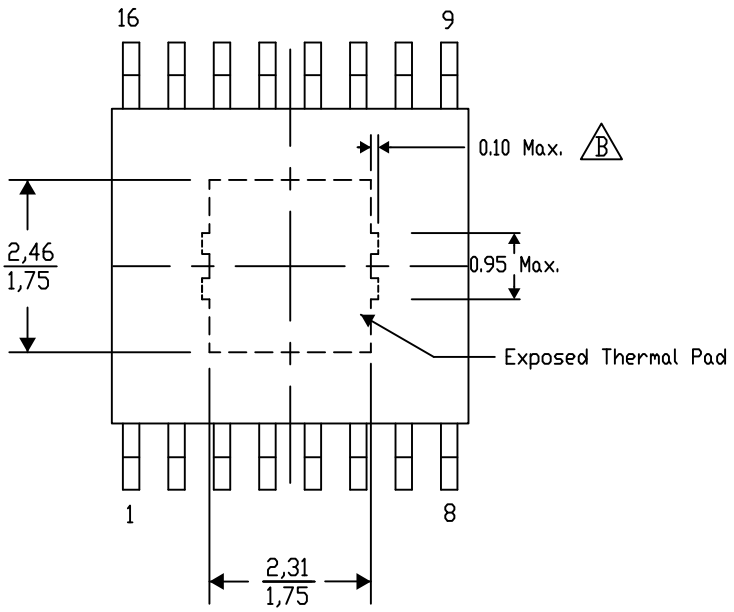
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–45/AG 08/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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