LOW I_Q, DUAL SYNCHRONOUS BUCK CONTROLLER

Check for Samples: TPS43350-Q1, TPS43351-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Test Guidance With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature**
  - **Device HBM ESD Classification Level H2**
  - **Device HBM CDM Classification Level C2**
- **Two Synchronous Buck Controllers**
- **Input Range up to 40 V, (Transients up to 60 V)**
- **Low-Power Mode I_Q: 30 µA (One Buck On), 35 µA (Two Bucks On)**
- **Low Shutdown Current I_{sh} < 4 µA**
- **Buck Output Range 0.9 V to 11 V**
- **Programmable Frequency and External Synchronization Range 150 kHz to 600 kHz**
- **Separate Enable Inputs (ENA, ENB)**
- **Frequency Spread Spectrum (TPS43351-Q1)**
- **Selectable Forced Continuous Mode or Automatic Low-Power Mode at Light Loads**
- **Sense Resistor or Inductor DCR Sensing**
- **Out-of-Phase Switching Between Buck Channels**
- **Peak Gate Drive Current 1.5 A**
- **Thermally Enhanced, 38-Pin HTSSOP (DAP) PowerPAD™ Package**

APPLICATIONS

- **Automotive Infotainment, Navigation, and Instrument Cluster Systems**
- **Industrial or Automotive Multi-Rail DC Power Distribution Systems and Electronic Control Units**

DESCRIPTION

The TPS43350-Q1 and TPS43351-Q1 include two current-mode synchronous buck controllers designed for the harsh environment in automotive applications. The devices are ideal for use in a multi-rail system with low quiescent requirements, as they automatically operate in low-power mode (consuming only 30 µA) at light loads. The devices offer protection features such as thermal, soft-start, and overcurrent protection. During short-circuit conditions of the regulator output, activation of the current-foldback feature can limit the current through the MOSFETs for control of power dissipation. The two independent soft-start inputs allow ramp-up of the output voltage independently during start-up.

The programmable range of the switching frequency is from 150 kHz to 600 kHz, as is the frequency of an external clock to which the devices can synchronize. Additionally, the TPS43351-Q1 offers frequency-hopping spread-spectrum operation.

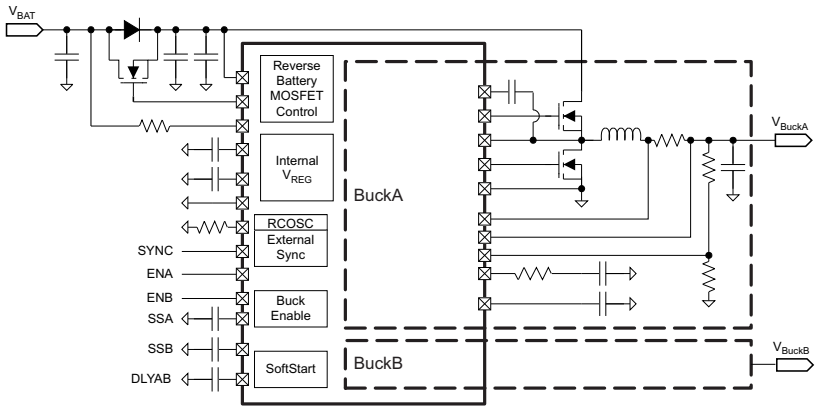


Figure 1. Typical Application Diagram

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE AND ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

			MIN	MAX	UNIT
Voltage	Input voltage: VBAT		–0.3	60	V
Voltage (Buck function: BuckA and BuckB)	Ground: PGNDA–AGND, PGNDB–AGND		–0.3	0.3	V
	Enable inputs: ENA, ENB		–0.3	60	V
	Bootstrap inputs: CBA, CBB		–0.3	68	V
	Bootstrap inputs: CBA–PHA, CBB–PHB		–0.3	8.8	V
	Phase inputs: PHA, PHB		–0.7	60	V
	Phase inputs: PHA, PHB (for 150 ns)		–1		V
	Feedback inputs: FBA, FBB		–0.3	13	V
	Error amplifier outputs: COMPA, COMPB		–0.3	13	V
	High-side MOSFET driver: GA1–PHA, GB1–PHB		–0.3	8.8	V
	Low-side MOSFET drivers: GA2–PGNDA, GB2–PGNDB		–0.3	8.8	V
	Current-sense voltage: SA1, SA2, SB1, SB2		–0.3	13	V
	Soft start: SSA, SSB		–0.3	13	V
	Power-good output: PGA, PGB		–0.3	13	V
	Power-good delay: DLYAB		–0.3	13	V
	Switching-frequency timing resistor: RT		–0.3	13	V
	SYNC, EXTSUP		–0.3	13	V
Voltage (PMOS driver)	P-channel MOSFET driver: GC2		–0.3	60	V
	P-channel MOSFET driver: -GC2		–0.3	8.8	V
	Gate-driver supply: VREG		–0.3	8.8	V
Temperature	Junction temperature: T_J		–40	150	°C
	Operating temperature: T_A		–40	125	°C
	Storage temperature: T_{stg}		–55	165	°C
Electrostatic discharge ratings	Human-body model (HBM) AEC-Q100 Classification Level H2		±2		kV
	Charged-device model (CDM) AEC-Q100 Classification Level C2	FBA, FBB, RT, DLYAB	±400		V
		VBAT, SYNC,	±750		
		All other pins	±500		
	Machine model (MM)	PGA, PGB	±150		
		All other pins	±200		

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to AGND, unless otherwise stated.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS4335x-Q1 DAP 38 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	27.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	19.6	
θ_{JB}	Junction-to-board thermal resistance(4)	15.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.24	
ψ_{JB}	Junction-to-board characterization parameter(6)	6.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	1.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Buck function: BuckA and BuckB voltage	Input voltage: , VBAT	4	40	V
	Enable inputs: ENA, ENB	0	40	V
	Boot inputs: CBA, CBB	4	48	V
	Phase inputs: PHA, PHB	–0.6	40	V
	Current-sense voltage: SA1, SA2, SB1, SB2	0	11	V
	Power-good output: PGA, PGB	0	11	V
	SYNC, EXTSUP	0	9	V
	Operating temperature: T_A	–40	125	°C

DC ELECTRICAL CHARACTERISTICS

V_{IN} = 8 V to 18 V, T_J = –40°C to 150°C (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.0	**Input Supply**						
1.1	V_{Bat}	Supply voltage	After initial start-up, condition is satisfied.	4		40	V
1.2	V_{IN}	Input voltage required for device on initial start-up		6.5		40	V
		Buck regulator operating range after initial start-up		4		40	V
1.3	$V_{IN\ UV}$	Buck undervoltage lockout	V_{IN} falling. After a reset, initial start-up conditions may apply.(1)	3.5	3.6	3.8	V
			V_{IN} rising. After a reset, initial start-up conditions may apply.(1)		3.8	4	V
1.5	$I_{q\_LPM\_}$	LPM quiescent current: T_A = 25°C(2)	V_{IN} = 13 V, BuckA: LPM, BuckB: off		30	40	µA
			V_{IN} = 13 V, BuckB: LPM, BuckA: off				
			V_{IN} = 13 V, BuckA, B: LPM		35	45	µA
1.6	I_{q_LPM}	LPM quiescent current: T_A = 125°C(2)	V_{IN} = 13 V, BuckA: LPM, BuckB: off		40	50	µA
			V_{IN} = 13 V, BuckB: LPM, BuckA: off				
			V_{IN} = 13 V, BuckA, B: LPM		45	55	µA
1.7	I_{q_NRM}	Quiescent current: T_A = 25°C(2)	Normal operation, SYNC = High				
			V_{IN} = 13 V, BuckA: CCM, BuckB: off		4.85	5.3	mA
			V_{IN} = 13 V, BuckB: CCM, BuckA: off				
			V_{IN} = 13 V, BuckA, B: CCM		7	7.6	mA
1.8	I_{q_NRM}	Quiescent current: T_A = 125°C(2)	Normal operation, SYNC = High				
			V_{IN} = 13 V, BuckA: CCM, BuckB: off		5	5.5	mA
			V_{IN} = 13 V, BuckB: CCM, BuckA: off				
			V_{IN} = 13 V, BuckA, B: CCM		7.5	8	mA
1.9	I_{BAT_sh}	Shutdown current	BuckA, B: off, V_{BAT} = 13 V		2.5	4	µA
2.0	**Input Voltage - Overvoltage Lockout**						
2.1	V_{OVLO}	Overvoltage shutdown	V_{IN} rising	45	46	47	V
			V_{IN} falling	43	44	45	V
2.2	$OVLO_{Hys}$	Hysteresis		1	2	3	V
2.3	$OVLO_{filter}$	Filter time			5		µs
	Gate Driver for PMOS						
3.1	$r_{DS(on)}$	PMOS OFF			10	20	Ω
3.2	I_{PMOS_ON}	Gate current	V_{IN} = 13.5 V, V_{GS} = –5 V	10			mA
3.3	t_{delay_ON}	Turnon delay	C = 10 nF		5	10	µs
4.0	**Buck Controllers**						
4.1	$V_{BuckA/B}$	Adjustable output voltage range		0.9		11	V
4.2	$V_{REF,\ NRM}$	Internal reference voltage and tolerance in normal mode	Measure FBX pin	0.792	0.8	0.808	V
				–1%		1%	
4.3	$V_{REF,\ LPM}$	Internal reference voltage and tolerance in low-power mode	Measure FBX pin	0.784	0.8	0.816	V
				–2%		2%	
4.4	V_{SENSE}	V sense for forward current limit in CCM	FBx = 0.75 V (low duty cycles)	60	75	90	mV
4.5		V sense for reverse current limit in CCM	FBx = 1 V	–65	–37.5	–23	mV
4.6	$V_{I\text{-}Foldback}$	V sense for output short	FBx = 0 V	17	32.5	48	mV
4.7	t_{dead}	Shoot-through delay, blanking time			100		ns
4.8	DC_{NRM}	High-side minimum on-time			100		ns
		Maximum duty cycle (digitally controlled)			98.75%		
4.9	DC_{LPM}	Duty cycle LPM				80%	

(1) If V_{BAT} and V_{REG} remain adequate, the buck can continue to operate if V_{IN} is > 3.8 V.
(2) Quiescent current specification is non-switching current consumption without including the current in the external feedback resistor divider.

DC ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 8 V to 18 V, T_J = –40°C to 150°C (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.10	I_{LPM_Entry}	LPM entry threshold load current as fraction of maximum set load current	The exit threshold is specified to be always higher than entry threshold		1%	(3)	
	I_{LPM_Exit}	LPM exit threshold load current as fraction of maximum set load current		(3)	10%		
	High-Side External NMOS Gate Drivers for Buck Controller						
4.11	I_{GX1_peak}	Gate driver peak current			1.5		A
4.12	$r_{DS(on)}$	Source and sink driver	V_{REG} = 5.8 V, I_{GX1} current = 200 mA			2	Ω
	Low-Side NMOS Gate Drivers for Buck Controller						
4.13	I_{GX2_peak}	Gate-driver peak current			1.5		A
4.14	$r_{DS(on)}$	Source and sink driver	V_{REG} = 5.8 V, I_{GX2} current = 200 mA			2	Ω
	Error Amplifier (OTA) for Buck Converters						
4.15	Gm_{BUCK}	Transconductance	COMPA, COMPB = 0.8 V, source/sink = 5 µA, test in feedback loop	0.72	1	1.35	mS
4.16	I_{PULLUP_FBx}	Pullup current at FBx pins	FBx = 0 V	50	100	200	nA
5.0	**Digital Inputs: ENA, ENB, SYNC**						
5.1	V_{IH}	Higher threshold	V_{IN} = 13 V	1.7			V
5.2	V_{IL}	Lower threshold	V_{IN} = 13 V			0.7	V
5.3	R_{IH_SYNC}	Resistance	V_{SYNC} = 5 V		500		kΩ
5.5	I_{IL_ENx}	Pullup current source on ENA, ENB	V_{ENx} = 0 V		0.5	2	µA
6.0	**Switching Parameters – Buck DC-DC Controllers**						
6.1	f_{SW_Buck}	Buck switching frequency	RT pin: GND	360	400	440	kHz
6.2	f_{SW_Buck}	Buck switching frequency	RT pin: 60-kΩ external resistor	360	400	440	kHz
6.3	f_{SW_adj}	Buck adjustable range with external resistor	RT pin: external resistor	150		600	kHz
6.4	f_{SYNC}	Buck synchronization range	External clock input	150		600	kHz
6.5	f_{SS}	Spread-spectrum spreading	TPS43351-Q1 only		5%		
7.0	**Internal Gate-Driver Supply**						
7.1	V_{REG}	Internal regulated supply	V_{IN} = 8 V to 18 V, EXTSUP = 0 V, SYNC = High	5.5	5.8	6.1	V
		Load regulation	I_{VREG} = 0 mA to 100 mA, EXTSUP = 0 V, SYNC = High		0.2%	1%	
7.2	$V_{REG(EXTSUP)}$	Internal regulated supply	EXTSUP = 8.5 V	7.2	7.5	7.8	V
		Load regulation	I_{EXTSUP} = 0 mA to 125 mA, SYNC = High EXTSUP = 8.5 V to 13 V		0.2%	1%	
7.3	V_{EXTSUP_th}	EXTSUP switch-over voltage threshold	I_{VREG} = 0 mA to 100 mA , EXTSUP ramping positive	4.4	4.6	4.8	V
7.4	$V_{EXTSUP\text{-}Hys}$	EXTSUP switch-over hysteresis		150		250	mV
7.5	$I_{REG\text{-}Limit}$	Current limit on VREG	EXTSUP = 0 V, normal mode as well as LPM	100		400	mA
7.6	$I_{REG\_EXTSUP\text{-}Limit}$	Current limit on VREG when using EXTSUP	I_{VREG} = 0 mA to 100 mA, EXTSUP = 8.5 V, SYNC = High	125		400	mA
8.0	**Soft Start**						
8.1	I_{SSx}	Soft-start source current	SSA and SSB = 0 V	0.75	1	1.25	µA
9.0	**Oscillator (RT)**						
9.1	V_{RT}	Oscillator reference voltage			1.2		V
10.0	**Power-Good / Delay**						
10.1	PG_{pullup}	Pullup for A and B to Sx2			50		kΩ
10.2	PG_{th1}	Power-good threshold	FBx falling	–5%	–7%	–9%	
10.3	PG_{hys}	Hysteresis			2%		
10.4	PG_{drop}	Voltage drop	I_{PGA} = 5 mA			450	mV
10.5			I_{PGA} = 1 mA			100	mV
10.6	PG_{leak}	Leakage	VSx2 = VPGx = 13 V			1	µA

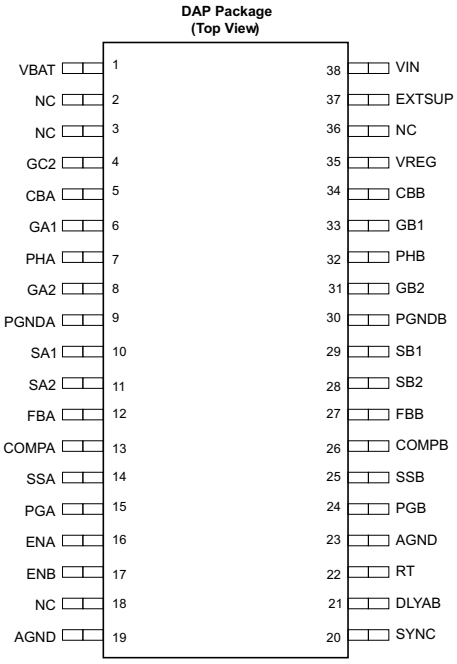
(3) The exit threshold specification is to be always higher than the entry threshold.

DC ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 8 V to 18 V, T_J = –40°C to 150°C (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
10.7	$t_{deglitch}$	Power-good deglitch time		2		16	µs
10.8	t_{delay}	Reset delay	External capacitor = 1 nF $V_{BuckX} < PG_{th1}$		1		ms
10.9	t_{delay_fix}	Fixed reset delay	No external capacitor, pin open		20	50	µs
10.10	I_{OH}	Activate current source (current to charge external capacitor)		30	40	50	µA
10.11	I_{IL}	Activate current sink (current to discharge external capacitor)		30	40	50	µA
11.0	**Overtemperature Protection**						
11.1	$T_{shutdown}$	Junction temperature shutdown threshold		150	165		°C
11.2	T_{hys}	Junction temperature hysteresis			15		°C

DEVICE INFORMATION



PIN FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
AGND	19, 23	O	Analog ground reference
CBA	5	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck controller BuckA. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge.
CBB	34	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck controller BuckB. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge.
COMPA	13	O	Error amplifier output of BuckA and compensation node for voltage-loop stability. The voltage at this node sets the target for the peak current through the inductor of BuckA. Clamping his voltage on the upper and lower ends provides current-limit protection for the external MOSFETs.
COMPB	26	O	Error amplifier output of BuckB and compensation node for voltage-loop stability. The voltage at this node sets the target for the peak current through the inductor of BuckB. Clamping his voltage on the upper and lower ends provides current-limit protection for the external MOSFETs.
DLYAB	21	O	The capacitor at the DLYAB pin sets the power-good delay interval used to de-glitch the outputs of the power-good comparators. Leaving this pin open sets the power-good delay to an internal default value of 20 µs typical.
ENA	16	I	Enable input for BuckA (active-high with an internal pullup current source). An input voltage higher than 1.7 V enables the controller, whereas an input voltage lower than 0.7 V disables the controller. When both ENA and ENB are low, the device shuts down and consumes less than 4 µA of current.
ENB	17	I	Enable input for BuckB (active-high with an internal pullup current source). An input voltage higher than 1.7 V enables the controller, whereas an input voltage lower than 0.7 V disables the controller. When both ENA and ENB are low, the device shuts down and consumes less than 4 µA of current.
EXTSUP	37	I	One can use EXTSUP to supply the VREG regulator from one of the TPS43350-Q1 or TPS43351-Q1 buck regulator rails to reduce power dissipation in cases where there is an expectation of high VIN. If EXTSUP is unused, leave the pin open without a capacitor installed.
FBA	12	I	Feedback voltage pin for BuckA. The buck controller regulates the feedback voltage to the internal reference of 0.8 V. A suitable resistor divider network between the buck output and the feedback pin sets the desired output voltage.
FBB	27	I	Feedback voltage pin for BuckB. The buck controller regulates the feedback voltage to the internal reference of 0.8 V. A suitable resistor divider network between the buck output and the feedback pin sets the desired output voltage.

PIN FUNCTIONS (continued)

NAME	NO.	I/O	DESCRIPTION
GA1	6	O	This output can drive the external high-side N-channel MOSFET for buck regulator BuckA. The output provides high peak currents to drive capacitive loads. The gate-drive reference is to a floating ground provided by PHA that has a voltage swing provided by CBA.
GA2	8	O	This output can drive the external low-side N-channel MOSFET for buck regulator BuckA. The output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin.
GB1	33	O	This output can drive the external high-side N-channel MOSFET for buck regulator BuckB. The output provides high peak currents to drive capacitive loads. The gate drive reference is to a floating ground provided by PHB that has a voltage swing provided by CBB.
GB2	31	O	This output can drive the external low-side N-channel MOSFET for buck regulator BuckB. The output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin.
GC2	4	O	This pin makes a floating output drive available to control the external P-channel MOSFET. This MOSFET can bypass the boost rectifier diode or a reverse-protection diode when the boost is not switching or if boost is disabled, and thus reduce power losses.
NC	2, 3, 18, 36	–	No connection
PGNDA	9	O	Power ground connection to the source of the low-side N-channel MOSFETs of BuckA.
PGNDB	30	O	Power ground connection to the source of the low-side N-channel MOSFETs of BuckB
PGA	15	O	Open-drain power-good indicator pin for BuckA. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls below 93% of the set value.
PGB	24	O	Open-drain power-good indicator pin for BuckB. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls below 93% of the set value.
PHA	7	O	Switching terminal of buck regulator BuckA, providing a floating ground reference for the high-side MOSFET gate-driver circuitry and used to sense current reversal in the inductor when discontinuous-mode operation is desired.
PHB	32	O	Switching terminal of buck regulator BuckB, providing a floating ground reference for the high-side MOSFET gate-driver circuitry and used to sense current reversal in the inductor when discontinuous-mode operation is desired.
RT	22	O	Connecting a resistor to ground on this pin sets the operational switching frequency of the buck and boost controllers. A short circuit to ground on this pin defaults operation to 400 kHz for the buck controllers and 200 kHz for the boost controller.
SA1	10	I	High-impedance differential-voltage inputs from the current-sense element (sense resistor or inductor DCR) for each buck controller. Choose the current-sense element to set the maximum current through the inductor based on the current-limit threshold (subject to tolerances) and considering the typical characteristics across duty cycle and V_{IN}. (SA1 positive node, SA2 negative node).
SA2	11	I	
SB1	29	I	High-impedance differential voltage inputs from the current-sense element (sense resistor or inductor DCR) for each buck controller. Choose the current-sense element to set the maximum current through the inductor based on the current-limit threshold (subject to tolerances) and considering the typical characteristics across duty cycle and V_{IN}. (SB1 positive node, SB2 negative node).
SB2	28	I	
SSA	14	O	Soft-start or tracking input for buck controller BuckA. The buck controller regulates the FBA voltage to the lower of 0.8 V or the SSA pin voltage. An internal pullup current source of 1 µA is present at the pin, and an appropriate capacitor connected here sets the soft-start ramp interval. Alternatively, a resistor divider connected to another supply can provide a tracking input to this pin.
SSB	25	O	Soft-start or tracking input for buck controller BuckB. The buck controller regulates the FBB voltage to the lower of 0.8 V or the SSB pin voltage. An internal pullup current source of 1 µA is present at the pin, and an appropriate capacitor connected here sets the soft-start ramp interval. Alternatively, a resistor divider connected to another supply can provide a tracking input to this pin.
SYNC	20	I	If an external clock is present on this pin, the device detects it, and the internal PLL locks on to the external clock. This overrides the internal oscillator frequency. The device can synchronize to frequencies from 150 kHz to 600 kHz. A high logic level on this pin ensures forced continuous-mode operation of the buck controllers and inhibits transition to low-power mode. An open or low allows discontinuous-mode operation and entry into low-power mode at light loads. On the TPS43351-Q1, a high level enables frequency-hopping spread spectrum, whereas an open or a low level disables it.
VBAT	1	I	Supply pin
VIN	38	I	Main input pin. This is the buck controller input pin. Additionally, it powers the internal control circuits of the device.
VREG	35	O	The device requires an external capacitor on this pin to provide a regulated supply for the gate drivers of the buck and boost controllers. TI recommends capacitance on the order of 4.7 µF. The regulator obtain its power from either or EXTSUP. This pin has current-limit protection; do not use it to drive any other loads.

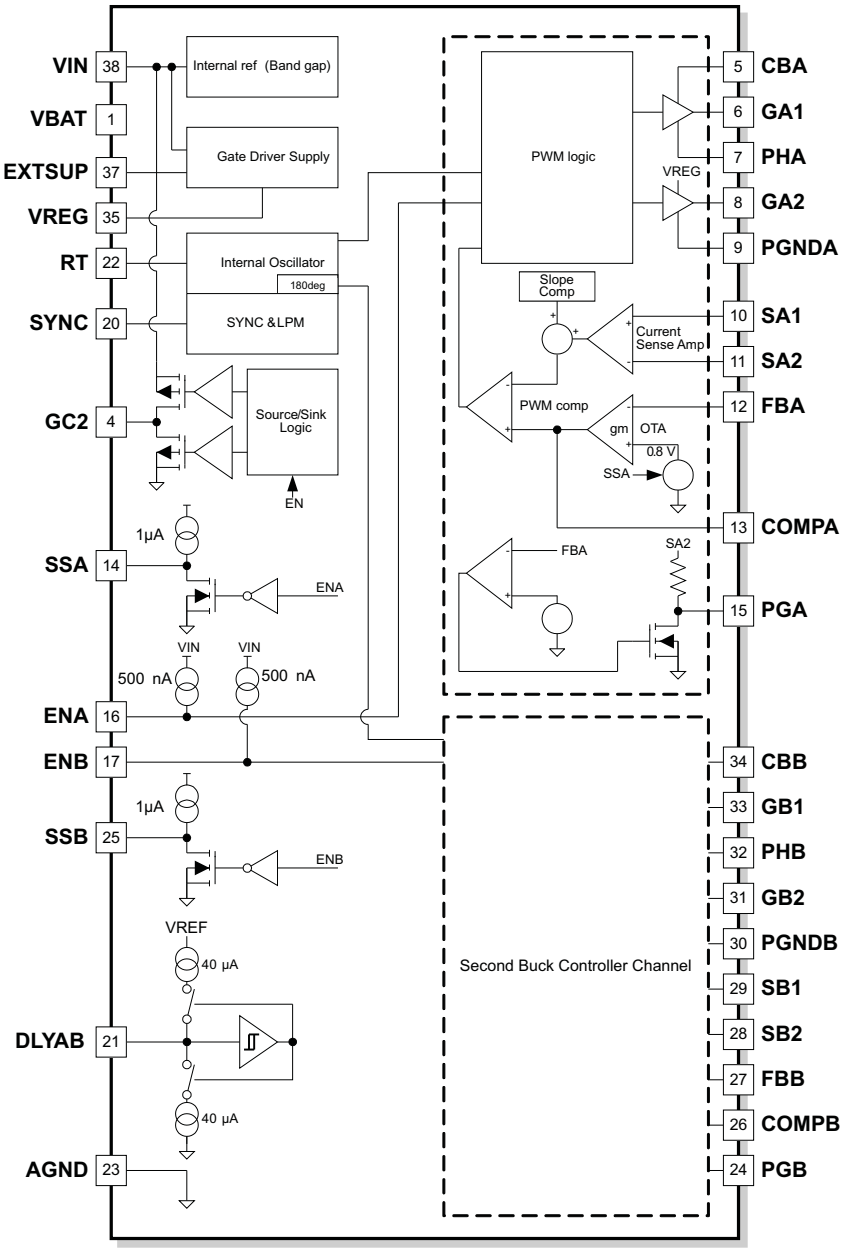


Figure 2. Functional Block Diagram

TYPICAL CHARACTERISTICS

EFFICIENCY ACROSS OUTPUT CURRENTS (BUCKS)
V_{IN} = 12 V, V_{OUT} = 5 V, SWITCHING FREQUENCY = 400 kHz
INDUCTOR = 4.7 µH, R_{SENSE} = 10 mΩ

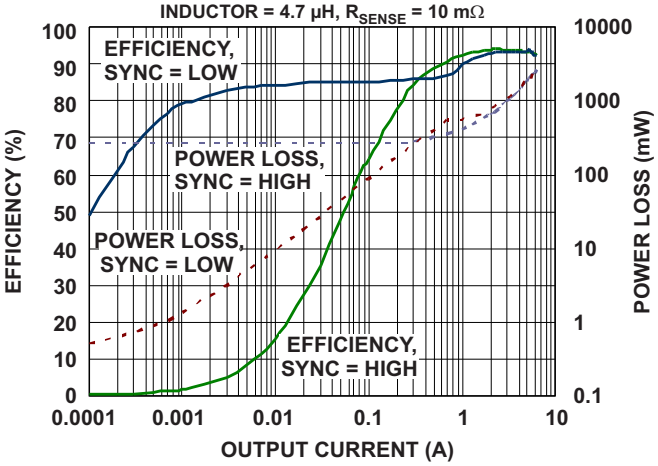


Figure 3.

INDUCTOR CURRENTS (BUCK)
V_{IN} = 12 V, V_{OUT} = 5 V, SWITCHING FREQUENCY = 400 kHz
INDUCTOR = 4.7 µH, R_{SENSE} = 10 mΩ

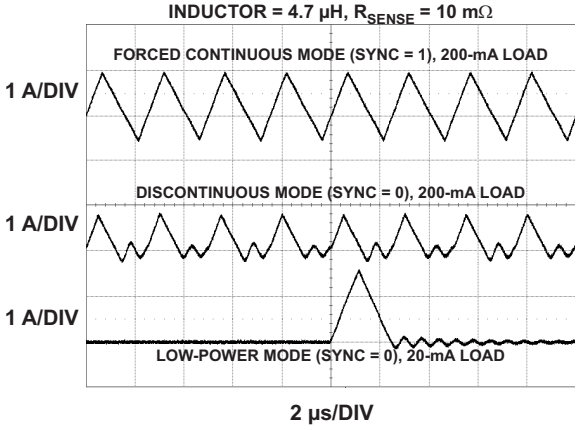


Figure 4.

BUCK LOAD STEP: FORCED CONTINUOUS MODE
(0 TO 4 A AT 2.5 A/µs)
V_{IN} = 12 V, V_{OUT} = 5 V, SWITCHING FREQUENCY = 400 kHz
INDUCTOR = 4.7 µH, R_{SENSE} = 10 mΩ

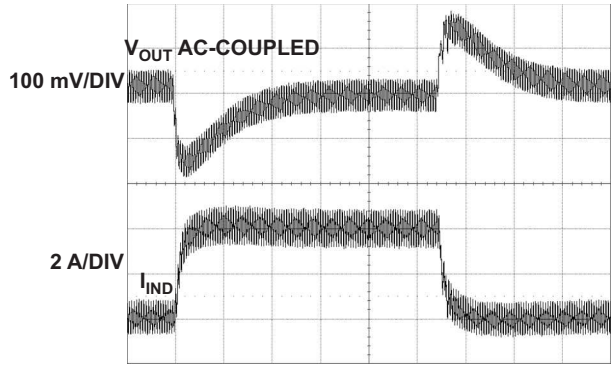


Figure 5.

SOFT-START OUTPUTS (BUCK)

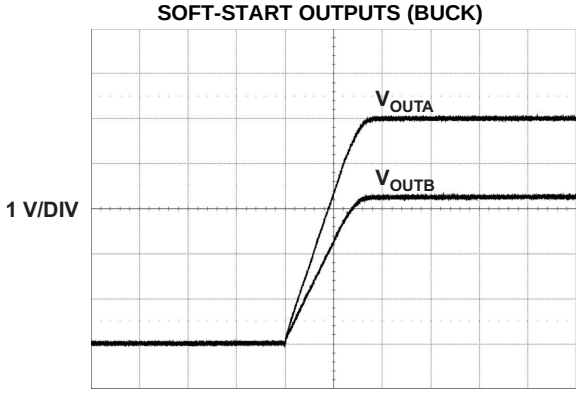


Figure 6.

BUCK LOAD STEP: LOW-POWER-MODE ENTRY
4 A TO 90 mA AT 2.5 A/µs
V_{IN} = 12 V, V_{OUT} = 5 V, SWITCHING FREQUENCY = 400 kHz
INDUCTOR = 4.7 µH, R_{SENSE} = 10 mΩ

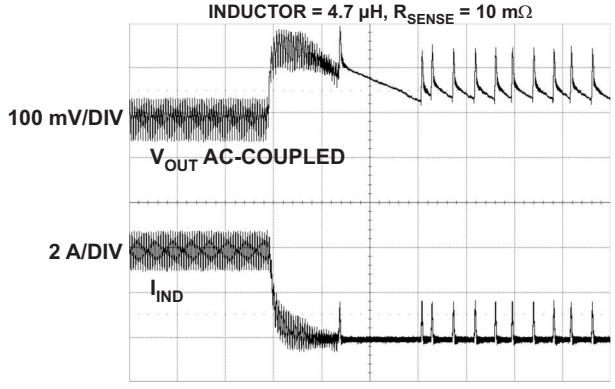


Figure 7.

BUCK LOAD STEP: LOW-POWER-MODE EXIT
90 mA TO 4 A AT 2.5 A/µs
V_{IN} = 12 V, V_{OUT} = 5 V, SWITCHING FREQUENCY = 400 kHz
INDUCTOR = 4.7 µH, R_{SENSE} = 10 mΩ

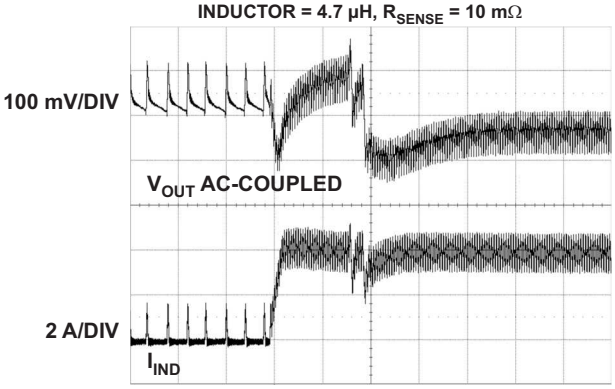


Figure 8.

TYPICAL CHARACTERISTICS (continued)

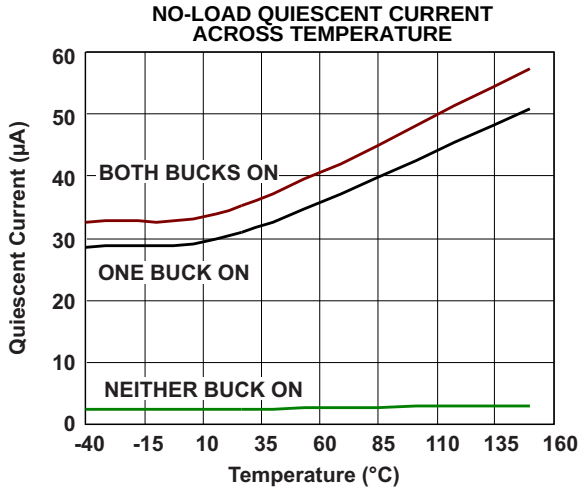


Figure 9.

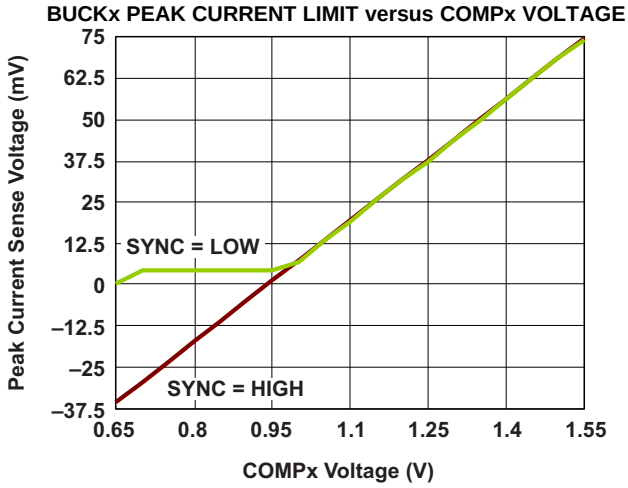


Figure 10.

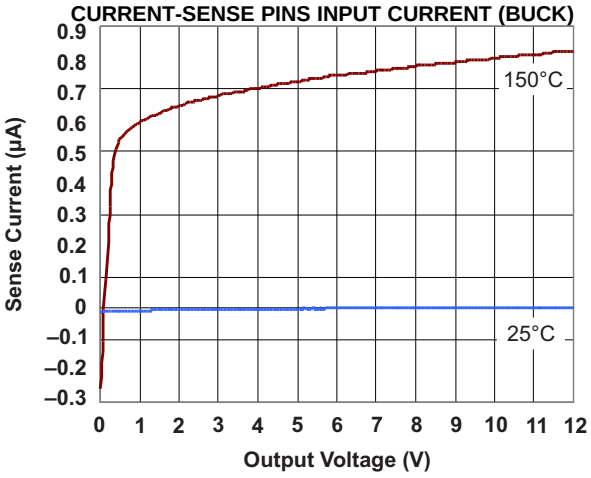


Figure 11.

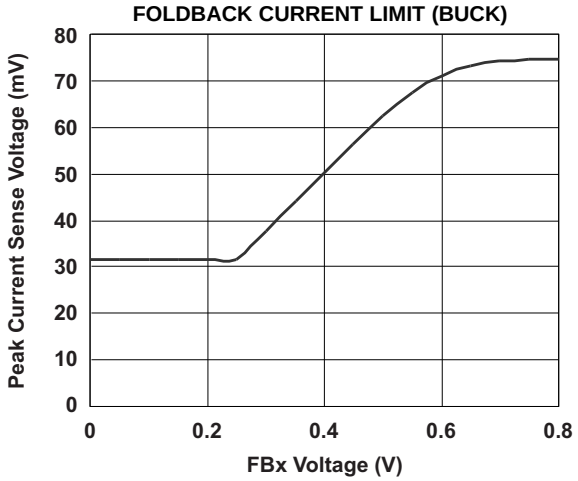


Figure 12.

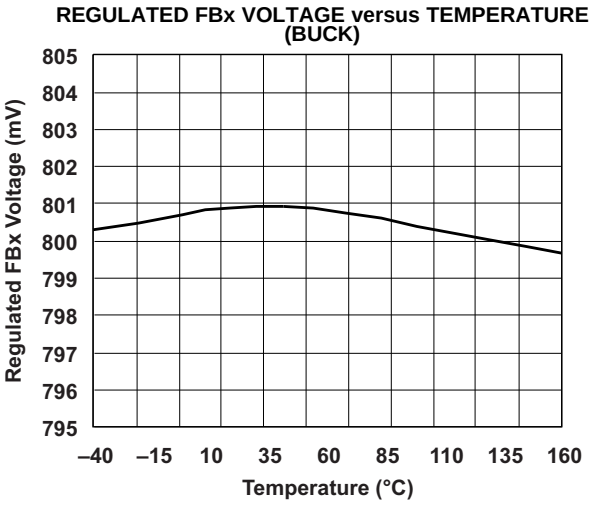


Figure 13.

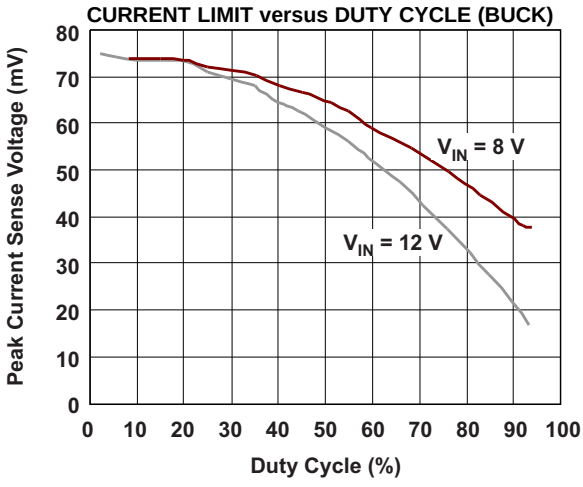


Figure 14.

DETAILED DESCRIPTION

BUCK CONTROLLERS: NORMAL MODE PWM OPERATION

Frequency Selection and External Synchronization

The buck controllers operate using constant-frequency peak-current mode control for optimal transient behavior and ease of component choices. The switching frequency is programmable between 150 kHz and 600 kHz, depending upon the resistor value at the RT pin. A short circuit to ground at this pin sets the default switching frequency to 400 kHz. Using a resistor at RT, one can set another frequency according to the formula:

$$f_{SW} = \frac{X}{RT} \quad (X = 24\ k\Omega \times MHz)$$

$$f_{SW} = 24 \times \frac{10^9}{RT}$$

For example,

600 kHz requires 40 kΩ

150 kHz requires 160 kΩ

It is also possible to synchronize to an external clock at the SYNC pin in the same frequency range of 150 kHz to 600 kHz. The device detects clock pulses at this pin, and an internal PLL locks on to the external clock within the specified range. The device can also detect a loss of clock at this pin, and on detection of this condition, the device sets the switching frequency to the internal oscillator. The two buck controllers operate at identical switching frequencies, 180 degrees out of phase.

Enable Inputs

Independent enable inputs from the ENA and ENB pins enable the buck controllers. These are high-voltage pins, with a threshold of 1.7 V for the high level, and with direct connection to the battery permissible for self-bias. The low threshold is 0.7 V. Both these pins have internal pullup currents of 0.5 µA (typical). As a result, an open circuit on these pins enables the respective buck controllers. But with both buck controllers disabled, the device shuts down and consumes a current less than 4 µA.

Feedback Inputs

The right resistor feedback divider network connected to the FBx (feedback) pins sets the output voltage. Choose this network such that the regulated voltage at the FBx pin equals 0.8 V. The FBx pins have a 100-nA pullup current source as a protection feature in case the pins open up as a result of physical damage.

Soft-Start Inputs

In order to avoid large inrush currents, the buck controllers have independent programmable soft-start timers. The voltage at the SSx pins acts as the soft-start reference voltage. The 1-µA pullup current available at the SSx pins, in combination with a suitably chosen capacitor, generates a ramp of the desired soft-start speed. After start-up, the pullup current ensures that this node is higher than the internal reference of 0.8 V, which then becomes the reference for the buck controllers. The following equation calculates the soft-start ramp time:

$$C_{SS} = \frac{I_{SS} \times \Delta t}{\Delta V} \quad \text{(Farads)}$$

where,

I_{SS} = 1 µA (typical)

ΔV = 0.8 V

C_{SS} is the required capacitor for Δt, the desired soft-start time.

An alternative use of the soft-start pins is as tracking inputs. In this case, connect them to the supply to be tracked via a suitable resistor-divider network.

Current-Mode Operation

Peak-current-mode control regulates the peak current through the inductor to maintain the output voltage at its set value. The error between the feedback voltage at FBx and the internal reference produces a signal at the output of the error amplifier (COMPx) which serves as a target for the peak inductor current. The device senses the current through the inductor as a differential voltage at Sx1–Sx2 and compares voltage with this target during each cycle. A fall or rise in load current produces a rise or fall in voltage at FBx, causing COMPx to fall or rise respectively, thus increasing or decreasing the current through the inductor until the average current matches the load. This process maintains the output voltage in regulation.

The top N-channel MOSFET turns on at the beginning of each clock cycle and stays on until the inductor current reaches its peak value. Once this MOSFET turns off, and after a small delay (shoot-through delay) the lower N-channel MOSFET turns on until the start of the next clock cycle. In dropout operation, the high-side MOSFET stays on continuously. In every fourth clock cycle, there is a limit on the duty cycle of 95% in order to charge the bootstrap capacitor at CBx. This allows a maximum duty cycle of 98.75% for the buck regulators. During dropout, the buck regulator switches at one-fourth of its normal frequency.

Current Sensing and Current Limit With Foldback

Clamping of the maximum value of COMPx is such as to limit the maximum current through the inductor to a specified value. When the output of the buck regulator (and hence the feedback value at FBx) falls to a low value due to a short-circuit or overcurrent condition, the clamped voltage at COMPx successively decreases, thus providing current foldback protection. This protects the high-side external MOSFET from excess current (forward-direction current limit).

Similarly, if a fault condition shorts the output to a high voltage and the low-side MOSFET turns fully on, the COMPx node drops low. A clamp is on its lower end as well, in order to limit the maximum current in the low-side MOSFET (reverse-direction current limit).

An external resistor senses the current through the inductor. Choose the sense resistor such that the maximum forward peak current in the inductor generates a voltage of 75 mV across the sense pins. This specified value is for low duty cycles only. At typical duty-cycle conditions around 40% (assuming 5-V output and 12-V input), 50 mV is a more reasonable value, considering tolerances and mismatches. The typical characteristics provide a guide for using the correct current-limit sense voltage.

The current-sense pins Sx1 and Sx2 are high-impedance pins with low leakage across the entire output range. This allows DCR current sensing using the dc resistance of the inductor for higher efficiency. Figure 15 shows DCR sensing. Here, the series resistance (DCR) of the inductor is the sense element. Place the filter components close to the device for noise immunity. Remember that while the DCR sensing gives high efficiency, it is inaccurate due to the temperature sensitivity and a wide variation of the parasitic inductor series resistance. Hence, it may often be advantageous to use the more-accurate sense resistor for current sensing.

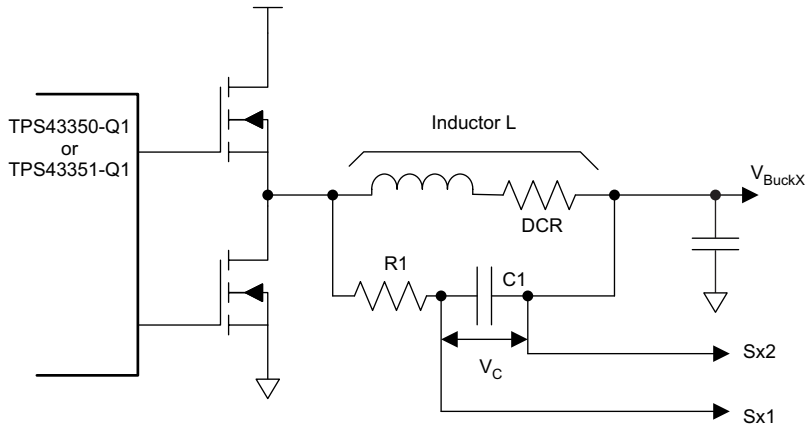


Figure 15. DCR Sensing Configuration

Slope Compensation

Optimal slope compensation, which is adaptive to changes in input voltage and duty cycle, allows stable operation at all conditions. For optimal performance of this circuit, choose the inductor and sense resistor according to the following:

$$\frac{L \times f_{SW}}{R_S} = 200$$

where

L is the buck regulator inductor in henries.

R_S is the sense resistor in ohms.

f_{sw} is the buck-regulator switching frequency in hertz.

Power-Good Outputs and Filter Delays

Each buck controller has an independent power-good comparator monitoring the feedback voltage at the FBx pins and indicating whether the output voltage has fallen below a specified power-good threshold. This threshold has a typical value of 93% of the regulated output voltage. The power-good indicator is available as an open-drain output at the PGx pins. An internal 50-kΩ pullup resistor to Sx2 is available, or use of an external resistor is possible. Shutdown of a buck controller causes an internal pulldown of the power-good indicator. Connecting the pullup resistor to a rail other than the output of that particular buck channel causes a constant current flow through the resistor when the buck controller is in the powered-down state.

In order to avoid triggering the power-good indicators due to noise or fast transients on the output voltage, the device uses an internal delay circuit for de-glitching. Similarly, when the output voltage returns to its set value after a long negative transient, assertion of the power-good indicator (release of the open-drain pin) occurs after the same delay. Use of this delay can pause the reset of circuits powered from the buck regulator rail. Program the duration of the delay of by using a suitable capacitor at the DLYAB pin according to the equation:

$$\frac{t_{DELAY}}{C_{DLYAB}} = \frac{1\,ms}{1\,nF}$$

When the DLYAB pin is open, the delay setting is for a default value of 20 µs typical. The power-good delay timing is common to both the buck rails, but the power-good comparators and indicators function independently.

Light-Load PFM Mode

An external clock or a high level on the SYNC pin results in forced continuous-mode operation of the bucks. An open or low on the SYNC pin allows the buck controllers to operate in discontinuous mode at light loads by turning off the low-side MOSFET on detection of a zero-crossing in the inductor current.

In discontinuous mode, as the load decreases, the duration when both the high-side and low-side MOSFETs turn off increases (deep discontinuous mode). In case the duration exceeds 60% of the clock period and VBAT > 8 V, the buck controller switches to a low-power operation mode. The design ensures that this typically occurs at 1% of the set full-load current if the inductor and the sense resistor have been chosen appropriately as recommended in the *Slope Compensation* section.

In low-power PFM mode, the buck monitors the FBx voltage and compares it with the 0.8-V internal reference. Whenever the FBx value falls below the reference, the high-side MOSFET turns on for a pulse duration inversely proportional to the difference – Sx2. At the end of this on-time, the high-side MOSFET turns off and the current in the inductor decays until it becomes zero. The low-side MOSFET does not turn on. The next pulse occurs the next time FBx falls below the reference value. This results in a constant volt-second t_{on} hysteretic operation with a total device quiescent current consumption of 30 µA when a single buck channel is active and 35 µA when both channels are active.

As the load increases, the pulses become more and more frequent and move closer to each other until the current in the inductor becomes continuous. At this point, the buck controller returns to normal fixed-frequency current-mode control. Another criterion to exit the low-power mode is when VIN falls low enough to require higher than 80% duty cycle of the high-side MOSFET.

The TPS43350-Q1 and TPS43351-Q1 can support the full current load during low-power mode until the transition to normal mode takes place. The design ensures that exit of the low-power mode occurs at 10% (typical) of full-load current if the selection of inductor and sense resistor is as recommended. Moreover, there is always a hysteresis between the entry and exit thresholds to avoid oscillating between the two modes.

In the event that both buck controllers are active, low-power mode is only possible when both buck controllers have light loads that are low enough for low-power-mode entry.

Frequency-Hopping Spread Spectrum (TPS43351-Q1 Only)

The TPS43351-Q1 features a frequency-hopping pseudo-random spectrum spreading architecture. On this device, whenever the SYNC pin is high, the internal oscillator frequency varies from one cycle to the next within a band of ±5% around the value programmed by the resistor at the RT pin. The implementation uses a linear feedback shift register that changes the frequency of the internal oscillator based on a digital code. The shift register is long enough to make the hops pseudo-random in nature and is designed in such a way that the frequency shifts only by one step at each cycle to avoid large jumps in the buck switching frequencies.

Table 1. Frequency Hopping Control

SYNC TERMINAL	FREQUENCY SPREAD SPECTRUM (FSS)	COMMENTS
External clock	Not active	Device in forced continuous mode, internal PLL locks into external clock between 150 kHz and 600 kHz.
Low or open	Not active	Device can enter discontinuous mode. Automatic LPM entry and exit, depending on load conditions
High	TPS43350-Q1: FSS not active	Device in forced continuous mode
	TPS43351-Q1: FSS active	

Table 2. Mode of Operation

ENABLE AND INHIBIT PINS			BUCK CONTROLLER STATUS	DEVICE STATUS	QUIESCENT CURRENT
ENA	ENB	SYNC			
Low	Low	X	Shutdown	Shutdown	Approximately 4 µA
Low	High	Low	BuckB running	BuckB: LPM enabled	Approximately 30 µA (light loads)
		High		BuckB: LPM inhibited	mA range
High	Low	Low	BuckA running	BuckA: LPM enabled	Approximately 30 µA (light loads)
		High		BuckA: LPM inhibited	mA range
High	High	Low	BuckA and BuckB running	BuckA and BuckB: LPM enabled	Approximately 35 µA (light loads)
		High		BuckA and BuckB: LPM inhibited	mA range

Gate-Driver Supply (VREG, EXTSUP)

The gate-driver supplies of the buck and boost controllers are from an internal linear regulator whose output (5.8 V typical) is on the VREG pin and requires decoupling with a ceramic capacitor in the range of 3.3 µF to 10 µF. This pin has internal current-limit protection; do not use it to power any other circuits.

VIN powers the VREG linear regulator by default when the EXTSUP voltage is lower than 4.6 V (typical). In case VIN expected to go to high levels, there can be excessive power dissipation in this regulator, especially at high switching frequencies and when using large external MOSFETs. In this case, it is advantageous to power this regulator from the EXTSUP pin, which can be connected to a supply lower than V_{IN} but high enough to provide the gate drive. When the voltage on EXTSUP is greater than 4.6 V, the linear regulator automatically switches to EXTSUP as its input, to provide this advantage. Efficiency improvements are possible when using one of the switching regulator rails from the TPS4335x-Q1 or any other voltage available in the system to power EXTSUP. The maximum voltage for application to EXTSUP is 9 V.

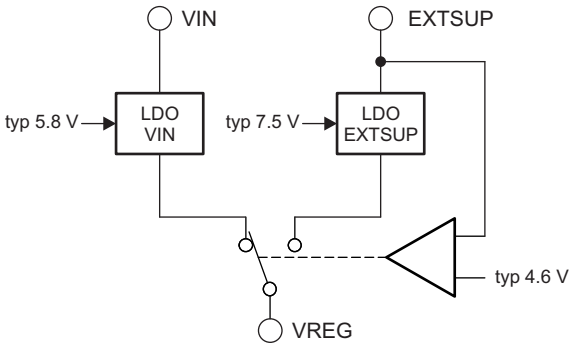


Figure 16. Internal Gate-Driver Supply

Using a voltage above 5.8 V (sourced by VIN) for EXTSUP is advantageous, as it provides a large gate drive and hence better on-resistance of the external MOSFETs. When using EXTSUP, always keep the buck rail supplying EXTSUP enabled. Alternatively, if it is necessary to switch off the buck rail supplying EXTSUP, place a diode between the buck rail and EXTSUP. During low-power mode, the EXTSUP functionality is not available. The internal regulator operates as a shunt regulator powered from VIN and has a typical value of 7.5 V. Current-limit protection for VREG is available in low-power mode as well. If EXTSUP is unused, leave the pin open without a capacitor installed.

External P-Channel Drive (GC2) and Reverse-Battery Protection

The TPS4335x-Q1 includes a gate driver for an external P-channel MOSFET which can be connected across the reverse-battery diode. This is useful to reduce power losses and the voltage drop over a typical diode. The gate driver provides a swing of 6 V typical below the V_{IN} voltage in order to drive a P-channel MOSFET.

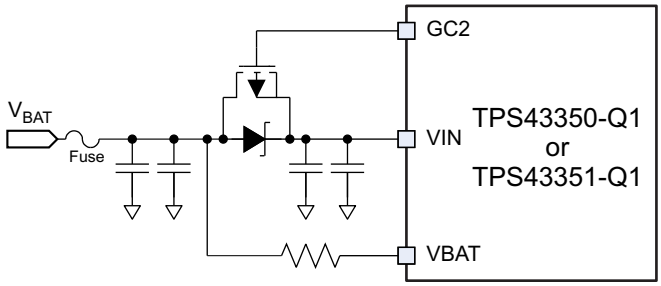


Figure 17. Reverse-Battery Protection Option

Undervoltage Lockout and Overvoltage Protection

The TPS4335x-Q1 starts up at a V_{IN} voltage of 6.5 V (minimum), required for the internal supply (VREG). Once it has started up, the device operates down to a V_{IN} voltage of 3.6 V; below this voltage level, the undervoltage lockout disables the device. Note: if V_{IN} drops, V_{REG} drops as well; hence, the gate-drive voltage decreases, whereas the digital logic is fully functional. A voltage of 46 V at V_{IN} triggers the overvoltage comparator, which shuts down the device. In order to prevent transient spikes from shutting down the device, under- and overvoltage protection have filter times of 5 µs (typical).

When the voltages return to the normal operating region, the enabled switching regulators start including a new soft-start ramp for the buck regulators.

Thermal Protection

The TPS4335x-Q1 protects itself from overheating using an internal thermal shutdown circuit. If the die temperature exceeds the thermal shutdown threshold of 165ºC due to excessive power dissipation (for example, due to fault conditions such as a short circuit at the gate drivers or VREG), the controllers turn off and then restart when the temperature has fallen by 15ºC.

APPLICATION INFORMATION

The following example illustrates the design process and component selection for the TPS43350-Q1. Table 3 lists the design-goal parameters.

Table 3. Application Example

PARAMETER	V_{BuckA}	V_{BuckB}
Input voltage	V_{IN} = 6 V to 30 V 12 V - typical	V_{IN} = 6 V to 30 V 12 V - typical
Output voltage, V_{OUTx}	5 V	3.3 V
Maximum output current, I_{OUTx}	3 A	2 A
Load step output tolerance, $\Delta V_{OUT} + \Delta V_{OUT(Ripple)}$	±0.2 V	±0.12 V
Current output load step, ΔI_{OUTx}	0.1 A to 3 A	0.1 A to 2 A
Converter switching frequency, f_{SW}	400 kHz	400 kHz

This is a starting point, and theoretical representation of the values to be used for the application; improving the performance of the device may require further optimization of the derived components.

BuckA Component Selection

Minimum ON Time, $t_{ON\ min}$

$$t_{ON\,min} = \frac{V_{OUTA}}{V_{IN\,max} \times f_{SW}} = \frac{5\ V}{30\ V \times 400\ kHz} = 416\ ns$$

This is higher than the minimum on-time specified (100 ns typical). Hence, the minimum duty cycle is achievable at this frequency.

Current-Sense Resistor R_{SENSE}

Based on the typical characteristics for V_{SENSE} limit with V_{IN} versus duty cycle, the sense limit is approximately 65 mV (at V_{IN} = 12 V and duty cycle of 5 V / 12 V = 0.416). Allowing for tolerances and ripple currents, choose V_{SENSE} with a maximum of 50 mV.

$$R_{SENSE} = \frac{50\ mV}{3\ A} = 17\ m\Omega$$

Select 15 mΩ.

Inductor Selection L

As explained in the description of the buck controllers, for optimal slope compensation and loop response, the inductor should be chosen such that:

$$L = K_{FLR} \times \frac{R_{SENSE}}{f_{SW}} = 200 \times \frac{15\ m\Omega}{400\ kHz} = 7.5\ \mu H$$

K_{FLR} = Coil selection constant = 200

Choose a standard value of 8.2 µH. For the buck converter, the inductor saturation currents and core should be chosen to sustain the maximum currents.

Inductor Ripple Current I_{RIPPLE}

At nominal input voltage of 12 V, this inductor value causes a ripple current of 30% of $I_{O\ max}$ ≈ 1 A.

Output Capacitor C_{OUTA}

Select an output capacitance C_{OUTA} of 100 µF with low ESR in the range of 10 mΩ. This gives $\Delta V_{O(Ripple)}$ ≈ 15 mV and ΔV drop of ≈ 180 mV during a load step, which does not trigger the power-good comparator and is within the required limits.

$$C_{OUTA} \approx \frac{2 \times \Delta I_{OUTA}}{f_{SW} \times \Delta V_{OUTA}} = \frac{2 \times 2.9\ A}{400\ kHz \times 0.2\ V} = 72.5\ \mu F$$

$$V_{OUTA(Ripple)} = \frac{I_{OUTA(Ripple)}}{8 \times f_{SW} \times C_{OUTA}} + I_{OUTA(Ripple)} \times ESR = \frac{1\ A}{8 \times 400\ kHz \times 100\ \mu F} + 1\ A \times 10\ m\Omega = 13.1\ mV$$

$$\Delta V_{OUTA} = \frac{\Delta I_{OUTA}}{4 \times f_C \times C_{OUTA}} + \Delta I_{OUTA} \times ESR = \frac{2.9\ A}{4 \times 50\ kHz \times 100\ \mu F} + 2.9\ A \times 10\ m\Omega = 174\ mV$$

Bandwidth of Buck Converter f_C

Use the following guidelines to set frequency poles, zeroes and crossover values for a tradeoff between stability and transient response.

- Crossover frequency f_C between f_{SW} / 6 and f_{SW} / 10. Assume f_C = 50 kHz.
- Select the zero $f_z \approx f_C$ / 10.
- Make the second pole $f_{P2} \approx f_{SW}$ / 2.

Selection of Components for Type II Compensation

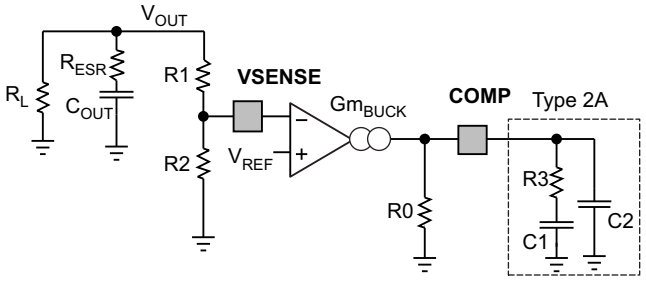


Figure 18. Buck Compensation Components

$$R3 = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUTx}}{Gm_{BUCK} \times K_{CFB} \times V_{REF}} = \frac{2\pi \times 50\ kHz \times 5\ V \times 100\mu F}{Gm_{BUCK} \times K_{CFB} \times V_{REF}} = 23.57\ k\Omega$$

Use the standard value of R3 = 24 kΩ,

Where V_{OUT} = 5 V, C_{OUTx} = 100 µF, Gm_{BUCK} = 1 mS, V_{REF} = 0.8 V

K_{CFB} = 0.125 / R_{SENSE} = 8.33 S (0.125 is an internal constant)

$$C1 = \frac{10}{2\pi \times R3 \times f_C} = \frac{10}{2\pi \times 24\ k\Omega \times 50\ kHz} = 1.33\ nF$$

Use the standard value of 1.5 nF.

$$C2 = \frac{C1}{2\pi \times R3 \times C1\left(\frac{f_{SW}}{2}\right) - 1} = \frac{1.5\ nF}{2\pi \times 24k\Omega \times 1.5\ nF\left(\frac{400\ kHz}{2}\right) - 1} = 33\ pF$$

The resulting bandwidth of buck converter, f_C

$$f_C = \frac{Gm_{BUCK} \times R3 \times K_{CFB}}{2\pi \times C_{OUTx}} \times \frac{V_{REF}}{V_{OUT}}$$

$$f_C = \frac{1mS \times 24\ k\Omega \times 8.33\ S \times 0.8\ V}{2\pi \times 100\ \mu F \times 5\ V} = 50.9\ kHz$$

This is close to the target bandwidth of 50 kHz.

The resulting zero frequency f_{Z1}

$$f_{Z1} = \frac{1}{2\pi \times R3 \times C1} = \frac{1}{2\pi \times 24\ k\Omega \times 1.5\ nF} = 4.42\ kHz$$

This is close to the f_C / 10 guideline of 5 kHz.

The second pole frequency f_{P2}

$$f_{P2} = \frac{1}{2\pi \times R3 \times C2} = \frac{1}{2\pi \times 24\ k\Omega \times 33\ pF} = 201\ kHz$$

This is close to the f_{SW} / 2 guideline of 200 kHz. Hence, the design satisfies all requirements for a good loop.

Resistor Divider Selection for Setting V_{OUTA} Voltage

$$\beta = \frac{V_{REF}}{V_{OUTA}} = \frac{0.8\ V}{5\ V} = 0.16$$

Choose the divider current through R1 and R2 to be 50 µA. Then

$$R1 + R2 = \frac{5\ V}{50\ \mu A} = 66\ k\Omega$$

and

$$\frac{R2}{R1 + R2} = 0.16$$

Therefore, R2 = 16 kΩ and R1 = 84 kΩ.

BuckB Component Selection

Using the same method as for V_{BuckA} produces the following parameters and components.

$$t_{ON\,min} = \frac{V_{OUTB}}{V_{IN\,max} \times f_{SW}} = \frac{5\ V}{30\ V \times 400\ kHz} = 416\ ns$$

This is higher than the minimum duty cycle specified (100 ns typical).

$$R_{SENSE} = \frac{60\ mV}{2\ A} = 30\ m\Omega$$

$$L = 200 \times \frac{30\ m\Omega}{400\ kHz} = 15\ \mu H$$

ΔI_{ripple} current ≈ 0.4 A (approximately 20% of $I_{OUT\ max}$)

Select an output capacitance C_O of 100 µF with low ESR in the range of 10 mΩ. Assume f_C = 50 kHz.

$$C_{OUTB} \approx \frac{2 \times \Delta I_{OUTB}}{f_{SW} \times \Delta V_{OUTB}} = \frac{2 \times 1.9\ A}{400\ kHz \times 0.12\ V} = 46\ \mu F$$

$$V_{OUTB(Ripple)} = \frac{I_{OUTB(Ripple)}}{8 \times f_{SW} \times C_{OUTB}} + I_{OUTB(Ripple)} \times ESR = \frac{0.4\ A}{8 \times 400\ kHz \times 100\ \mu F} + 0.4\ A \times 10\ m\Omega = 5.3\ mV$$

$$\Delta V_{OUTB} = \frac{\Delta I_{OUTB}}{4 \times f_C \times C_{OUTB}} + \Delta I_{OUTB} \times ESR = \frac{1.9\ A}{4 \times 50\ kHz \times 100\ \mu F} + 1.9\ A \times 10\ m\Omega = 114\ mV$$

$$R3 = \frac{2\pi \times f_C \times V_{OUTB} \times C_{OUTB}}{Gm_{BUCK} \times K_{CFB} \times V_{REF}}$$

$$= \frac{2\pi \times 50\ kHz \times 3.3\ V \times 100\ \mu F}{1\ mS \times 4.16\ S \times 0.8\ V} = 31\ k\Omega$$

Use the standard value of R3 = 30 kΩ.

$$C1 = \frac{10}{2\pi \times R3 \times f_C} = \frac{10}{2\pi \times 30\ k\Omega \times 50\ kHz} = 1.1\ nF$$

$$C2 = \frac{C1}{2\pi \times R3 \times C1 \times \left(\frac{f_{SW}}{2}\right) - 1}$$

$$= \frac{1.1\,nF}{2\pi \times 30\,k\Omega \times 1.1\,nF \times \left(\frac{400\,kHz}{2}\right) - 1} = 27\,pF$$

$$f_C = \frac{Gm_{BUCK} \times R3 \times K_{CFB}}{2\pi \times C_{OUTB}} \times \frac{V_{REF}}{V_{OUTB}}$$

$$= \frac{1\,mS \times 30\,k\Omega \times 4.16\,S \times 0.8\,V}{2\pi \times 100\,\mu F \times 3.3\,V} = 48\,kHz$$

This is close to the target bandwidth of 50 kHz.

The resulting zero frequency f_{Z1}

$$f_{Z1} = \frac{1}{2\pi \times R3 \times C1} = \frac{1}{2\pi \times 30\,k\Omega \times 1.1\,nF} = 4.8\,kHz$$

This is close to the f_C guideline of 5 kHz.

The second pole frequency f_{P2}

$$f_{P2} = \frac{1}{2\pi \times R3 \times C2} = \frac{1}{2\pi \times 30\,k\Omega \times 27\,pF} = 196\,kHz$$

This is close to the f_{SW} / 2 guideline of 200 kHz.

Hence, the design satisfies all requirements for a good loop.

Resistor Divider Selection for Setting V_{OUT} Voltage

$$\beta = \frac{V_{REF}}{V_{OUT}} = \frac{0.8\,V}{3.3\,V} = 0.242$$

Choose the divider current through R1 and R2 to be 50 µA. Then

$$R1 + R2 = \frac{3.3\,V}{50\,\mu A} = 66\,k\Omega$$

and

$$\frac{R2}{R1 + R2} = 0.242$$

Therefore, R2 = 16 kΩ and R1 = 50 kΩ.

BuckX High-Side and Low-Side N-Channel MOSFETs

An internal supply, which is 5.8 V typical under normal operating conditions, provides the gate-drive supply for these MOSFETs. The output is a totem pole allowing full voltage drive of V_{REG} to the gate with peak output current of 1.5 A. The reference for the high-side MOSFET is a floating node at the phase terminal (PHx), and the reference for the low-side MOSFET is the power-ground (PGx) terminal. For a particular application, select these MOSFETs with consideration for the following parameters: $r_{DS(on)}$, gate charge Qg, drain-to-source breakdown voltage BVDSS, maximum dc current IDC(max), and thermal resistance for the package.

The times t_r and t_f denote the rising and falling times of the switching node and have a relationship to the gate-driver strength of the TPS43350x-Q1 and gate Miller capacitance of the MOSFET. The first term denotes the conduction losses, which are minimal when the on-resistance of the MOSFET is low. The second term denotes the transition losses, which arise due to the full application of the input voltage across the drain-source of the MOSFET as it turns on or off. They are lower at low currents and when the switching time is low.

$$P_{BuckTOPFET} = (I_{OUT})^2 \times r_{DS(on)}(1+TC)\times D + \left(\frac{V_{IN}\times I_{OUT}}{2}\right)\times (t_r + t_f)\times f_{SW}$$

$$P_{BuckLOWERFET} = (I_{OUT})^2 \times r_{DS(on)}(1+TC)\times (1-D) + V_F \times I_{OUT} \times (2\times t_d)\times f_{SW}$$

In addition, during dead time t_d when both the MOSFETs are off, the body diode of the low-side MOSFET conducts, increasing the losses. The second term in the foregoing equation denotes this. Using external Schottky diodes in parallel to the low-side MOSFETs of the buck converters helps to reduce this loss.

Note: The $r_{DS(on)}$ has a positive temperature coefficient, and TC term for $r_{DS(on)}$ accounts for that fact. TC = d × delta T[°C]. The temperature coefficient d is available as a normalized value from MOSFET data sheets and can be assumed to be 0.005 / °C as a starting value.

Schematic

The following section summarizes the previously calculated example and gives schematic and component proposals. Table 3.

Table 4. Application Example

PARAMETER	V_{BuckA}	V_{BuckB}
Input voltage	V_{IN} = 6 V to 30 V 12 V - typical	V_{IN} = 6 V to 30 V 12 V - typical
Output voltage, V_{OUTx}	5 V	3.3 V
Maximum output current, I_O	3 A	2 A
Load step output tolerance, $\Delta V_{OUT} + \Delta V_{OUT(Ripple)}$	±0.2 V	±0.12 V
Current output load step, ΔI_{OUTx}	0.1 A to 3 A	0.1 A to 2 A
Converter switching frequency, f_{SW}	400 kHz	400 kHz

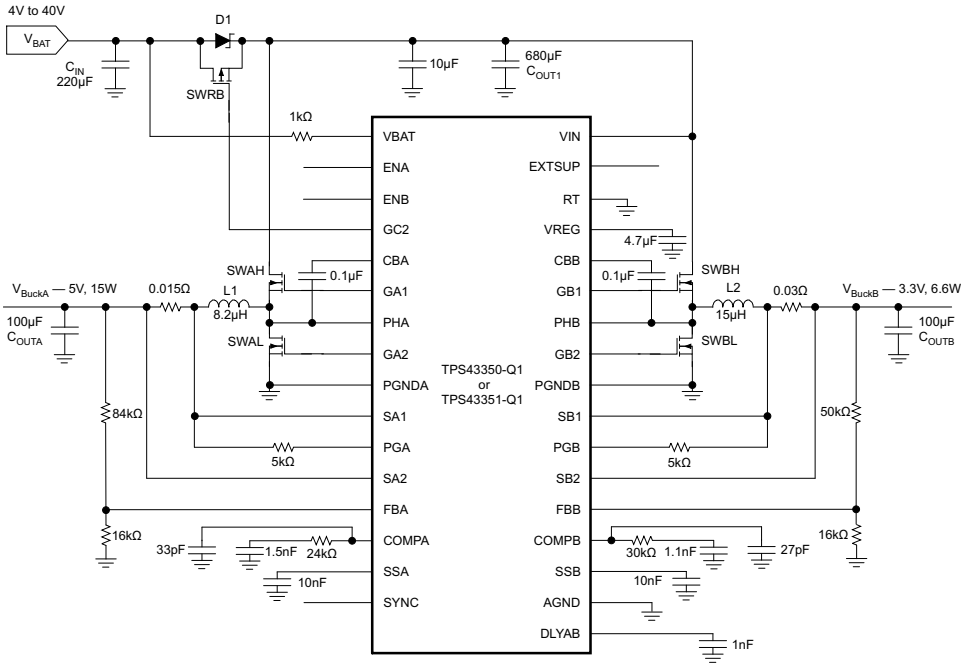


Figure 19. Simplified Application Schematic Example

Table 5. Application Example – Component Proposals

NAME	COMPONENT PROPOSAL	VALUE
L1	MSS1278T-822ML (Coilcraft)	8.2 µH
L2	MSS1278T-153ML (Coilcraft)	15 µH
D1	SK103 (Micro Commercial Components)	
SWRB	IRF7416 (International Rectifier)	
SWAH, SWAL, SWBH, SWBL	Si4840DY-T1-E3 (Vishay)	
C_{OUTA}, C_{OUTB}	ECASD91A107M010K00 (Murata)	100 µF
C_{IN}	EEEFK1V331P (Panasonic)	330 µF

Power Dissipation Derating Profile, 38-Pin HTTSOP PowerPAD Package

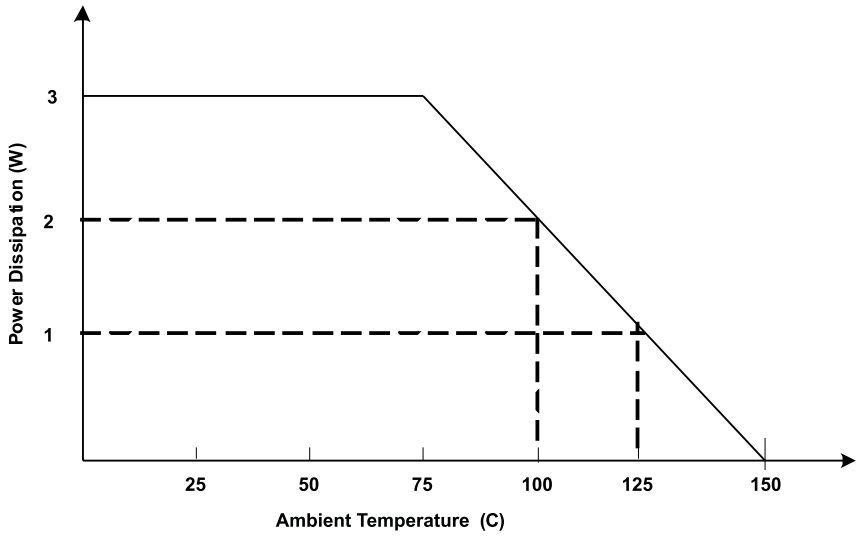


Figure 20. Power Dissipation Derating Profile Based on High-K JEDEC PCB

PCB Layout Guidelines

Grounding and PCB Circuit Layout Considerations

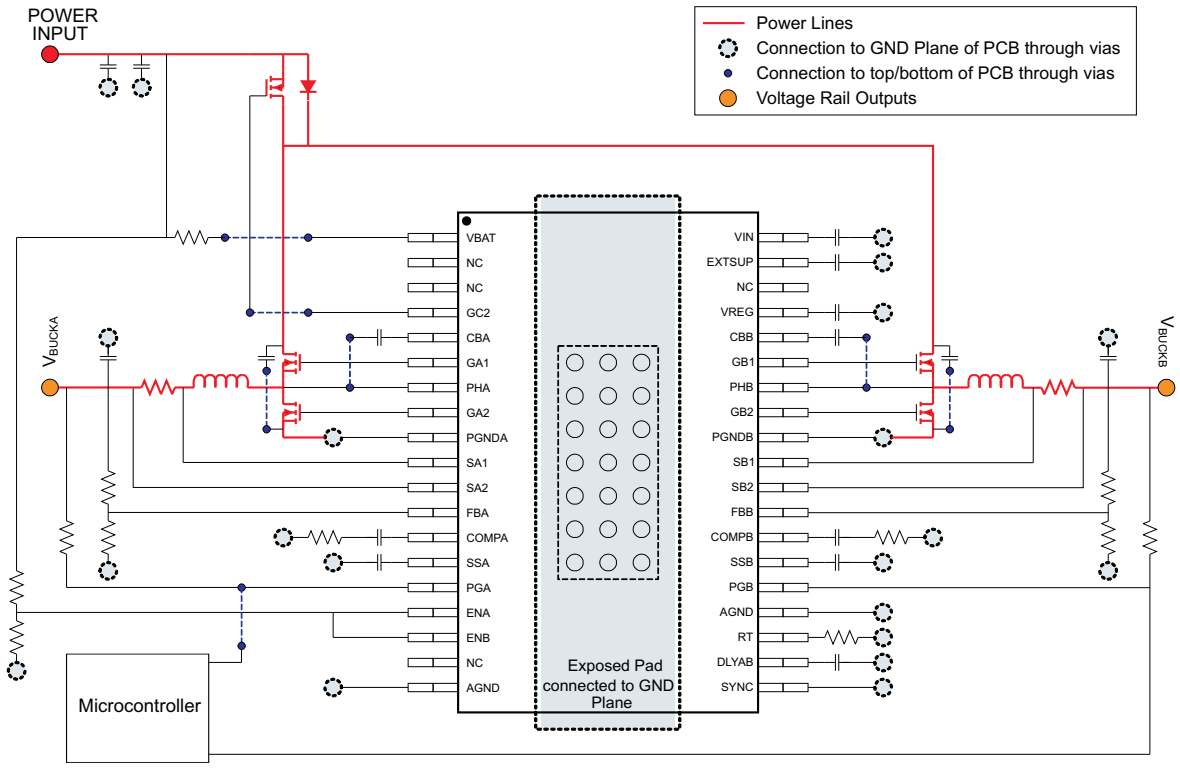
Buck Converter

1. Connect the drain of SWAH and SWBH MOSFETs together with the positive terminal of the input capacitor C_{OUTA}. The trace length between these terminals should be short.
2. Connect a local decoupling capacitor between the drain of SWxH and source of SWxL.
3. The Kelvin-current sensing for the shunt resistor should have traces with minimum spacing, routed in parallel with each other. Place any filtering capacitors for noise near the IC pins.
4. The resistor divider for sensing output voltage connects between the positive terminal of the respective output capacitor and C_{OUTA} or C_{OUTB} and the IC signal ground. Do not locate these components and their traces near any switching nodes or high-current traces.

Other Considerations

1. Short PGNDx and AGND to the thermal pad. Use a star ground configuration if connecting to a nonground plane system. Use tie-ins for the EXTSUP capacitor, compensation-network ground, and voltage-sense feedback-ground networks to this star ground.
2. Connect a compensation network between the compensation pins and IC signal ground. Connect the oscillator resistor (frequency setting) between the RT pin and IC signal ground. Do not locate these sensitive circuits near the dv/dt nodes; these include the gate-drive outputs and phase pins.
3. Reduce the surface area of the high-current-carrying loops to a minimum by ensuring optimal component placement. Ensure the bypass capacitors are located as close as possible to their respective power and ground pins.

PCB Layout


POWER INPUT
Power Lines
Connection to GND Plane of PCB through vias
Connection to top/bottom of PCB through vias
Voltage Rail Outputs
VBUCKA
VBUCKB
VBAT
NC
NC
GC2
CBA
GA1
PHA
GA2
PGNDA
SA1
SA2
FBA
COMPA
SSA
PGA
ENA
ENB
NC
AGND
VIN
EXTSUP
NC
VREG
CBB
GB1
PHB
GB2
PGNDB
SB1
SB2
FBB
COMPB
SSB
PGB
AGND
RT
DLYAB
SYNC
Exposed Pad connected to GND Plane
Microcontroller

REVISION HISTORY

Changes from Revision C (September 2012) to Revision D **Page**

- Deleted Ordering Information table 2
- Revised Absolute Maximum Ratings table 2
- Changed pinout diagram 7

Changes from Revision B (June 2011) to Revision C **Page**

- Corrected AEC specification in ESD ratings 2
- Multiple changes throughout Electrical Characteristics table 4
- Changed input-voltage value for pins ENA and ENB 7
- Added a sentence to EXTSUP pin description 7
- Changed upper threshold voltage for ENx pins to 1.7 V 12
- Text deletion from second paragraph of Light-Load PFM Mode section 14
- Changed value of gate-driver decoupling capacitor 15
- Added upper voltage limit for EXTSUP pin 15
- Replaced paragraphs following the figure at end of Gate-Driver Supply section 16
- Clarified parameter definition in Application Example table 17
- Added equations for Output Capacitor C_{OUTA} section 18
- Added equations for BuckB Component Selection sectiion 20
- Changed peak output current in BuckX High-Side and Low-Side N-Channel MOSFETs section 22
- Clarified parameter description in Application Example table 23
- Revised diagram of Simplified Application Schematic Example 23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS43350QDAPRQ1	ACTIVE	HTSSOP	DAP	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS43350Q1	Samples
TPS43351QDAPRQ1	ACTIVE	HTSSOP	DAP	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS43351Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

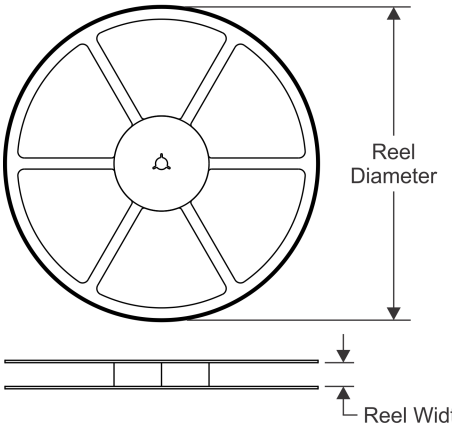
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

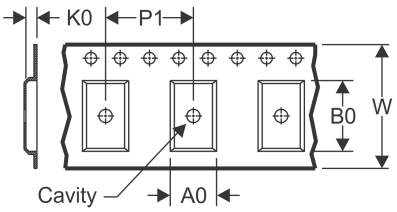
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

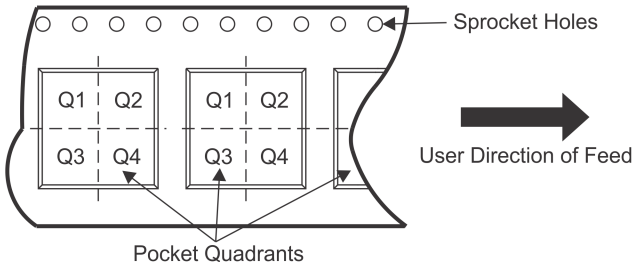


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

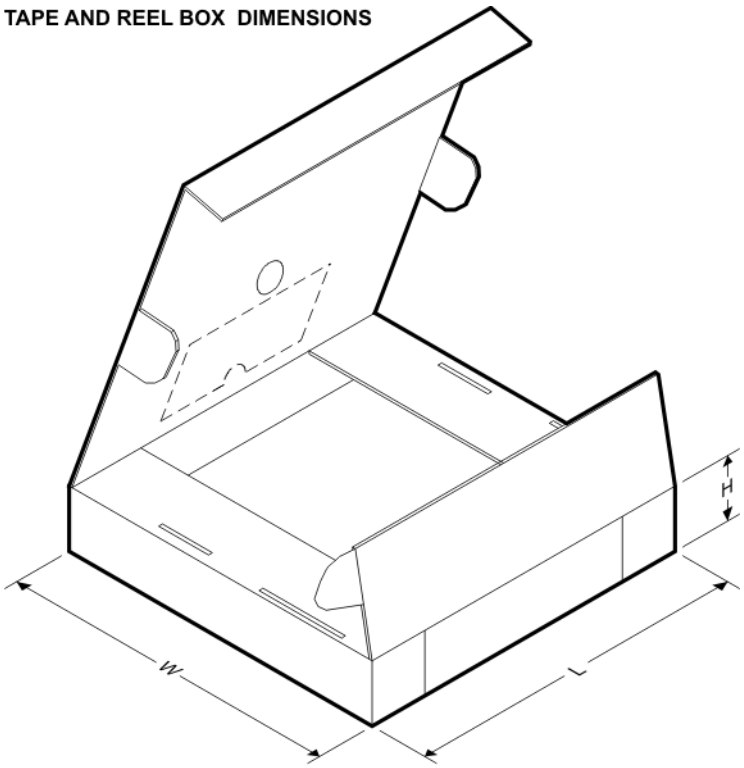
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS43350QDAPRQ1	HTSSOP	DAP	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
TPS43351QDAPRQ1	HTSSOP	DAP	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

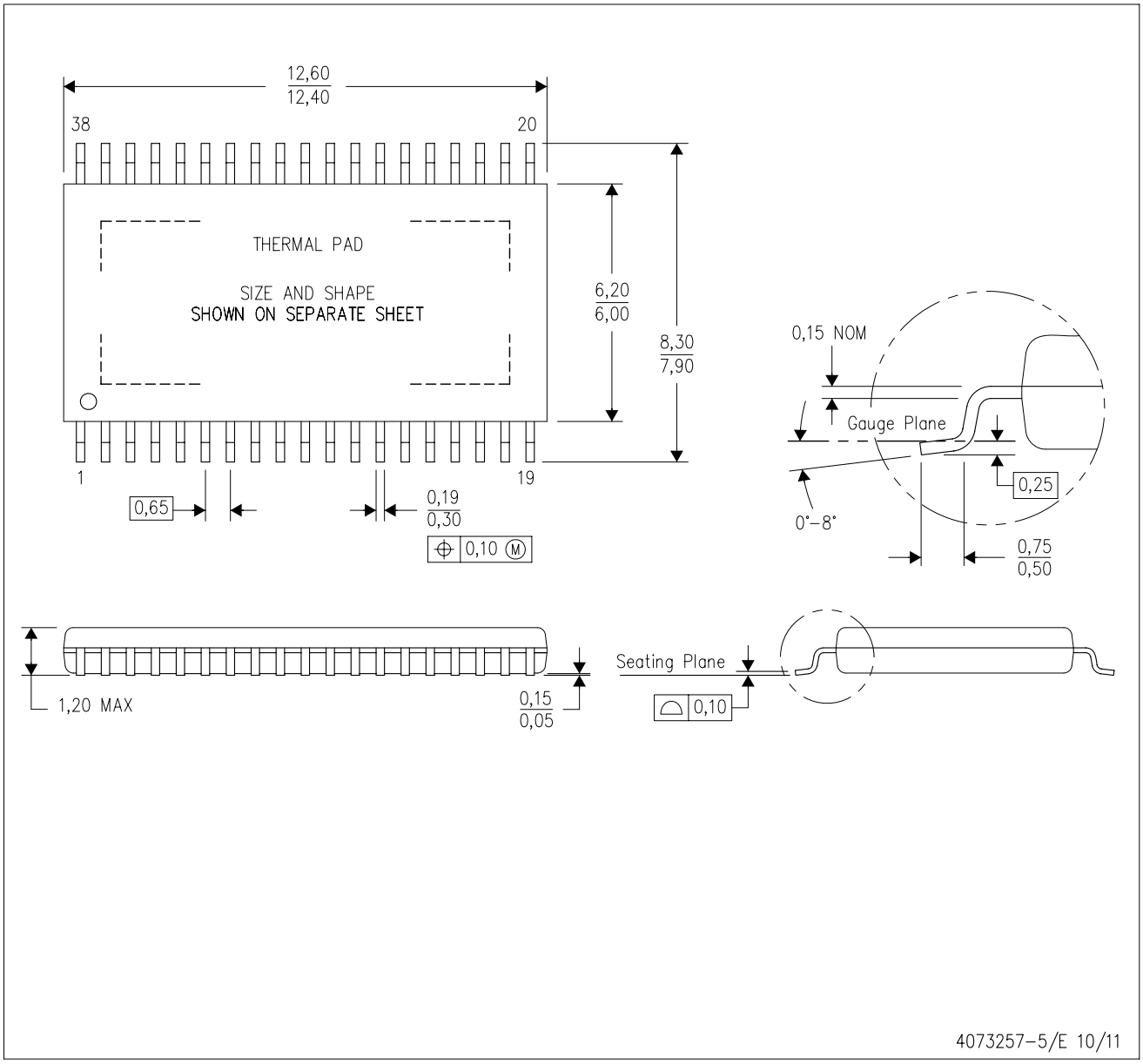
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS43350QDAPRQ1	HTSSOP	DAP	38	2000	367.0	367.0	45.0
TPS43351QDAPRQ1	HTSSOP	DAP	38	2000	367.0	367.0	45.0

DAP (R–PDSO–G38) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153 Variation DDT–1.

PowerPAD is a trademark of Texas Instruments.

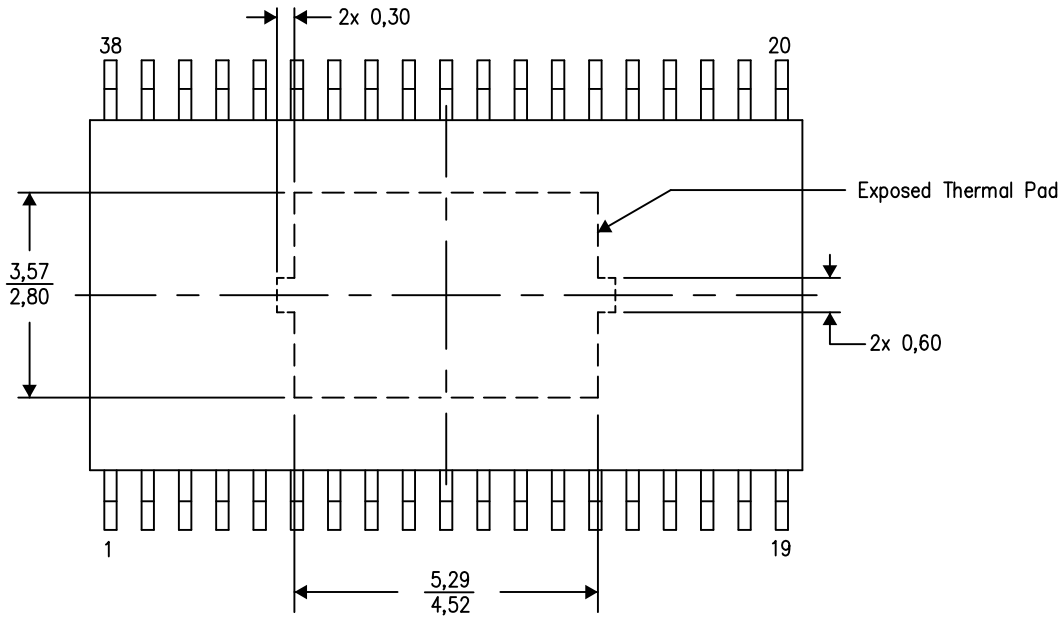
DAP (R–PDSO–G38) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206319–9/L 07/13

NOTE: All linear dimensions are in millimeters

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