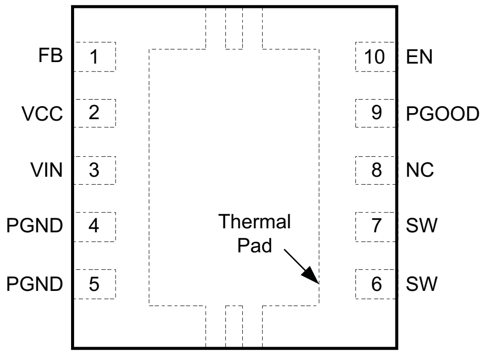
5-V Input or 3.3-V Input, 3-A, Fully Integrated Converter

Check for Samples: TPS51313

FEATURES

- **Input Voltage VIN Range : 3.1 V to 5.5 V**
- **Bias Voltage VCC Range: 3.1 V to 5.5 V**
- **Output Voltage Range: 0.6 V to 3.3 V**
- **0.6-V, 1% Voltage Reference Accuracy**
- **Switching Frequency: 1 MHz**
- **No External Compensation is Required**
- **Fixed Voltage Servo Soft-Start Function**
- **Thermal Shutdown**



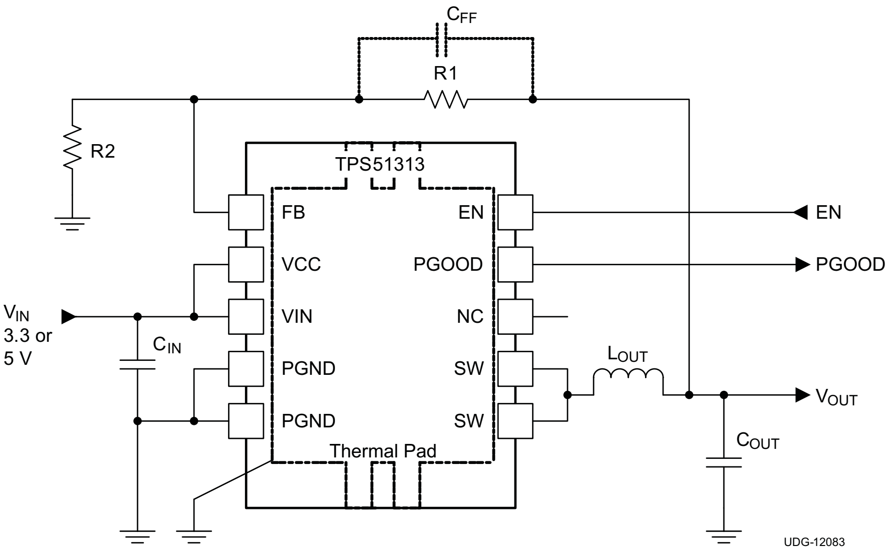
APPLICATIONS

- **Discrete Graphics PCIe® PEX Rail**
- **Low-Voltage Point-of-Load (POL) Rails**

DESCRIPTION

The TPS51313 is an easy-to-use, fully integrated, synchronous buck converter for low voltage point-of-load applications. It is designed to meet the NVIDIA™ OpenVreg Type 0 specifications, including the package and footprint requirement. It supports 3-A (maximum) of dc output current at output voltages from 0.6 V to 3.3 V. The D-CAP2™ mode adaptive, constant on-time control with 1-MHz switching frequency allows a small footprint when designed using all ceramic output capacitors and offers a low external component count. The device also features auto-skip function at light load condition, pre-biased start-up and internally fixed soft-start time. When the device is disabled, the output capacitor is discharged through internal resistor. The TPS51313 is available in a 3 mm x 3 mm, 10-pin DRC package (Green RoHS compliant and Pb free) and is specified between –10°C and 85°C.

SIMPLIFIED APPLICATION



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE DEVICE NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ECO PLAN
–10°C to 85°C	Plastic SON (DRC)	TPS51313DRCR	10	Tape and reel	3000	Green (RoHS and no Pb/Br)
		TPS51313DRCT		Mini reel	250	

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE		UNIT
		MIN	MAX	
Input voltage range(2)	VIN, VCC	–0.3	6.0	V
	SW	–2.0	6.0	
	SW (transient 20nsec)	-3.0	8.5	
	EN	–0.3	6.0	
	FB	–1	3.6	
Output voltage range(2)	PGOOD	–0.3	6.0	V
Junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS51313	UNITS
		DRC (10-PIN)	
θ_{JA}	Junction-to-ambient thermal resistance	42.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	53.9	
θ_{JB}	Junction-to-board thermal resistance	18.1	
ψ_{JT}	Junction-to-top characterization parameter	1.1	
ψ_{JB}	Junction-to-board characterization parameter	18.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	6.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Input voltage range	VIN, VCC	–0.1	5.5	V
	SW	–0.1	5.5	
	EN	–0.1	5.5	
	FB	–0.1	3.5	
Output voltage range	PGOOD	–0.1	5.5	V
Operating free-air temperature, T_A		–10	85	°C

ELECTRICAL CHARACTERISTICS

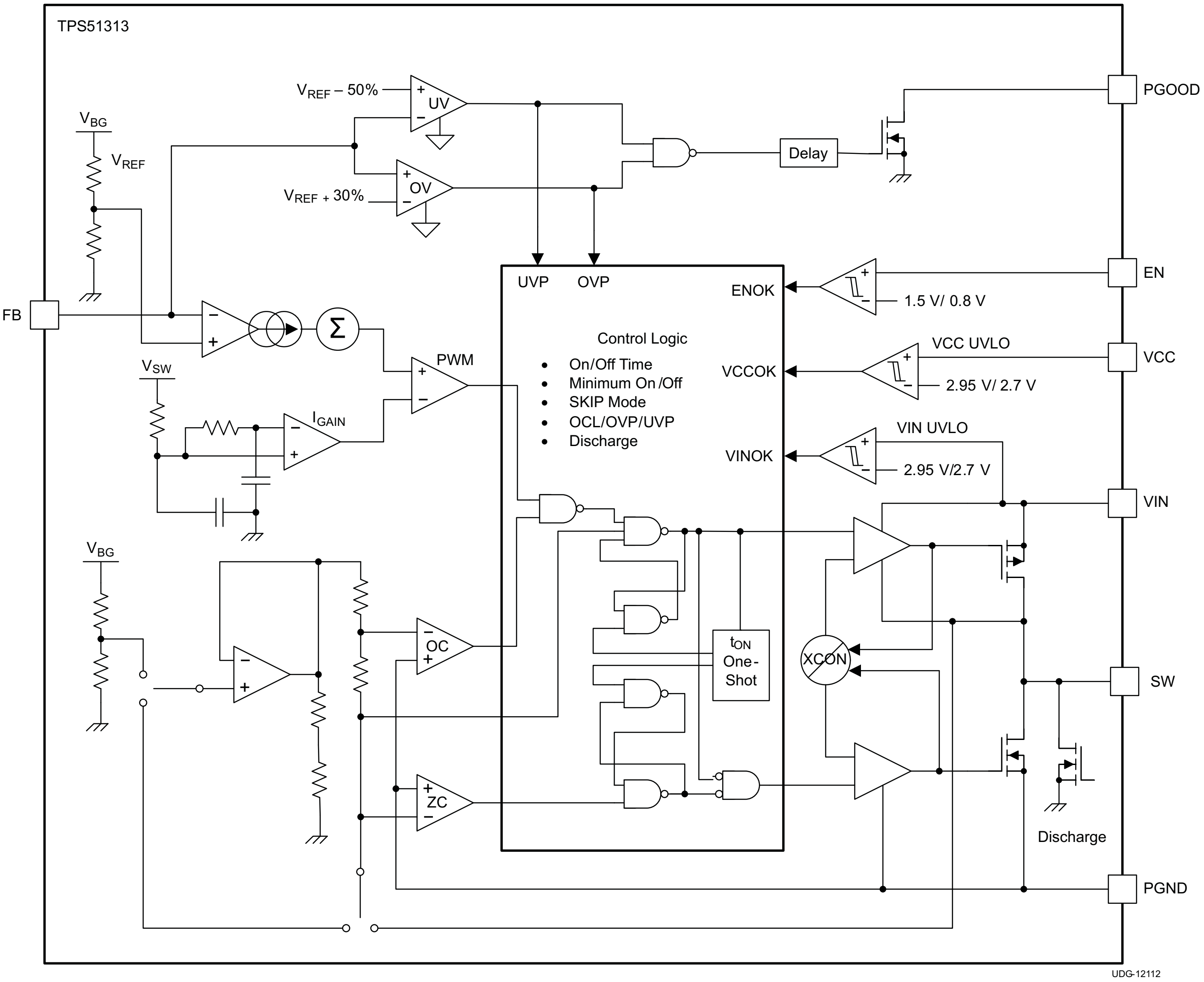
Over operating free-air temperature range, V_{IN} = 5 V, V_{CC} = 5 V, V_{EN} = 3.3 V (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Supply voltage		3.1		5.5	V
V_{CC}	Supply voltage		3.1		5.5	V
SUPPLY CURRENT						
I_{IN}	Input voltage supply current	EN = High			100	μA
I_{SD}	Input voltage shutdown current	EN = Low			12	μA
$I_{VCC(in)}$	VCC supply current	EN = High		700		μA
$I_{VCC(sd)}$	VCC shutdown current	EN = Low, T_A = 25°C			20	μA
VFB REFERNCE VOLTAGE						
V_{FBREF}	Reference voltage			0.6		V
$V_{FBREFTOL}$	Reference voltage tolerance	T_A = 25°C	–1%		1%	
I_{FB}	Feedback pin leakage current		–100		100	nA
SMPS FREQUENCY						
f_{SW}	Switching frequency	EVM close loop measurement. V_{IN} = 5 V, V_{OUT} = 1.05 V, I_{OUT} = 3 A		1		MHz
$t_{OFF(min)}$	Minimum off-time		110	190	270	ns
t_{DEAD}	Deadtime(1)	SW node high, V_{IN} = 5 V		9		ns
		SW node low, V_{IN} = 5 V		10		
LOGIC THRESHOLD						
V_{LL}	EN low-level voltage				0.8	V
V_{LH}	EN high-level voltage		1.5			V
I_{LLK}	EN input leakage current	V_{IN} = V_{CC} = 3.3 V	–3	1	3	μA
SOFT START						
t_{SS}	Soft-start time(1)	V_{FB} rising from 0 V to 0.6 V		300		μs
PGOOD COMPARATOR						
V_{PGTH}	PGOOD threshold	PGOOD out to higher w/r/t V_{FB}		130%		
		PGOOD out to lower w/r/t V_{FB}		50%		
t_{PGDLY}	PGOOD high delay time	Delay for PGOOD in, after EN = Hi		1.3		ms
I_{PGLK}	PGOOD leakage current		–1	0	1	μA
CURRENT DETECTION						
I_{OCL}	Current limit threshold	Valley current limit, V_{IN} = V_{CC} = 3.3 V, T_A = 25°C	4.8			A
PROTECTIONS						
V_{IN_UVLO}	VIN UVLO threshold voltage	Wake-up	2.85	2.95	3.05	V
		Shutdown	2.6	2.7	2.8	
V_{CC_UVLO}	VCC UVLO threshold voltage	Wake-up	2.85	2.95	3.05	
		Shutdown	2.6	2.7	2.8	
V_{OVP}	OVP threshold voltage	OVP detect voltage, overdrive = 100 mV		130%		
t_{OVP}	OVP delay time	Overdrive = 100 mV		1.9		μs
V_{UVP}	UVP threshold voltage	UVP detect voltage, overdrive = 100 mV		50%		
t_{UVPDLY}	UVP delay time	Overdrive = 100 mV		2.4		μs
SW PULL DOWN						
R_{SWPD}	Switch node pull down resistance	EN = Lo		260		Ω
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold(1)	Shutdown temperature		145		°C
		Hysteresis		20		

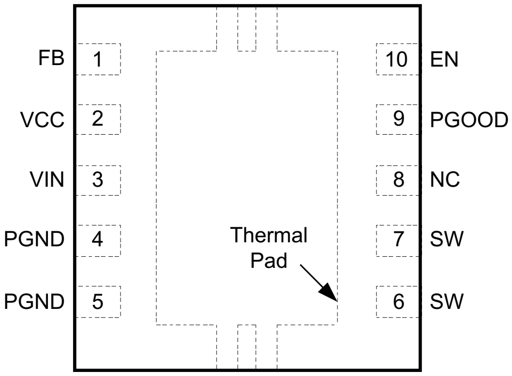
(1) Specified by design. Not production tested.

DEVICE INFORMATION

Functional Block Diagram



**DRC PACKAGE
10 PINS
(TOP VIEW)**



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	10	I	Enable function for the switched-mode power supply (SMPS) (3.3-V logic compatible)
FB	1	I	Voltage feedback. Also used for OVP, UVP and PGOOD determination.
NC	8	I	No connect. Make no external connection to this pin.
PGND	4 5	I	Device ground
PGOOD	9	O	Power good indicator. Requires external pull-up resistor.
SW	6 7	I	Switching node output. Connect to external inductor. Also serve as current sensing negative input for over current protection purpose
VCC	2	I	Power supply for analog circuit.
VIN	3		Main power conversion input and gate-drive voltage supply for output FETs.
Thermal Pad			Connect to PGND.

TYPICAL CHARACTERISTICS

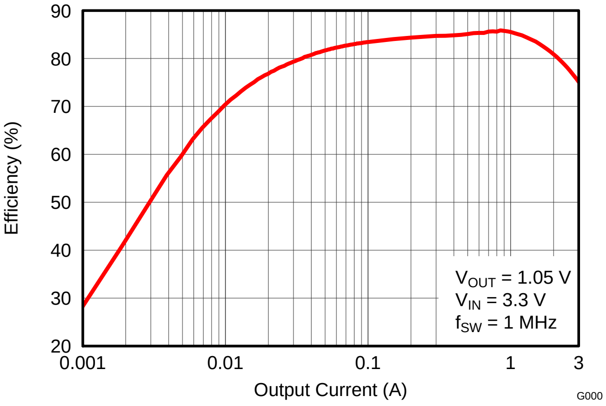


Figure 1. Efficiency vs. Output Current

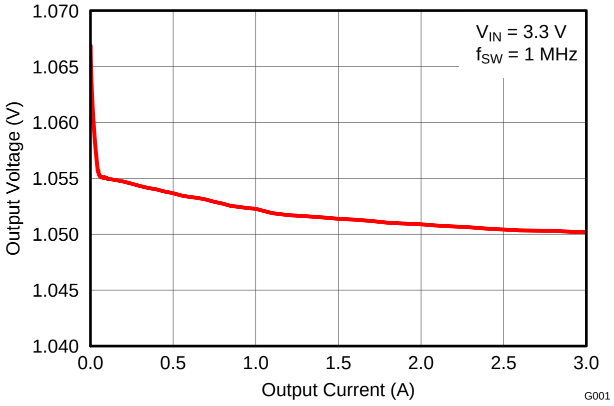


Figure 2. DC Load Regulation

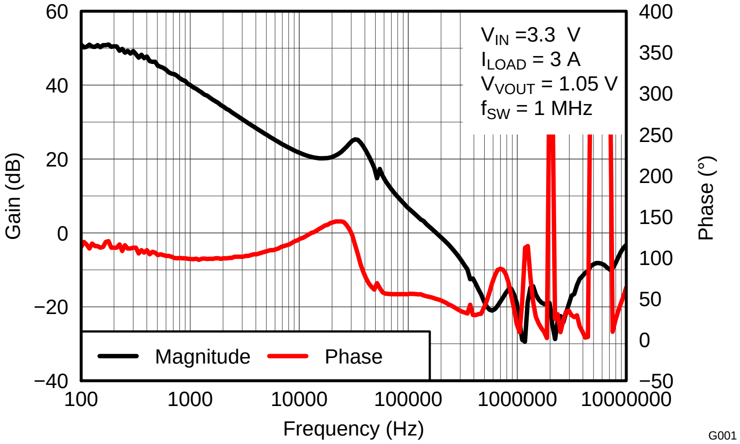
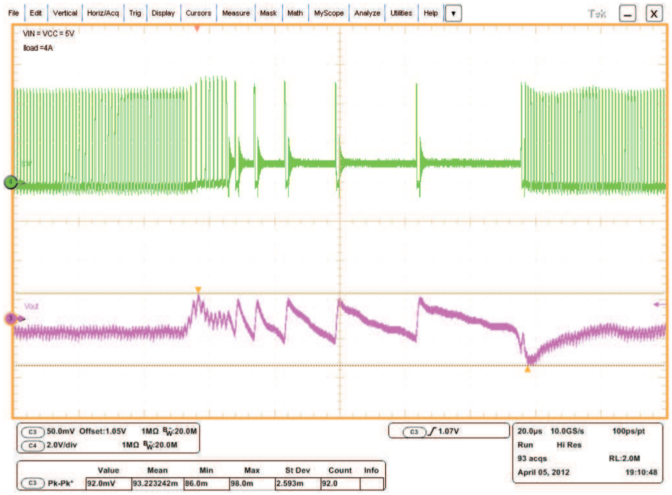


Figure 3. Bode Plot



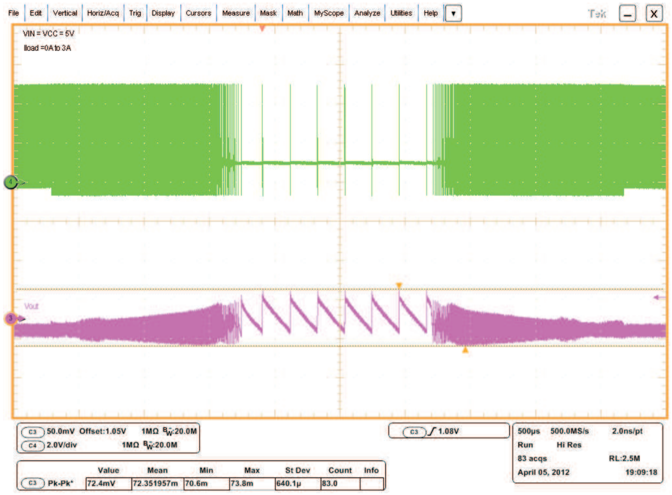
C3 50.0mV Offset:1.05V 1MΩ B_W:20.0M
C4 2.0V/div 1MΩ B_W:20.0M

C3 ∫ 1.07V

20.0μs 10.0GS/s 100ps/pt
Run Hi Res
93 acqs RL:2.0M
April 05, 2012 19:10:48

	Value	Mean	Min	Max	St Dev	Count	Info
C3 Pk-Pk*	92.0mV	93.223242m	86.0m	98.0m	2.593m	92.0	

Figure 4. Fast 0-A to 3-A Transient Response



C3 50.0mV Offset:1.05V 1MΩ B_W:20.0M
C4 2.0V/div 1MΩ B_W:20.0M

C3 ∫ 1.08V

500μs 500.0MS/s 2.0ns/pt
Run Hi Res
83 acqs RL:2.5M
April 05, 2012 19:09:18

	Value	Mean	Min	Max	St Dev	Count	Info
C3 Pk-Pk*	72.4mV	72.351957m	70.6m	73.8m	640.1μ	83.0	

Figure 5. Slow 0-A to 3-A Transient Response

APPLICATION INFORMATION

Functional Overview

TPS51313 is a D-CAP2 mode adaptive on time converter with internal integrator. Monolithically integrate high side and low side FET supports output current to a maximum of 3-ADC. The converter automatically runs in discontinuous conduction mode to optimize light load efficiency. A switching frequency of 1-MHz enables optimization of the power train for the cost, size and efficiency performance of the design.

PWM Operation

The PWM operation is comprised of three separate loops, A, B and C as shown in Figure 6.

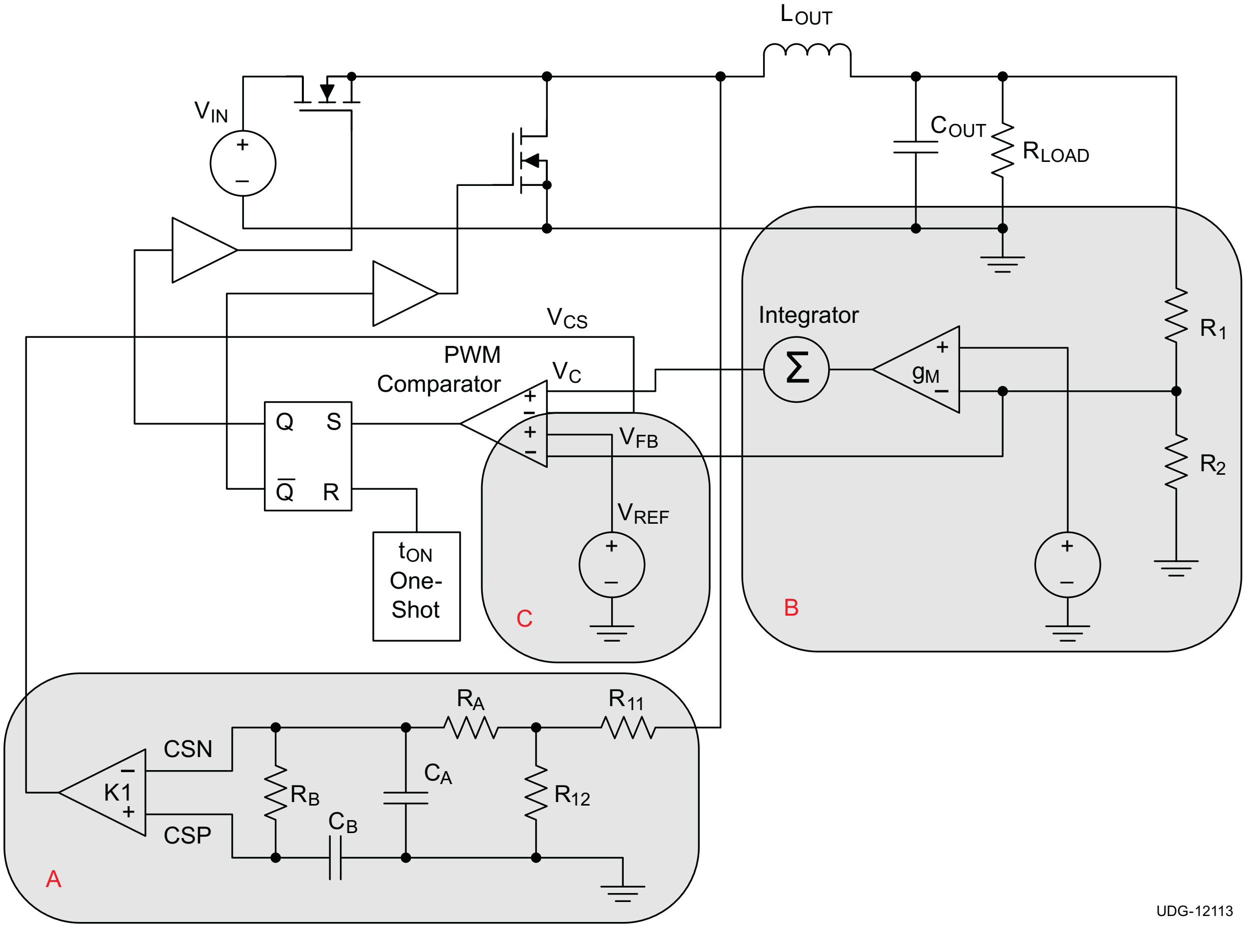


Figure 6. PWM Operation

Internal Current Loop (A)

Loop A is the internal current loop. The current information is sampled, divided and averaged at the SW node. The RC time constant and the gain of the current sense amplifier is chosen to cover the wide range of power stage design intended for this application.

Internal Voltage Loop (B)

Loop B is the internal voltage loop. The feedback voltage information is compared to the voltage reference at the input of the g_M amplifier, the internal integrator is designed to provide a zero at the double pole location to boost phase margin at the desired crossover frequency.

Fast Feedforward Loop (C)

Loop C is the additional loop that acts a direct fast feedforward loop to enhance the transient response.

In steady state operation as shown in Figure 7, the on time is initiated by the interaction of the three loops mentioned above. When the (V_C– V_{CS}) is rising above threshold defined by (V_{FB} – V_{REF}), the PWM comparator issues the on time pulse after the propagation delay. The demand of on time occurs when the artificial current has reached the valley point. The load regulation is maintained by the integrator provided by the g_M amplifier and internal integrator.

In transient operation as shown in Figure 8, the benefit of this topology is becoming evident. In an all MLCC output configuration, especially when the output capacitance is low, when the load step is applied, the output voltage is immediately discharged to try to keep the load demand. The immediate reflection of the load demand is instantly reflected in the FB voltage. The (V_{FB} – V_{REF}) is thus served as a termination voltage level for the (V_C – V_{CS}), thus modulating the initiation of the on time. The transient response can be improved further by amplifying the difference between V_{FB} and the V_{REF} reference.

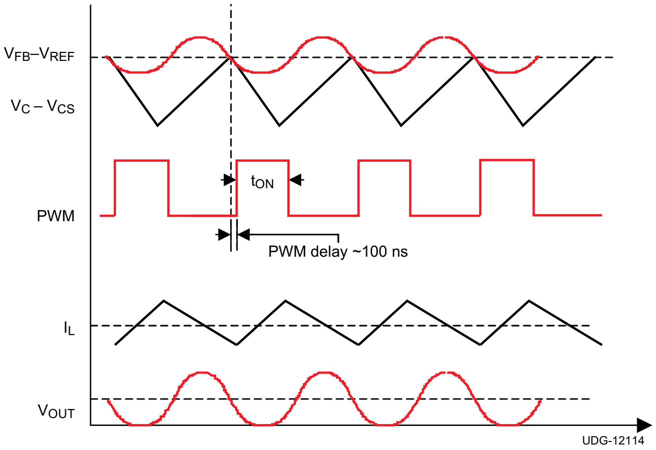


Figure 7. Steady-State Operation

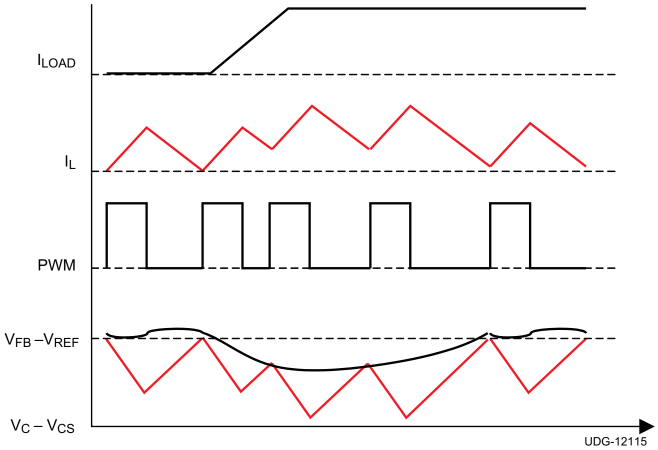


Figure 8. Transient Operation

PWM Frequency

The TPS51313 operates at a switching frequency of 1 MHz.

Light Load Power Saving Features

The TPS51313 offers an automatic pulse-skipping feature to provide excellent efficiency over the entire load range. The converter senses the current when the low-side FET is on and prevents negative current flow by turning off the low side FET. This saves power by eliminating re-circulation of the inductor current. When the bottom FET is turned off, the converter enters discontinuous mode, and the switching frequency decreases, reducing switching loss.

Power Sequences

TPS51313 initiates the soft-start process when the EN, VIN and VCC pins are ready. The soft-start time 300 µs when the reference voltage is between 0 V and 0.6 VREF. The actual output ramp-up time is the same as that of the VREF start-up time, which is 300 µs.

Power Good Signal

The TPS51313 has one open-drain power good (PGOOD) pin. During initial startup, there is a 1.3-ms power good high propagation delay after EN goes high. The PGOOD de-asserts when the EN is pulled low or an undervoltage condition on VCC or VIN or any other faults (such as V_{OUT}, UVP, OCP, OVP) that require latch off action is detected.

Protection Features

The TPS51313 offers many features to protect the converter power chain as well as the system electronics.

Input Undervoltage Protection on V_{CC} and V_{IN} (UVLO)

The TPS51313 continuously monitor the voltage on the V_{CC} and V_{IN} to ensure the voltage level is high enough to bias the converter properly and to provide sufficient gate drive potential to maintain high efficiency for the converter. The converter starts with V_{CC} and V_{IN} approximately 2.95 V and has a nominal of 250 mV of hysteresis, assuming EN is above the logic threshold level. If the UVLO level is reached for either V_{CC} or V_{IN}, the converter transitions the SW node into a tri-state and remains off until the device is reset by both V_{CC} and V_{IN} reaches 2.95 V (nominal). The PGOOD is deasserted when UVLO is detected and remains low until the device is reset. The device resumes operation when VIN recoveres to 2.95 V (nominal).

Output Overvoltage Protection (OVP)

The TPS51313 has OVP protection circuit. An OVP event is detected when the FB voltage is approximately 130% x 0.6VREF. In this case, the converter de-asserts the PGOOD signal and performs the overvoltage protection function. The converter latches off both high-side and low-side FET (after a typical delay of 1.9 µs) and remains in this state until the device is reset by EN, or V_{CC} or V_{IN}.

Output Undervoltage Protection (UVP)

Output undervoltage protection works in conjunction wit the current protection described in the Overcurrent and Current Limit Protection section. If the FB voltage drops below 50% x 0.6 V_{REF}, after a delay of 2.4 µs, the converter latches off. Undervoltage protection can be reset by EN, V_{CC} or V_{IN}.

Overcurrent and Current Limit Protection

The TPS51313 provides an overcurrent protection function. The minimum OCP level is 4.8-A DC. When the current limit is exceeded for consecutive 9 cycles, the converter latches off and remains latched off until it is reset by EN, V_{CC} or V_{IN}.

The TPS51313 also provides current limit protection function. If the sense current is above the OCL setting, the converter delays the next on pulse until the current level drops below the OCL limit. Current limiting occurs on a pulse-by-pulse basis. During a fast or very fast overcurrent event, the output voltage tends to droop until the UVP limit is reached. Then the converter de-asserts the PGOOD signal, and latches off after a delay between 1 µs and 2 µs . The converter remains in this state until the device is reset by EN, V_{CC} or V_{IN}.

Thermal Protection

The TPS51313 has an internal temperature sensor. When the die temperature reaches a nominal of 145°C, the device shuts down until the temperature cools by approximately 20°C. Then the converter restarts. The thermal shutdown is an non-latched behavior.

REFERENCE DESIGN

Application Schematic

This section describes a simplified design procedure for a discrete graphics processor PEX rail application using the TPS51313 converter. Figure 9 shows the application schematic..

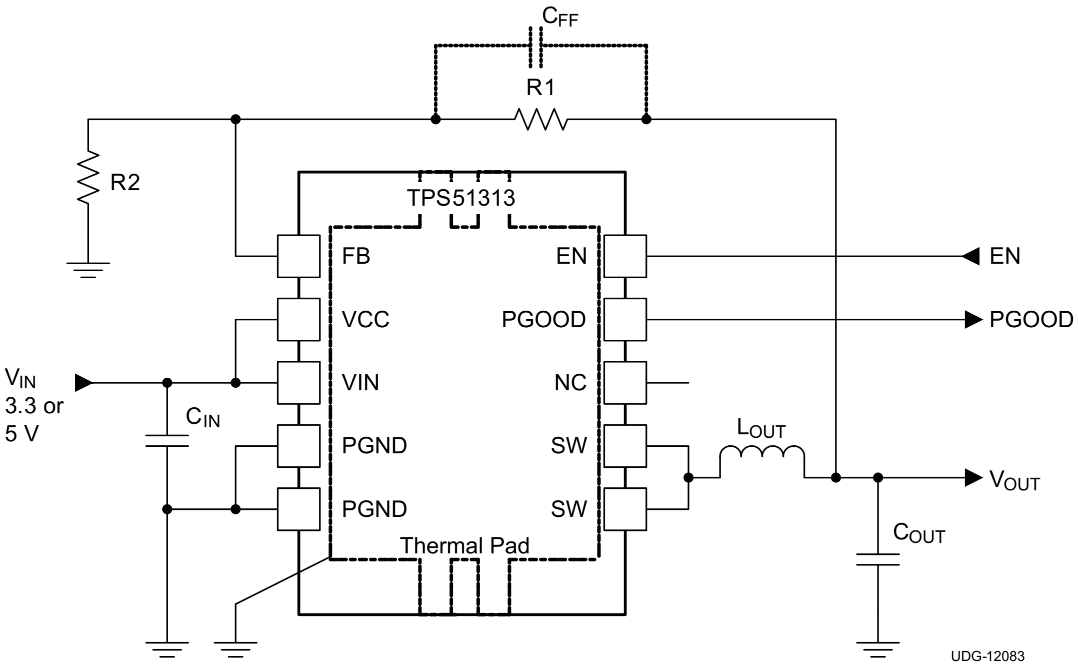


Figure 9. Reference Design Schematic

Table 1. Reference Design List of Materials

FUNCTION	MANUFACTURER	PART NUMBER
Output Inductor	Vishay	IHLP-1212AB-11
Ceramic Output Capacitors	Panasonic	ECJ2FB0J226M
	Murata	GRM21BR60J226ME39L

Design Procedure

Step One. Determine the specifications.

. The PEX rail requirement provides the following key paramaters.

- V_{OUT} = 1.05 V
- $I_{CC(max)}$ = 3 A
- ΔI = 2A (transient load step and release)
- di/dt = 2.5A/µs

Step Two. Determine the system parameters.

The input voltage range and operating frequency are of primary interest. For example,

- $V_{IN} = V_{CC}$ = 3.3 V
- f_{SW} = 1 MHz.
- Maximum height of power chain components = 1.2 mm

Step Three. Set the output voltage.

Use Equation 1 to determine the output voltage.

$$V_{OUT} = V_{REF} \times \frac{(R1 + R2)}{R2} \tag{1}$$

The output voltage is determined by 0.6-V votlage reference and the resistor dividers (R1 and R2). The output voltage is regulated to the FB pin. For this V_{OUT} = 1.05 V, reference design, select R1 = 30 kΩ and R2 = 40 kΩ. (see Figure 9) To improve signal-to-noise performance of the converter, add a small feedforward capacitor (typically approximately 27 pF or less) in parallel with the upper resistor (R1).

Step Four. Determine inductor value and choose inductor.

Smaller inductance yields better transient performance but the consequence is higher ripple and lower efficiency. Higher values have the opposite characteristics. It is common practice to limit the ripple current to 25% to 50% of the maximum current. In this case, use 40%:

$$I_{P-P} = 3\,A \times 0.4 = 1.2\,A \tag{2}$$

where

- f_{SW} = 1 MHz
- V_{IN} = 3.3 V
- V_{OUT} = 1.05 V

$$L = \frac{V \times dT}{I_{P-P}} = \left(\frac{(V_{IN} - V_{OUT})}{I_{P-P}}\right) \times \left(\frac{V_{OUT}}{(f_{SW} \times V_{IN})}\right) = 0.596\,\mu H \tag{3}$$

For this application, a 0.56-µH, 18.7-mΩ inductor from Vishay with part number IHLP-1212AB-11 is chosen. Maximum height for this inductor is 1.2 mm.

Step Five. Determine the output capacitance.

To determine C_{OUT} based on transient and stability requirement, first calculate the minimum output capacitance for a given transient.

Equation 4 and Equation 5 calculate the minimum output capacitance for meeting the transient requirement, which is 33.8-µF assuming a ±3% voltage allowance for load step and release.

$$C_{OUT(min\_under)} = \frac{L \times \Delta I_{LOAD(max)}{}^{2} \times \left(\frac{V_{VOUT} \times t_{SW}}{V_{IN(min)}} + t_{MIN(off)}\right)}{2 \times \Delta V_{LOAD(insert)} \times \left(\left(\frac{V_{IN(min)} - V_{VOUT}}{V_{IN(min)}}\right) \times t_{SW} - t_{MIN(off)}\right) \times V_{VOUT}} \tag{4}$$

$$C_{OUT(min\_over)} = \frac{L_{OUT} \times \left(\Delta I_{LOAD(max)}\right)^{2}}{2 \times \Delta V_{LOAD(release)} \times V_{VOUT}} \tag{5}$$

This design uses 3 22-µF capacitors with consideration of the MLCC derating effect (60% derating for both AC and DC effect).

Step Six. Establishing the internal compensation loop.

The TPS51313 is designed with an internal compensation loop. The internal integrator zero location is approximately 60 kHz. When the power stage double pole frequency contributed by the L_{OUT} and C_{OUT} is less than or equal to that of the zero frequency location, the converter is stable with sufficient margin.

Step Seven. Select decoupling and peripheral components.

For TPS51313 peripheral capacitors use the following minimum value of ceramic capacitance, X5R or better temperature coefficient is recommended. Tighter tolerances and higher voltage ratings are always appropriate.

V_{CC} and V_{IN} decoupling ≥ 2 × 10 µF, 6.3 V

Pull up resistor on PGOOD = 100 kΩ

Step Eight. (Optional) Snubber design for optimizing maximum switch node ringing.

For TPS51313 layout design, if the maximum switch node voltage is above 8.5 V for 20 ns, snubber circuit is recommended to limit the maximum voltage to be within the absolute maximum voltage rating (see Absolute maximum rating table on page 2). A series combination of R and C (where the value of R is approximately 2.2 Ω, and the value of C is approximately 470 pF) from SW node to PGND can be added to achieve effective snubbing for SW node.

Layout Considerations

Good layout is essential for stable power supply operation. Follow these guidelines for an efficient PCB layout.

- Widen the PGND connection area as much as possible.
- Place V_{IN}, V_{CC} decoupling capacitors as close to the device as possible.
- Use wide traces for the VIN, SW and PGND pins. These nodes carry high current and also serve as heat sinks.
- Place FB and voltage setting dividers as close to the device as possible.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS51313DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-10 to 85	S51313	Samples
TPS51313DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-10 to 85	S51313	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Only one of markings shown within the brackets will appear on the physical device.

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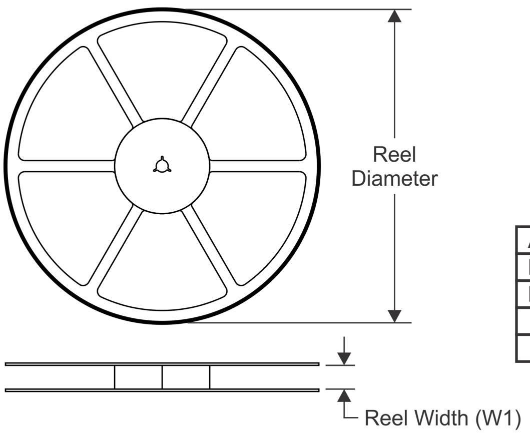
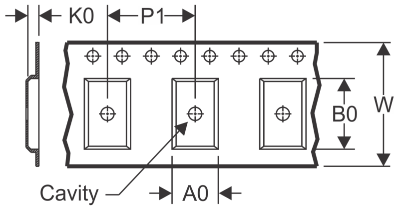
TAPE AND REEL INFORMATION

REEL DIMENSIONS

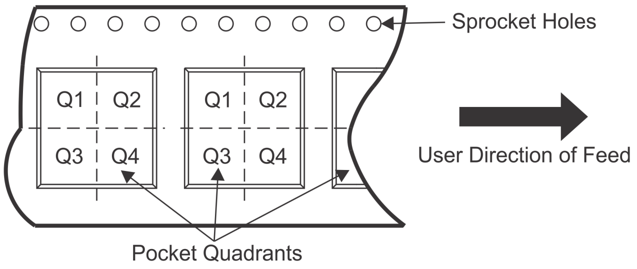


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

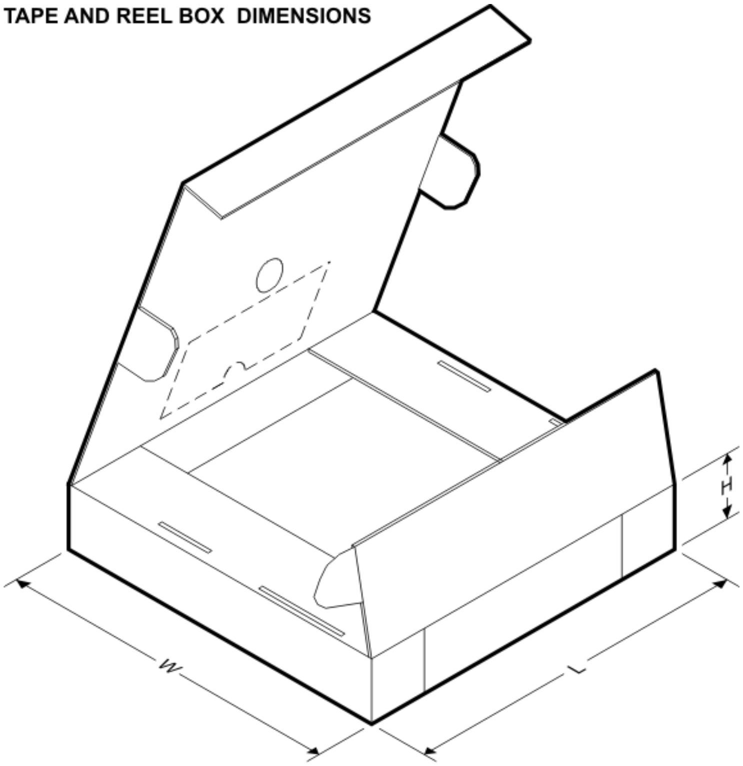
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51313DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51313DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

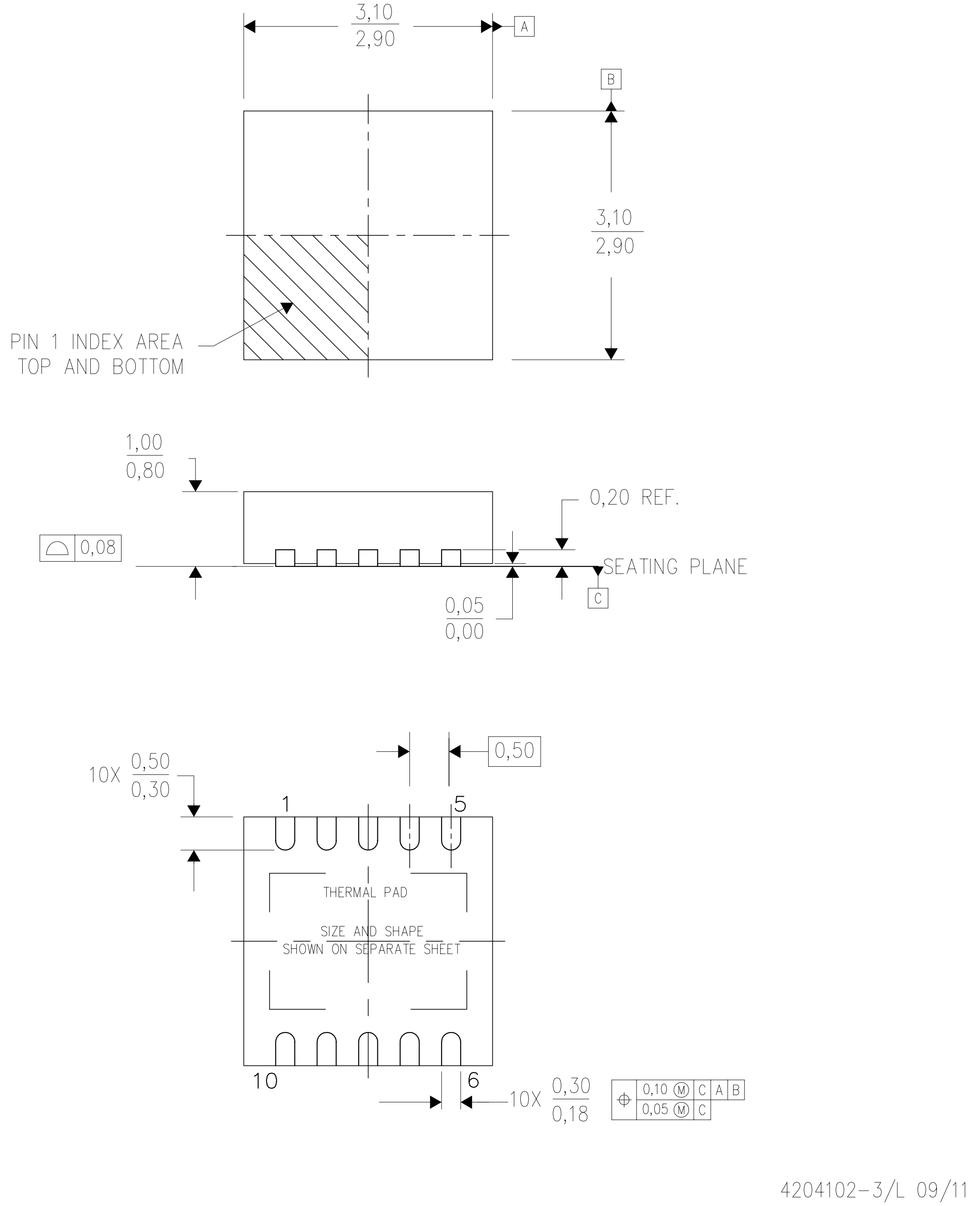
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51313DRCR	SON	DRC	10	3000	367.0	367.0	35.0
TPS51313DRCT	SON	DRC	10	250	210.0	185.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

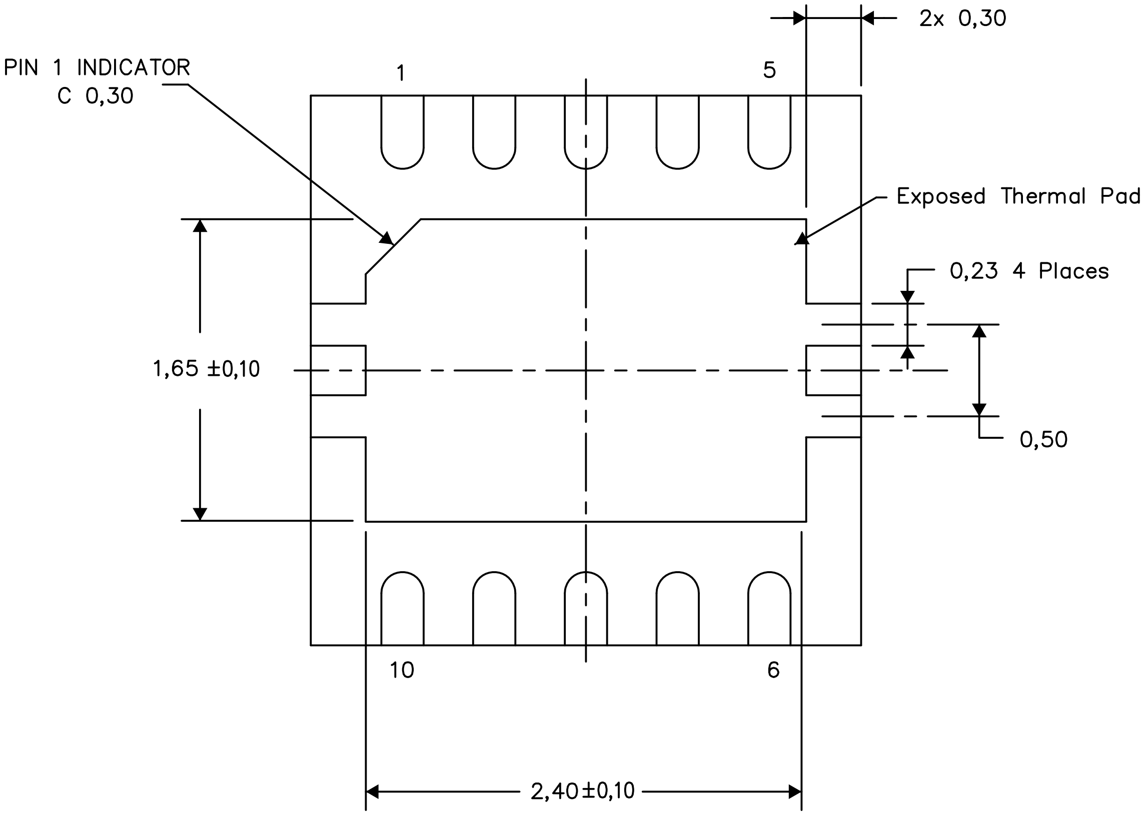
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



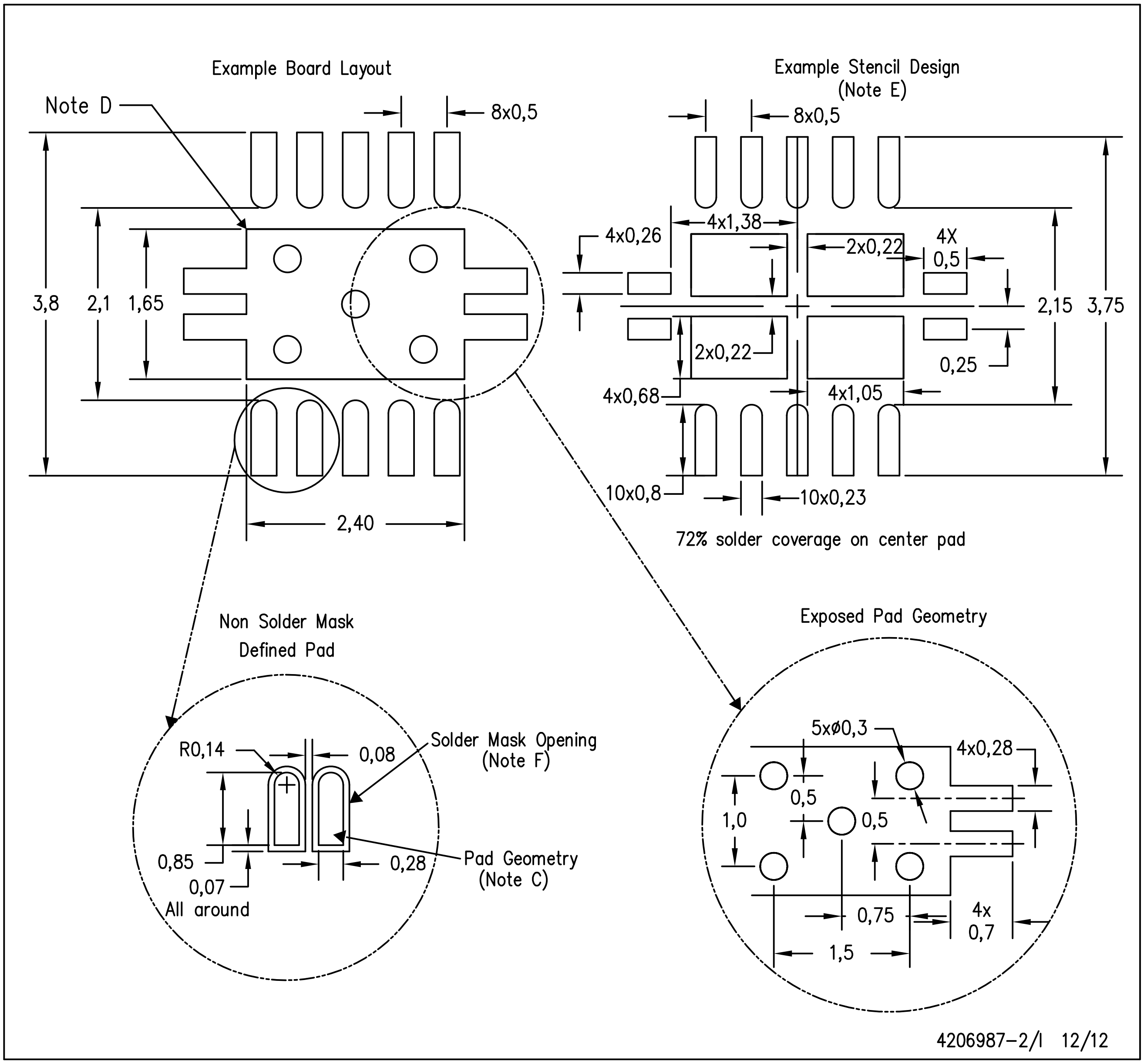
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/Q 12/12

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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