2.95V To 6V Input, 2W, Isolated DC/DC Converter with Integrated FETs

Check for Samples: TPS55010

FEATURES

- **Isolated Fly-Buck™ Topology**
- **Primary Side Feedback**
- **100 kHz to 2000 kHz Switching Frequency**
- **Synchronizes to External Clock**
- **Adjustable Slow Start**
- **Adjustable Input Voltage UVLO**
- **Open Drain Fault Output**
- **Cycle-by-Cycle Current Limit**
- **Thermal Shutdown Protection**
- **3 mm x 3 mm 16 Pin QFN Package**

APPLICATIONS

- **Noise Immunity in PLCs, Data Acquisition and Measurement Equipment**
- **Isolated RS-232 and RS-485 Communication Channels**
- **Powers Line Drivers, ISO Amplifiers, Sensors, CAN Transceivers**
- **Floating Supplies for IGBT Gate Drivers**
- **Promotes Safety in Medical Equipment**

DESCRIPTION

The TPS55010 is a transformer driver designed to provide isolated power for isolated interfaces, such as RS-485 and RS-232, from 3.3V or 5V input supply.

The device uses fixed frequency current mode control and half bridge power stage with primary side feedback to regulate the output voltage for power levels up to 2W. The switching frequency is adjustable from 100 kHz to 2000 kHz so solution size, efficiency and noise can be optimized. The switching frequency is set with a resistor or is synchronized to external clock using the RT/CLK pin. To minimize inrush currents, a small capacitor can be connected to the SS pin. The EN pin can be used as an enable pin or to increase the default input UVLO voltage from 2.6V.

With the same transformer the TPS55010 can provide a solution for different input and output voltage combinations by adjusting the primary side voltage. Off the shelf transformers are available to provide single positive, or dual positive and negative output voltages.

The TPS55010 is available in a 3 mm x 3 mm 16 pin QFN package with thermal pad.
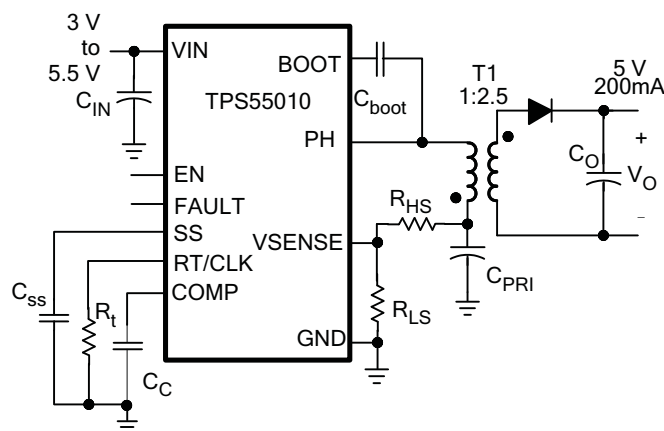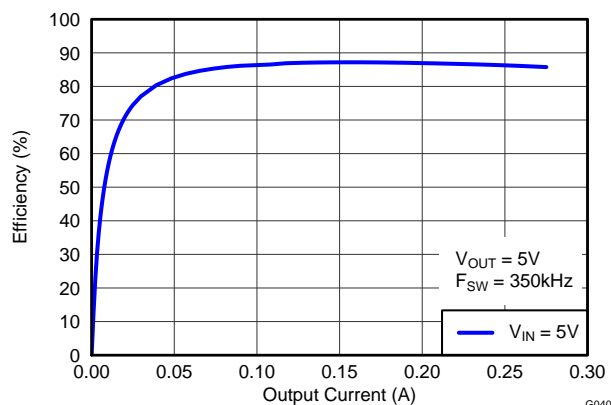
Figure 1. SIMPLIFIED SCHEMATIC

Figure 2. Efficiency vs Load Current

⚠️ These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN CONFIGURATION

**RTE PACKAGE
(TOP VIEW)**
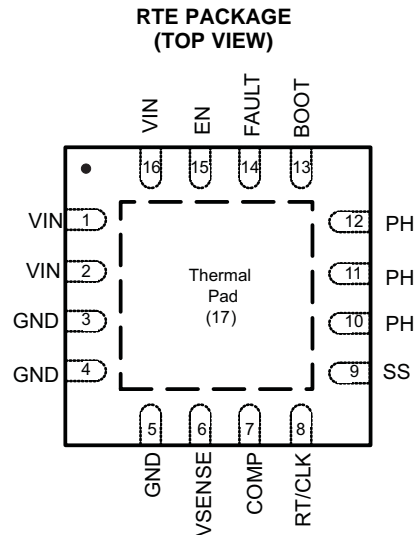
Table 1. PIN FUNCTIONS

| Pin Name	Number	Description
VIN	1, 2, 16	Supplies the control circuitry and switches of the power converter.
GND	3, 4, 5	Power Ground. This pin should be electrically connected directly to the thermal pad under the IC.
VSENSE	6	Inverting node of the gm error amplifier.
COMP	7	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
RT/CLK	8	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to a resistor set function.
SS	9	Slow-start. An external capacitor connected to this pin sets the output rise time.
PH	10, 11, 12	The source of the internal high side power MOSFET, and drain of the internal low side MOSFET.
BOOT	13	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
FAULT	14	An open drain output. Active low if the output voltage is low due to thermal shutdown, dropout, overvoltage or EN shut down.
EN	15	Enable pin, internal pull-up current source. Pull below 1.2V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
THERMAL PAD	17	GND pin should be connected to the exposed thermal pad for proper operation. This thermal pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.

Product Folder Links : *TPS55010*

FUNCTIONAL BLOCK DIAGRAM
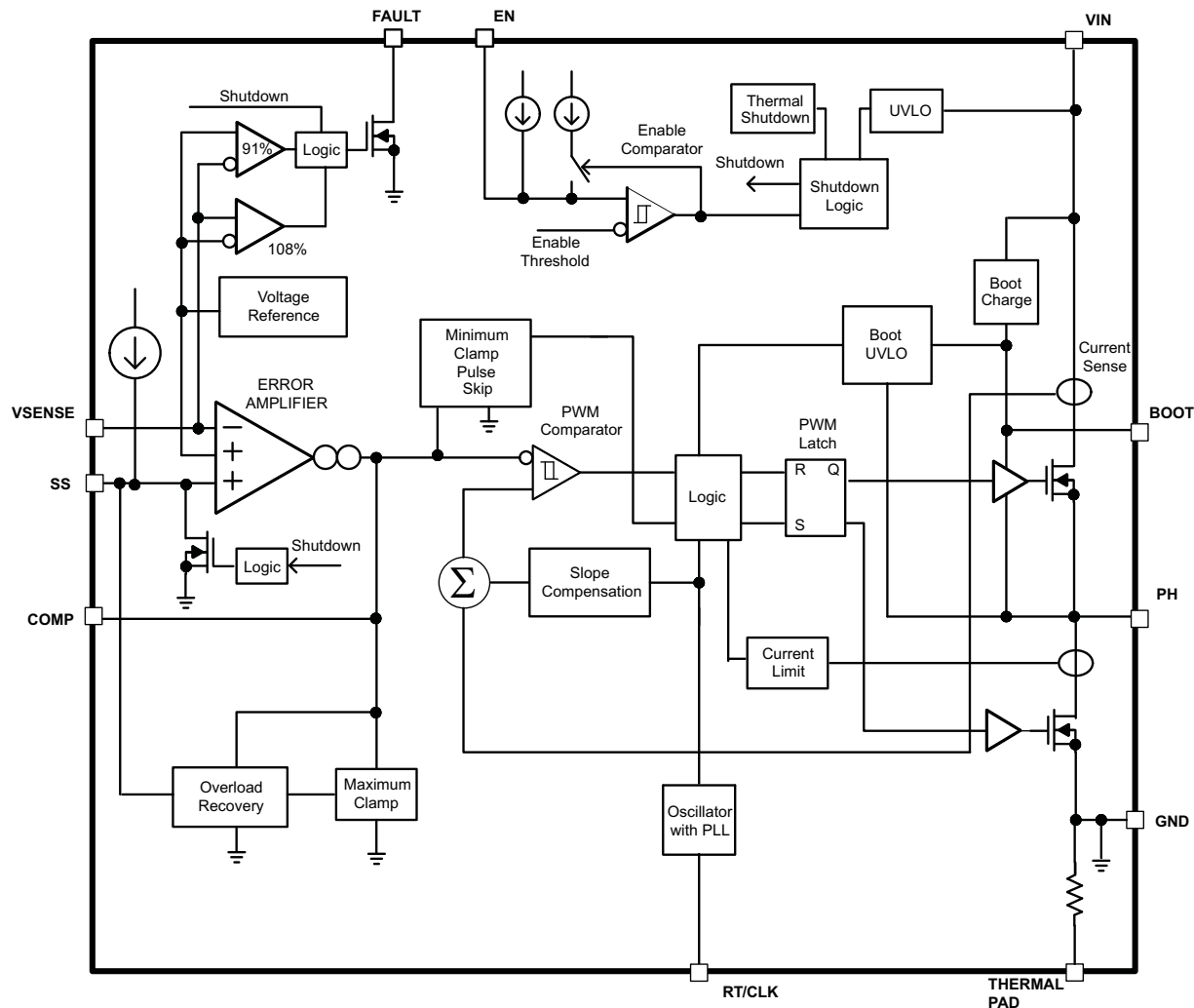
ORDERING INFORMATION[1]

T_J	PACKAGE	PART NUMBER
-40°C to 150°C	3 x 3 mm QFN	TPS55010RTE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at ww.w.ti.com.

ABSOLUTE MAXIMUM RATINGS [1]

over operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Voltage	VIN	-0.3	7	V
	EN	-0.3	3.6	V
	BOOT		PH + 7	V
	VSENSE	-0.3	3	V
	COMP	-0.3	3	V
	FAULT	-0.3	7	V
	SS	-0.3	3	V
	RT/CLK	-0.3	6	V
	BOOT-PH		7	V
	PH	-0.6	7	V
	PH, 10ns Transient	-2	10	V
Current	EN		100	µA
	RT/CLK		100	µA
	COMP		100	uA
	FAULT		10	mA
	SS		100	µA
Electrostatic Discharge (HBM) [2]	QSS 009-105 (JESD22-A114A)		2	kV
Electrostatic Discharge (CDM) [2]	QSS 009-147 (JESD22-C101B.01)		500	V
Operating Junction Temperature		-40	150	ºC
Storage Temperature		-65	150	ºC

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ELECTRICAL SPECIFICATIONS is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

THERMAL INFORMATION

THERMAL METRIC[1]		TPS55010 RTE (16 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	60	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	55.5	
θ_{JB}	Junction-to-board thermal resistance	24.9	
ψ_{JT}	Junction-to-top characterization parameter	1.0	
ψ_{JB}	Junction-to-board characterization parameter	24.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	9.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

T_J = −40°C TO 150°C, VIN = 2.95V TO 6V (unless otherwise noted)

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE					
Operating input voltage	VIN	2.95		6	V
Shutdown current	EN = 0V, 25°C		2	5	µA
Operating current	VSENSE = 0.9V, 25°C		360	575	µA
Internal undervoltage lockout			2.6	2.9	V
ENABLE					
Enable threshold	rising		1.25	1.37	V
	falling	1.15	1.18		
Input current	Threshold - 50mV		-1.2		µA
	Threshold + 50mV		-4.6		µA
Hysteresis			3.4		
VOLTAGE REFERENCE					
Reference	3V < VIN < 6V	0.804	0.829	0.854	V
MOSFET					
High side switch resistance	BOOT- PH = 5 V		45	81	mΩ
Low side switch resistance	VIN = 5 V		45	81	mΩ
ERROR AMPLIFIER					
Input current			50		nA
Error amp transconductance	-2 µA < $I_{(COMP)}$ < 2 µA		245		uMhos
Error amp dc gain	VSENSE = 0.8 V		500		V/V
Minimum unity gain Bandwidth			3		MHz
Error amp source/sink	$V_{(COMP)}$ = 1V, 100 mV overdrive		±16		µA
COMP to Iph gm	Iph = 0.5 A		7.5		A/V
CURRENT LIMIT					
High side sourcing current limit	VIN = 3 V	2	2.75		A
Low Side Sinking Current Limit	VIN = 3 V	-3	-4.5		A
THERMAL SHUTDOWN					
Thermal Shutdown			171		°C
OT Hysteresis			12		°C
RT/CLK					
Switching frequency using RT mode		100		2000	kHz
Switching Frequency	$R_{(RT/CLK)}$ = 195 kΩ	400	500	600	kHz
RT/CLK voltage	$R_{(RT/CLK)}$ = 195 kΩ		0.5		V
RT/CLK high threshold			1.6	2.2	V
RT/CLK low threshold		0.4	0.6		V
Switching frequency using CLK mode		300		2000	kHz
Minimum CLK pulse width			75		ns
PLL lock in time			50		µs
RT/CLK falling edge to PH rising edge delay			90		ns
PH					
Minimum On time	Measured at 10% to 10% of VIN		130		ns
BOOT					
Boot UVLO			2.5		V

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C TO 150°C, VIN = 2.95V TO 6V (unless otherwise noted)

| DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SS Slow Start					
VIN UVLO to SS start time			100		µs
Charge current	$V_{(SS)}$ = 0.4 V	0.5	2.2	4	µA
SS to VSENSE matching	$V_{(SS)}$ = 0.4 V		35		mV
SS to reference Crossover	98% reference		1.1		V
SS discharge current (overload)	VSENSE = 0 V		325		µA
SS discharge voltage	VSENSE = 0V		46		mV
SS discharge current (UVLO, EN, thermal fault)	$V_{(SS)}$ = 0.5 V		1.2		mA
FAULT Pin					
VSENSE threshold	VSENSE falling		91		% VREF
	VSENSE rising		108		% VREF
Output high leakage	VSENSE = V_{REF}, $V_{(FAULT)}$ = 5.5 V		2		nA
Output low	$I_{(FAULT)}$ = 3 mA		0.3		V
Minimum VIN for valid output	$V_{(FAULT)}$ < 0.5 V at 100 µA			1.6	V

TYPICAL CHARACTERISTICS
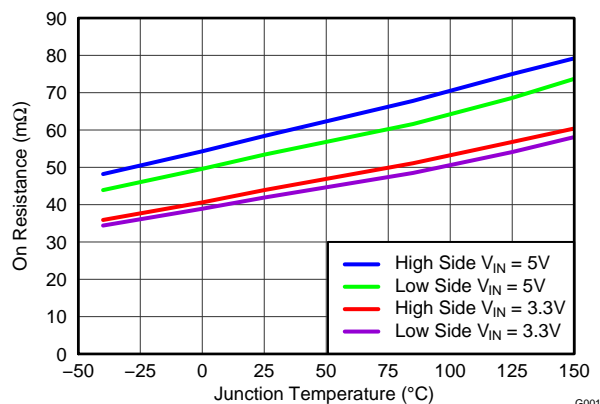
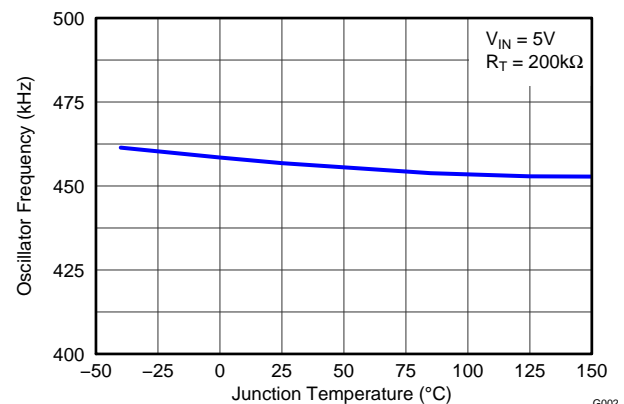Figure 3. HIGH SIDE AND LOW SIDE $R_{DS(on)}$
vs TEMPERATURE

Figure 4. FREQUENCY vs TEMPERATURE
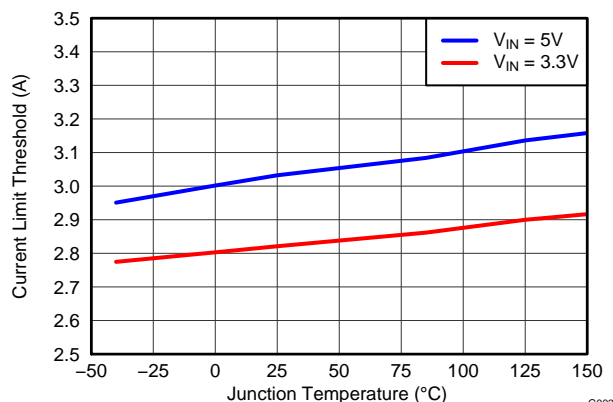

Figure 5. HIGH SIDE CURRENT LIMIT (SOURCING) vs
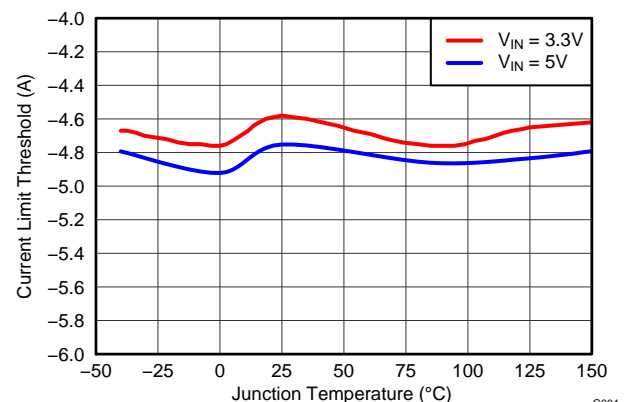JUNCTION TEMPERATURE

Figure 6. LOW SIDE CURRENT LIMIT (SINKING) vs
JUNCTION TEMPERATURE

Product Folder Links :TPS55010
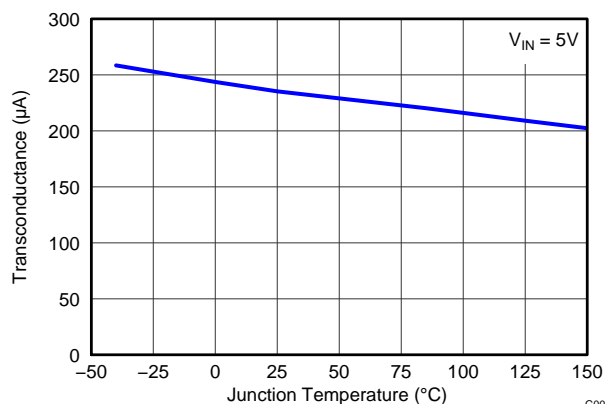
TYPICAL CHARACTERISTICS (continued)

Figure 7. ERROR AMPLIFIER TRANSCONDUCTANCE vs TEMPERATURE
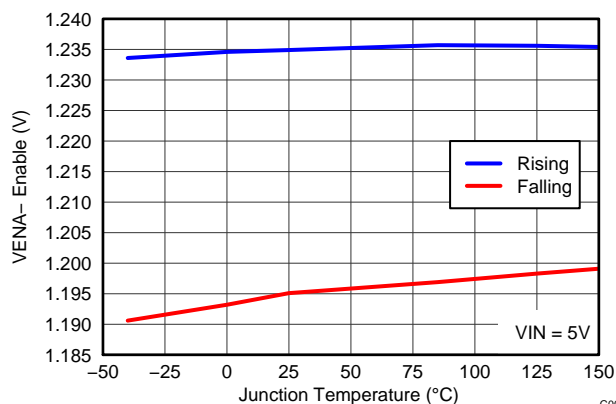

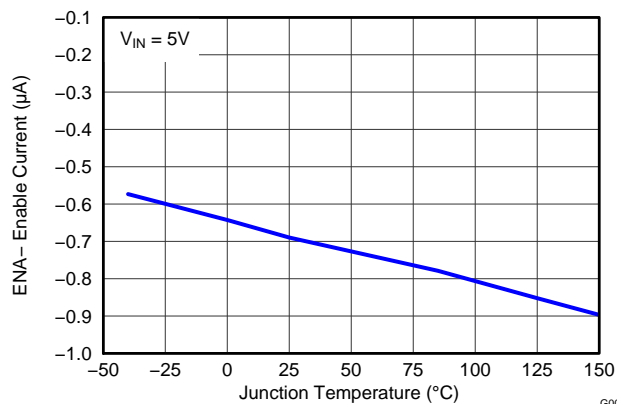**Figure 8. EN PIN VOLTAGE vs TEMPERATURE**

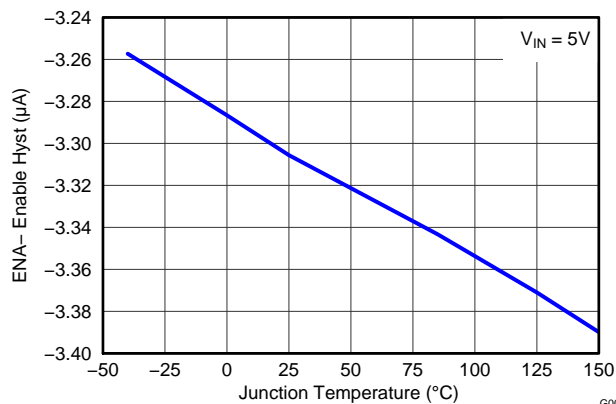**Figure 9. EN PIN PULLUP vs TEMPERATURE (V$_{EN}$ = Threshold -50 mV)**

Figure 10. EN PIN HYSTERESIS CURRENT vs TEMPERATURE
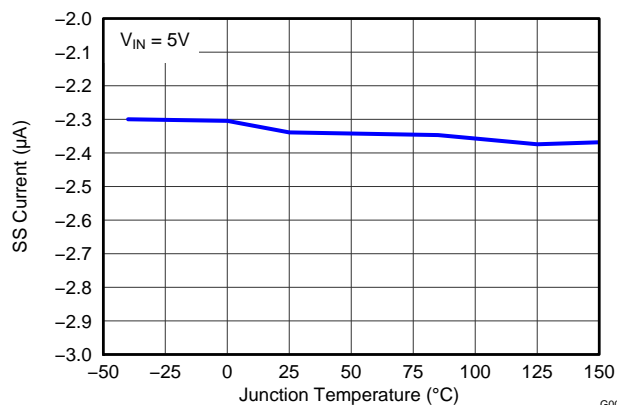
Figure 11. SS CHARGE CURRENT vs TEMPERATURE
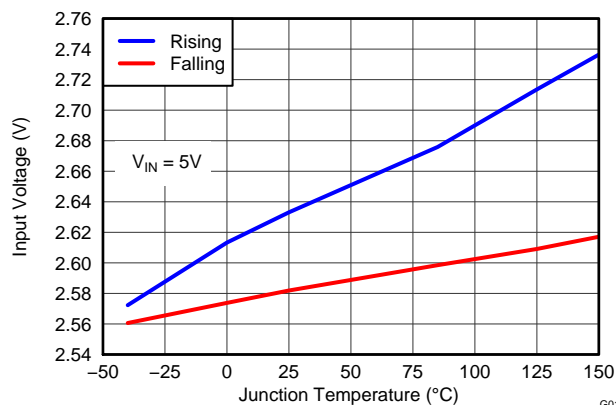

Figure 12. INPUT START and STOP VOLTAGE vs TEMPERATURE
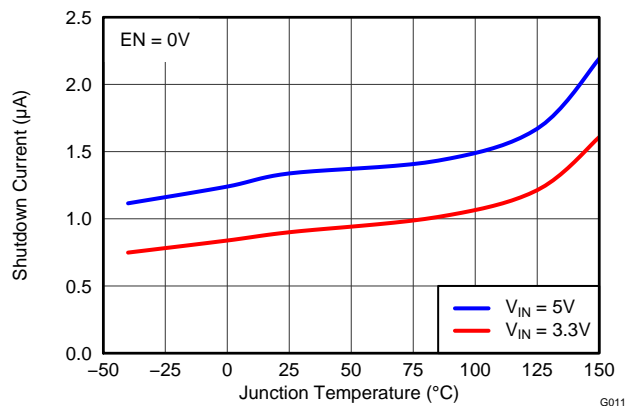
TYPICAL CHARACTERISTICS (continued)

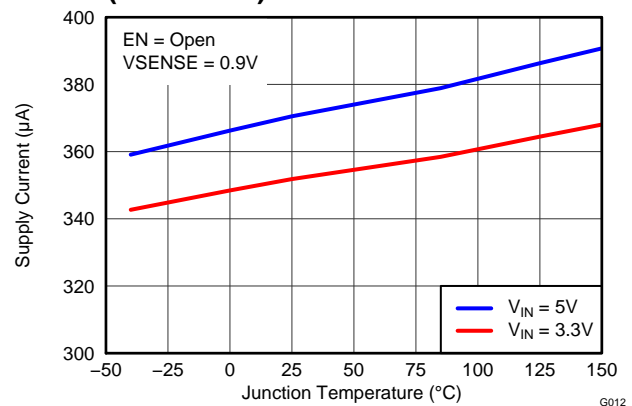Figure 13. SHUTDOWN SUPPLY CURRENT vs TEMPERATURE

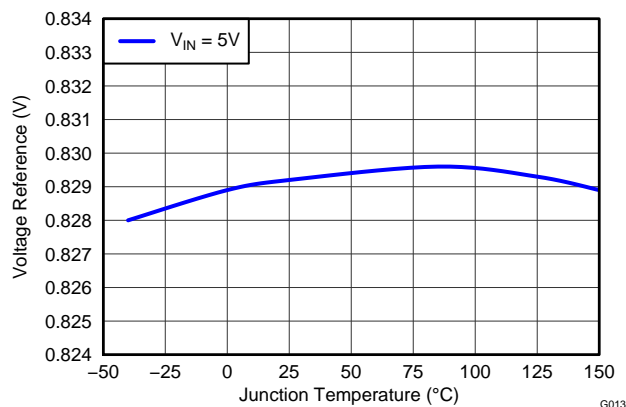Figure 14. VIN SUPPLY CURRENT vs TEMPERATURE

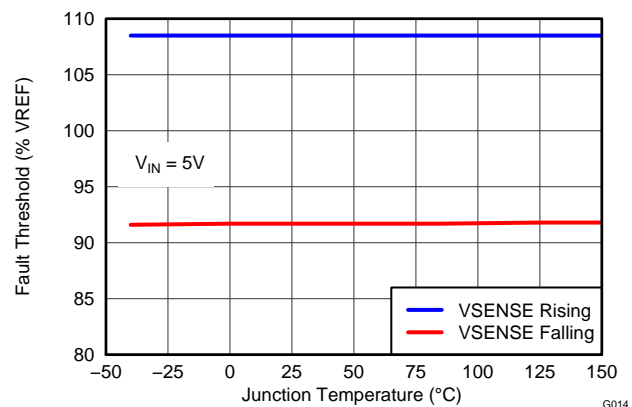
Figure 15. VOLTAGE REFERENCE vs TEMPERATURE

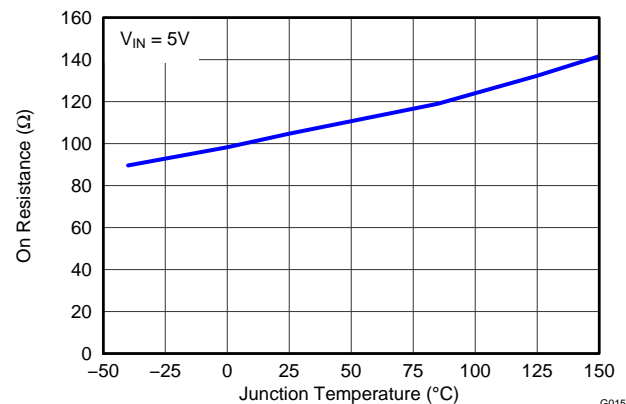Figure 16. FAULT THRESHOLD vs TEMPERATURE
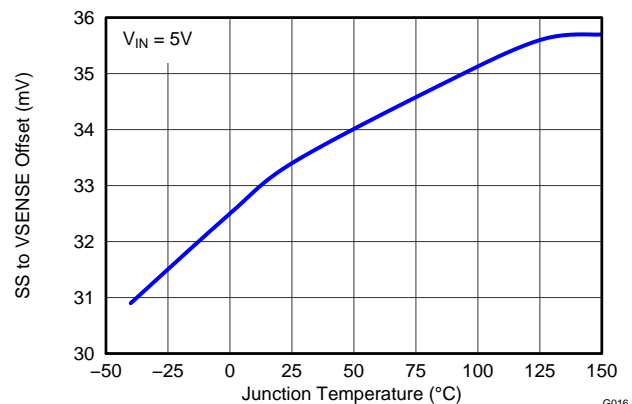

Figure 17. FAULT ON-RESISTANCE vs TEMPERATURE

Figure 18. SS to VSENSE OFFSET vs TEMPERATURE

Detailed Description

The TPS55010 is a half bridge transformer driver designed to implement a high efficiency, low power isolated supply. The primary side feedback implemented using two resistors and a primary side capacitor provides excellent regulation over line and load compared to an open loop push pull converter.

The half bridge power stage consists of two integrated n-channel MOSFETs with 45 mΩ on resistance. The drive voltage for the integrated high side MOSFET is supplied by a capacitor between the BOOT and PH pins. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the high side power switch turn on to a falling edge of an external system clock. The wide switching frequency of 100 kHz to 2000 kHz (300kHz to 2000kHz in CLK mode) allows for efficiency, size optimization or noise avoidance when selecting the switching frequency. The TPS55010 has a typical default start up voltage of 2.6 V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the pull up current provides a default condition when the EN pin is floating for the device to operate. The total operating current for the TPS55010 is typically 360 µA when not switching and under no load. When the device is disabled, the supply current is less than 5 µA. The slow start (SS) pin is used to minimize inrush currents during start up.

Fixed Frequency PWM Control

The TPS55010 uses an adjustable fixed frequency, peak current mode control. The primary voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the COMP voltage level the high side power switch is turned off and the low side power switch is turned on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level. The TPS55010 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations as duty cycle increases.

Half Bridge and Bootstrap Voltage

The TPS55010 has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric and a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

Error Amplifier

The TPS55010 uses a transconductance error amplifier. The amplifier compares the VSENSE voltage to the lower of the SS pin voltage or the internal 0.829 V voltage reference. The transconductance of the error amplifier is 245 µA/V. The frequency compensation components are placed between the COMP pin and ground.

Voltage Reference

The voltage reference system produces a precise ±3.0% voltage reference over temperature by scaling the output of a temperature-stable band gap circuit. The band gap and scaling circuits produce 0.829 V at the non-inverting input of the error amplifier.

Adjusting the Output Voltage

The primary side voltage is set with a resistor divider from the primary side capacitor to the VSENSE pin. It is recommended to use 1% tolerance or better divider resistors. Start with a 10 kΩ for the R_{LS} resistor and use Equation 1 to calculate R_{HS}. The output voltage is a function of the primary voltage, transformer turns ratio and forward voltage of the diode.

$$R_{HS} = R_{LS} \times \left(\frac{V_{PRI} - 0.829V}{0.829V} \right)$$

(1)

$$V_{OUT} = V_{PRI} \times \frac{N_{SEC}}{N_{PRI}} - V_{fd}$$

(2)
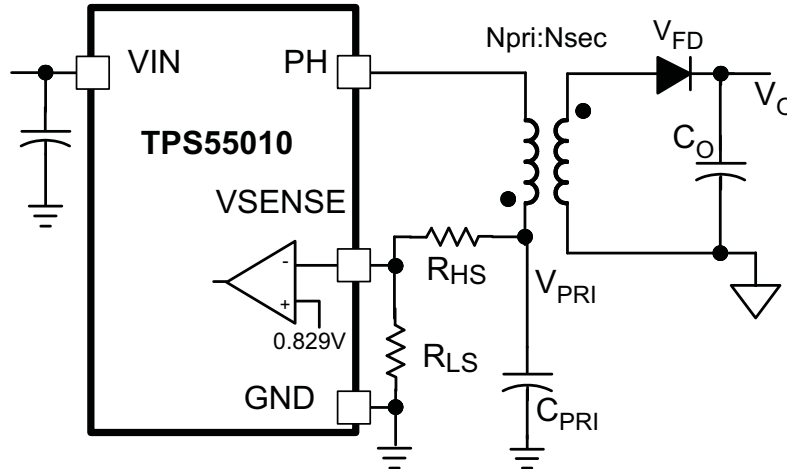
Figure 19. Setting the Output Voltage

Enable and Adjusting Undervoltage Lockout

The TPS55010 is disabled when the VIN pin voltage falls below 2.6 V. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in Figure 20 to adjust the input voltage UVLO by using two external resistors. The EN pin has an internal pull-up current source of 1.2 μA that provides the default condition of the TPS55010 operating when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, an additional 3.4 μA of hysteresis is added. When the EN pin is pulled below 1.18 V, the hysteresis current is removed.
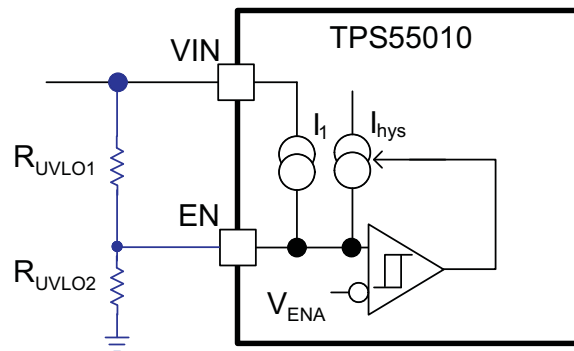
Figure 20. Adjustable Under Voltage Lock Out

$$R_{UVLO1} = \frac{V_{START}\left(\dfrac{V_{ENfalling}}{V_{ENrising}}\right) - V_{STOP}}{I1 \times \left(1 - \dfrac{V_{ENfalling}}{V_{ENrising}}\right) + I_{HYS}}$$

(3)

$$R_{UVLO2} = \frac{R_{UVLO1} \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R_{UVLO1} \times \left(I1 + I_{HYS}\right)}$$

(4)

Adjusting Slow Start Time

A capacitor on the SS pin to ground implements a slow start time to minimize inrush current during startup. The TPS55010 regulates to the lower of the SS pin and the internal reference voltage. The TPS55010 has an internal pull-up current source of 2.2 µA which charges the external slow start capacitor. Equation 5 calculates the required slow start capacitor value where T_{SS} is the desired slow start time in ms, Iss is the internal slow start charging current of 2.2 µA, and V_{REF} is the internal voltage reference of 0.829 V.

If during normal operation, the VIN goes below the UVLO, EN pin pulled below 1.18 V, or a thermal shutdown event occurs, the TPS55010 stops switching. When the VIN goes above UVLO, EN is released or pulled high, or a thermal shutdown is exited, then SS is discharged to below 40 mV before reinitiating a powering up sequence. The VSENSE voltage will follow the SS pin voltage with a 35 mV offset up to 85% of the internal voltage reference. When the SS voltage is greater than 85% on the internal reference voltage the offset increases as the effective system reference transitions from the SS voltage to the internal voltage reference. If no slow start time is needed, the SS pin can be left open. The slow start capacitor should be less than 0.47 µF.

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(uA)}{V_{REF}(V)}$$

(5)

Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS55010 is adjustable over a wide range from 100 kHz to 2000 kHz by placing a maximum of 1070 kΩ and minimum of 42.2 kΩ, respectively, on the RT/CLK pin. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. The RT/CLK is typically 0.5 V. To determine the timing resistance for a given switching frequency, use Equation 6.

To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 130 ns.

$$R_T(k\Omega) = \frac{156000}{f_{sw}(kHz)^{1.0793}}$$

(6)

How to Interface to RT/CLK Pin

The RT/CLK pin can be used to synchronize the regulator to an external system clock. To implement the synchronization feature connect a square wave to the RT/CLK pin through one of the circuit networks shown in Figure 21. The square wave amplitude must transition lower than 0.4V and higher than 2.2V on the RT/CLK pin and have a high time greater than 75 ns. The synchronization frequency range is 300 kHz to 2000 kHz. The rising edge of the PH is synchronized to the falling edge of RT/CLK pin signal.

The external synchronization circuit should be designed in such a way that the device has the default frequency set resistor connected from the RT/CLK pin to ground should the synchronization signal turn off. It is recommended to use a frequency set resistor connected as shown in Figure 21 through another resistor (e.g 50 Ω) to ground for clock signal that are not Hi-Z or tri-state during the off state. The RT resistor value should set the switching frequency close to the external CLK frequency. It is recommended to ac couple the synchronization signal through a 10 pF ceramic capacitor to RT/CLK pin. The first time the CLK is pulled above the CLK threshold the device switches from the RT resistor frequency to PLL mode. The internal 0.5 V voltage source is removed and the CLK pin becomes high impedance as the PLL starts to lock onto the external signal. Since there is a PLL on the regulator the switching frequency can be higher or lower than the frequency set with the external resistor. The device transitions from the resistor mode to the PLL mode and then will increase or decrease the switching frequency until the PLL locks onto the external CLK frequency within 50 microseconds. When the device transitions from the PLL to resistor mode the switching frequency will slow down from the CLK frequency to 150 kHz, then reapply the 0.5V voltage and the resistor will then set the switching frequency.

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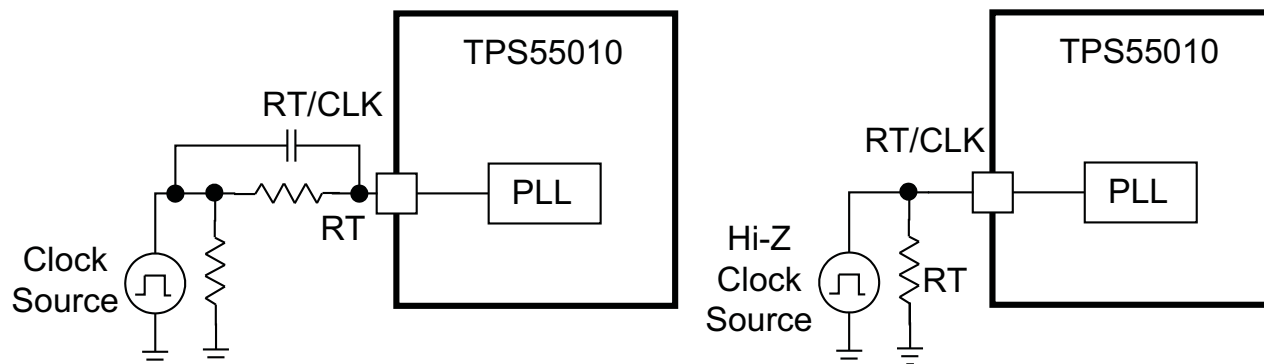
Figure 21. Synchronizing to a System Clock

Overcurrent Protection

The TPS55010 implements a cycle by cycle current limit. During each switching cycle the high side switch current is compared to the voltage on the COMP pin. When the instantaneous switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a switch current limit.

Reverse Overcurrent Protection

The TPS55010 implements low side current protection by detecting the voltage across the low side MOSFET. When the converter sinks current through its low side FET, the control circuit turns off the low side MOSFET if the reverse current is more than 4.5 A

FAULT Pin

The Fault pin output is an open drain MOSFET. The output is pulled low when the VSENSE voltage is below 91% or rising above 108% of the nominal internal reference voltage. It is recommended to use a pull-up resistor between the values of 1kΩ and 100kΩ to a voltage source that is 6 V or less. The Fault pin is in a valid state once the VIN input voltage is greater than 1.6 V. The FAULT pin is pulled low, if the input UVLO or thermal shutdown is asserted, or the EN pin is pulled low.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 171°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 159°C, the device reinitiates the power up sequence by discharging the SS pin to below 40 mV. The thermal shutdown hysteresis is 12°C.

OPERATION OF THE Fly-Buck™ CONVERTER

Figure 22 shows a simplified schematic and the two primary operational states of the Fly-Buck converter. The power supply is a variation of a Flyback converter and consists of a half bridge power stage S_{HS} and S_{LS}, transformer, primary side capacitor, diode and output capacitor. The output voltage is regulated indirectly by using the primary side capacitor voltage, V_{PRI}, as feedback. The Fly-Buck is a portmanteau of flyback and buck since the transformer is connected as a flyback converter and the input to output voltage relationship is similar to a buck derived converter, assuming the converter is operating in steady state and the transformer has negligible leakage inductance.

The C_{PRI} and L_{PRI} are charged by the input voltage source VIN during the time the high side switch S_{HS} is on. During this time, diode D1 is reversed biased and the load current is supplied by output capacitor C_O.

During the off time of S_{HS}, S_{LS} conducts and the voltage on C_{PRI} continues to increase during a portion of the S_{LS} conduction time. The voltage increase is due to the energy transfer from L_{PRI} to C_{PRI}. For the remaining portion of the S_{LS} conduction time, the C_{PRI} voltage decreases because of current in L_{PRI} reverses; see the IL_{PRI} and V_{PRI} waveforms in Figure 23. By neglecting the diode voltage drop, conduction dead time and leakage inductance, the input to output voltage conversion ratio can be derived as shown in Equation 7 from the flux balance in L_{PRI}. It can be seen in Equation 7 that the input to output relationship is the same as a buck-derived converter with transformer isolation. The dc voltage V_{PRI} on the primary side capacitor in Equation 8 has the same linear relationship to the input voltage as a buck converter.
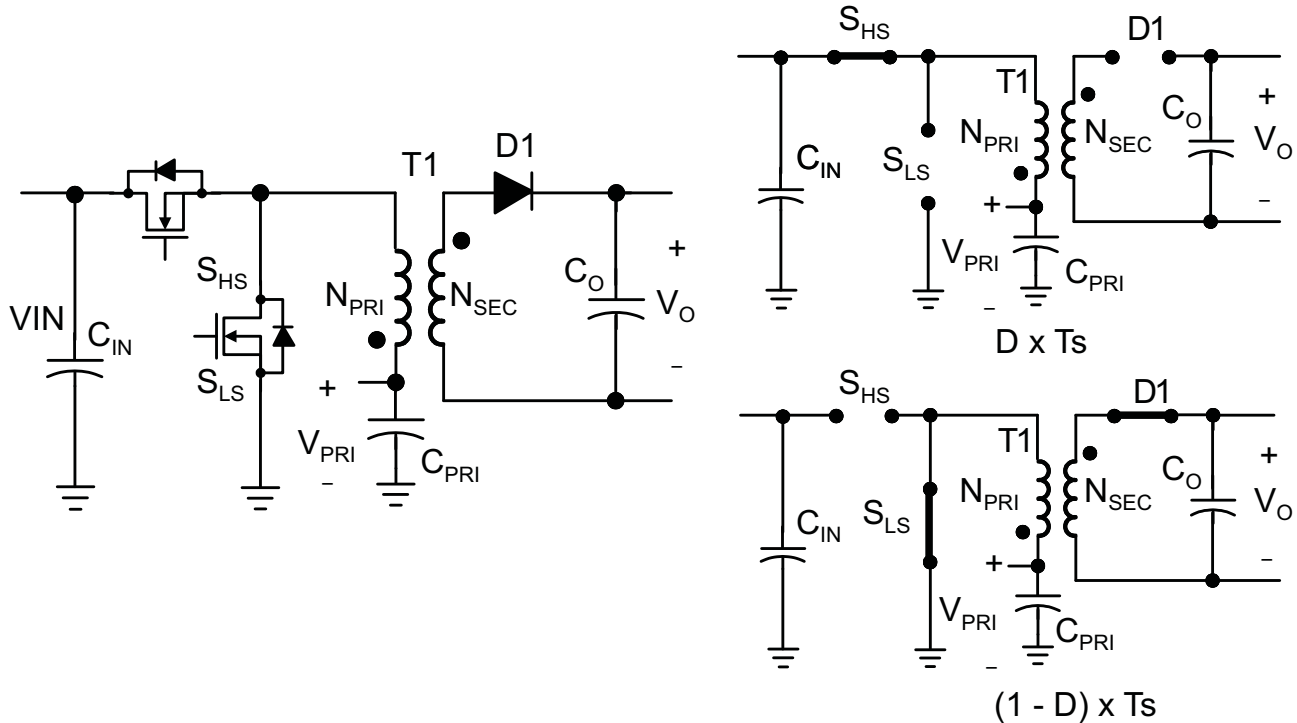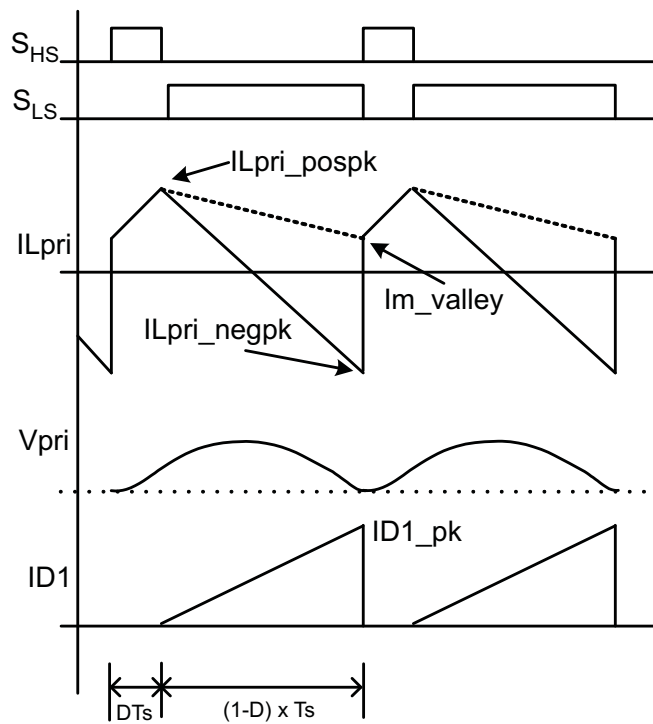

Figure 22.

The small signal model for the Fly-Buck is derived by changing the transformer to the inductor equivalent and reflecting the output filter to the primary side for the circuit shown in Figure 22. Assuming negligible leakage inductance and equivalent series resistance for the capacitors, the V_{PRI} transfer function is similar to the current mode control buck power stage transfer function with the exception that the C_O and load are in parallel with the C_{PRI} only for the 1-D time. Averaging the secondary side components, an approximate transfer function is shown in Equation 9 and pole location in Equation 10. R_O is the secondary side load resistance and the R_{LM} is the dc resistance of the primary. R_i is the inverse of the Comp to PH gm.

$$\frac{V_O}{V_{IN}} = \frac{N_{SEC}}{N_{PRI}} \times D \tag{7}$$

$$\frac{V_{PRI}}{V_{IN}} = D \tag{8}$$

Product Folder Links :TPS55010

$$\frac{\hat{V}_{PRI}}{\hat{V}_C} \approx \frac{R_{LM} + \left(\frac{R_O}{(1-D)} \times \left(\frac{N_{PRI}}{N_{SEC}} \right)^2 \right)}{R_i \times \left(1 + \frac{s}{2 \times \pi \times f_{POLE}} \right)}$$

(9)

$$f_{POLE} = \frac{1}{2 \times \pi \times \left(\frac{R_O}{(1-D)} \times \left(\frac{N_{PRI}}{N_{SEC}} \right)^2 \right) \times \left((1-D) \times C_O \times \left(\frac{N_{SEC}}{N_{PRI}} \right)^2 + C_{PRI} \right)}$$

(10)

Figure 23. Simplified Voltage and Current Waveforms

Overview

The following design example illustrates how to determine the components for a single output isolated power supply. TI offers an EVM (TPS55010EVM-009) with user guide (SLVU459) and excel calculator tool (SLVC363) to expedite the design process. The support material is available on the TPS55010 product folder at www.ti.com.
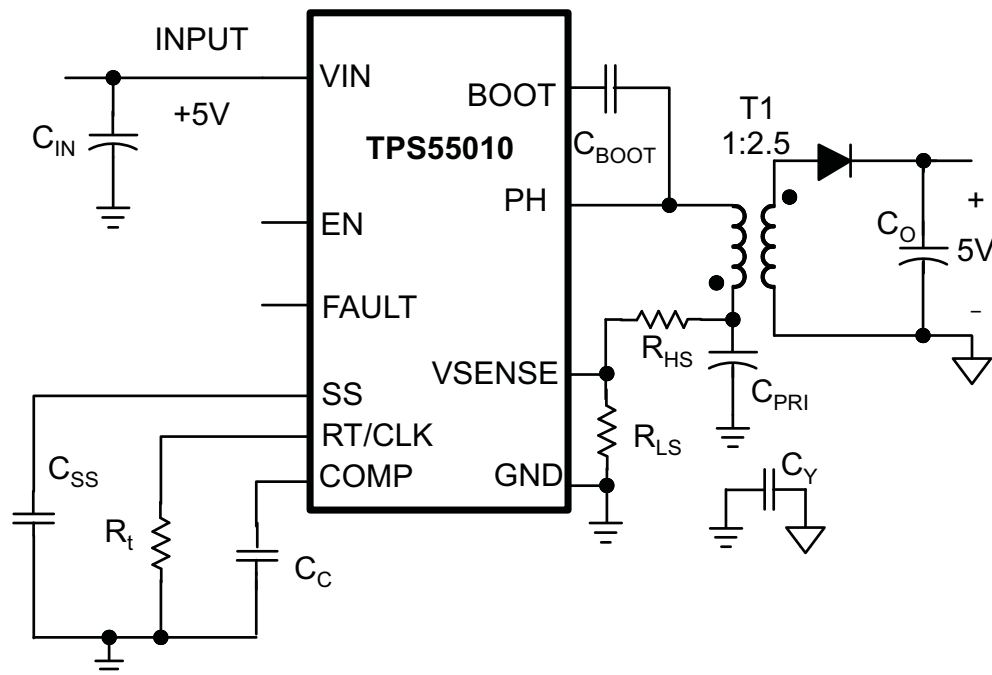
Figure 24. 5V to 5V ISOLATED POWER SUPPLY Schematic

DESIGN GUIDE – STEP-BY-STEP DESIGN PROCEDURE

Input Voltage	5V nominal (4.5V to 5.5V)
Output Voltage	5V
Output Voltage Ripple	<0.5%
Output Current	200mA
Start Voltage	4.5V
Stop Voltage	4V

PRIMARY SIDE VOLTAGE

The output voltage is a function of the primary voltage, transformer turns ratio and the diode voltage. The primary voltage is a function of the duty cycle and input voltage, and is similar to a step down (buck) regulator as shown in Equation 11. The primary side voltage must be lower than the minimum operating input voltage by 500 mV to avoid maximum duty cycle problems and allow sufficient time for energy transfer during the low side power switch on time. Typically, a primary side voltage that is 50% of the input voltage is ideal, but 20% to 80% is acceptable. Using the design constraints, the primary side voltage could be from 3.6 V to 1.1 V. A 2.2 V primary side voltage is selected, and the duty cycle is approximately 45%.

$$D = \frac{V_{PRI}}{V_{IN}}$$

(11)

TURNS RATIO

The transformer turns ratio is calculated using the desired output voltage, diode voltage and the primary voltage. Assuming a diode voltage of 0.5 V, V_{OUT} of 5 V, V_{PRI} of 2.2 V yields a $N_{PRI}:N_{SEC}$ turns ratio of 1:2.5.

$$\frac{N_{SEC}}{N_{PRI}} = \frac{V_{OUT} + V_{FD}}{V_{PRI}}$$

(12)

VOLTAGE FEEDBACK

Selecting 61.9 kΩ for the R_{LS}, R_{HS} is calculated to be 102.4 kΩ using Equation 13. Choose 100 kΩ as the nearest standard value.

It may be necessary to adjust the feedback resistors to optimize the output voltage over the full load range. Usually checking and setting the output voltage to the nominal voltage at 50% load, yields the best results.

$$R_{HS} = R_{LS} \times \left(\frac{V_{PRI} - 0.829V}{0.829V} \right)$$

(13)

SELECTING THE SWITCHING FREQUENCY and PRIMARY INDUCTANCE

The selection of switching frequency is usually a trade-off between efficiency and component size. However, when isolation is a requirement, switching frequency is not the key variable in determining solution size. Low switching frequency operation improves efficiency by reducing gate drive losses and MOSFET and diode switching losses. However, a lower switching frequency operation requires a larger primary inductance which will have more windings and higher dc resistance.

The optimal primary inductance should be selected between two inductance values, L_{OMAX} and L_{OMIN}. The primary inductance should be less than L_{OMAX} to maintain good efficiency and greater than Lomin to avoid the peak switch current from exceeding the high side power switch current limit. Once the primary inductance is selected, check against the low side current limit using the Equation 17 and the high side current limit. For this design example, the switching frequency is selected to be 350 kHz. Using Equation 6, the resistor value is 280 kΩ. L_{OMAX} and Lomin are calculated to be 3.52 µH and 1.17 µH respectively assuming a current limit of 2 A. Selecting a primary inductance of the 2.5 µH, the positive and negative peak current are calculated as 1.204 A and -1.99 A in the primary which do not exceed the current limits of the power switch. The rms currents can be calculated and used to determine the power dissipation in the device.

The magnetizing ripple current is caculated as 1.41 A using Equation 18. The highside FET and lowside FET rms currents are calculated as 0.43 A and 0.61 A, respectively using Equation 19 and Equation 20. The sum of these currents, i.e. 1.04 A is the primary side rms current for the magnetics.

$$L_{OMAX} = \frac{V_{IN} \times D \times (1 - D)}{2 \times \frac{N_{SEC}}{N_{PRI}} \times I_{OUT} \times f_{sw}}$$

(14)

$$L_{OMIN} = \frac{V_{IN} \times D \times (1 - D)}{2 \times f_{sw} \times \left(I_{HSCL} - I_{OUT} \times \frac{N_{SEC}}{N_{PRI}} \right)}$$

(15)

$$ILpri\_pospk \approx I_{OUT} \frac{N_{SEC}}{N_{PRI}} + \frac{V_{IN} \times D \times (1 - D)}{2 \times f_{sw} \times L_{OPRI}}$$

(16)

Product Folder Links :*TPS55010*

$$\text{ILpri\_negpk} \approx - I_{OUT} \frac{N_{SEC}}{N_{PRI}} \times \left(\frac{1 + D}{1 - D} \right) - \frac{V_{IN} \times D \times (1\text{-}D)}{2 \times f_{sw} \times L_{OPRI}}$$

(17)

$$\text{Im\_ripple} = \frac{V_{IN} \times D \times (1 - D)}{f_{sw} \times L_{OPRI}}$$

(18)

$$\text{Ihs\_rms} \approx \left(D \times \left(I_{OUT} \frac{N_{SEC}}{N_{PRI}} \right)^2 + \frac{D}{12} \times \text{Im\_ripple}^2 \right)^{\frac{1}{2}}$$

(19)

$$\text{Ils\_rms} \approx \left(\frac{3 \times D\text{-}1}{3 \times (1\text{-}D)} \times \left(I_{OUT} \times \frac{N_{SEC}}{N_{PRI}} \right)^2 + \frac{\text{Im\_ripple} \times I_{OUT} \times N_{SEC}}{3 \times N_{PRI}} + \frac{1 - D}{12} \times \text{Im\_ripple}^2 \right)^{\frac{1}{2}}$$

(20)

$$\text{ILrms} \approx \text{IHS\_rms} + \text{ILS\_rms}$$

(21)

PRIMARY SIDE CAPACITOR

The ΔV_{PRI} voltage should be less than 10% of V_{PRI}. The rated RMS current of C_{PRI} should be greater than Equation 22. It is desirable to have a larger primary capacitance to minimize ripple but this will slow the transient response. For this design example, assuming the ΔV_{PRI} is 0.22 V, the primary side capacitance is 4.74 µF and the rms current is 1.04 A. A 4.7 µF/10V X5R ceramic capacitor is used.

$$I_{CPRI\_rms} = \text{ILrms}$$

(22)

$$I_{CPRI\_ch} \approx IL_{CPRI}\_\text{pospk} \times \sqrt{ \frac{D + (1 - D) \times \dfrac{IL_{PRI}\_\text{pospk}}{IL_{PRI}\_\text{pospk} - IL_{PRI}\_\text{negpk}}}{3} }$$

(23)

$$t_{CPRI} \approx \frac{D}{f_{SW}} + \frac{(1 - D)}{f_{SW}} \times \frac{IL_{PRI}\_\text{pospk}}{IL_{PRI}\_\text{pospk} - IL_{PRI}\_\text{negpk}}$$

(24)

$$C_{PRI} = \frac{I_{CPRI\_ch} \times t_{CPRI}}{\Delta V_{PRI}}$$

(25)

SECONDARY SIDE DIODE

The diode should be selected to handle the voltage stress and rms current calculated in Equation 26 and Equation 27. Typically, a low duty cycle or high turns ratio design will have a larger voltage stress on the diode. At the maximum input voltage of 5.5V, the Vdiode_max voltage is calculated at 13.3 V. The rms current is calculated as 0.31 A. The diode peak current is 0.71 A using Equation 28 and the power dissipated in the diode is 0.1 W. The B120 diode is used which is rated for 20 V and 1 A.

$$Vdiode\_max = \left(V_{IN} - V_{PRI}\right) \times \frac{N_{SEC}}{N_{PRI}} + V_{OUT}$$
(26)

$$Idiode\_rms = 2 \times I_{OUT} \times \left(\frac{1}{3 \times (1 - D)}\right)^{\frac{1}{2}}$$
(27)

$$Idiode\_peak = 2 \times \frac{I_{OUT}}{1 - D}$$
(28)

$$Pdiode = V_{fd} \times I_{OUT}$$
(29)

SECONDARY SIDE CAPACITOR

The ΔV_{CO} voltage should be 0.25% to 1% of V_{CO} voltage. The converter transfers energy each switching period to the secondary, since the converter has primary side feedback, at light or no load conditions the output voltage may rise above the desired output. If the application will experience a no load condition, attention to the capacitor voltage ratings should be considered. Adding a ballast load, zener diode or linear regulator can help prevent the overvoltage at light or no load.

The output capacitance is calculated to be 10.1 µF using Equation 30 and the rms current is 0.24 A.

Two 10 µF/10V X5R ceramic capactors are used. The effective capacitance is lower than the 20 µF, because of dc voltage bias.

$$C_O = \frac{I_{OUT} \times D}{f_{SW} \times \Delta V_{CO}}$$
(30)

$$IC_{O\_}rms = \sqrt{Idiode\_rms^2 - I_{OUT}^2}$$
(31)

INPUT CAPACITOR

The ΔV_{CIN} voltage should be 0.25% to 1% of V_{IN}. The TPS55010 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 2.2 µF of effective capacitance or larger coupled to VIN and GND pins and in some applications additional bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS55010.

The input ripple current can be calculated using Equation 33. The value of a ceramic capacitor varies significantly overtemperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable overtemperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. In applications with significant unload transients, the bulk input capacitance must be sized to include energy transfer from the primary side capacitor to the input capacitor.

The input capacitance is calculated 12.6 µF using Equation 32 and the rms current is 0.46 A. A 47 µF/10V X5R ceramic capacitor is used on the input. A 0.1 µF ceramic capacitor is placed as close to the VIN and GND pins as possible for a good bias supply.

$$C_{IN} = \frac{I_{OUT} \dfrac{N_{SEC}}{N_{PRI}} \times D}{f_{SW} \times \Delta V_{CIN}}$$

$$\hspace{10cm} (32)$$

$$ICin\_rms = ILpri\_pospk \times \sqrt{\frac{D}{3}}$$

$$\hspace{10cm} (33)$$

Y – Capacitor

The Y-capacitor should be used between the primary and secondary to attenuate common mode (CM) noise in noise sensitive applications. When connecting the primary and secondary grounds with a large loop area, the primary side switching noise can be injected via the interwinding capacitance of the isolation transformer, creating common mode noise in the secondary. A Y-capacitor can be used to provide a local return path for these currents with a small capacitor connected between the secondary ground and the primary ground. The voltage rating of the Y-capacitor should be equivalent to the transformer insulation voltage. If the converter is used for safety isolation there is an upper limit on the amount of capacitance. The inter-winding capacitances of the transformer and maximum leakage current (e.g. UL60950 Class I equipment leakage current <3.5 mA) allowed by the safety standard will set the maximum value. It is not recommended to use the Y-capacitor in applications which experience large voltage transients such as a floating gate drive supply in a power inverter.

SLOW START CAPACITOR

To minimize overshoot during power up or recovery from an overload condition a slow start capacitor is used. A 35-ms slow start is desired and using Equation 5 a 0.1 µF capacitor is calculated.

BOOTSTRAP CAPACITOR SELECTION

A 0.1 µF ceramic capacitor must be connected between the BOOT to PH pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10 V or higher voltage rating.

UVLO Resistors

Using the start and stop voltages of 4.5 V and 4 V, respectively, the uvlo resistors 71.5 kΩ and 26.7 kΩ are calculated using Equation 3 and Equation 4.

COMPENSATION

There are several methods used to compensate DC/DC regulators. The method presented here ignores the effects of the slope compensation that is internal to the device. Since the slope compensation is ignored, the actual cross over frequency should be lower than the cross over frequency used in the calculations. This method assumes the cross over frequency is between the modulator pole and 20 times greater the modulator pole. When choosing a crossover frequency with the single compensation capacitor method (i.e. type 1), use the lower end of the recommended range when developing a supply if the primary capacitor ripple voltage is <1%. Type 2 or 3 compensation should be considered if a low primary ripple design is preferred. To get started, the modulator pole frequency, f_{POLE}, determined from Equation 10 should be used to select the crossover frequency, f_{CO}. In this example, 5 kHz is selected as the crossover frequency. The next step is to determine the compensation gain, A_{COMP}, at the crossover frequency to compensate the loop. Equation 35 uses the dc gain of the power stage, modulator pole, and crossover frequency to estimate the gain. R_i is the current sense gain which is the inverse of the Comp to IPH transconductance, which is 7.5 A/V. 10.1 dB is calculated for A_{COMP}. The compensation pole frequency f_{COMP_POLE} can be calculated using Equation 36. A_{OL} in Equation 36 is the open loop gain of the error amplifier and is 500 V/V. f_{COMP_POLE} is calculated as 8.27 Hz. Using Equation 37, C_{COMP} is calculated to be 0.01 µF.

$$\frac{w_{POLE}}{2 \times \pi} < f_{CO} < 20 \times \frac{w_{POLE}}{2 \times \pi}$$

(34)

$$A_{COMP} = 20 \times \log\left(\frac{R_{LM} + \frac{R_O}{(1-D)}}{R_i}\right) - 20 \times \log\left(\frac{2 \times \pi \times f_{CO}}{2 \times \pi \times f_{POLE}}\right)$$

(35)

$$f_{COMP\_POLE} = \frac{V_{PRI}}{10^{\frac{Acomp}{20}} \times A_{OL} \times V_{REF}} \times f_{CO}$$

(36)

$$C_{COMP} = \frac{1}{2 \times \pi \times \frac{A_{OL}}{gmea} \times f_{COMP\_POLE}} - \frac{gmea}{2 \times \pi \times BW}$$

(37)

VENDORS

At the time of the product release, there are two catalog transformers available for the TPS55010. The transformers are available at Digikey or directly through Wurth Elektronics Midcom.

Table 2.

Part Number	Specifications	Vendor
750311880	2.5 µH, 1:2.5 Turns Ratio, Basic Insulation, 2500 Vrms	Wurth Elektronics Midcom www.we-online.com/midcom
750311780	2.0 µH, 1:8:8 Turns Ratio, Basic Insulation, 2000 Vrms	

Product Folder Links :*TPS55010*

HOW TO SPECIFY A Fly-Buck TRANSFORMER

If a catalog or standard off the shelf transformer is not available, use this section to determine the transformer specifications to supply a vendor. Selecting the magnetizing inductance is similar to the conventional flyback converter operating in continuous conduction mode. One distinction is the voltage across the transformer during the on time is different. The voltage is the difference in the input voltage and voltage across the primary capacitor. For a conventional flyback, only the input voltage is across the primary. Another distinction is the peak current in the primary is the negative current peak.

Table 3. Transformer Design Form

Input Voltage Range (V)			
Output Voltage (V)			
Output Current (A)			
Operating Mode	Continuous Conduction Mode		
Primary Voltage (V)	Use Equation 11 and Equation 12		
Duty Cycle Range (%)	Use Equation 11		
Turns Ratio (N_{PRI}:N_{SEC})	Use Equation 12		
Switching Frequency (Hz)	Use Equation 14 to Equation 17		
Primary Inductance (H)	Use Equation 14 to Equation 17		
Peak Current Positive (A)	Use Equation 14 to Equation 17		
Peak Current Negative (A)	Use Equation 14 to Equation 17		
Insulation Requirements	Functional, Basic, Reinforced		
Regulatory Agencies/Specification	UL, IEC		
Dielectric Withstand Voltage		AC	DC
Working Voltage		AC	DC
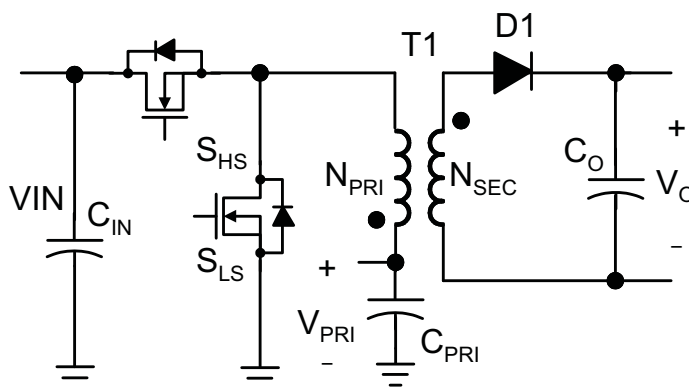
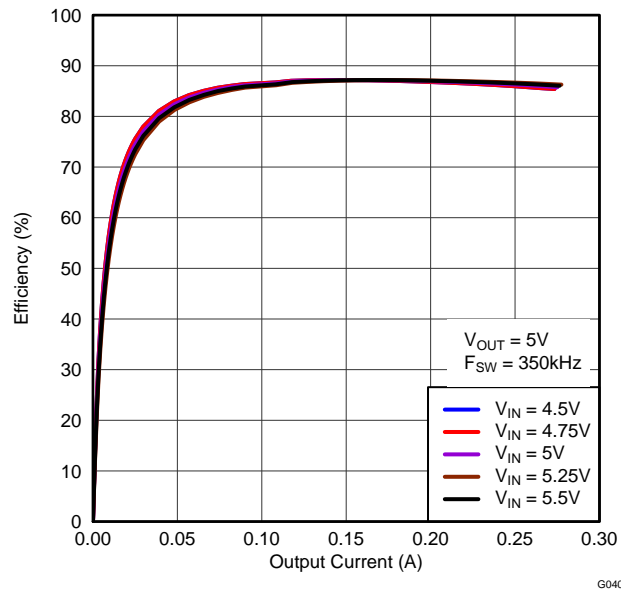**Figure 25. Topology**

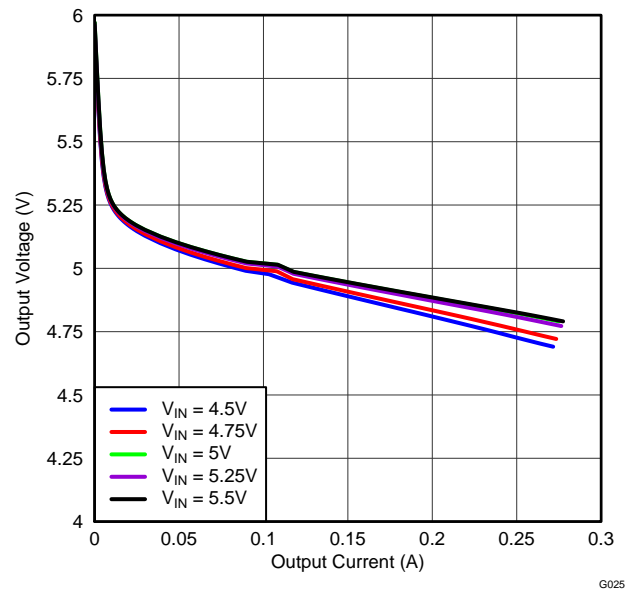## CHARACTERISTICS

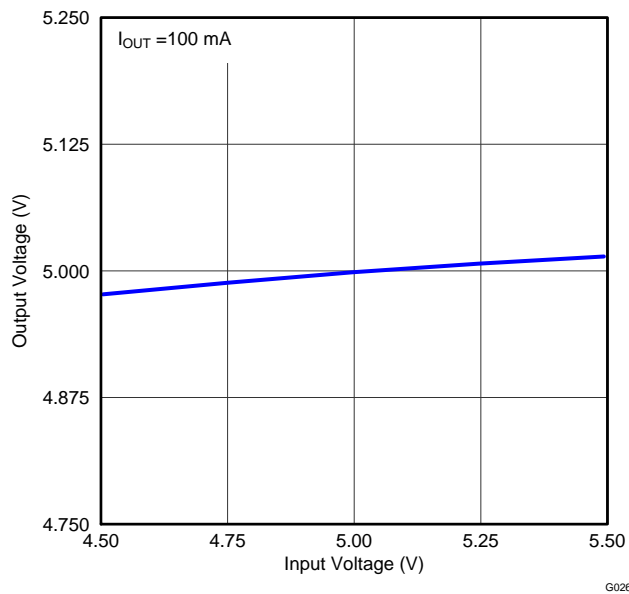Figure 26. Efficiency vs Output Current

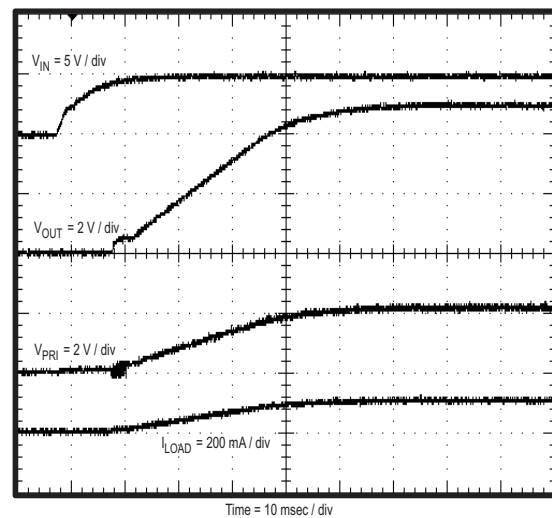Figure 27. Output Voltage vs Output Current

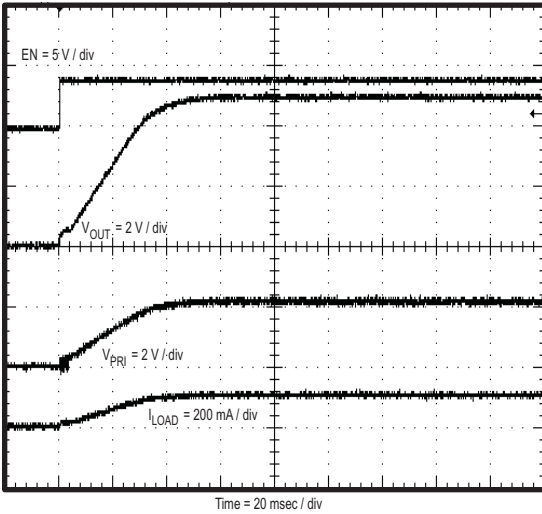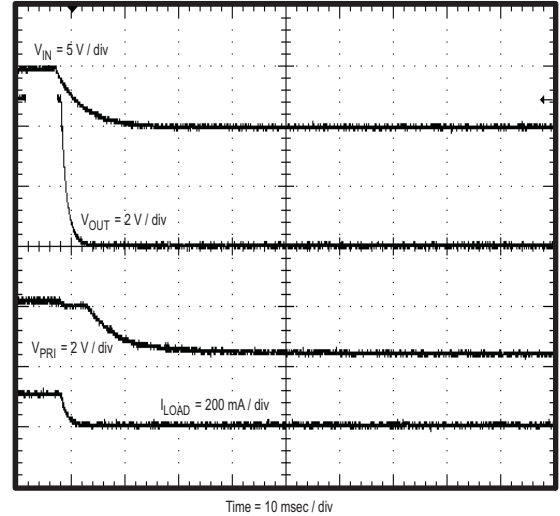Figure 28. Output Voltage vs Input Voltage

Figure 29. Power Up with Input Voltage

Product Folder Links :*TPS55010*
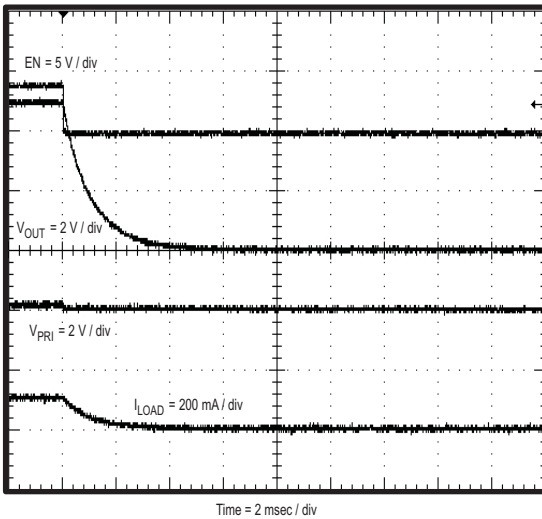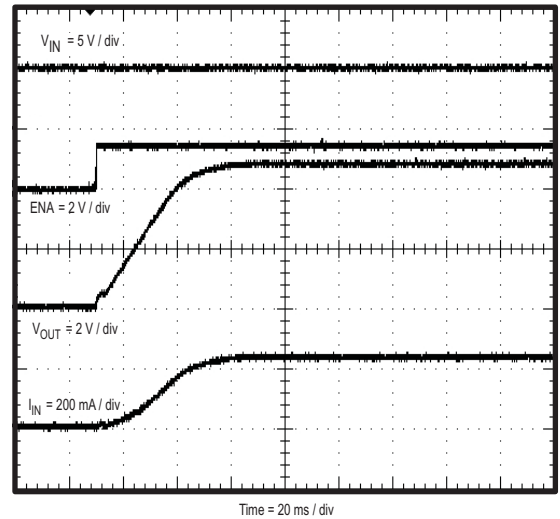
Figure 30. Power Up with Enable Pin

Figure 31. Power Down with Input Voltage

Figure 32. Power Down with Enable Pin

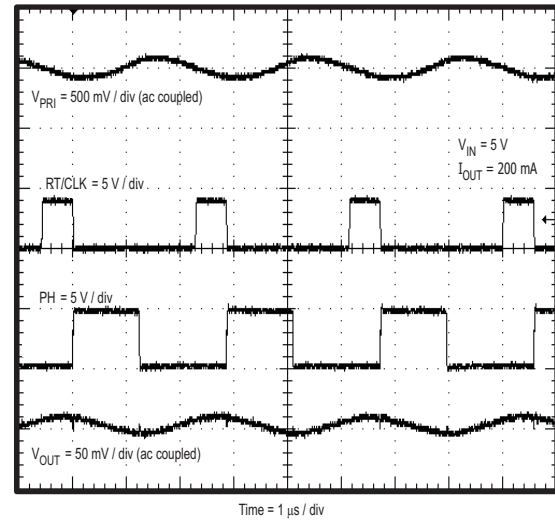**Figure 33. Inrush Current During Power Up**

V$_{IN}$ = 50 mV / div (ac coupled)

RT/CLK = 5 V / div

V$_{IN}$ = 5 V
I$_{OUT}$ = 200 mA

PH = 5 V / div

V$_{OUT}$ = 50 mV / div (ac coupled)

Time = 1 μs / div
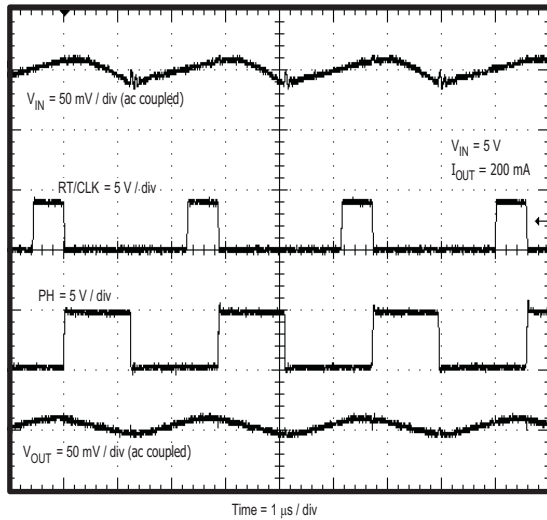
Figure 34. Output Ripple Voltage

V$_{PRI}$ = 500 mV / div (ac coupled)

RT/CLK = 5 V / div

V$_{IN}$ = 5 V
I$_{OUT}$ = 200 mA

PH = 5 V / div

V$_{OUT}$ = 50 mV / div (ac coupled)

Time = 1 μs / div

Figure 35. Synchronize to External Clock

V$_{OUT}$ = 200 mV / div (ac coupled)

I$_{LOAD}$ = 100 mA / div

V$_{IN}$ = 5 V

Time = 100 μs / div
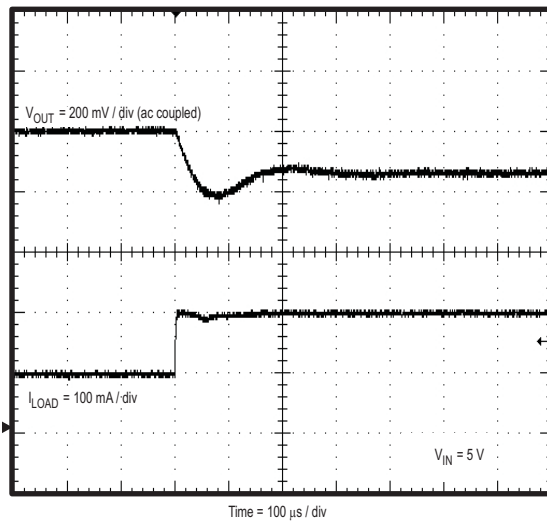
Figure 36. Load Step Response

V$_{OUT}$ = 200 mV / div (ac coupled)

I$_{LOAD}$ = 100 mA / div

V$_{IN}$ = 5 V

Time = 100 μs / div
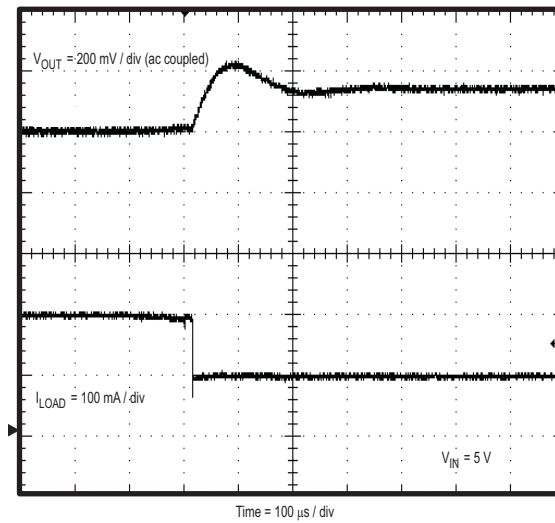
Figure 37. Load Step Response
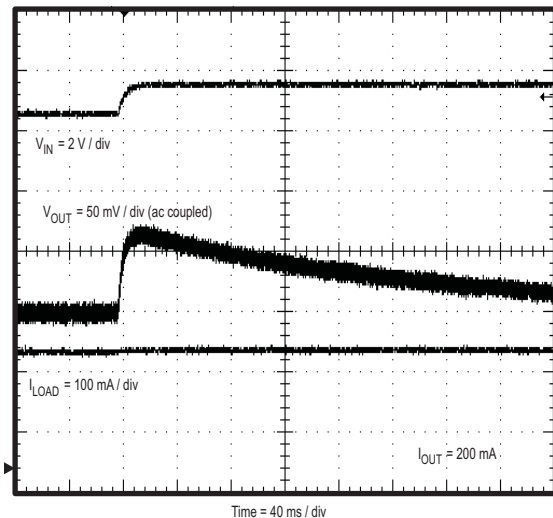
Figure 38. Line Step Response

Figure 39. Line Step Response

Figure 40. Steady State Waveforms

Figure 41. Frequency Response

Table 4. Reference Design for Common Applications

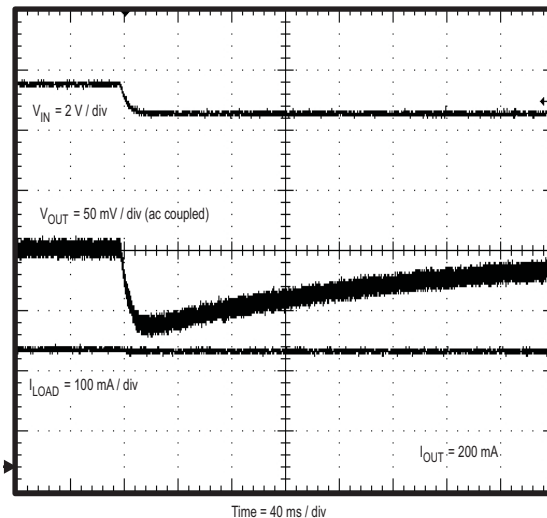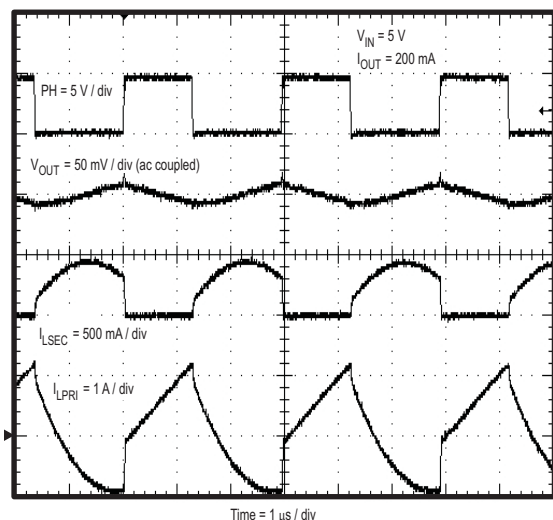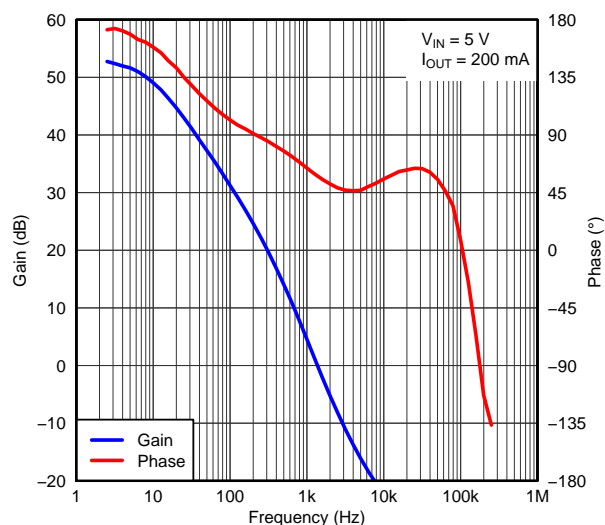|	5V to 5V/0.2A	3.3V to 5V/0.2A	5V to 3.3V/0.3A	3.3V to 3.3V/0.3A
C_{IN}	47 µF X5R 6.3V	100 µF X5R 6.3V	47 µF X5R 6.3V	100 µF X5R 6.3V
C_{OUT}	2 x 10 µF X5R 10V	47 µF X5R 6.3V	22 µF X5R 6.3V	47 µF X5R 6.3V
C_{PRI}	4.7 µF X5R 10V	22 µF X5R 6.3V	10 µF X5R 6.3V	10 µF X5R 6.3V
C_{BOOT}	0.1 µF X5R 10V	0.1 µF X5R 10V	0.1 µF X5R 10V	0.1 µF X5R 10V
C_{SS}	0.1 µF X5R 10V	0.1 µF X5R 10V	0.1 µF X5R 10V	0.1 µF X5R 10V
C_C	0.01 µF X5R 10V	0.022 µF X5R 10V	0.01 µF X5R 10V	0.01 µF X5R 10V
R_{HS}	16.5k	16.5k	8.25k	8.25k
R_{LS}	10k	10k	10k	10k
R_T	280k	511k	332k	511k
T1	750311880 Wurth Electronics Midcom	750311880 Wurth Electronics Midcom	750311880 Wurth Electronics Midcom	750311880 Wurth Electronics Midcom
D1	B120	B120	B120	B120

POWER DISSIPATION
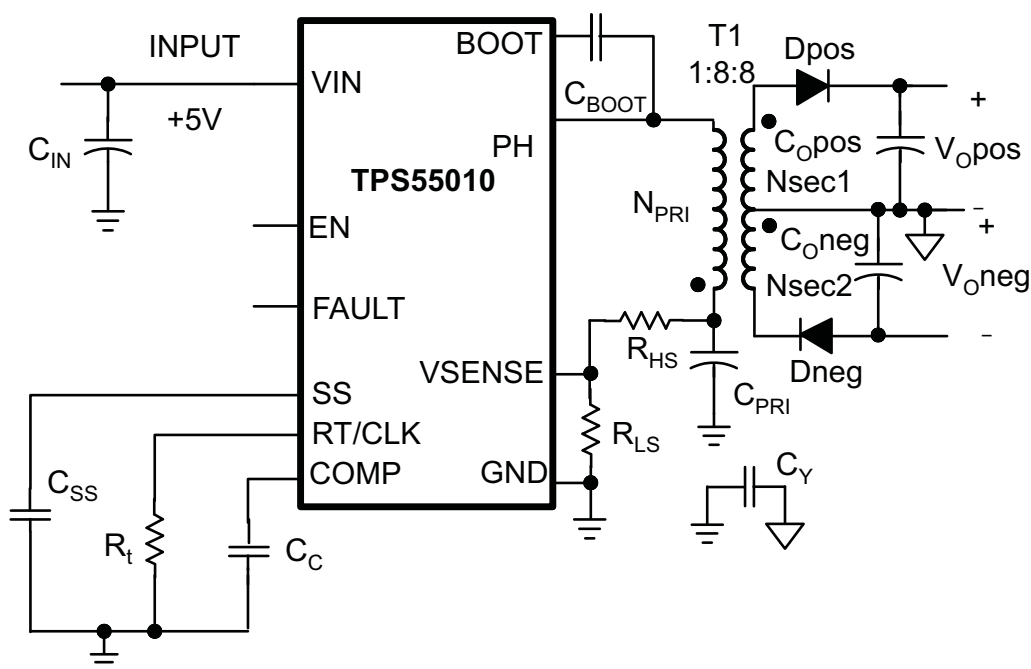
Figure 42. 5V to 15V/-15V Isolated Power Supply

DESIGN GUIDE – STEP-BY-STEP DESIGN PROCEDURE

Table 5.

Input Voltage	5V nominal (4.5V to 5.5V)
Positive Output Voltage, Vopos	+15V
Negative Output Voltage, Voneg	-15V
Output Voltage Ripple	<0.5%
Output Current Iopos, Ioneg	40mA
Start Voltage	4.5V
Stop Voltage	4V

PRIMARY SIDE VOLTAGE FOR DUAL OUTPUT

Similar to the single output design, the dual output voltages are a function of the primary voltage, transformer turns ratio and the diode voltages. Using the same design constraints as the single, the primary side voltage could be from 3.6 V to 1.1 V. A 1.93 V primary side voltage is selected, and the duty cycle is approximately 38.5%.

$$D = \frac{V_{PRI}}{V_{IN}}$$

(38)

Turns Ratio

The transformer turns ratio is calculated using the desired output voltages, diode voltages and the primary voltage. Assuming diode voltages of 0.5 V, $V_O$pos of 15 V, $V_O$neg of -15V and a V_{PRI} of 1.93 V yields a N_{PRI} x N_{SEC1} x N_{SEC2} turns ratio of 1:8:8. Since the TPS55010 is flexible on the adjusting the primary side, a couple iterations of selecting turns ratio may help find a solution that is good for multiple applications with the same transformer.

$$\frac{N_{SEC1} + N_{SEC2}}{N_{PRI}} = \frac{V_{OPOS} - V_{ONEG} + 2 \times V_{FD}}{V_{PRI}}$$

(39)

VOLTAGE FEEDBACK

Selecting 10 kΩ for the R_{LS} , R_{HS} is calculated to be 13.28 kΩ using Equation 40. Choose 13.7 kΩ as the nearest standard value.

$$R_{HS} = R_{LS} \times \left(\frac{V_{PRI} - 0.829V}{0.829V} \right)$$

(40)

SELECTING THE SWITCHING FREQUENCY and PRIMARY INDUCTANCE

For this design example, the switching frequency is selected to be 400 kHz. Using Equation 6, the timing resistor value is 243 kΩ. $L_O$max and $L_O$min are calculated to be 2.31 µH and 1.09 µH respectively assuming a current limit of 2 A. Selecting a primary inductance of the 2 µH, the positive and negative peak current are calculated as 1.38 A and -2.19 A in the primary which do not exceed the current limits of the power switch. The rms currents can be calculated and used to determine the power dissipation in the device. The magnetizing ripple current is calculated as 1.48 A using Equation 46.

The highside FET and lowside FET rms currents are calculated as 0.478 A and 0.681 A, respectively using Equation 47 and Equation 48. The sum of these currents, i.e. 1.16 A is the primary side rms current for the magnetics.

$$I_{OPN} = \left(I_{OPOS} \frac{N_{SEC1}}{N_{PRI}} + I_{ONEG} \frac{N_{SEC2}}{N_{PRI}} \right)$$

(41)

$$L_{OMAX} = \frac{V_{IN} \times D \times (1 - D)}{2 \times I_{OPN} \times f_{SW}}$$

(42)

$$L_{OMIN} = \frac{V_{IN} \times D \times (1 - D)}{2 \times f_{SW} \times (I_{HSCL} - I_{OPN})}$$

(43)

$$ILpri\_pospk \approx I_{OPN} + \frac{V_{IN} \times D \times (1 - D)}{2 \times f_{SW} \times L_{OPRI}}$$

(44)

$$ILpri\_negpk \approx -I_{OPN} \times \left(\frac{1 + D}{1 - D} \right) - \frac{V_{IN} \times D \times (1 - D)}{2 \times f_{SW} \times L_{OPRI}}$$

(45)

$$Im\_ripple = \frac{V_{IN} \times D \times (1 - D)}{f_{sw} \times L_{OPRI}}$$

(46)

$$IHS\_rms \approx \left(D \times I_{OPN}^2 + \frac{D}{12} \times Im\_ripple^2 \right)^{\frac{1}{2}}$$

(47)

$$ILS\_rms \approx \left(\frac{3 \times D - 1}{3 \times (1 - D)} \times I_{OPN}^2 + \frac{Im\_ripple}{3} \times I_{OPN} + \frac{1 - D}{12} \times Im\_ripple^2 \right)^{\frac{1}{2}}$$

(48)

PRIMARY SIDE CAPACITOR

The ΔV_{PRI} voltage should be less than 10% of V_{PRI}. The rated RMS current of C_{PRI} should be greater than Equation 49. It is desirable to have a larger primary capacitance to minimize ripple but this will slow the transient response. For this design example, the charging current and time need to be calculated using Equation 50 and Equation 51. The I_{CPRI_ch} is 0.63 A and the t_{CPRI} is 1.56 µs. Assuming the ΔV_{PRI} is 0.193 V, the primary side capacitance is 5.09 µF using Equation 49. The rms current is 1.16 A from Equation 49. A 10 µF/25 V X5R ceramic capacitor is used.

$$ICPRI\_rms \approx ILS\_rms + IHS\_rms$$

(49)

$$I_{CPRI\_ch} \approx ILpri\_pospk \times \sqrt{\frac{D + (1 - D) \times \dfrac{ILpri\_pospk}{ILpri\_pospk - ILpri\_negpk}}{3}}$$

(50)

$$t_{CPRI} \approx \frac{D}{f_{SW}} + \frac{(1 - D)}{f_{SW}} \times \frac{ILpri\_pospk}{ILpri\_pospk - ILpri\_negpk}$$

(51)

$$C_{PRI} = \frac{\left(I_{CPRI\_ch} \times t_{CPRI} \right)}{\Delta V_{PRI}}$$

(52)

SECONDARY SIDE DIODE

The diodes should be selected to handle the voltage stresses and rms currents calculated in Equation 53 and Equation 55. Typically, a low duty cycle or high turns ratio design will have a larger voltage stress on the diode

At the maximum input voltage of 5.5 V, the V_{diode_max} voltage is calculated at 43.56 V. The rms current is calculated as 0.059 A. The diode peak current is 0.130 A using Equation 54 and the power dissipated in the diode is 0.02 W. The B1100 diode will be used which is rated for 100 V and 1 A.

$$V_{diode\_max} = (V_{IN\_max} - V_{PRI}) \times \frac{N_{SEC1}}{N_{PRI}} + V_{OPOS} = (V_{IN\_max} - V_{PRI}) \times \frac{N_{SEC2}}{N_{PRI}} + V_{ONEG}$$

(53)

$$I_{diode\_peak} = 2 \times \frac{I_{OPOS}}{1 - D} = 2 \times \frac{I_{ONEG}}{1 - D} \tag{54}$$

$$I_{diode\_rms} = 2 \times I_{OPOS} \times \left(\frac{1}{3 \times (1 - D)}\right)^{\frac{1}{2}} = 2 \times I_{ONEG} \times \left(\frac{1}{3 \times (1 - D)}\right)^{\frac{1}{2}} \tag{55}$$

$$P_{diode} = V_{FD} \times I_{OPOS} = V_{FD} \times I_{ONEG} \tag{56}$$

SECONDARY SIDE CAPACITOR

The ΔV_{COPOS} and ΔV_{CONEG} voltage should be 0.25% to 1% of the respective nominal voltage. The converter transfers energy each switching period to the secondary, since the converter has primary side feedback, at light or no load conditions the output voltage may rise above the desired output. If the application will experience a no load condition, attention to the capacitor voltage ratings should be considered. Adding a ballast load, zener diode or linear regulator can help prevent the overvoltage at light or no load.

The output capacitance is calculated to be 0.51 µF assuming a ΔV_{COPOS} of 75 mV using Equation 57 and the rms current is 0.043 A from Equation 58. 10 µF/25 V capacitors are used for V_{OPOS} and V_{ONEG} output.

$$C_O = \frac{I_{OPOS} \times D}{f_{SW} \times \Delta V_{COPOS}} = \frac{I_{ONEG} \times D}{f_{SW} \times \Delta V_{CONEG}} \tag{57}$$

$$I_{CO\_rms} = \sqrt{I_{diode\_rms}^2 - I_{OPOS}^2} \tag{58}$$

INPUT CAPACITOR

The ΔV_{CIN} voltage should be 0.25% to 1% of V_{IN}. The TPS55010 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 2.2 µF of effective capacitance or larger coupled to VIN and GND pins and in some applications additional bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The input ripple current can be calculated using Equation 60, select a capacitor with a larger ripple current rating.

In applications with significant unload transients, the bulk input capacitance must be sized to include energy transfer from the primary side capacitor to the input capacitor. The input capacitance is calculated 12.4 µF using Equation 59 and the rms current is 0.495 A. A 47 µF/10 V X5R ceramic capacitor is used on the input. A 0.1 µF ceramic capacitor is placed as close to the VIN and GND pins as possible for a good bias supply.

$$C_{IN} = \frac{I_{OPN} \times D}{f_{SW} \times \Delta V_{CIN}} \tag{59}$$

$$I_{CIN\_rms} = ILpri\_pospk \times \sqrt{\frac{D}{3}} \tag{60}$$

COMPENSATION

Similar to the single output design, there are several methods used to compensate DC/DC regulators. Since the slope compensation is ignored, the actual cross over frequency could be lower than the cross over frequency used in the calculations. This method assumes the cross over frequency is between the modulator pole and 20 times greater the modulator pole. When choosing a crossover frequency with the single capacitor compensation method (i.e. type 1), use the lower end of the recommended range when developing a supply if the primary

capacitor ripple voltage is <1%. Type 2 or 3 compensation should be considered if a low primary ripple design is preferred. To get started, the modulator pole frequency, f_{POLE}, determined from Equation 61 should be used to select the crossover frequency, f_{CO}. In this example, 0.4 kHz is selected as the crossover frequency. The next step is to determine the compensation gain, A_{COMP}, at the crossover frequency to compensate the loop. Equation 64 uses the dc gain of the power stage, modulator pole, and crossover frequency to estimate the gain. R_i is the current sense gain which is the inverse of the C_{COMP} to I_{PH} transconductance, which is 7.5 A/V. 11.58 dB is calculated for A_{COMP}. The compensation pole frequency f_{COMP_POLE} can be calculated using Equation 65. A_{OL} in Equation 65 is the open loop gain of the error amplifier and is 500 V/V. f_{COMP_POLE} is calculated as 0.49 Hz. Using Equation 66, C_{COMP} is calculated to be 0.159 µF. A 0.1 µF capacitor will be used for C_{COMP}.

$$\frac{\hat{V}_{PRI}}{\hat{V}_C} \approx \frac{R_{LM} + \left(\frac{V_{PRI}}{I_{OPN} \times (1-D)} \times \left(\frac{N_{PRI}}{N_{SEC}}\right)^2 \right)}{R_i \times \left(1 + \frac{s}{2 \times \pi \times f_{POLE}}\right)} \tag{61}$$

$$f_{POLE} = \frac{1}{2 \times \pi \times \left(\frac{V_{PRI}}{I_{OPN}} \times \frac{1}{(1-D)}\right) \times \left((1-D) \times \left(\frac{C_{OPOS} \times C_{ONEG}}{C_{OPOS} + C_{ONEG}} \times \left(\frac{N_{SEC1} + N_{SEC2}}{N_{PRI}}\right)^2\right) + C_{PRI}\right)} \tag{62}$$
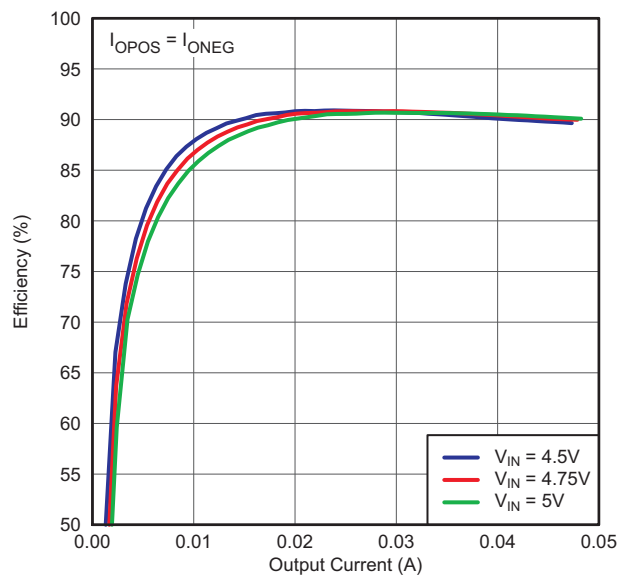
$$\frac{w_{POLE}}{2 \times \pi} < f_{CO} < 20 \times \frac{w_{POLE}}{2 \times \pi} \tag{63}$$

$$A_{COMP} = 20 \times \log\left(\frac{R_{LM} + \frac{V_{PRI}}{I_{OPN} \times (1-D)}}{R_i}\right) - 20 \times \log\left(\frac{2 \times \pi \times f_{CO}}{2 \times \pi \times f_{POLE}}\right) \tag{64}$$
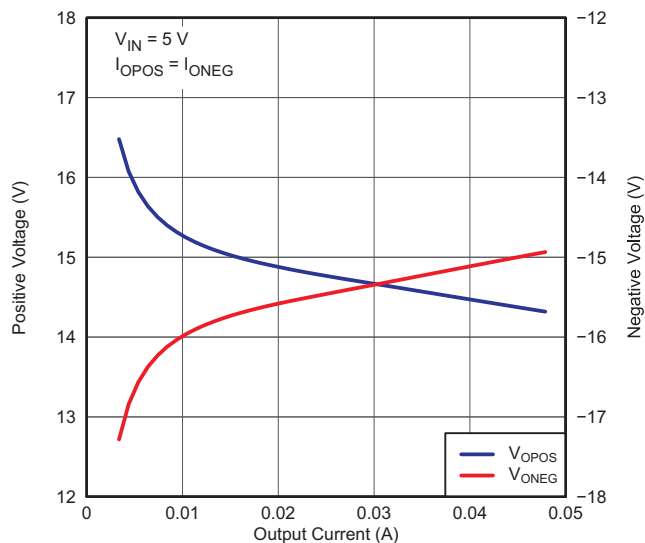
$$f_{COMP\_POLE} = \frac{V_{PRI}}{10^{\frac{Acomp}{20}} \times A_{OL} \times V_{REF}} \times f_{CO} \tag{65}$$

$$C_{COMP} = \frac{1}{2 \times \pi \times \frac{A_{OL}}{gmea} \times f_{COMP\_POLE}} - \frac{gmea}{2 \times \pi \times BW} \tag{66}$$
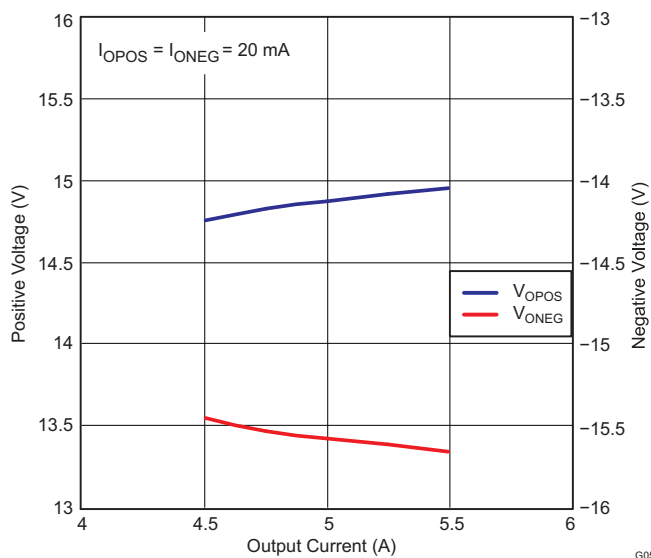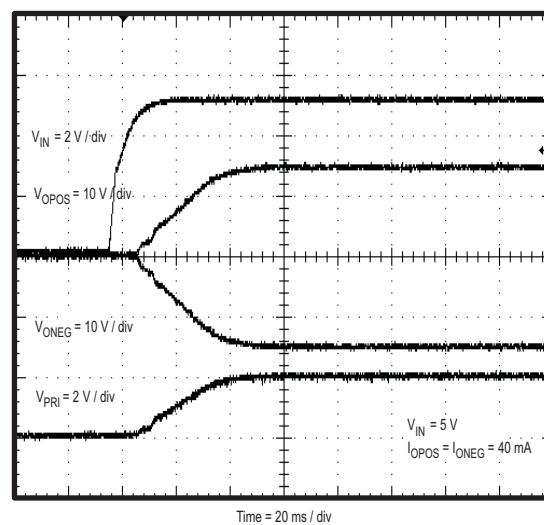
CHARACTERISTICS

Figure 43. Efficiency vs Output Current

Figure 44. Output Voltage vs Output Current
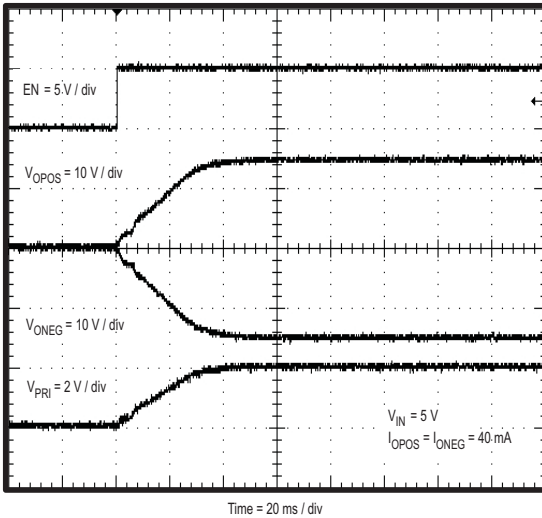

Figure 45. Output Voltage vs Input Voltage
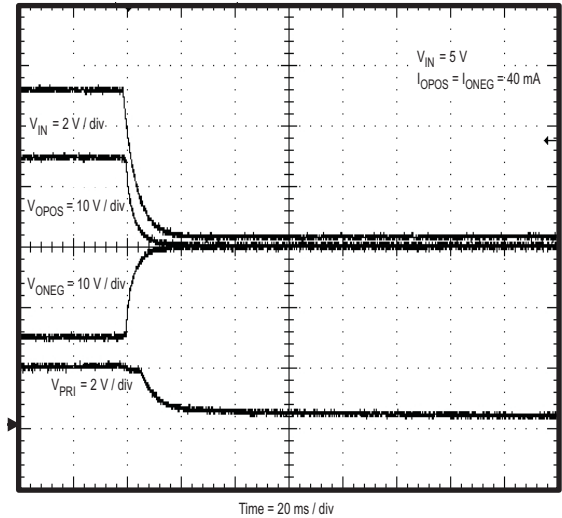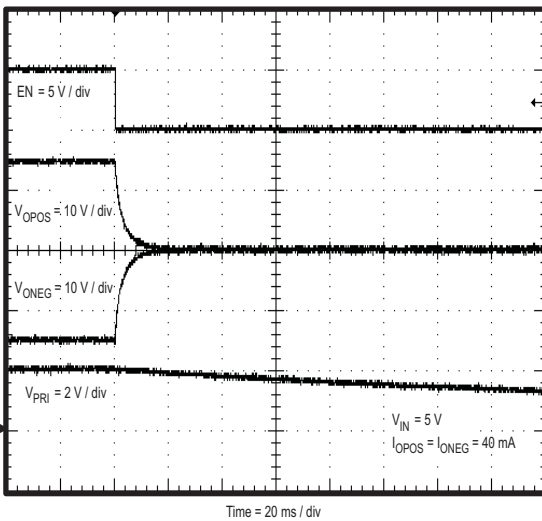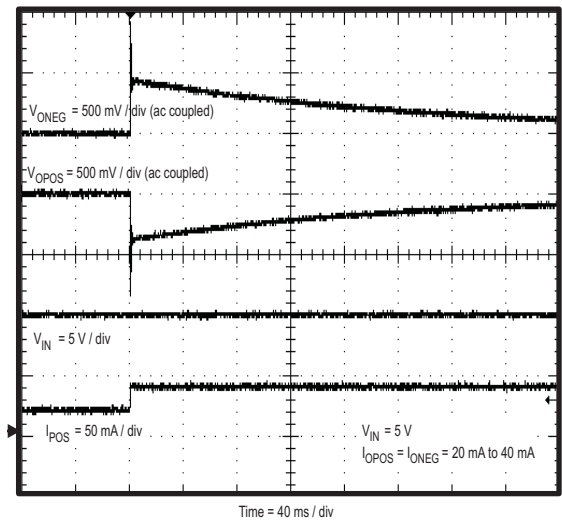

Figure 46. Power Up with Input Voltage

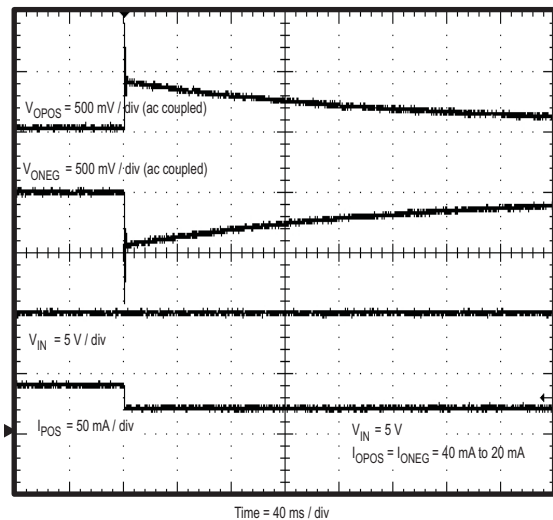**Figure 47. Power Up with Enable Pin**

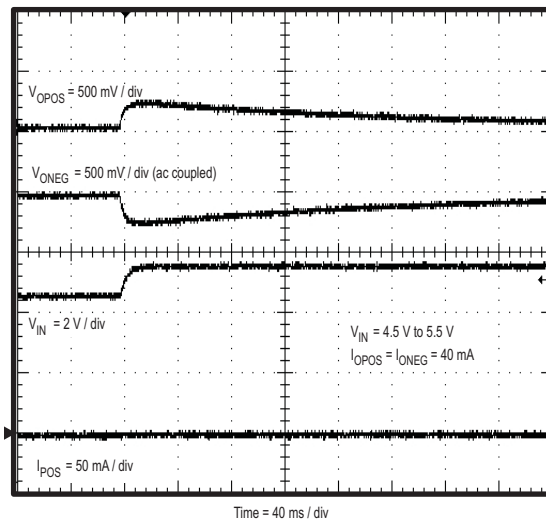
Figure 48. Power Down with Input Voltage

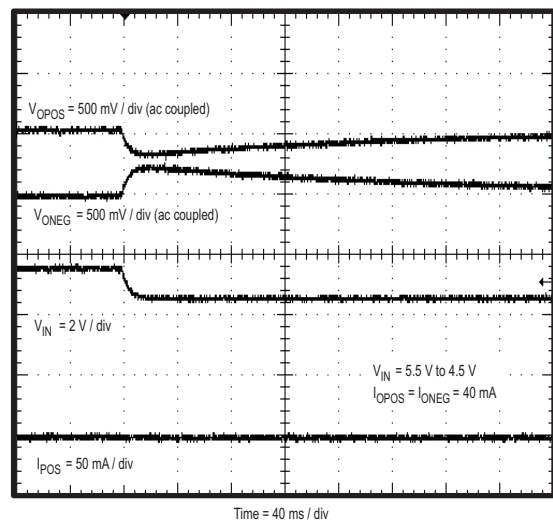**Figure 49. Power Down with Enable Pin**

Figure 50. Load Step Response

Figure 51. Load Step Response

Figure 52. Line Step Response

Figure 53. Line Step Response
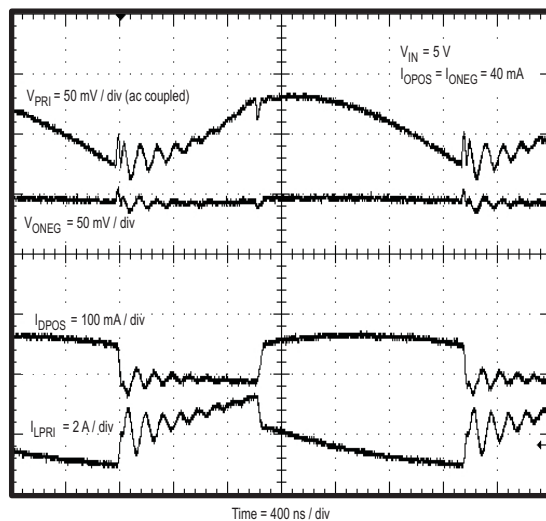
Figure 54. Steady State Waveforms
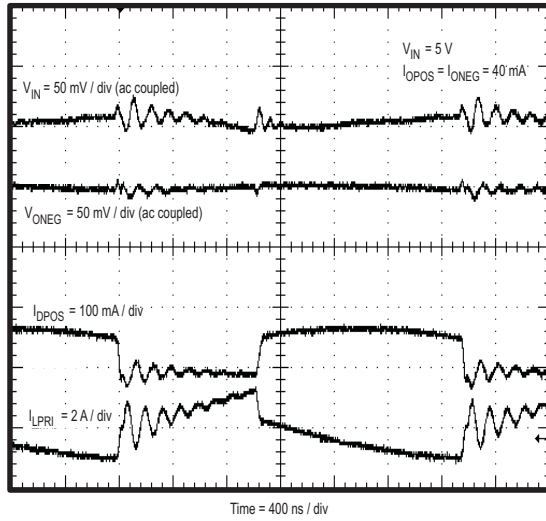
Figure 55. Steady State Waveforms
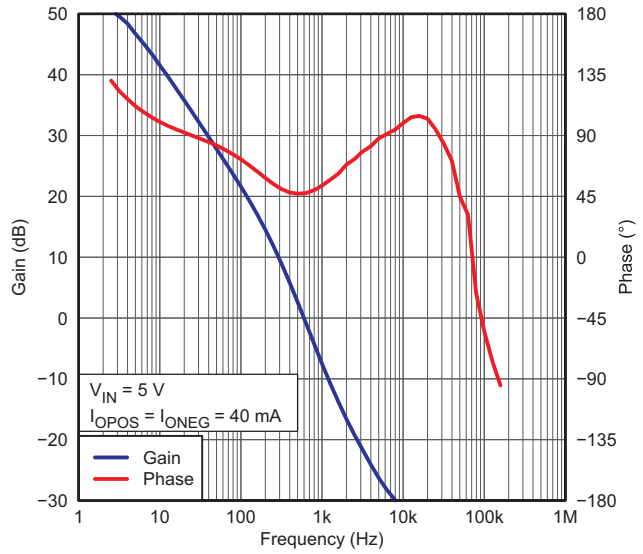
Figure 56. Frequency Response

Table 6. Reference Design BOM for Dual Output Application

	5V to +15V/-15V/0.04A
C_{IN}	47uF X5R 6.3V
C_{OPOS}, C_{ONEG}	10uF X5R 25V
C_{PRI}	10uF X5R 10V
C_{boot}	0.1uF X5R 10V
C_{SS}	0.1uF X5R 10V
Cc	0.1uF X5R 10V
R_{HS}	13.7k
R_{LS}	10k
R_t	243k
T1	750311780 Wurth Electronics Midcom
D_{POS}, D_{NEG}	B1100

Product Folder Links : *TPS55010*

PCB LAYOUT

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. Care should be taken to minimize the loop area formed by the bypass capacitor connections and the VIN pins. See Figure 57 for a PCB layout example. The GND pins should be tied directly to the thermal pad under the IC. The power pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. Additional vias can be used to connect the top side ground area to the internal planes near the input and output capacitors.

Locate the input bypass capacitor as close to the IC as possible. The PH pin should be routed to the primary side of the transformer. Since the PH connection is the switching node, the transformer should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The boot capacitor must also be located close to the device. The sensitive analog ground connections for the feedback voltage divider, compensation component, slow start capacitor and frequency set resistor should be connected to a separate analog ground trace as shown. The RT/CLK pin is particularly sensitive to noise so the R_T resistor should be located as close as possible to the IC and routed with minimal lengths of trace. Avoid connecting y capacitor on nodes which experience high dv/dt.
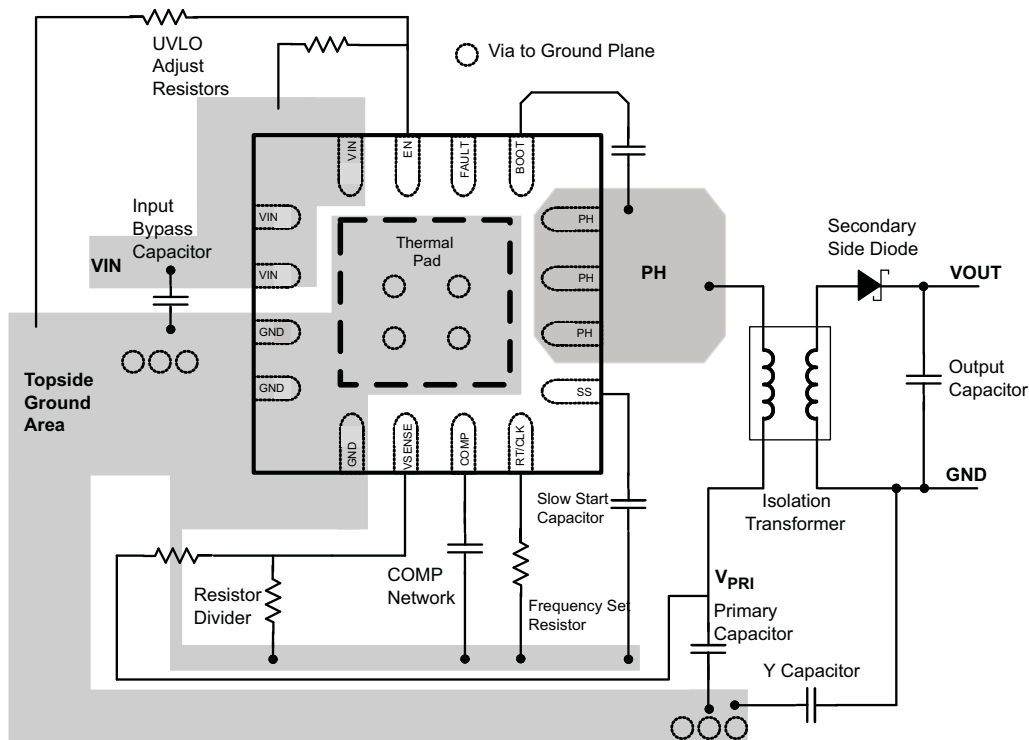
Figure 57. PCB Layout

REVISION HISTORY

Changes from Original (April 2010) to Revision A   **Page**

- Added production data 1

TEXAS INSTRUMENTS

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11-Apr-2013

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS55010RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55010	Samples
TPS55010RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55010	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
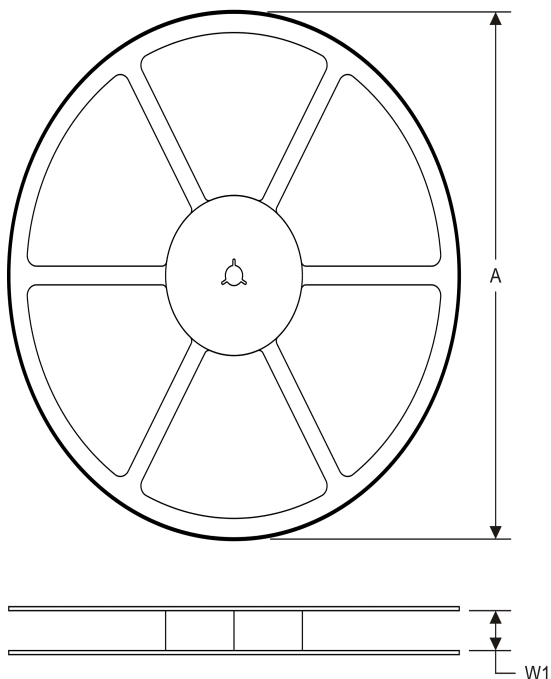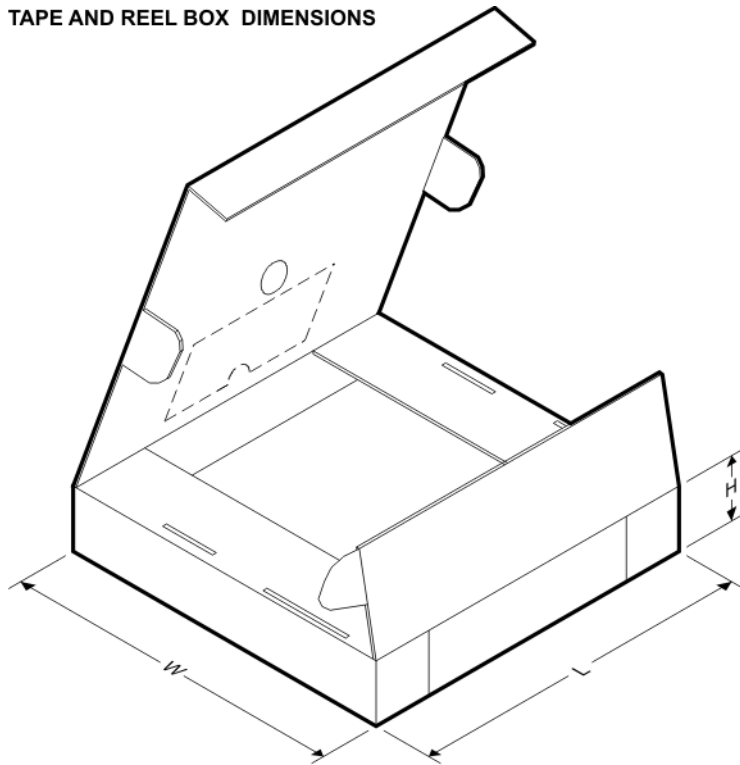
TAPE DIMENSIONS
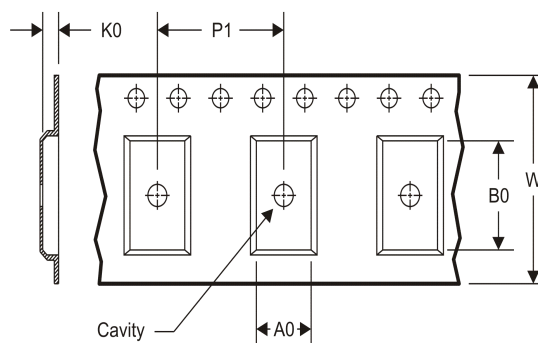
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55010RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS55010RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55010RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS55010RTET	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S−PWQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

3,15
2,85   [A]

[B]

3,15
2,85

16

PIN 1 INDEX AREA
TOP AND BOTTOM

1

0,80
0,70

0,20 REF.

[C]

SEATING PLANE

[D] 0,08

0,05
0,00

16X 0,50
     0,30

1

16

EXPOSED THERMAL PAD
/D\

16X 0,30
     0,18

⊕ | 0,10 Ⓜ | C | A | B |
  | 0,05 Ⓜ | C |

0,50
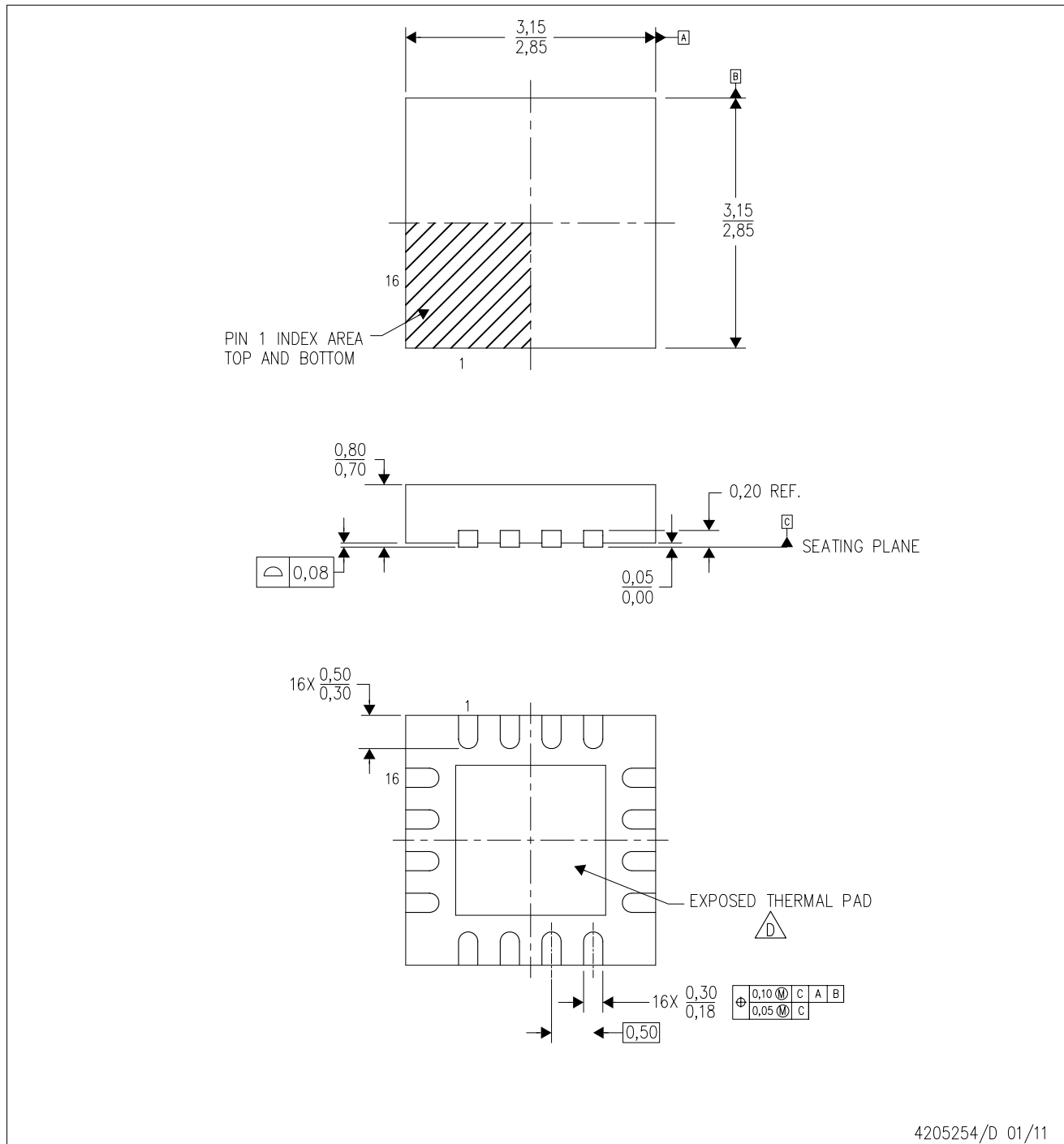
4205254/D 01/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          C.   Quad Flatpack, No−leads (QFN) package configuration.
       /D\   The package thermal pad must be soldered to the board for thermal and mechanical performance.
               See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
          E.   Falls within JEDEC MO−220.

TEXAS INSTRUMENTS
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RTE (S−PWQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
C 0,30

Exposed Thermal Pad

1,65±0,10

1,65±0,10
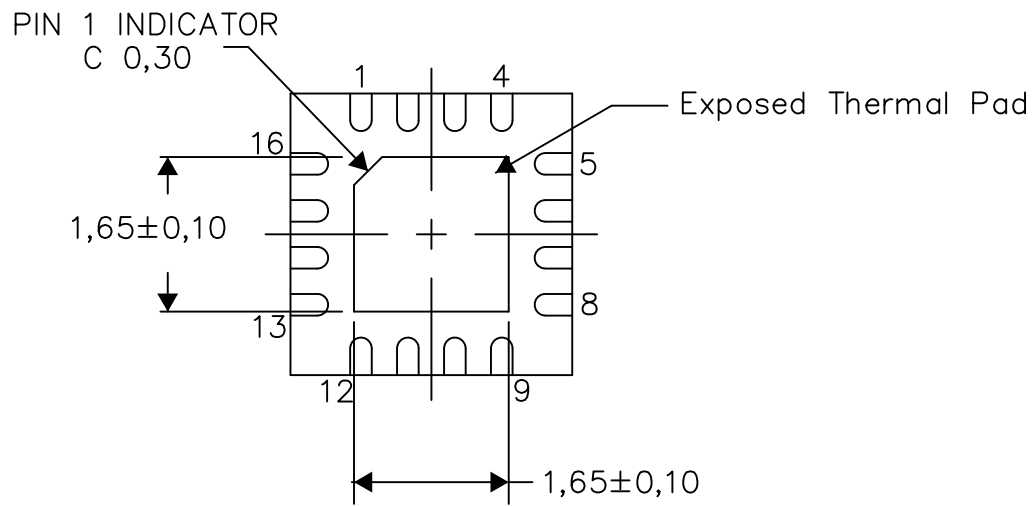
Bottom View

Exposed Thermal Pad Dimensions

4206446−4/O 09/13

NOTE: A. All linear dimensions are in millimeters

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No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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