Integrated 5-A 40-V Wide Input Range Boost/SEPIC/Flyback DC-DC Regulator

Check for Samples: TPS55340

FEATURES

- **Internal 5-A, 40-V Low-Side MOSFET Switch**
- **2.9-V to 32-V Input Voltage Range**
- **±0.7% Reference Voltage**
- **0.5mA Operating Quiescent Current**
- **2.7µA Shutdown Supply Current**
- **Fixed Frequency Current Mode PWM Control**
- **Frequency Adjustable from 100kHz to 1.2MHz**
- **Synchronization Capability to External Clock**
- **Adjustable Soft-Start Time**
- **Pulse-Skipping for Higher Efficiency at Light Loads**
- **Cycle-by-Cycle Current Limit, Thermal Shutdown, and UVLO Protection**
- **QFN-16 (3mmx3mm) and HTSSOP-14 Packages with PowerPad™**
- **Wide –40°C to 150°C Operating T_J Range**

APPLICATIONS

- **3.3-V, 5-V, 12-V, 24-V Power Conversion**
- **Boost, SEPIC, and Flyback Topologies**
- **Thunderbolt Port, Power Docking for Tablets and Portable PCs**
- **Industrial Power Systems**
- **ADSL Modems**

DESCRIPTION

The TPS55340 is a monolithic non-synchronous switching regulator with integrated 5-A, 40-V power switch. It can be configured in several standard switching-regulator topologies, including boost, SEPIC and isolated flyback. The device has a wide input voltage range to support applications with input voltage from multi-cell batteries or regulated 3.3-V, 5-V, 12-V, and 24-V power rails.

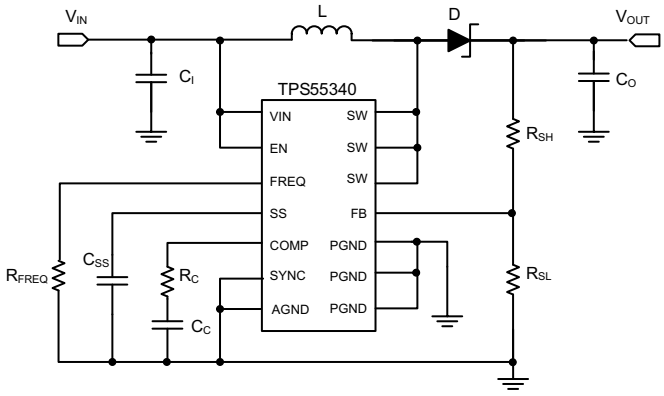
The TPS55340 regulates the output voltage with current mode PWM (pulse width modulation) control, and has an internal oscillator. The switching frequency of PWM is set by either an external resistor or by synchronizing to an external clock signal. The user can program the switching frequency from 100 kHz to 1.2 MHz.

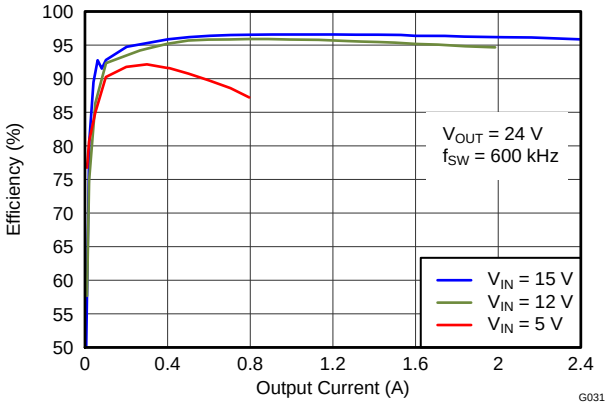
The device features a programmable soft-start function to limit inrush current during start-up and has other built-in protection features including cycle-by-cycle over current limit and thermal shutdown.

The TPS55340 is available in a small 3mm x 3mm 16-pin QFN as well as 14-pin HTSSOP packages with PowerPad™ for enhanced thermal performance.

The 5-A, 40-V TPS55340 Boost Converter in the HTSSOP-14 package is pin-to-pin compatible with the 3-A, 40-V TPS61175 and it extends the maximum input voltage from 18 V to 32 V.

TYPICAL APPLICATION (BOOST)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPad is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

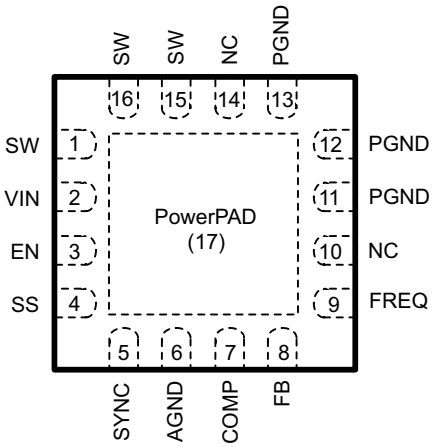
ORDERING INFORMATION(1)

T_J	PART NUMBER	PACKAGE
-40°C to 150°C	TPS55340RTE	QFN-16
	TPS55340PWP	HTSSOP-14

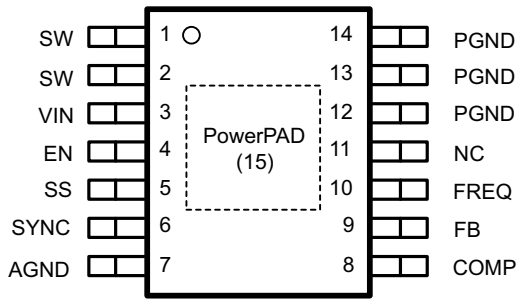
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN ASSIGNMENTS

QFN-16 PACKAGE
(Top View)



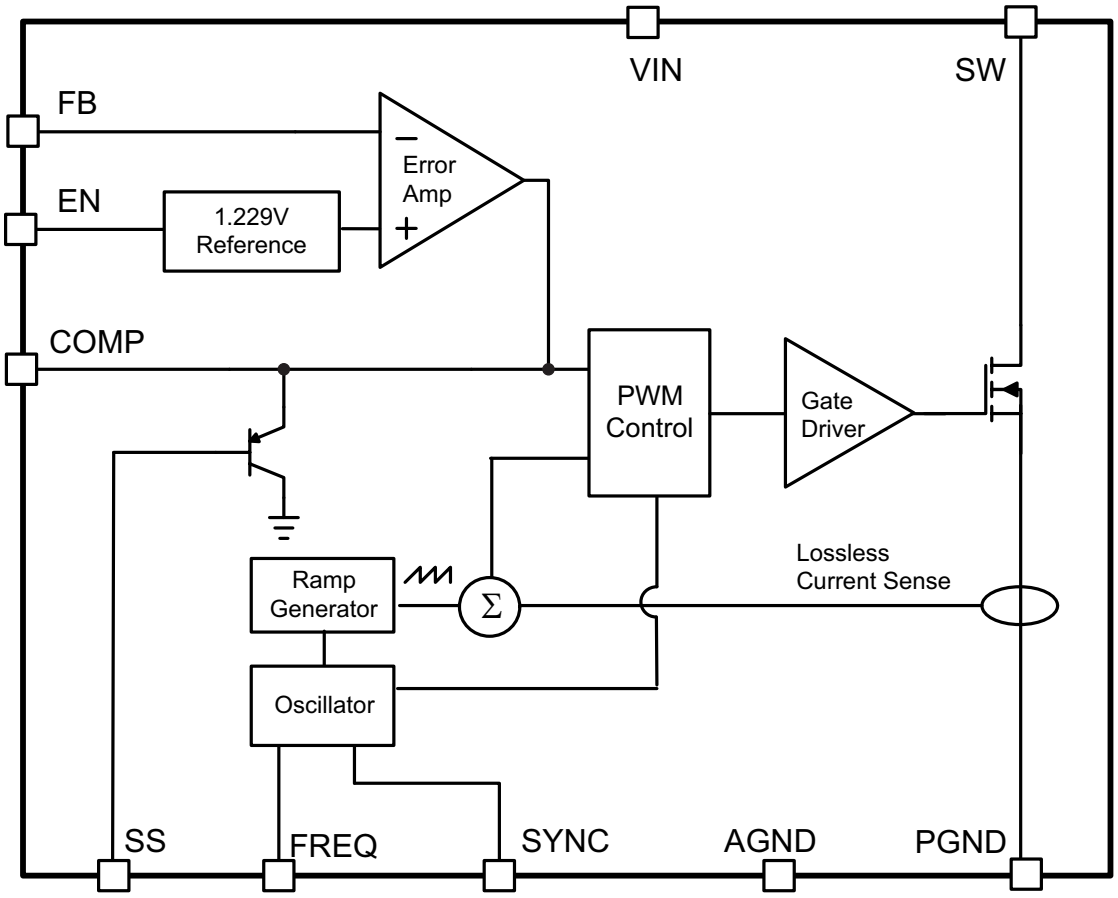
HTSSOP-14 PACKAGE
(Top View)



PIN FUNCTIONS

PIN			DESCRIPTION
NAME	NO.		
	QFN-16	HTSSOP-14	
VIN	2	3	The input supply pin to the IC. Connect VIN to a supply voltage between 2.9V and 32V. It is acceptable for the voltage on the pin to be different from the boost power stage input.
SW	1, 15, 16	1, 2	SW is the drain of the internal power MOSFET. Connect SW to the switched side of the boost or SEPIC inductor or the flyback transformer.
FB	8	9	Error amplifier input and feedback pin for positive voltage regulation. Connect to the center tap of a resistor divider to program the output voltage.
EN	3	4	Enable pin. When the voltage of this pin falls below the enable threshold for more than 1ms, the IC turns off.
COMP	7	8	Output of the transconductance error amplifier. An external RC network connected to this pin compensates the regulator feedback loop.
SS	4	5	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start timing.
FREQ	9	10	Switching frequency program pin. An external resistor connected between the FREQ pin and AGND sets the switching frequency.
AGND	6	7	Signal ground of the IC.
PGND	11, 12, 13	12, 13, 14	Power ground of the IC. It is connected to the source of the internal power MOSFET switch.
SYNC	5	6	Switching frequency synchronization pin. An external clock signal can be used to set the switching frequency between 200kHz and 1.0MHz. If not used, this pin should be tied to AGND.
NC	10, 14	11	Reserved pin that must be connected to ground.
PowerPAD	17	15	The PowerPAD should be soldered to the AGND. If possible, use thermal vias to connect to internal ground plane for improved power dissipation.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltages on pin VIN(2)		–0.3	34	V
Voltage on pin EN(2)		–0.3	34	V
Voltage on pins FB, FREQ, and COMP(2)		–0.3	3	V
Voltage on pin SS(2)		–0.3	5	V
Voltage on pin SYNC(2)		–0.3	7	V
Voltage on pin SW(2)		–0.3	40	V
Operating junction temperature range		–40	150	°C
Storage temperature range		–65	150	°C
Electrostatic discharge	(HBM) QSS 009-105 (JESD22-A114A)		2	kV
	(CDM) QSS 009-147 (JESD22-C101B 01)		500	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal

THERMAL INFORMATION

THERMAL METRIC(1)		TPS55340		UNITS
		QFN (16-PINS)	HTSSOP (14-PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	43.3	43.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	38.7	33.3	
θ_{JB}	Junction-to-board thermal resistance	14.5	28.3	
ψ_{JT}	Junction-to-top characterization parameter	0.4	1.3	
ψ_{JB}	Junction-to-board characterization parameter	14.5	28.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.5	3.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.9		32	V
V_{OUT}	Output voltage range	V_{IN}		38	V
V_{EN}	EN voltage range	0		32	V
V_{SYN}	External switching frequency logic input range	0		5	V
T_A	Operating free-air temperature	–40		125	°C
T_J	Operating junction temperature	–40		150	°C

ELECTRICAL CHARACTERISTICS

Vin=5V, T_J = –40°C to +150°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.9		32	V
I_Q	Operating quiescent current into Vin	Device non-switching, V_{FB} = 2 V		0.5		mA
I_{SD}	Shutdown current	EN = GND		2.7	10	µA
V_{UVLO}	Under-voltage lockout threshold	V_{IN} falling		2.5	2.7	V
V_{hys}	Under-voltage lockout hysteresis		120	140	160	mV

ELECTRICAL CHARACTERISTICS (continued)

Vin=5V, T_J = –40°C to +150°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE AND REFERENCE CONTROL						
V_{EN}	EN threshold voltage	EN rising input	0.9	1.08	1.30	V
V_{ENh}	EN threshold hysteresis		0.1	0.16	0.22	V
R_{EN}	EN pull down resistor		400	950	1600	kΩ
T_{off}	Shutdown delay, SS discharge	EN high to low		1.0		ms
V_{SYNh}	SYN logic high voltage		1.2			
V_{SYNl}	SYN logic low voltage				0.4	V
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		1.204	1.229	1.254	V
		T_A = 25°C	1.220	1.229	1.238	
I_{FB}	Voltage feedback input bias current	T_A = 25°C		1.6	20	nA
I_{sink}	Comp pin sink current	$V_{FB} = V_{REF}$+200 mV, V_{COMP} = 1 V		42		µA
I_{source}	Comp pin source current	$V_{FB} = V_{REF}$–200 mV, V_{COMP} = 1 V		42		µA
V_{CCLP}	Comp pin Clamp Voltage	High Clamp, V_{FB} = 1 V Low Clamp, V_{FB} = 1.5 V		3.1 0.75		V
V_{CTH}	Comp pin threshold	Duty cycle = 0%		1.04		V
G_{ea}	Error amplifier transconductance		240	360	440	µmho
R_{ea}	Error amplifier output resistance			10		MΩ
f_{ea}	Error amplifier crossover frequency			500		kHz
FREQUENCY						
f_{SW}	Frequency	R_{FREQ} = 480 kΩ	75	94	130	kHz
		R_{FREQ} = 80 kΩ	460	577	740	
		R_{FREQ} = 40 kΩ	920	1140	1480	
D_{max}	Maximum duty cycle	V_{FB} = 1.0 V, R_{FREQ} = 80 kΩ	89%	96%		
V_{FREQ}	FREQ pin voltage			1.25		V
T_{min_on}	Minimum on pulse width	R_{FREQ} = 80 kΩ		77		ns
POWER SWITCH						
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = 5 V V_{IN} = 3 V		60 70	110 120	mΩ
I_{LN_NFET}	N-channel leakage current	V_{DS} = 25 V, T_A = 25°C			2.1	µA
OCP and SS						
I_{LIM}	N-Channel MOSFET current limit	D = D_{max}	5.25	6.6	7.75	A
I_{SS}	Soft-start bias current	Vss = 0 V		6		µA
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			165		°C
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		°C

TYPICAL CHARACTERISTICS

Vin = 5 V, T_A = 25°C (unless otherwise noted)

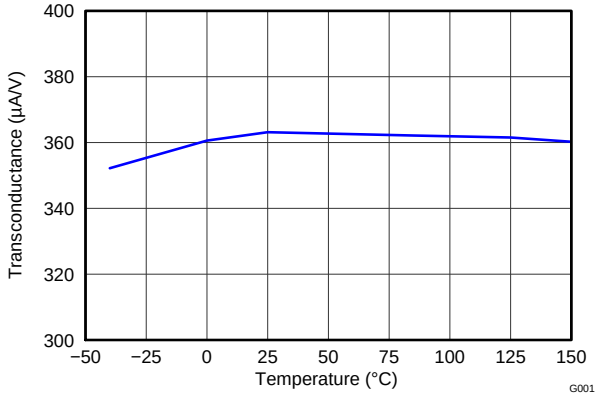


Figure 1. Error Amplifier Transconductance vs Temperature

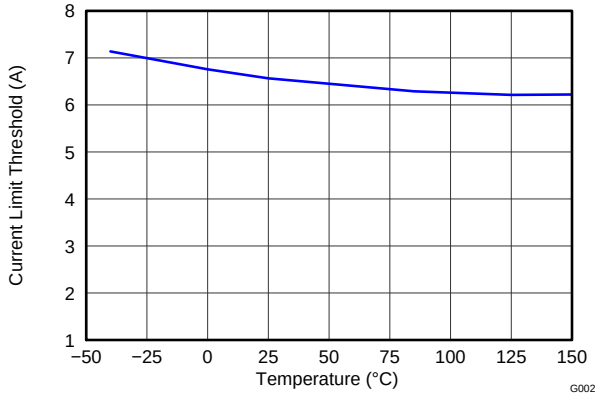


Figure 2. Switch Current Limit vs Temperature

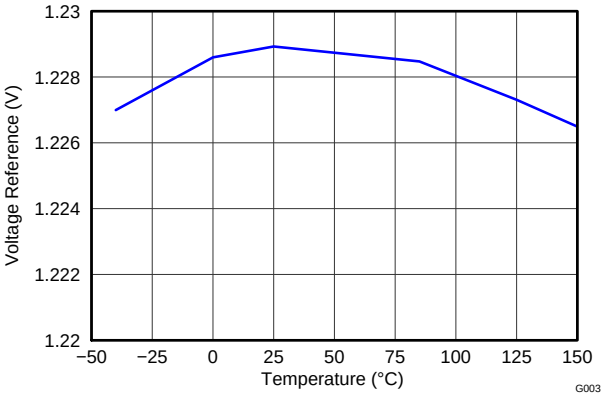


Figure 3. Feedback Voltage Reference vs Temperature

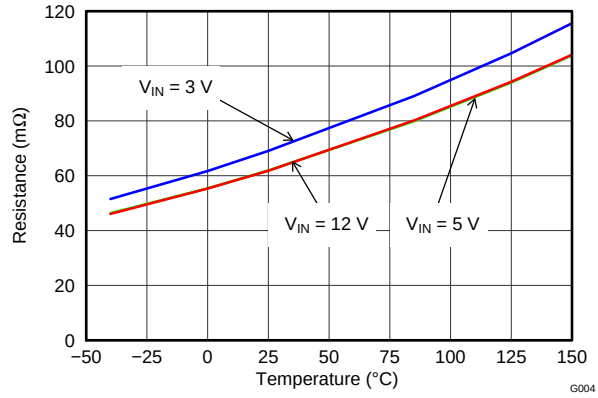


Figure 4. $R_{DS(ON)}$ vs Temperature

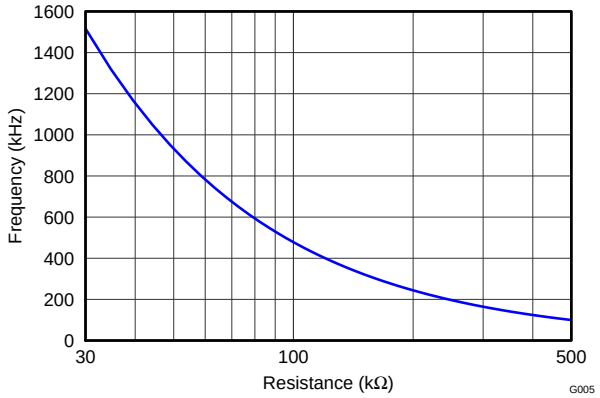


Figure 5. Frequency vs FREQ Resistance

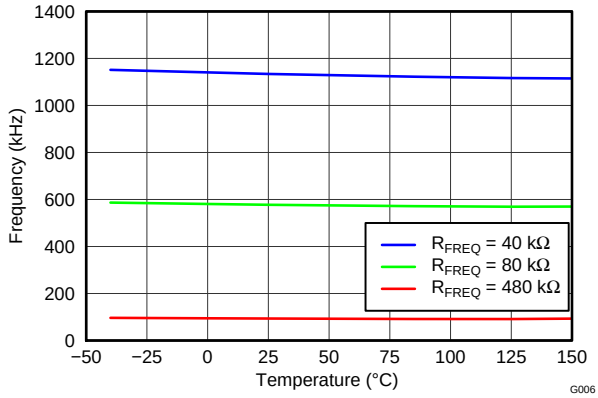


Figure 6. Frequency vs Temperature

TYPICAL CHARACTERISTICS (continued)

Vin = 5 V, T_A = 25°C (unless otherwise noted)

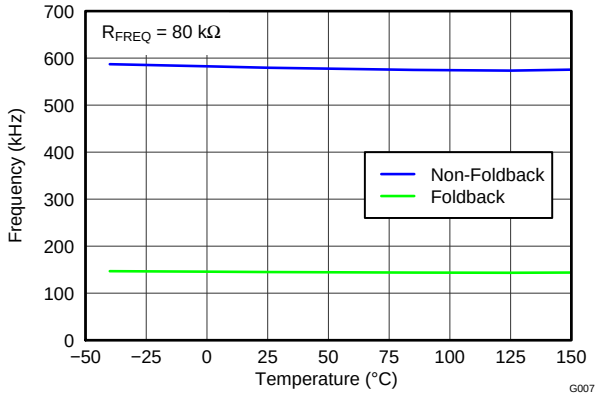


Figure 7. Non-Foldback Frequency vs Foldback Frequency

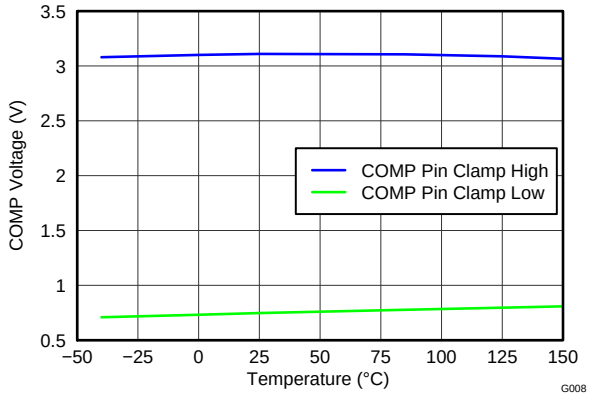


Figure 8. COMP Clamp Voltage vs Temperature

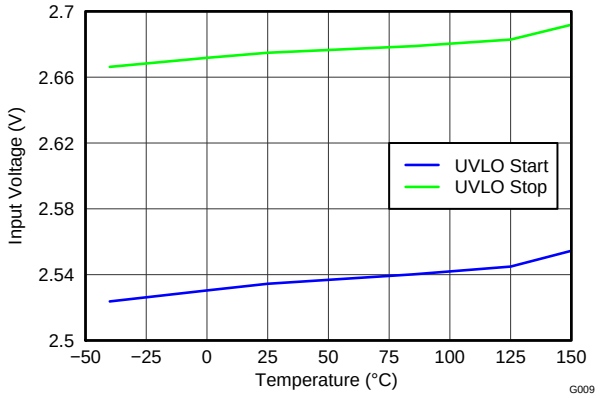


Figure 9. Input Voltage UVLO vs Temperature

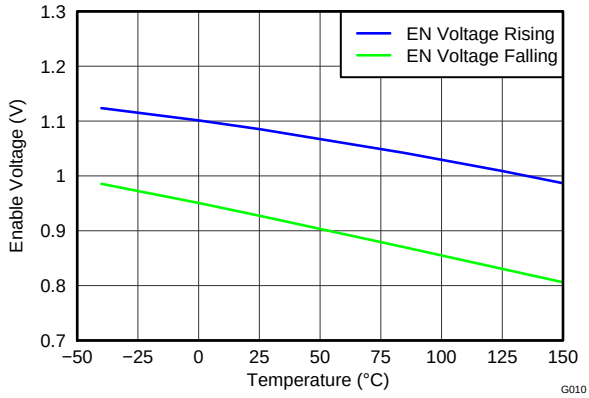


Figure 10. Enable Voltage vs Temperature

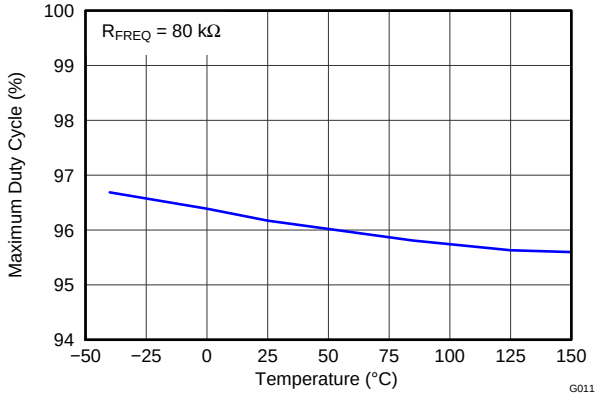


Figure 11. Maximum Duty Cycle vs Temperature

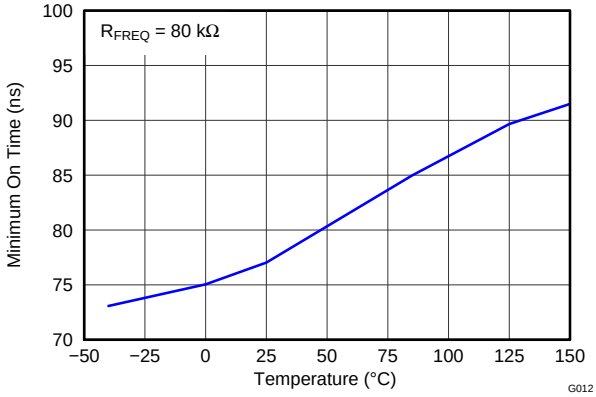


Figure 12. Minimum On Time vs Temperature

TYPICAL CHARACTERISTICS (continued)

Vin = 5 V, T_A = 25°C (unless otherwise noted)

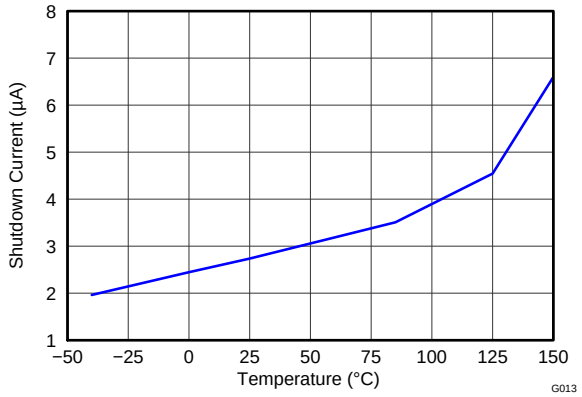


Figure 13. Shutdown Current vs Temperature

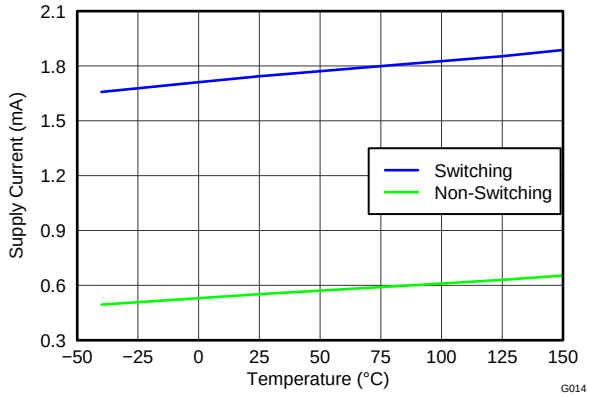


Figure 14. Supply Current vs Temperature

DETAILED DESCRIPTION

OPERATION

The TPS55340 integrates a 5 A, 40 V low side n-channel MOSFET for boost converter output up to 38V. The TPS55340 regulates the output with current mode PWM (pulse width modulation) control. The PWM control circuitry turns on the switch at the beginning of each oscillator clock cycle. The input voltage is applied across the inductor and stores the energy as inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current reaches a threshold level set by the error amplifier output, the power switch turns off and the external Schottky diode is forward biased to allow the inductor current to flow to the output. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats every switching cycle. The duty cycle of the converter is determined by the PWM control comparator which compares the error amplifier output and the current signal. The oscillator frequency is programmed by the external resistor or synchronized to an external clock signal.

A ramp signal from the oscillator is added to the inductor current ramp to provide slope compensation. Slope compensation is necessary to avoid sub-harmonic oscillation that is intrinsic to peak current mode control at duty cycles higher than 50%. If the inductor value is too small, the internal slope compensation may not be adequate to maintain stability.

The PWM control feedback loop regulates the FB pin to a reference voltage through a transconductance error amplifier. The output of the error amplifier is connected to the COMP pin. An external RC compensation network connected to the COMP pin is chosen for feedback loop stability and optimum transient response.

SWITCHING FREQUENCY

The switching frequency is set by a resistor (R_{FREQ}) connected to the FREQ pin of the TPS55340. The relationship between the timing resistance R_{FREQ} and frequency is shown in the Figure 5. Do not leave this pin open. A resistor must always be connected from the FREQ pin to ground for proper operation. The resistor value required for a desired frequency can be calculated using Equation 1.

$$R_{FREQ}(k\Omega) = 57500 \times f_{sw}(kHz)^{-1.03} \quad (1)$$

For the given resistor value, the corresponding frequency can be calculated by Equation 2.

$$f_{sw}(kHz) = 41600 \times R_{FREQ}(k\Omega)^{-0.97} \quad (2)$$

The TPS55340 switching frequency can be synchronized to an external clock signal that is applied to the SYNC pin. The required logic levels of the external clock are shown in the specification table. The recommended duty cycle of the clock is in the range of 10% to 90%. A resistor must be connected from the FREQ pin to ground when the converter is synchronized to the external clock and the external clock frequency must be within ±20% of the corresponding frequency set by the resistor. For example, if the frequency programmed by the FREQ pin resistor is 600kHz, the external clock signal should be in the range of 480kHz to 720kHz.

VOLTAGE REFERENCE AND SETTING OUTPUT VOLTAGE

An internal voltage reference provides a precise 1.229 V voltage reference at the error amplifier non-inverting input. To set the output voltage, select the FB pin resistor R_{SH} and R_{SL} according to Equation 3.

$$V_{OUT} = 1.229V \times \left(\frac{R_{SH}}{R_{SL}} + 1 \right) \quad (3)$$

SOFT-START

The TPS55340 has a built-in soft-start circuit which significantly reduces the start-up current spike and output voltage overshoot. When the IC is enabled, an internal bias current source (6 µA typical) charges a capacitor (C_{SS}) on the SS pin. The voltage at the capacitor clamps the output of the internal error amplifier that determines the peak current and duty cycle of PWM controller. Limiting the peak switch current during start-up with a slow ramp on the SS pin will reduce in-rush current and output voltage overshoot. Once the capacitor reaches 1.8V, the soft-start cycle is completed and the soft-start voltage no longer clamps the error amplifier output. When the EN is pulled low for at least 1ms, the IC enters the shutdown mode and the SS capacitor is discharged through a 5kΩ resistor to prepare for the next soft-start sequence.

SLOPE COMPENSATION

The TPS55340 has internal slope compensation to prevent sub-harmonic oscillations. The sensed current slope of boost converter can be expressed as Equation 4:

$$S_n = \frac{V_{IN}}{L} \times R_{SENSE} \quad (4)$$

The slope compensation dv/dt can be calculated using Equation 5.

$$S_e = \frac{0.32\ V / R_{FREQ}}{16 \times (1-D) \times 6\ pF} + \frac{0.5\ \mu A}{6\ pF} \quad (5)$$

In a converter with current mode control, in addition to the output voltage feedback loop, the inner current loop including the inductor current sampling effect as well as the slope compensation on the small signal response should be taken into account, which can be modeled as seen in Equation 6:

$$He(s) = \frac{1}{1 + \frac{s \times \left[\left(1 + \frac{S_e}{S_n}\right) \times (1-D) - 0.5\right]}{f_{sw}} + \frac{s^2}{(\pi \times f_{sw})^2}} \quad (6)$$

Where R_{SENSE} (15mΩ) is the equivalent current sense resistor, R_{FREQ} is timing resistor used to set frequency, and D is the duty cycle.

Note that if S_n << S_e, the converter operates in voltage mode control rather than current mode control, and Equation 6 is no longer valid.

OVER-CURRENT PROTECTION AND FREQUENCY FOLDBACK

The TPS55340 provides cycle-by-cycle over-current protection that turns off the power switch once the inductor current reaches the over-current limit threshold. The PWM circuitry resets itself at the beginning of the next switch cycle. During an over-current event, the output voltage begins to droop as a function of the load on the output. When the FB voltage through the feedback resistors, drops lower than 0.9 V, the switching frequency is automatically reduced to 1/4 of the normal value. Figure 7 shows the non-foldback frequency with an 80kΩ timing resistor and the corresponding foldback frequency. The switching frequency does not return to normal until the over-current condition is removed and the FB voltage increases above 0.9 V. The frequency foldback feature is disabled during soft-start.

ENABLE AND THERMAL SHUTDOWN

The TPS55340 enters shutdown when the EN voltage is less than 0.68 V (min) for more than 1ms. In shutdown, the input supply current for the device is less than 10μA (max). The EN pin has an internal 950kΩ pull down resistor to disable the device if the pin is floating.

An internal thermal shutdown turns off the device when the junction temperature exceeds 165°C (typical). The device will restart when the junction temperature drops by 15°C.

UNDER-VOLTAGE LOCKOUT (UVLO)

An under-voltage lockout circuit prevents mis-operation of the device at input voltages below 2.5 V (typical). When the input voltage is below the UVLO threshold, the device remains off and the internal power MOSFET is turned off. The UVLO threshold is set below minimum operating voltage of 2.9 V to ensure that a transient VIN dip will not cause the device to reset. For the input voltages between UVLO threshold and 2.9 V, the device attempts to operate, but the electrical specifications are **not** guaranteed.

MINIMUM ON TIME AND PULSE SKIPPING

The TPS55340 PWM control system has a minimum PWM pulse width of 77ns (typical). This minimum on-time determines the minimum duty cycle of the PWM, for any set switching frequency. When the voltage regulation loop of the TPS55340 requires a minimum on-time pulse width less than 77ns, the IC enters pulse-skipping mode. In this mode, the device will hold the power switch off for several switching cycles to prevent the output voltage from rising above the desired regulated voltage. This operation typically occurs in light load conditions when the PWM operates in discontinuous conduction mode. Pulse skipping increases the output ripple as shown in Figure 21.

LAYOUT COSIDERATIONS

As for all switching power supplies, especially those with high frequency and high switch current, printed circuit board (PCB) layout is an important design step. If the layout is not carefully designed, the regulator could suffer from instability as well as noise problems. To maximize efficiency, switch rise and fall times are made as short as possible. To prevent radiation of high frequency resonance problems, proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling. The high current path including the internal MOSFET switch, Schottky diode, and output capacitor, contains nanosecond rise and fall times and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the AGND pin in order to reduce the IC supply ripple.

THERMAL CONSIDERATIONS

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. This restriction limits the power dissipation of the TPS55340. The TPS55340 features a thermally enhanced QFN package. This package includes a PowerPad™ that improves the thermal capabilities of the package. The thermal resistance of the QFN package in any application greatly depends on the PCB layout and the PowerPad™ connection. The PowerPad™ must be soldered to the analog ground on the PCB. Use thermal vias underneath the PowerPad™ to achieve good thermal performance.

DESIGN GUIDE-STEP-BY-STEP DESIGN PROCEDURE OF BOOST CONVERTER

The following section provides a step-by-step design approach for configuring the TPS55340 as a voltage regulating boost converter, as shown in Figure 15. When configured as SEPIC or flyback converter, a different design approach is required. A design example of SEPIC converter is provided in the next section.

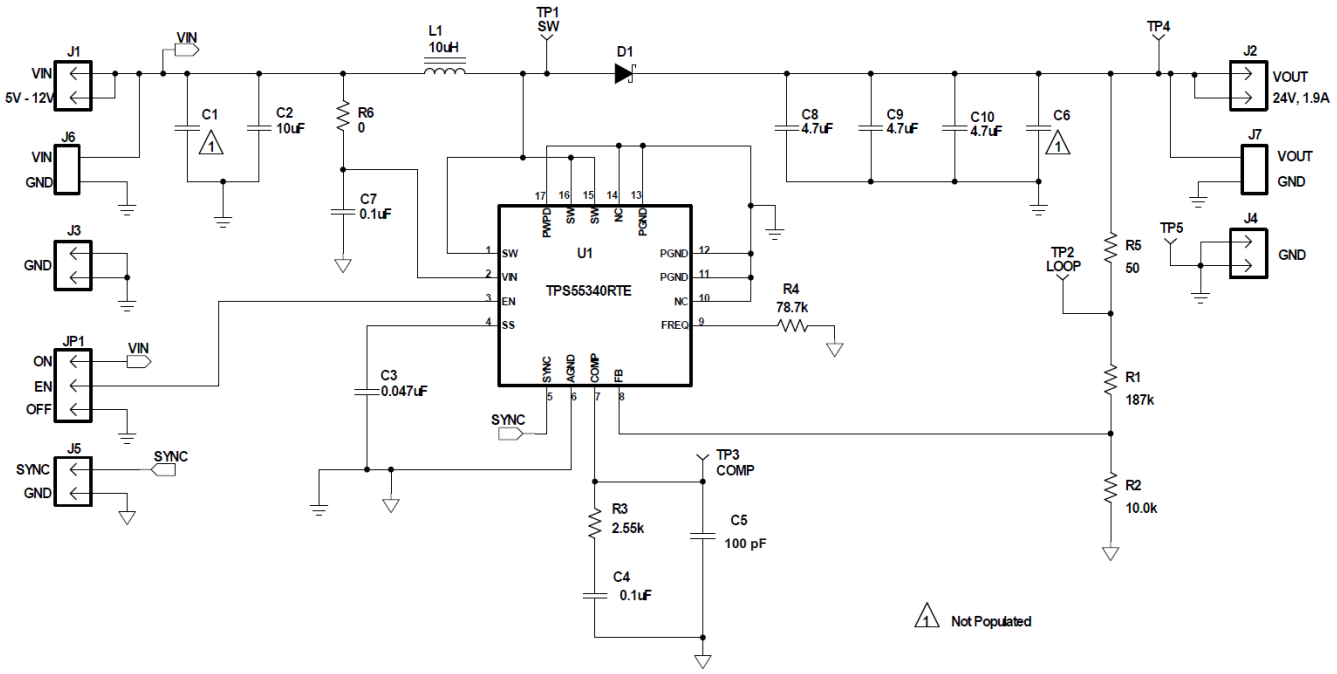


Figure 15. Boost Converter Application Schematic

A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we will start with the following known parameters:

Table 1. Key Parameters of Boost Converter Example

PARAMETER	VALUE
Output Voltage	24 V
Input Voltage	5 V to 12 V
Maximum Output Current	800 mA
Transient Response 50% load step (ΔV_{OUT} = 3%)	960 mV
Output Voltage Ripple (0.5% of V_{OUT})	120 mV

SELECTING THE SWITCHING FREQUENCY (R4)

The first step is to decide on a switching frequency for the regulator. There are tradeoffs to consider for a higher or lower switching frequency. A higher switching frequency allows for lower valued inductor and smaller output capacitors leading to the smallest solution size. A lower switching frequency will result in a larger solution size but better efficiency. The user will typically set the frequency for the minimum tolerable efficiency to avoid excessively large external components.

A switching frequency of 600 kHz is a good trade-off between efficiency and solution size. The appropriate resistor value is found from the resistance versus frequency graph of Figure 5, or calculated using Equation 1. R4 is calculated to be 78.4 kΩ and the nearest standard value resistor of 78.7 kΩ is selected. A resistor must be placed from the FREQ pin to ground, even if an external oscillation is applied for synchronization.

DETERMINING THE DUTY CYCLE

The input to output voltage conversion ratio of the TPS55340 is limited by the worst case maximum duty cycle of 89% and the minimum duty cycle which is determined by the minimum on-time of 77 ns and the switching frequency. The minimum duty cycle can be estimated with Equation 7. With a 600 kHz switching frequency the minimum duty cycle is 4%.

$$D_{PS} = T_{ON}\ min \times f_{sw} \quad (7)$$

The duty cycle at which the converter operates is dependent on the mode in which the converter is running. If the converter is running in discontinuous conduction mode (DCM), where the inductor current ramps to zero at the end of each cycle, the duty cycle varies with changes of the load much more than it does when running in continuous conduction mode (CCM). In continuous conduction mode, where the inductor maintains a minimum dc current, the duty cycle is related primarily to the input and output voltages as computed below. Assume a 0.5 V drop V_D across the Schottky rectifier. At the minimum input of 5 V, the duty cycle will be 80%. At the maximum input of 12 V, the duty cycle is 51%.

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D} \quad (8)$$

At light loads the converter will operate in DCM. In this case the duty cycle is a function of the load, input and output voltages, inductance and switching frequency as computed below. This can be calculated only after an inductance is chosen in the following section. While operating in DCM with very light load conditions the duty cycle demand will force the TPS55340 to operate with the minimum on time. The converter will then begin pulse skipping which can increase the output ripple.

$$D = \frac{\sqrt{2 \times (V_{OUT} + V_D - V_{IN}) \times L \times I_{OUT} \times f_{SW}}}{V_{IN}} \quad (9)$$

All converters using a diode as the freewheeling or catch component have a load current level at which they transit from discontinuous conduction mode to continuous conduction mode. This is the point where the inductor current just falls to zero during the off-time of the power switch. At higher load currents, the inductor current does not fall to zero and diode and switch current assume a trapezoidal wave shape as opposed to a triangular wave shape. The load current boundary between discontinuous conduction and continuous conduction can be found for a set of converter parameters as follows.

$$I_{OUT(crit)} = \frac{(V_{OUT} + V_D - V_{IN}) \times V_{IN}^2}{2 \times (V_{OUT} + V_D)^2 \times f_{SW} \times L} \quad (10)$$

For loads higher than the result of the Equation 10, the duty cycle is given by Equation 8. For loads less than the results of Equation 10, the duty cycle is given Equation 9. For Equation 7 through Equation 10, the variable definitions are as follows.

- V_{OUT} is the output voltage of the converter in V
- V_D is the forward conduction voltage drop across the rectifier or catch diode in V
- V_{IN} is the input voltage to the converter in V
- I_{OUT} is the output current of the converter in A
- L is the inductor value in H
- f_{SW} is the switching frequency in Hz

Unless otherwise stated, the design equations that follow assume that the converter is running in continuous conduction mode, which typically results in a higher efficiency for the power levels of this converter.

SELECTING THE INDUCTOR (L1)

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications: inductor value, DC resistance and saturation current. Considering inductor value alone is not enough. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, the effective inductance can fall to a fraction of the zero current value.

The minimum value of the inductor should be able to meet inductor current ripple (ΔI_L) requirement at worst case. In a boost converter, maximum inductor current ripple occurs at 50% duty cycle. For the applications where duty cycle is always smaller or larger than 50%, Equation 12 should be used with the duty cycle closest to 50% and corresponding input voltage to calculate the minimum inductance. For applications that need to operate with 50% duty cycle when input voltage is somewhere between the minimum and the maximum input voltage, Equation 13 should be used. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum input current ($I_{IN}DC = I_L avg$). The maximum input current can be estimated with Equation 11, with an estimated efficiency based on similar applications (η_{EST}). The inductor ripple current will be filtered by the output capacitor. Therefore, choosing high inductor ripple currents will impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value (K_{IND}) is at the discretion of the designer. However, the following guidelines may be used.

For CCM operation, it is recommended to use K_{IND} values in the range of 0.2 to 0.4. Choosing K_{IND} closer to 0.2 results in a larger inductance value, maximizes the converter's potential output current and minimizes EMI. Choosing K_{IND} closer to 0.4 results in a smaller inductance value, a physically smaller inductor, and improved transient response, but potentially worse EMI and lower efficiency. Using an inductor with a smaller inductance value may result in the converter operating in DCM. This reduces the boost converter's maximum output current, causes larger input voltage and output voltage ripple and reduced efficiency. For this design, choose K_{IND} = 0.3 and a conservative efficiency estimate of 85% with the minimum input voltage and maximum output current. Equation 12 is used with the maximum input voltage because this corresponds to duty cycle closest to 50%. The maximum input current is estimated at 4.52A and the minimum inductance is 7.53 µH. A standard value of 10 µH is chosen.

$$I_{IN}DC = \frac{V_{OUT} \times I_{OUT}}{\eta_{EST} \times V_{IN}\,min} \tag{11}$$

$$L_O\,min \geq \frac{V_{IN}}{I_{IN}DC \times K_{IND}} \times \frac{D}{f_{SW}} \quad , D \neq 50\%, V_{IN} \text{ with D closest to 50\%} \tag{12}$$

$$L_O\,min \geq \frac{(V_{OUT} + V_D)}{I_{IN}DC \times K_{IND}} \times \frac{1}{4 \times f_{SW}} \quad , D=50\% \tag{13}$$

After choosing the inductance, the required current ratings can be calculated. The inductor will be closest to its ratings with the minimum input voltage. The ripple with the chosen inductance is calculated with Equation 14. The RMS and peak inductor current can be found with Equation 15 and Equation 16. For this design the current ripple is 663mA, the RMS inductor current is 4.52 A, and the peak inductor current is 4.85 A. It is generally recommended for the peak inductor current rating of the selected inductor be 20% higher to account for transients during power up, faults or transient load conditions. The most conservative approach is to specify an inductor with a saturation current greater than the maximum peak current limit of the TPS55340. This helps to avoid saturation of the inductor. The chosen inductor is a Würth Elektronik 74437368100. It has a saturation current rating of 12.5 A, RMS current rating of 5.2 A, and typical DCR of 27.0mΩ.

$$\Delta I_L = \frac{V_{IN}\,min}{L_O} \times \frac{D\,max}{f_{SW}} \tag{14}$$

$$I_L rms = \sqrt{(I_{IN}DC)^2 + \left(\frac{\Delta I_L}{12}\right)^2} \tag{15}$$

$$I_L peak = I_{IN}DC + \frac{\Delta I_L}{2} \tag{16}$$

The TPS55340 has built-in slope compensation to avoid sub-harmonic oscillation associated with current mode control. If the inductor value is too small, the slope compensation may not be adequate, and the loop can be unstable.

COMPUTING THE MAXIMUM OUTPUT CURRENT

The over-current limit for the integrated power MOSFET limits the maximum input current and thus the maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output (I_{OUT}max). The current limit clamps the peak inductor current, therefore the ripple has to be subtracted to derive maximum DC current. Decreasing the K_{IND} or designing for a higher efficiency will increase the maximum output current. This can be evaluated with the chosen inductance or the chosen K_{IND}. This should be evaluated with the minimum input voltage and minimum peak current limit (I_{LIM}) of 5.25 A.

$$I_{OUT}\,max = \frac{V_{IN}\,min \times \left(I_{LIM} - \frac{\Delta I_L}{2}\right) \times \eta_{EST}}{V_{OUT}} = \frac{V_{IN}\,min \times I_{LIM} \times \left(1 - \frac{K_{IND}}{2}\right) \times \eta_{EST}}{V_{OUT}} \quad (17)$$

In this design with 5 V input boosted to 24 V output and a 10 µH inductor with an assumed the Schottky forward voltage of 0.5 V and estimated efficiency of 85%, the maximum output current is 871 mA. With the 12 V input and increased estimated efficiency of 90%, the maximum output current increases to 2.13 A. This circuit was evaluated to its maximum output currents with both the minimum and maximum input voltage.

SELECTING THE OUTPUT CAPACITOR (C8-C10)

At least 4.7 µF of ceramic type X5R or X7R capacitance is recommended at the output. The output capacitance is mainly selected to meet the requirements for the output ripple (V_{RIPPLE}) and voltage change during a load transient. Then the loop is compensated for the output capacitor selected. The output capacitance should be chosen based on the most stringent of these criteria. The output ripple voltage is related to the capacitance and equivalent series resistance (ESR) of the output capacitor. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by Equation 18. If high ESR capacitors are used it will contribute additional ripple. The maximum ESR for a specified ripple is calculated with Equation 19. ESR ripple can be neglected for ceramic capacitors but must be considered if tantalum or electrolytic capacitors are used. The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated by the Equation 20. Equation 21 can be used to calculate the RMS current that the output capacitor needs to support.

$$C_{OUT} \geq \frac{Dmax \times I_{OUT}}{f_{SW} \times V_{RIPPLE}} \quad (18)$$

$$ESR \leq \frac{\left(V_{RIPPLE} - \frac{Dmax \times I_{OUT}}{f_{SW} \times C_{OUT}}\right)}{\Delta I_L} \quad (19)$$

$$C_{OUT} \geq \frac{\Delta I_{TRAN}}{2 \times \pi \times f_{BW} \times \Delta V_{TRAN}} \quad (20)$$

$$I_{CO}rms = I_{OUT}\sqrt{\frac{Dmax}{(1 - Dmax)}} \quad (21)$$

Using Equation 18 for this design, the minimum output capacitance for the specified 120 mV output ripple is 8.8 µF. For a maximum transient voltage change (ΔV_{TRAN}) of 960 mV with a 400 mA load transient (ΔI_{TRAN}) and a 6 kHz control loop bandwidth (f_{BW}) with Equation 20, the minimum output capacitance is 11.1 µF. The most stringent criteria is the 11.1 µF for the required load transient. Equation 21 gives a 1.58 A RMS current in the output capacitor. The capacitor should also be properly rated for the desired output voltage.

Care must be taken when evaluating ceramic capacitors that derate under dc bias, aging and AC signal conditions. For example, larger form factor capacitors (in 1206 size) have self-resonant frequencies in the range of converter switching frequency. Self-resonance causes the effective capacitance to be significantly lower. The DC bias can also significantly reduce capacitance. Ceramic capacitors can lose as much as 50% of the capacitance whan operated at the rated voltage. Therefore, allow margin in selected capacitor voltage rating to ensure adequate capacitance at the required output voltage. For this example, three 4.7 µF, 50V 1210 X7R ceramic capacitors are used in parallel leading to a negligible ESR. Choosing 50 V capacitors instead of 35 V reduces the effects of DC bias and allows this example circuit to be rated for the maximum output voltage range of the TPS55340.

SELECTING THE INPUT CAPACITORS (C2, C7)

At least 4.7µF of ceramic input capacitance is recommended. Additional input capacitance may be required to meet ripple and/or transient requirements. High quality ceramic, type X5R or X7R are recommended to minimize capacitance variations over temperature. The capacitor must also have an RMS current rating greater than the maximum RMS input current of the TPS55340 calculated with Equation 22. The input capacitor must also be rated greater than the maximum input voltage. The input voltage ripple can be calculated with Equation 23.

$$I_{CI}rms = \frac{\Delta I_L}{\sqrt{12}} \quad (22)$$

$$V_I ripple = \frac{\Delta I_L}{4 \times f_{SW} \times C_{IN}} + \Delta I_L \times R_{CIN} \quad (23)$$

In the design example, the input RMS current is calculated to be 191 mA. The chosen input capacitor is a 10 µF, 35V 1210 X7R with 3 mΩ ESR. Although one with a lower voltage rating can be used, a 35 V rated capacitor was chosen to limit the affects of dc bias and to allow it the circuit to be rated for the entire input range of the TPS55340. The input ripple is calculated to be 30 mV. An additional 0.1 µF, 50V 0603 X5R is located close to the VIN and GND pins for extra decoupling.

SETTING OUTPUT VOLTAGE (R1, R2)

To set the output voltage in either DCM or CCM, select the values of R1 and R2 according to the following equations.

$$V_{OUT} = 1.229V \times \left(\frac{R1}{R2} + 1 \right) \quad (24)$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{1.229V} - 1 \right) \quad (25)$$

Considering the leakage current through the resistor divider and noise decoupling into FB pin, an optimum value for R2 is around 10 kΩ. The output voltage tolerance depends on the V_{FB} accuracy and the tolerance of R1 and R2. In this example with a 24 V output using Equation 25, R1 is calculated to 185.3 kΩ. The nearest standard value of 187 kΩ is used.

SETTING THE SOFT-START TIME (C7)

Choose the appropriate capacitor to set soft-start time and avoid overshoot. Increasing the soft-start time reduces the overshoot during start-up. A 0.047 µF ceramic capacitor is used in this example.

SELECTING THE SCHOTTKY DIODE (D1)

The high switching frequency of the TPS55340 demands high-speed rectification for optimum efficiency. Ensure that the diode's average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the regulated output voltage. The diode must also be rated for the power dissipated which can be calculated with Equation 26.

$$P_D = V_D \times I_{OUT} \quad (26)$$

In this conservative design example, the diode is chosen to be rated for the maximum output current of 2.13 A. During normal operation with 800 mA output current and assuming a Schottky diode drop of 0.5V, the diode must be capable of dissipating 400 mW. The recommended minimum ratings for this design are a 40 V, 3 A diode. However to improve the flexibility of this design, a Diodes Inc B540-13-F in an SMC package is used with voltage and current ratings of 40 V and 5A.

COMPENSATING THE CONTROL LOOP (R3, C4, C5)

The TPS55340 requires external compensation which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external resistor R3 and ceramic capacitor C4 are connected to the COMP pin to provide a pole and a zero, shown in the application circuit. This pole and zero, along with the inherent pole and zero of a boost converter, determine the closed loop frequency response. This is important for converter stability and transient response. Loop compensation should be designed for the minimum operating voltage.

The following equations summarize the loop equations for the TPS55340 configured as a CCM boost converter. They include the power stage output pole (f_{OUT}) and the right-half-plane zero (f_{RHPZ}) of a boost converter calculated with Equation 27 and Equation 28 respectively. When calculating f_{OUT} it is important to include the derating of ceramic output capacitors. In the example with an estimated 10.2 µF capacitance, these frequencies are calculated to 980 kHz and 22.1 kHz respectively. The DC gain (A) of the power stage is calculated with Equation 27 and is 39.9 dB in this design. The compensation pole (f_P) and zero (f_Z) generated by R3, C4 and internal transconductance amplifier are calculated with Equation 30 and Equation 31 respectively.

Most CCM boost converters will have a stable control loop if f_Z is set slightly above f_P through proper sizing of R3 and C4. A good starting point is C4 = 0.1 µF and R3 = 2kΩ. Increasing R3 or reducing C4 increases the closed loop bandwidth, and therefore improves the transient response. Adjusting R3 and C4 in opposite direction increases the phase and gain margin of the loop, which improves loop stability. It is generally recommended to limit the bandwidth of the loop to the lower of either 1/5 of the switching frequency f_{SW} or 1/3 the RHPZ frequency, f_{RHPZ} shown in Equation 28. The spreadsheet tool located in the TPS55340 product folder at www.ti.com can also be used to aid in compensation design.

$$f_{OUT} \approx \frac{2}{2\pi \times R_{OUT} \times C_{OUT}} \tag{27}$$

$$f_{RHPZ} \approx \frac{R_{OUT}}{2\pi \times L} \times \left(\frac{V_{IN}}{V_{OUT}} \right)^2 \tag{28}$$

$$A = \frac{1.229}{V_{OUT}} \times Gea \times 10M\Omega \times \frac{V_{IN}}{V_{OUT} \times R_{SENSE}} \times R_{OUT} \times \frac{1}{2} \tag{29}$$

$$f_P = \frac{1}{2\pi \times 10M\Omega \times C4} \tag{30}$$

$$f_Z = \frac{1}{2\pi \times R3 \times C4} \tag{31}$$

$$fco1 = \frac{f_{SW}}{5} \tag{32}$$

$$fco2 = \frac{f_{RHPZ}}{3} \tag{33}$$

Where

C_{OUT} is the equivalent output capacitor (C_{OUT}=C8+C9+C10)
R_{OUT} is the equivalent load resistance (V_{OUT}/I_{OUT})
Gea is the error amplifier transconductance located in the ELECTRICAL CHARACTERISTICS table
R_{SENSE} (15mΩ, typical) is the sense resistor in the current control loop
f_{co1} and f_{co2} are possible bandwith.

An additional capacitor from the COMP pin to GND (C5) can be used to place a high frequency pole in the control loop. This is not always necessary with ceramic output capacitors. If a non-ceramic output capacitor is used, there is an additional zero (f_{ZESR}) in the control loop which can be calculated with Equation 35. The value of C5 and the pole created by C5 can be calculated with Equation 36 and Equation 34 respectively. Finally if more phase margin is needed, an additional zero (f_{ZFF}) can be added by placing a capacitor (C_{FF}) in parallel with the top feedback resistor R1. It is recommended to place the zero at the target cross-over frequency or higher. The feed forward capacitor also adds a pole at a higher frequency. The recommended value of C_{FF} can be calculated with Equation 37.

$$f_{P2} = \frac{1}{2\pi \times R3 \times C5} \tag{34}$$

$$f_{ZESR} \approx \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{35}$$

$$C5 = \frac{R_{ESR} \times C_{OUT}}{R3} \tag{36}$$

$$C_{FF} = \frac{1}{2\pi \times R1 \times f_{ZFF} \times \sqrt{\frac{V_{REF}}{V_{OUT}}}} \quad (37)$$

where R_{ESR} is the ESR of the output capacitor.

If a network measurement tool is available, the most accurate compensation design can be achieved following this procedure. The power stage frequency response is first measured using a network analyzer at the minimum 5 V input and maximum 800 mA load. This measurement is shown in Figure 16. In this design only one pole and one zero are used, so the maximum phase increase from the compensation will be 180 degrees. For a 60 degree phase margin, the power stage phase must be –120 degrees at its lowest point. Based on the target 6 kHz bandwidth, the measured power stage gain, $K_{PS}(f_{BW})$, is 24.84 dB and the phase is –110.3 degrees.

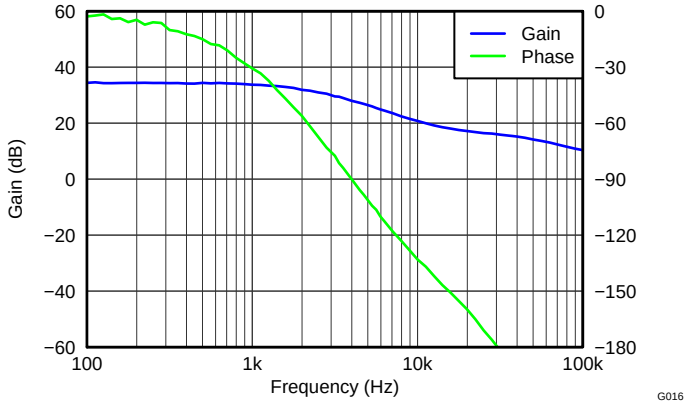


Figure 16. Power Stage Gain and Phase of the Boost Converter

R3 is then chosen to set the compensation gain to be the reciprocal of the power stage gain at the target bandwidth using Equation 38. C4 is then chosen to place a zero at 1/10 the target bandwidth with Equation 39. In this case R3 is calculated to be 2.56 kΩ, the nearest standard value 2.55 kΩ is used. C4 is calculated at 0.104 µF and the nearest standard value 0.100 µF is used. Although not necessary because this design uses all ceramic capacitors, a 100 pF capacitor is selected for C5 to add a high frequency pole at a frequency 100 times the target bandwidth.

$$R3 = \frac{1}{\left(Gea \times \frac{R1}{(R1+R2)} \times 10^{\frac{K_{PS}(f_{BW})}{20}} \right)} \quad (38)$$

$$C4 = \frac{1}{2\pi \times R3 \times \frac{f_{BW}}{10}} \quad (39)$$

CHARACTERISTICS OF THE BOOST CONVERTER

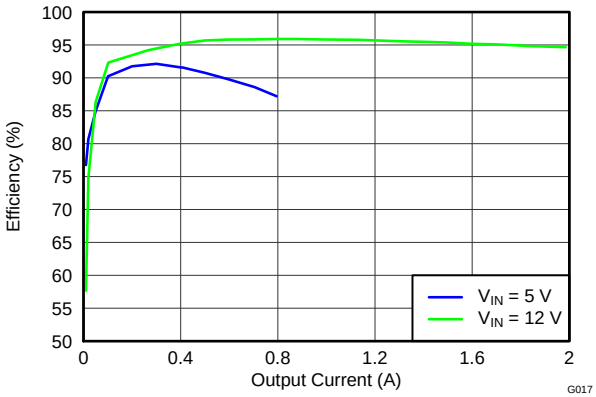


Figure 17. Efficiency vs Output Current

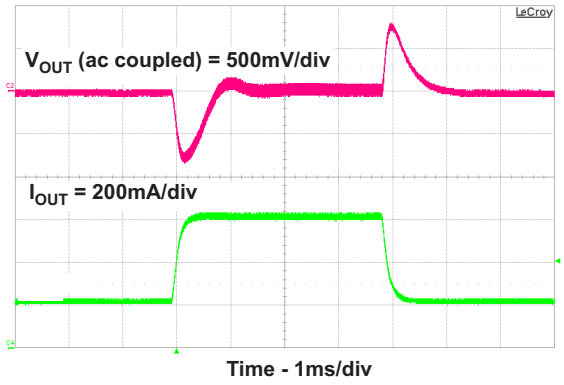


Figure 18. Load Transient Response

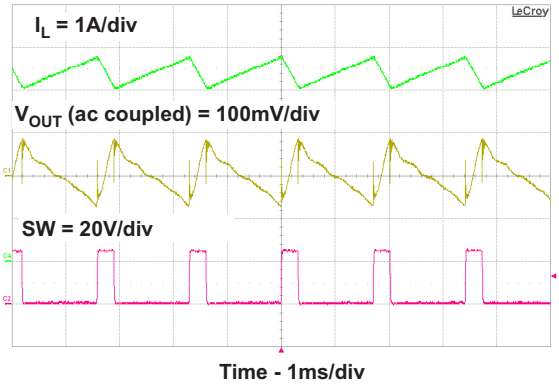


Figure 19. CCM PWM Operation

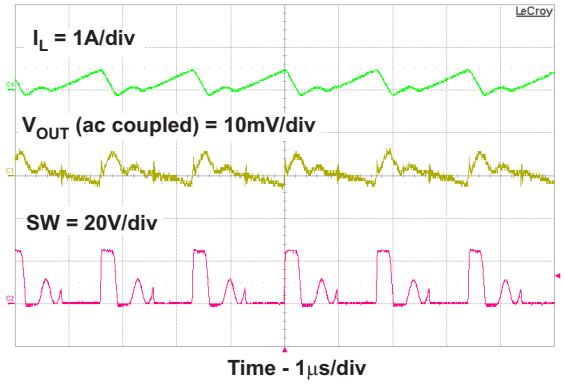


Figure 20. DCM PWM operation

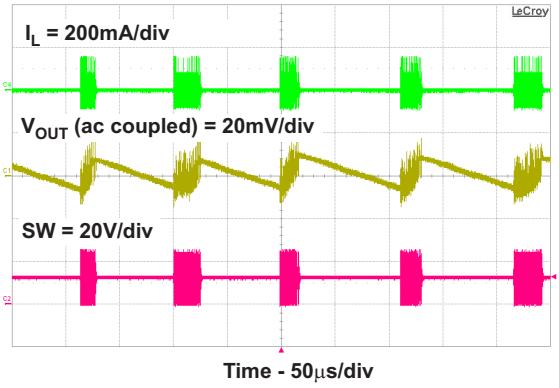


Figure 21. Pulse Skipping

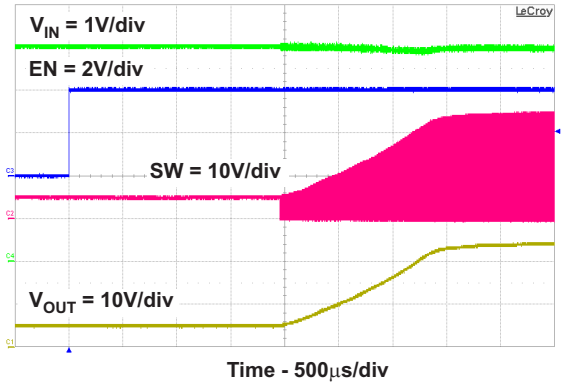


Figure 22. Start Up

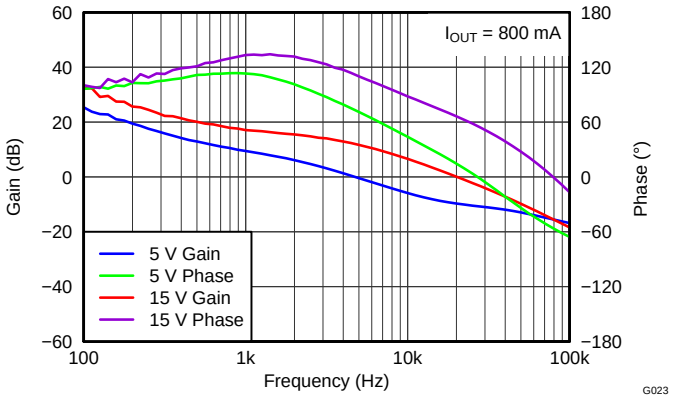


Figure 23. Closed Loop Gain and Phase of the Boost Converter

DESIGN GUIDE-STEP-BY-STEP DESIGN PROCEDURE OF SEPIC CONVERTER

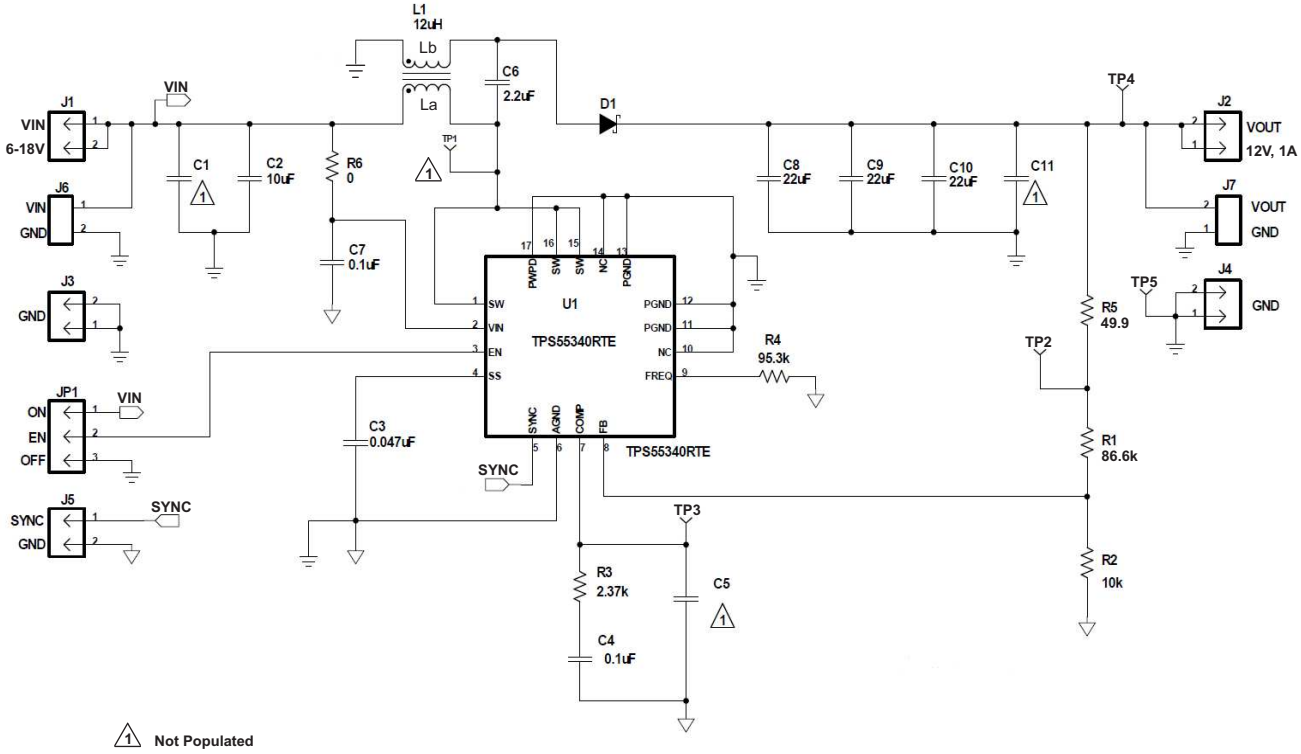


Figure 24. SEPIC Converter Application Schematic

The following parameters are used for a SEPIC converter design. These calculations are performed only for CCM operation, and the use of a coupled inductor is assumed.

Table 2. Key Parameters of SEPIC Converter Example

PARAMETER	VALUE
Output Voltage	12 V
Input Voltage	6 V to 18 V, 12 V nominal
Maximum Output Current	1 A
Transient Response 50% load step (ΔV_{OUT} = 4%)	480 mV
Output Voltage Ripple (0.5% of V_{OUT})	60 mV

SELECTING THE SWITCHING FREQUENCY (R4)

A 500 kHz switching frequency (f_{SW}) is selected for this design. Using Equation 1, R4 is calculated and the nearest standard value 95.3 kΩ is used.

DUTY CYCLE

The duty cycle of a SEPIC converter is calculated with Equation 40. With the 6 V minimum input the duty cycle is 68% and with the 18 V maximum input voltage the duty cycle is 41%.

$$D = \frac{V_{OUT} + V_D}{V_{OUT} + V_D + V_{IN}} \quad (40)$$

SELECTING THE INDUCTOR (L1)

With an estimated 85% efficiency, the input current is calculated with Equation 9 to be 2.35 A. With K_{IND} of 0.3 and the maximum 18 V input the minimum inductance is calculated to be 10.5µH using Equation 41. The nearest standard value of 12µH is used. As mentioned previously, this equation assumes a coupled inductor is used.

$$L \geq \frac{V_{IN}max \times Dmin}{2 \times f_{SW} \times I_{IN}DC \times K_{IND}} \quad (41)$$

The inductor ripple current is recalculated to be 615mA with Equation 42. The peak current is calculated to 3.69 A. The typical current limit is used as the saturation rating for the inductor used. The RMS current for La is approximately the average input current 2.35 A. The RMS current for Lb is approximately the output current of 1 A. For this design a CoilCraft MSD1260-123 is used with 6.86 A saturation, 74 mΩ DCR and 3.12 A RMS current rating for one winding.

$$\Delta I_L = \frac{V_{IN}max \times Dmin}{2 \times f_{SW} \times L} \quad (42)$$

$$I_L peak = I_{La}peak + I_{Lb}peak = \left(I_{IN}DC + \frac{\Delta I_L}{2}\right) + \left(I_{OUT} + \frac{\Delta I_L}{2}\right) \quad (43)$$

CALCULATING THE MAXIMUM OUTPUT CURRENT

The maximum output current with the minimum input voltage 6 V, chosen inductance 12µH, 5.25 A minimum current limit and estimated 85% efficiency is calculated to be 1.47 A using Equation 44.

$$I_{OUT}max = \frac{(I_{LIM} - \Delta I_L)}{\left(\frac{V_{OUT}}{V_{IN}min \times \eta_{EST}} + 1\right)} = \frac{(I_{LIM} - I_{IN}DC \times K_{IND})}{\left(\frac{V_{OUT}}{V_{IN}min \times \eta_{EST}} + 1\right)} \quad (44)$$

SELECTING THE OUTPUT CAPACITOR (C8-C10)

To meet the 60 mV ripple specification, the minimum output capacitance is calculated to be 22.5µF with Equation 45. This design uses ceramic output capacitors and the effects of ESR are ignored. To meet the transient response of 500mA with less than 480mV voltage change and a 7kHz control loop bandwidth, the minimum output capacitance is calculated to be 23.7µF using Equation 46. The RMS current is calculated with Equation 22 to be 1.44 A. The output capacitors used in this design is 3 x 22 µF, 25 V X7R 1210 ceramic capacitors. With voltage derating, the effective total output capacitance is estimated to be 30.4 µF.

$$C_{OUT} \geq \frac{Dmax \times I_{OUT}}{f_{SW} \times V_{RIPPLE}} \quad (45)$$

$$C_{OUT} \geq \frac{\Delta I_{TRAN}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} \quad (46)$$

SELECTING THE SERIES CAPACITOR (C6)

The series capacitor is chosen to limit the ripple current to 5% of the maximum input voltage. Using Equation 47 the minimum capacitance is 1.5 µF. Using Equation 48 the RMS current is calculated to be 1.63A. A 2.2 µF ceramic capacitor in a 1206 package is selected.

$$C_P \geq \frac{I_{OUT} \times Dmax}{0.05 \times V_{IN}max \times f_{SW}} \quad (47)$$

$$I_{CP}rms = I_{IN}DC \times \sqrt{\frac{(1 - Dmax)}{Dmax}} \quad (48)$$

SELECTING THE INPUT CAPACITOR (C2, C7)

Based on the minimum 4.7µF ceramic recommended for the TPS55340, a 10µF X7R input capacitor is used with an additional 0.1µF placed close to the VIN and GND pins. With an estimated 6 µF capacitance after voltage derating, the input ripple voltage is calculated to be 39.9mV using Equation 49. The RMS current of the input capacitance is calculated to be 0.177 A with Equation 50.

$$V_{Iripple} = \frac{\Delta I_L}{4 \times f_{SW} \times C_{IN}} \quad (49)$$

$$I_{CI}rms = \frac{\Delta I_L}{\sqrt{12}} \quad (50)$$

SELECTING THE SCHOTTKY DIODE (D1)

The selected diode must have a minimum breakdown voltage (V_{BR}) calculated with Equation 51 which is 30.5 V in this design. The average current rating is recommended to be greater than the maximum output current. With the maximum 18 V input, average current is calculated to be 2.6 A using Equation 17. The package must also be capable of handling the power dissipation. With an estimated 0.5V forward voltage, power dissipation is calculated with Equation 26 to be 500mW. Diodes Inc B340B is chosen with a 40 V, 3 A rating in a SMB package.

$$V_{BR} = V_O + V_{IN}max + V_F \quad (51)$$

SETTING THE OUTPUT VOLTAGE (R1, R2)

With R2 fixed at 10 kΩ using Equation 25 the nearest standard value of 86.6 kΩ is chosen for R1.

SETTING THE SOFT-START TIME (C3)

The recommended 0.047µF soft-start capacitor is used.

MOSFET RATING CONSIDERATIONS

In a SEPIC converter the MOSFET must be rated to handle the sum of the input and output voltages. In this design with the maximum input voltage of 18 V and output voltage of 12 V the FET will see approximately 30 V. A 10% tolerance is recommended to account for any ringing. The 40V rating of the TPS55340 power MOSFET comfortably satisfies this requirement.

COMPENSATING THE CONTROL LOOP (R3, C4)

This design was compensated by measuring the frequency response of the power stage at the lowest input voltage of 6 V and choosing the components for the desired bandwidth. The lowest right half plane zero (f_{RHPZ}) is calculated to be 36.7kHz with Equation 52. Using the recommendation to limit the bandwidth to 1/3 of f_{RHPZ} the maximum recommended is 12.2kHz.

$$f_{RHPZ} = \frac{\frac{V_{OUT}}{I_{OUT}}}{2 \times \pi \times L \times \left(\frac{D}{(1-D)}\right)^2} \quad (52)$$

This design also uses only one pole and one zero. In order to achieve approximately 60 degrees of phase margin, the power stage phase must be no lower than approximately –120 degrees at the desired bandwidth. To ensure a stable design, R3 was initially set to 1kΩ and C4 was 1µF. Figure 25 shows the measurement of the power stage At 7kHz the power stage has a gain of 19.52 dB and phase of –118.1 degrees.

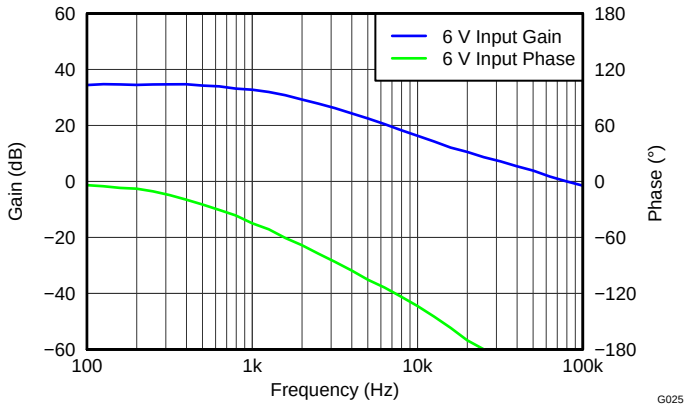


Figure 25. SEPIC Power Stage Gain and Phase

As there are no changes in the transconductance amplifier, the equations used to calculate the external compensation components in a boost design can be used in the SEPIC design. Using the maximum Gea from the electrical specification of 440 µmho, Equation 38 calculates the nearest standard value of R3 to be 2.37 kΩ. Using Equation 39, C4 is calculated to the nearest standard value of 0.1 µF.

CHARACTERISTICS OF THE SEPIC CONVERTER

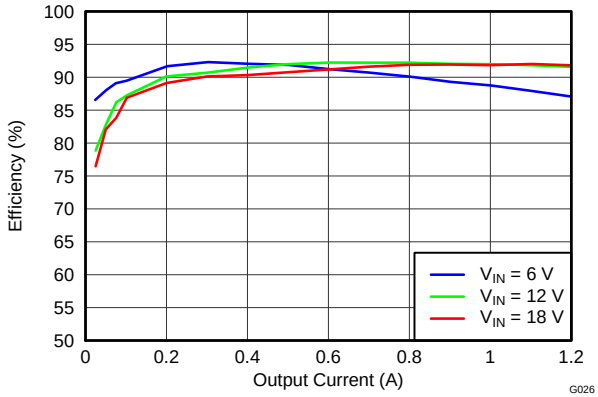


Figure 26. Efficiency vs Output Current

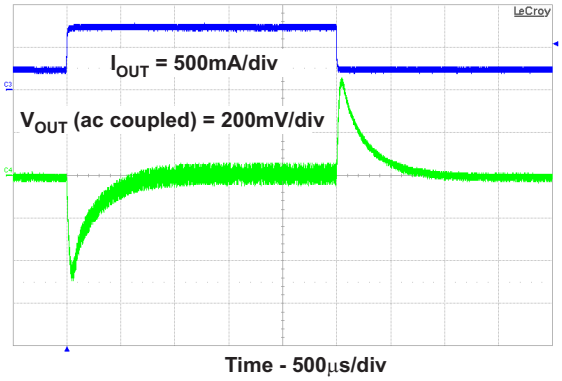


Figure 27. Load Transient Response

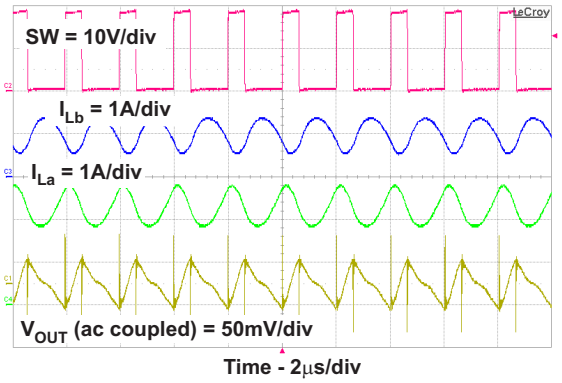


Figure 28. CCM PWM Operation

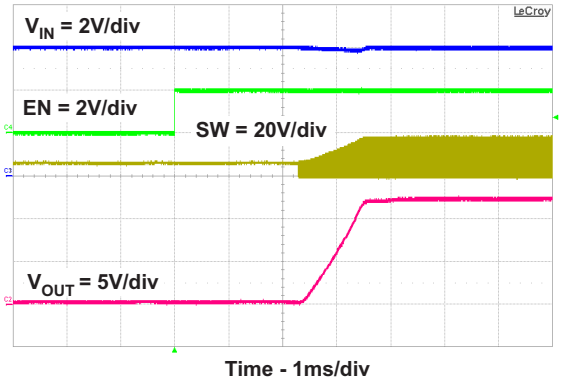


Figure 29. Output Voltage Soft-start

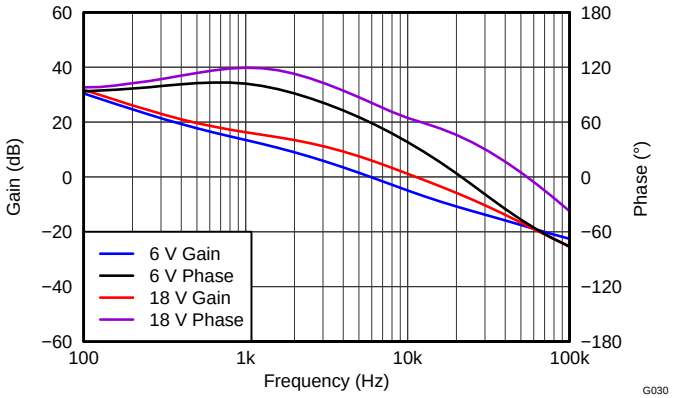


Figure 30. Closed Loop Gain and Phase of the SEPIC Converter

REVISION HISTORY

Changes from Original (May 2012) to Revision A **Page**

- Added PWP package 1
- Added HTSSOP-14 package to FEATURES 1
- Added 14-pin HTSSOP package to DESCRIPTION 1
- Added paragraph to end of DESCRIPTION 1
- Added PWP package to PIN ASSIGNMENTS 2
- Added PWP package to PIN FUNCTIONS 2
- Added HTSSOP package to THERMAL INFORMATION 4

Changes from Revision A (October 2012) to Revision B **Page**

- Corrected the pin numbers to the QFN-16 Package drawing 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS55340PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340	Samples
TPS55340PWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340	Samples
TPS55340RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340	Samples
TPS55340RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

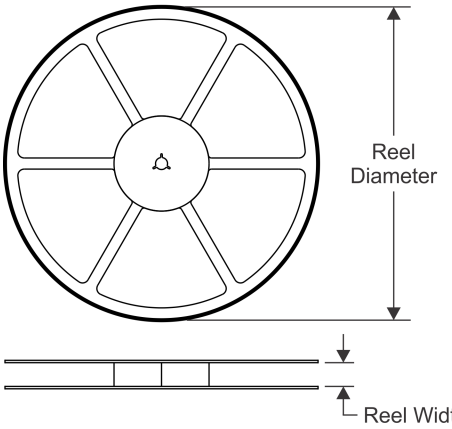
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

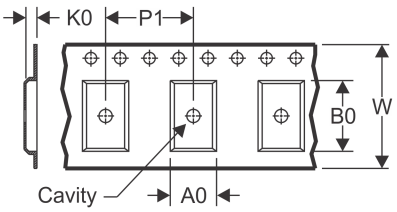
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

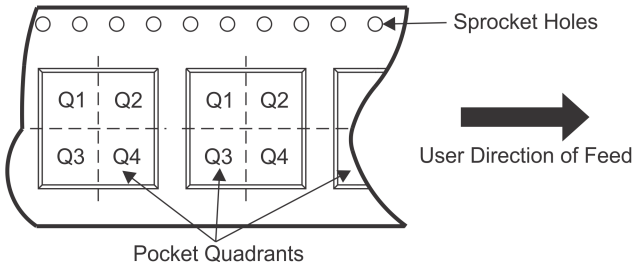


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

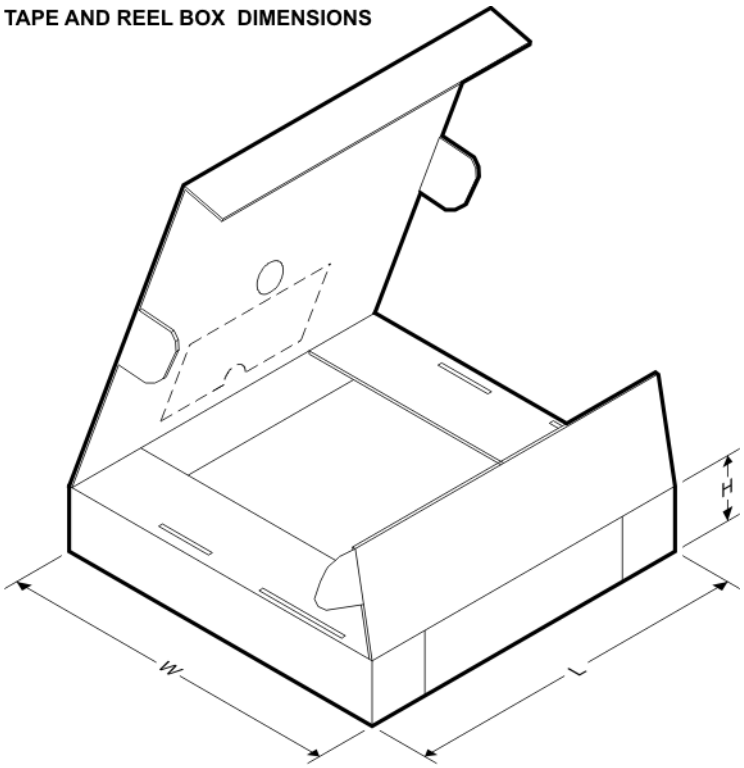
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55340PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS55340RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS55340RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

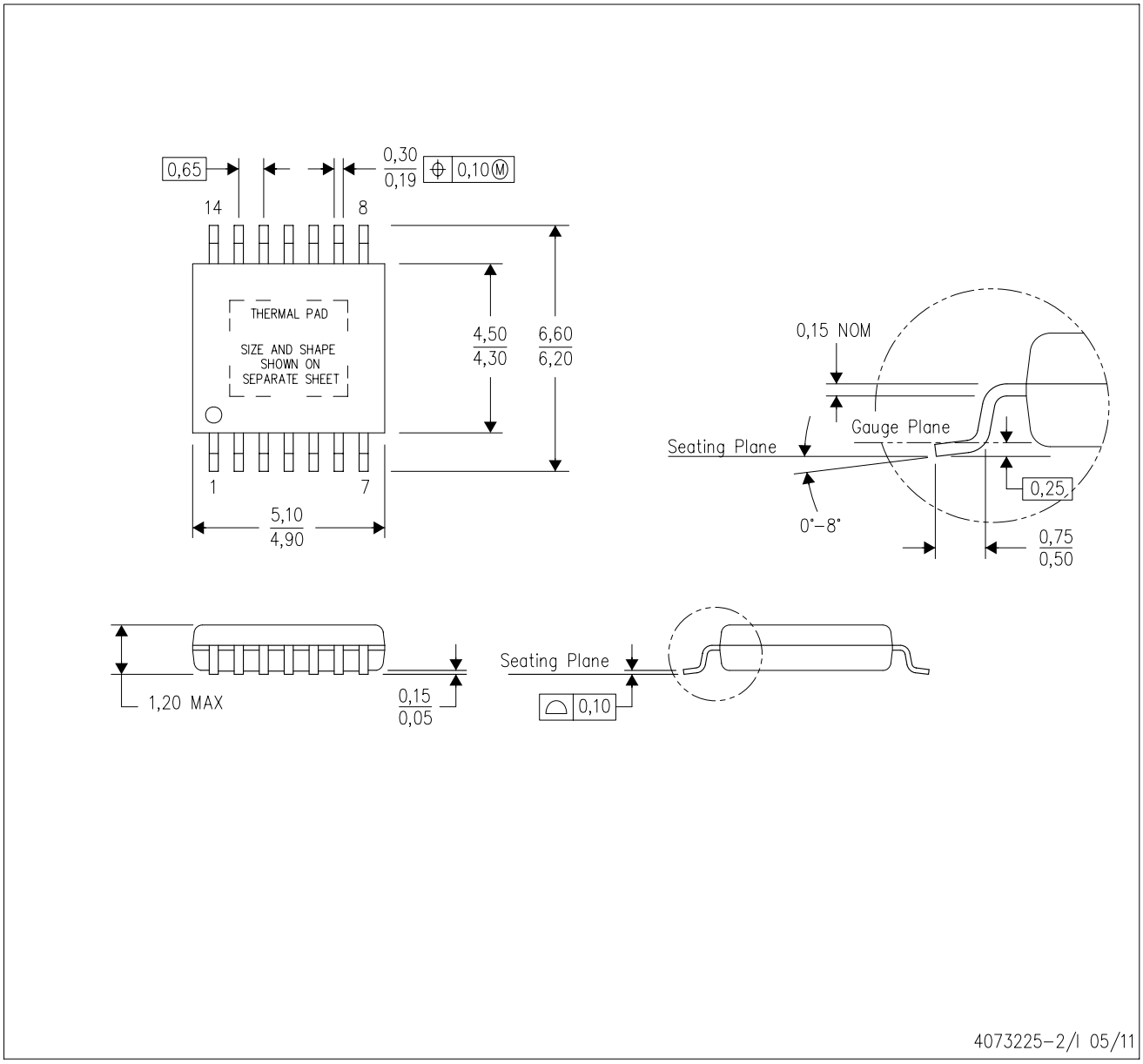
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55340PWPR	HTSSOP	PWP	14	2000	367.0	367.0	35.0
TPS55340RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS55340RTET	WQFN	RTE	16	250	210.0	185.0	35.0

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

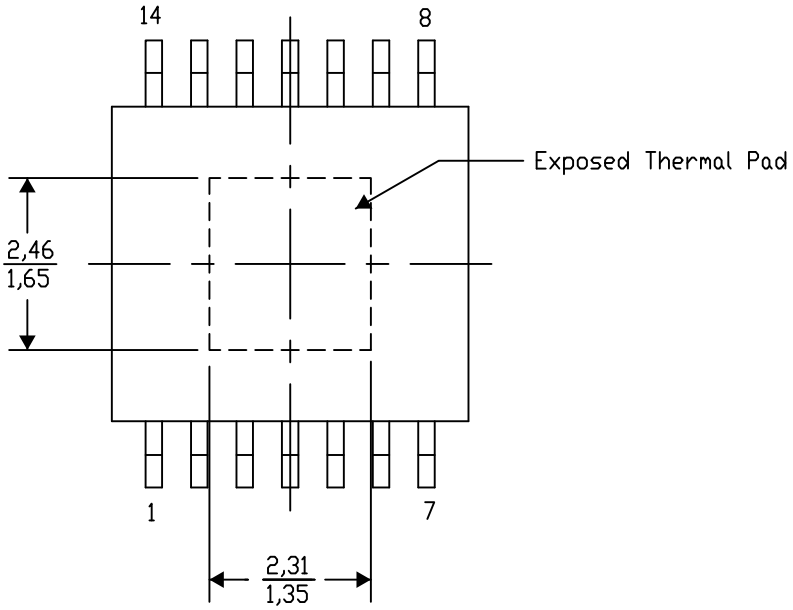
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

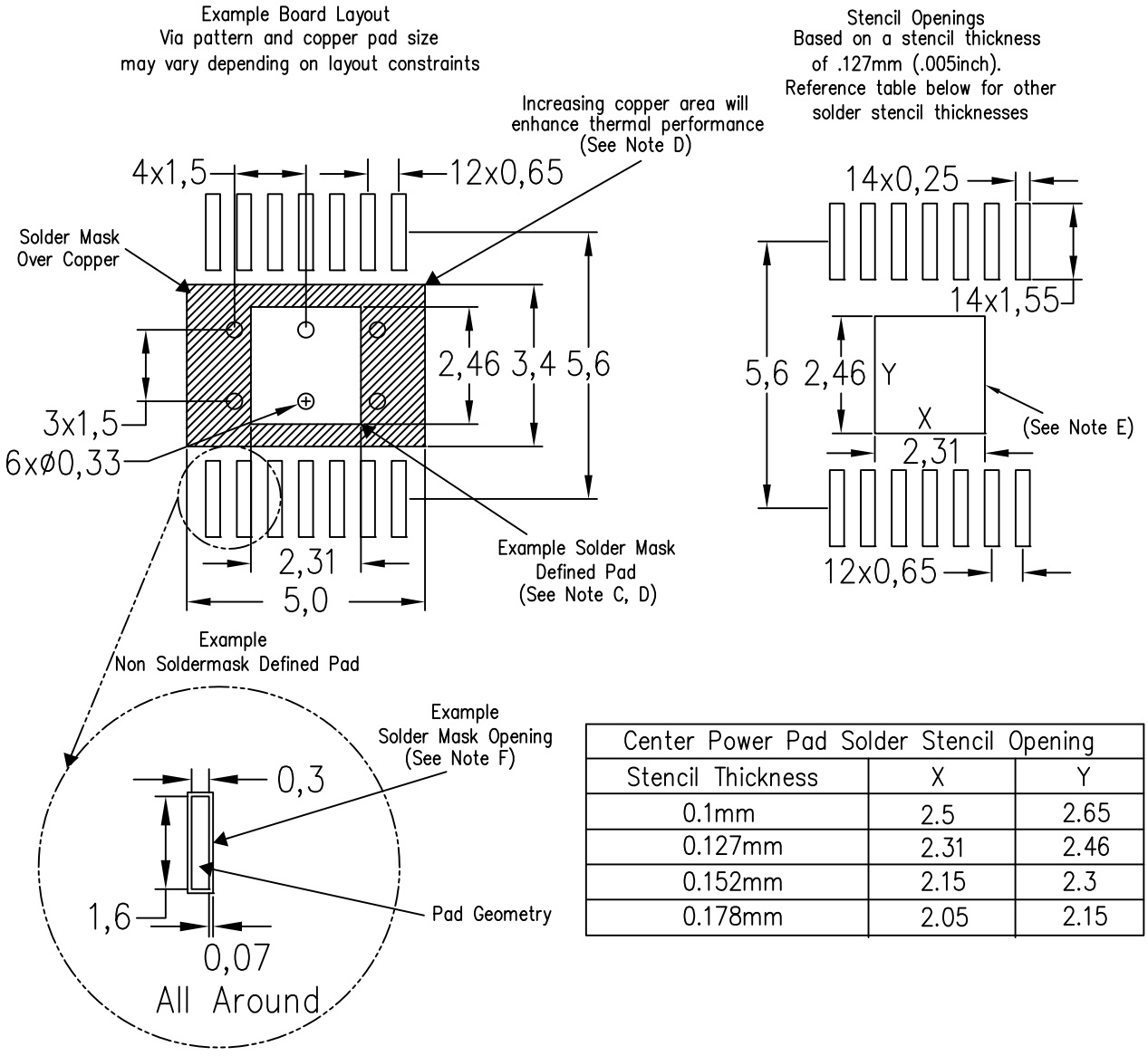
Exposed Thermal Pad Dimensions

4206332–2/AG 08/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

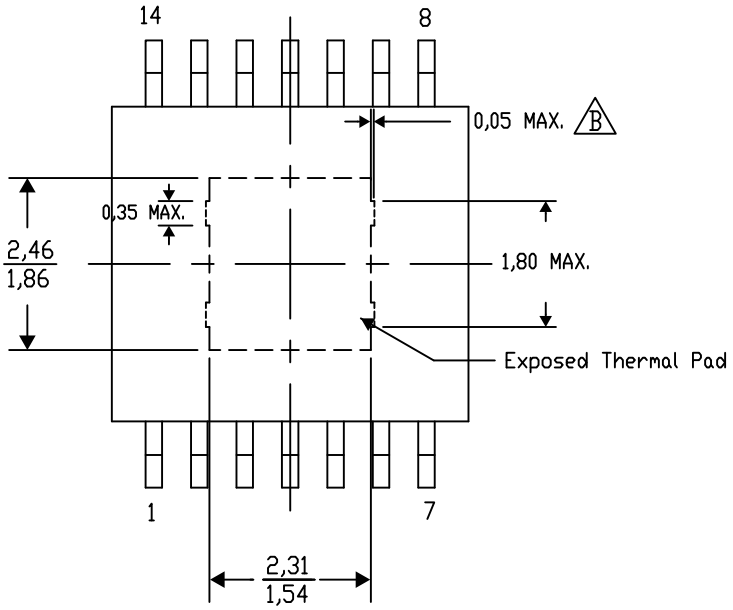
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

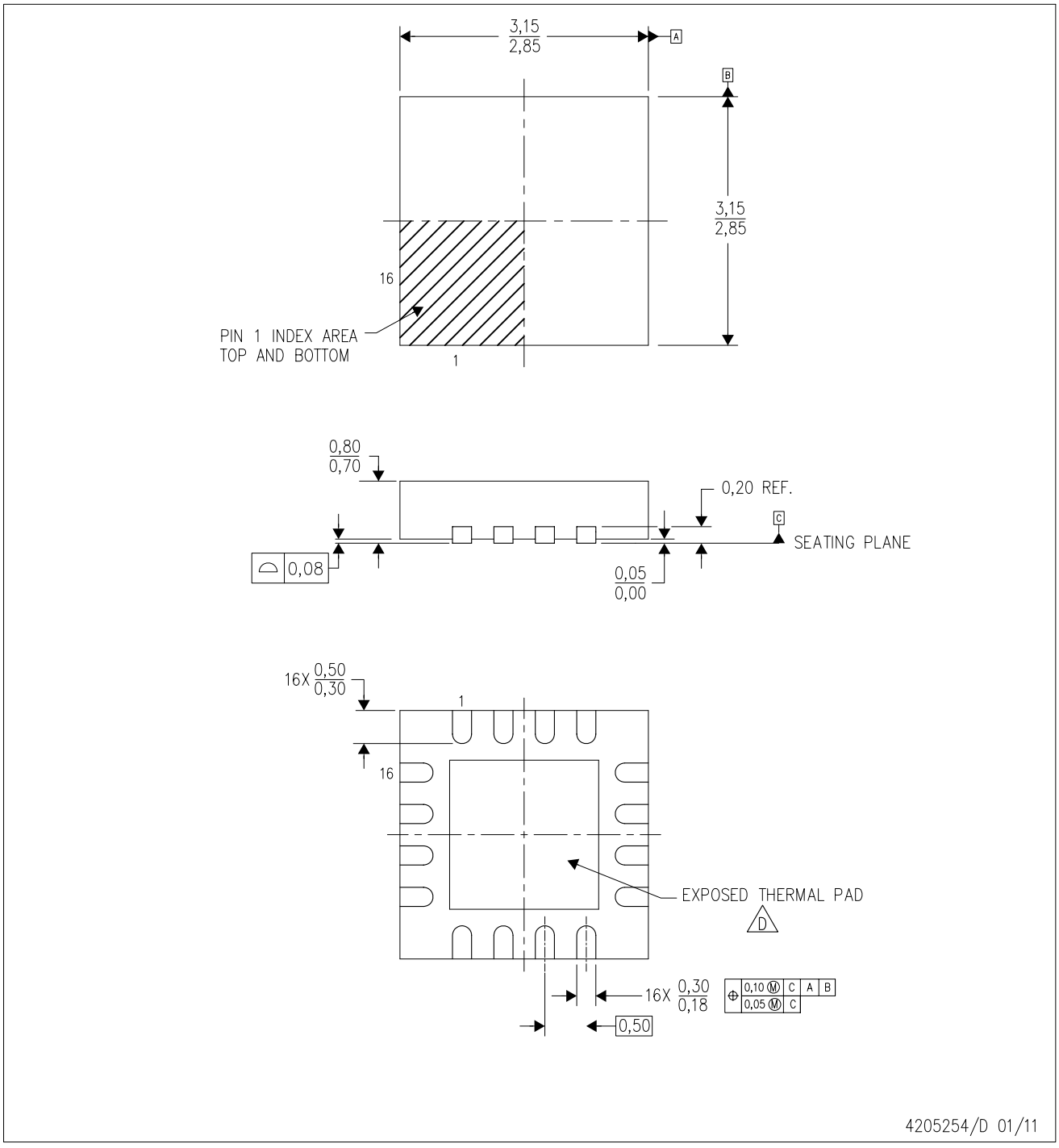
4206332–44/AF 06/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

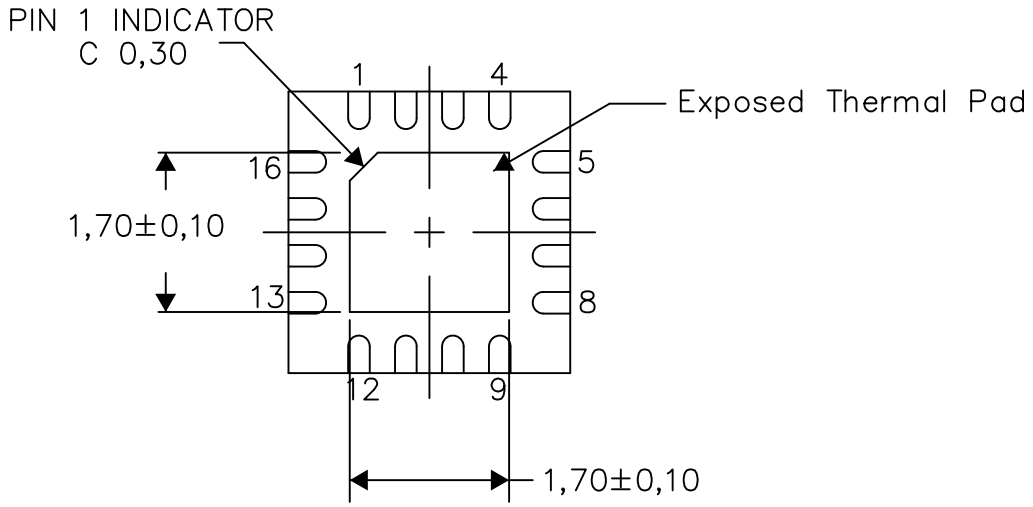
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



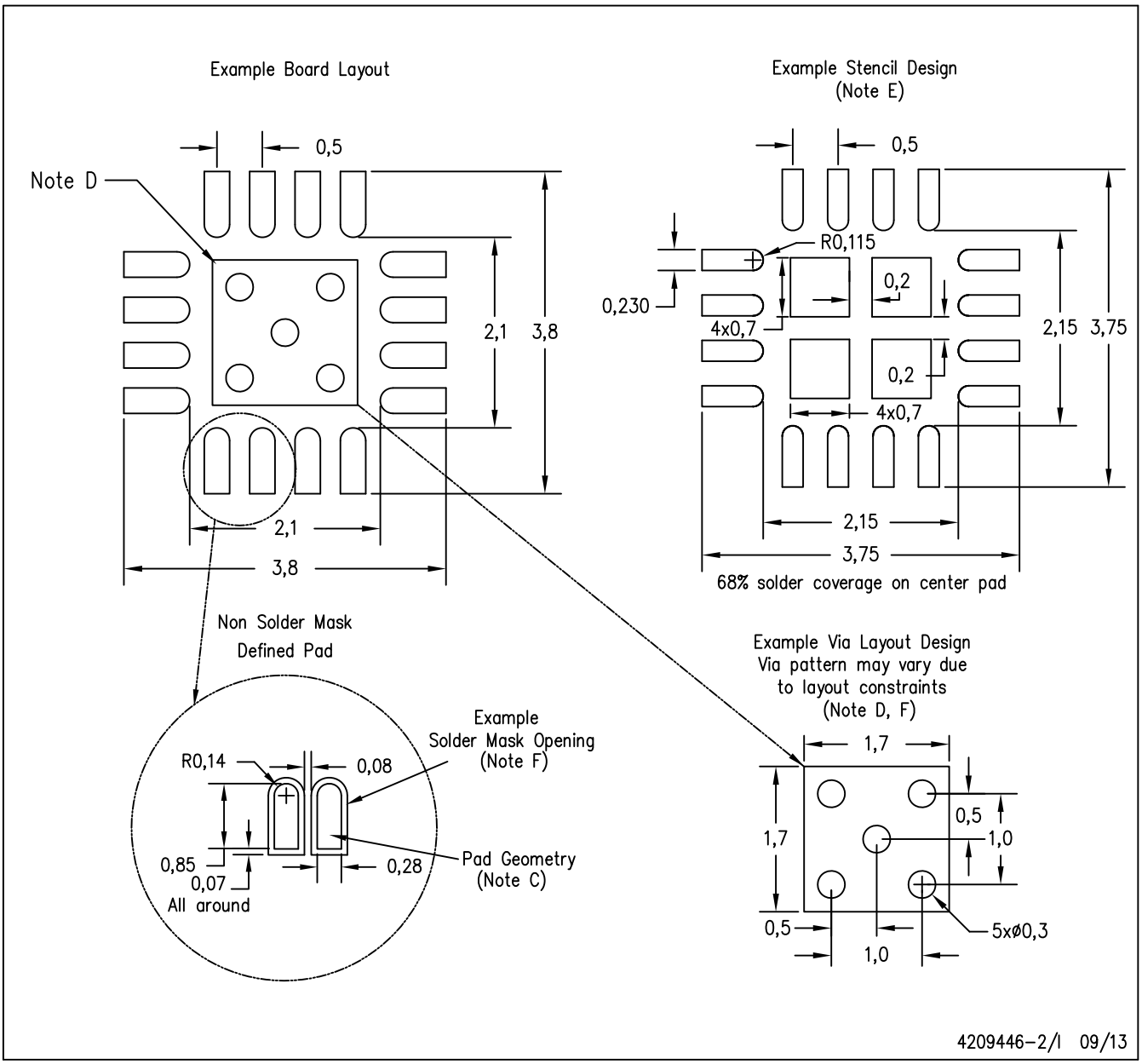
Bottom View

Exposed Thermal Pad Dimensions

4206446–3/0 09/13

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265