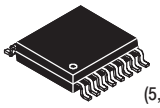
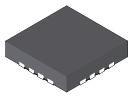




96% EFFICIENT SYNCHRONOUS BOOST CONVERTER WITH 4A SWITCH

Check for Samples: TPS61030, TPS61031, TPS61032

FEATURES

- **96% Efficient Synchronous Boost Converter With 1000-mA Output Current From 1.8-V Input**
- **Device Quiescent Current: 20-µA (Typ)**
- **Input Voltage Range: 1.8-V to 5.5-V**
- **Fixed and Adjustable Output Voltage Options Up to 5.5-V**
- **Power Save Mode for Improved Efficiency at Low Output Power**
- **Low Battery Comparator**
- **Low EMI-Converter (Integrated Antiringing Switch)**
- **Load Disconnect During Shutdown**
- **Over-Temperature Protection**
- **Available in a Small 4 mm x 4 mm QFN-16 or in a TSSOP-16 Package**

APPLICATIONS

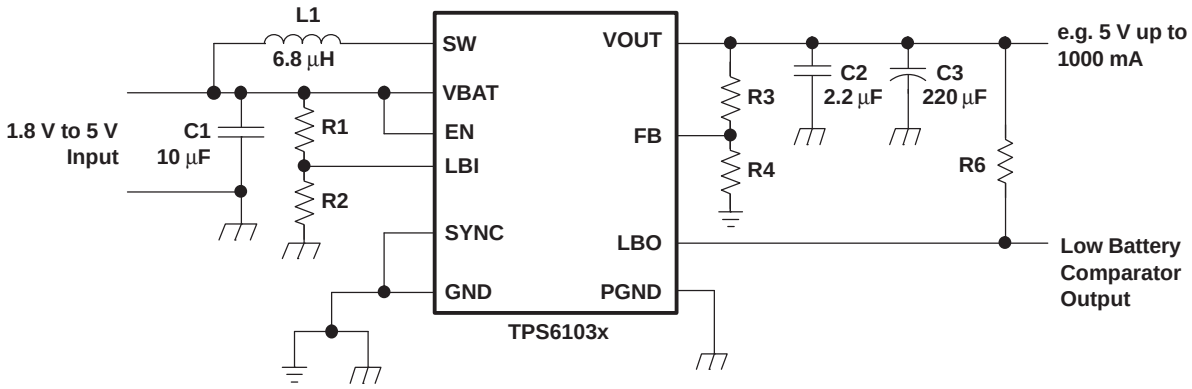
- **All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment**

DESCRIPTION

The TPS6103x devices provide a power supply solution for products powered by either a one-cell Li-Ion or Li-polymer, or a two to three-cell alkaline, NiCd or NiMH battery. The converter generates a stable output voltage that is either adjusted by an external resistor divider or fixed internally on the chip. It provides high efficient power conversion and is capable of delivering output currents up to 1 A at 5 V at a supply voltage down to 1.8 V. The implemented boost converter is based on a fixed frequency, pulse-width- modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency. At low load currents the converter enters Power Save mode to maintain a high efficiency over a wide load current range. The Power Save mode can be disabled, forcing the converter to operate at a fixed switching frequency. It can also operate synchronized to an external clock signal that is applied to the SYNC pin. The maximum peak current in the boost switch is limited to a value of 4500 mA.

The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. A low-EMI mode is implemented to reduce ringing and, in effect, lower radiated electromagnetic energy when the converter enters the discontinuous conduction mode.

The device is packaged in a 16-pin QFN package measuring 4 mm x 4 mm (RSA) or in a 16-pin TSSOP PowerPAD® package (PWP).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a registered trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OUTPUT VOLTAGE OPTIONS(1)

T_A	OUTPUT VOLTAGE DC/DC	PACKAGE	PART NUMBER(2)
-40°C to 85°C	Adjustable	16-Pin TSSOP PowerPAD™	TPS61030PWP
	3.3 V		TPS61031PWP
	5 V		TPS61032PWP
	Adjustable	16-Pin QFN	TPS61030RSA
	3.3 V		TPS61031RSA
	5 V		TPS61032RSA

(1) Contact the factory to check availability of other fixed output voltage versions.
(2) The packages are available taped and reeled. Add R suffix to device type (e.g., TPS61030PWPR or TPS61030RSAR) to order quantities of 2000 devices per reel for the PWP packaged devices and 3000 units per reel for the RSA package.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	TPS6103x
Input voltage range on LBI	-0.3 V to 3.6 V
Input voltage range on SW, VOUT, LBO, VBAT, SYNC, EN, FB	-0.3 V to 7 V
Maximum junction temperature T_J	-40°C to 150°C
Storage temperature range T_{stg}	-65°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage at VBAT, V_I	1.8		5.5	V
Operating ambient temperature range, T_A	-40		85	°C
Operating virtual junction temperaturerange, T_J	-40		125	°C

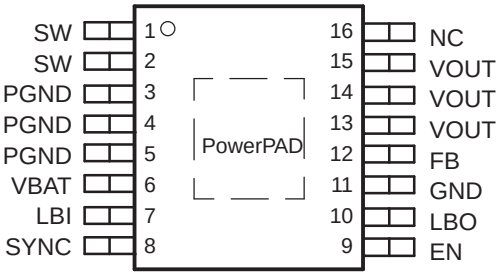
electrical characteristics

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

DC/DC STAGE							
PARAMETER			**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
V_I	Input voltage range			1.8		5.5	V
V_O	TPS61030 output voltage range			1.8		5.5	V
V_{FB}	TPS61030 feedback voltage			490	500	510	mV
f	Oscillator frequency			500	600	700	kHz
	Frequency range for synchronization			500		700	kHz
	Switch current limit		VOUT= 5 V	3600	4000	4500	mA
	Start-up current limit				0.4 x I_{SW}		mA
	SWN switch on resistance		VOUT= 5 V		55		mΩ
	SWP switch on resistance		VOUT= 5 V		55		mΩ
	Total accuracy			-3%		3%	
	Line regulation					0.6%	
	Load regulation					0.6%	
	Quiescent current	VBAT	I_O = 0 mA, V_{EN} = VBAT = 1.8 V, VOUT =5 V		10	25	µA
		VOUT	I_O = 0 mA, V_{EN} = VBAT = 1.8 V, VOUT = 5 V		10	20	µA
	Shutdown current		V_{EN}= 0 V, VBAT = 2.4 V		0.1	1	µA
CONTROL STAGE							
PARAMETER			**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
V_{UVLO}	Under voltage lockout threshold		V_{LBI} voltage decreasing		1.5		V
V_{IL}	LBI voltage threshold		V_{LBI} voltage decreasing	490	500	510	mV
	LBI input hysteresis				10		mV
	LBI input current		EN = VBAT or GND		0.01	0.1	µA
	LBO output low voltage		V_O = 3.3 V, I_{OI} = 100 µA		0.04	0.4	V
	LBO output low current				100		µA
	LBO output leakage current		V_{LBO}= 7 V		0.01	0.1	µA
V_{IL}	EN, SYNC input low voltage					0.2 × VBAT	V
V_{IH}	EN, SYNC input high voltage			0.8 × VBAT			V
	EN, SYNC input current		Clamped on GND or VBAT		0.01	0.1	µA
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

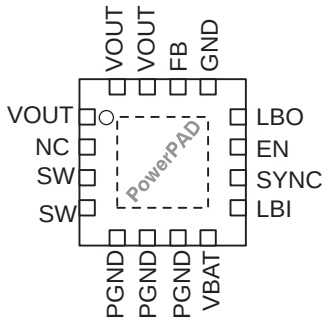
PIN ASSIGNMENTS

PWP PACKAGE
(TOP VIEW)



NC − No internal connection

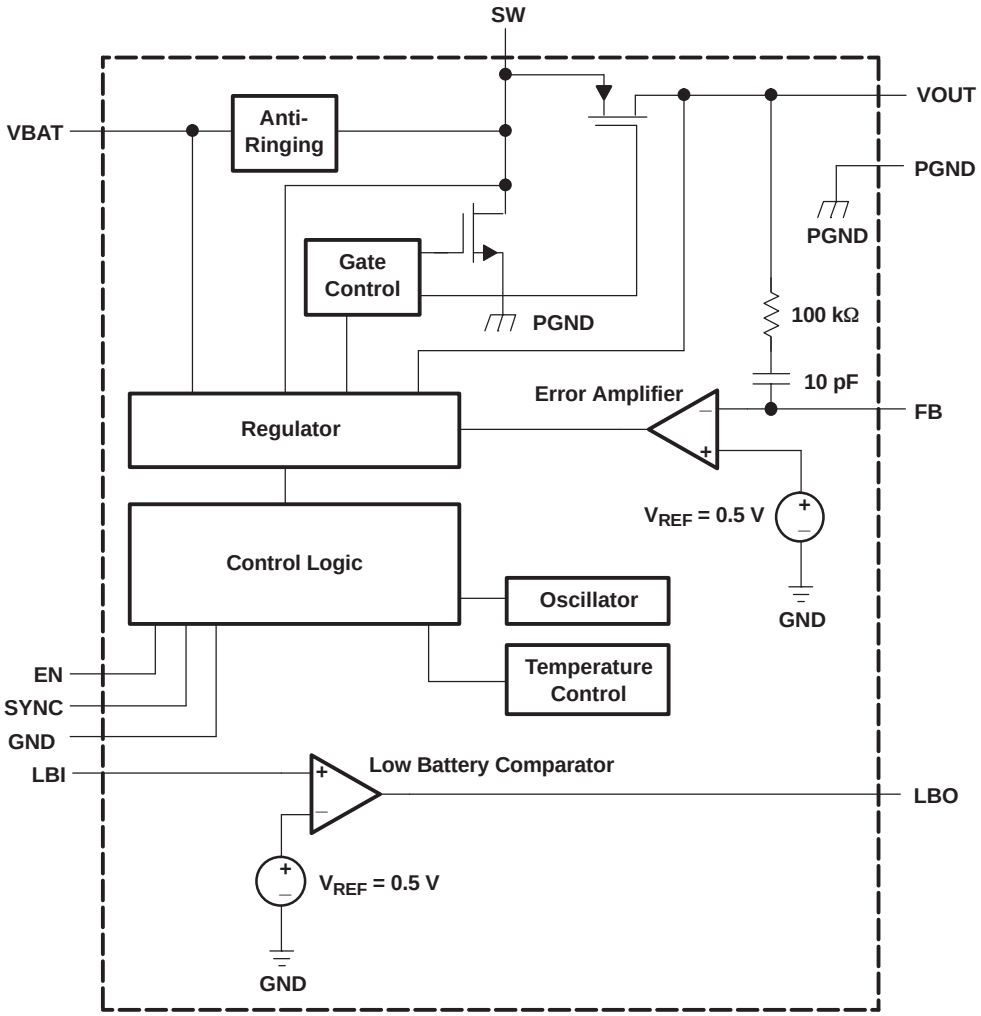
RSA PACKAGE
(TOP VIEW)



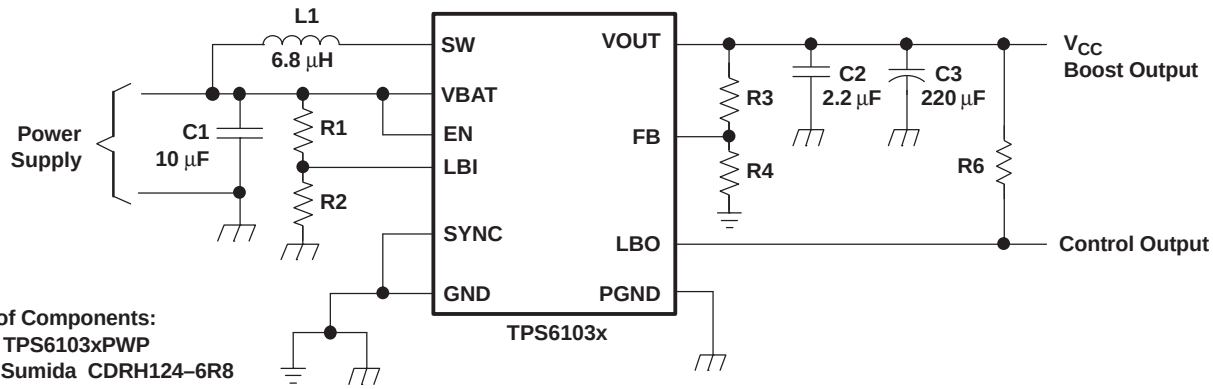
Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PWP	RSA		
EN	9	11	I	Enable input. (1/VBAT enabled, 0/GND disabled)
FB	12	14	I	Voltage feedback of adjustable versions
GND	11	13	I/O	Control/logic ground
LBI	7	9	I	Low battery comparator input (comparator enabled with EN)
LBO	10	12	O	Low battery comparator output (open drain)
NC	16	2		Not connected
SYNC	8	10	I	Enable/disable power save mode (1/VBAT disabled, 0/GND enabled, clock signal for synchronization)
SW	1, 2	3, 4	I	Boost and rectifying switch input
PGND	3, 4, 5	5, 6, 7	I/O	Power ground
VBAT	6	8	I	Supply voltage
VOUT	13, 14, 15	1, 15, 16	O	DC/DC output
PowerPAD™				Must be soldered to achieve appropriate power dissipation. Should be connected to PGND.

FUNCTIONAL BLOCK DIAGRAM



Parameter Measurement Information



List of Components:
U1 = TPS6103xPWP
L1 = Sumida CDRH124–6R8
C1, C2 = X7R/X5R Ceramic
C3 = Low ESR Tantalum

TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

DC/DC Converter		Figure
Maximum output current	vs Input voltage	1, 2
Efficiency	vs Output current (TPS61030) (V_O = 2.5 V, V_I = 1.8 V, VSYNC = 0 V)	3
	vs Output current (TPS61031) (V_O = 3.3 V, V_I = 1.8 V, 2.4 V, VSYNC = 0 V)	4
	vs Output current (TPS61032) (V_O = 5.0 V, V_I = 2.4 V, 3.3 V, VSYNC = 0 V)	5
	vs Input voltage (TPS61031) (I_O = 10 mA, 100 mA, 1000 mA, VSYNC = 0 V)	6
	vs Input voltage (TPS61032) (I_O = 10 mA, 100 mA, 1000 mA, VSYNC = 0 V)	7
Output voltage	vs Output current (TPS61031) (V_I = 2.4 V)	8
	vs Output current (TPS61032) (V_I = 3.3 V)	9
No-load supply current into VBAT	vs Input voltage (TPS61032)	10
No-load supply current into VOUT	vs Input voltage (TPS61032)	11
Minimum Load Resistance at Startup	vs Input voltage (TPS61032)	12
Waveforms	Output voltage in continuous mode (TPS61032)	13
	Output voltage in power save mode (TPS61032)	14
	Load transient response (TPS61032)	15
	Line transient response (TPS61032)	16
	DC/DC converter start-up after enable (TPS61032)	17

TPS61031
MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

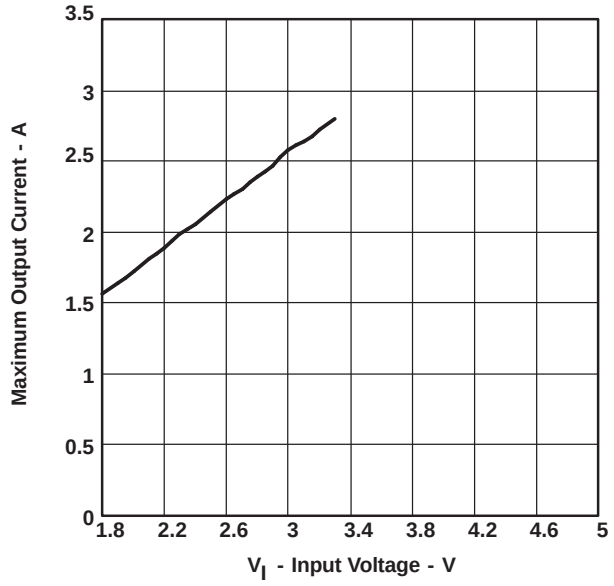


Figure 1.

TPS61032
MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

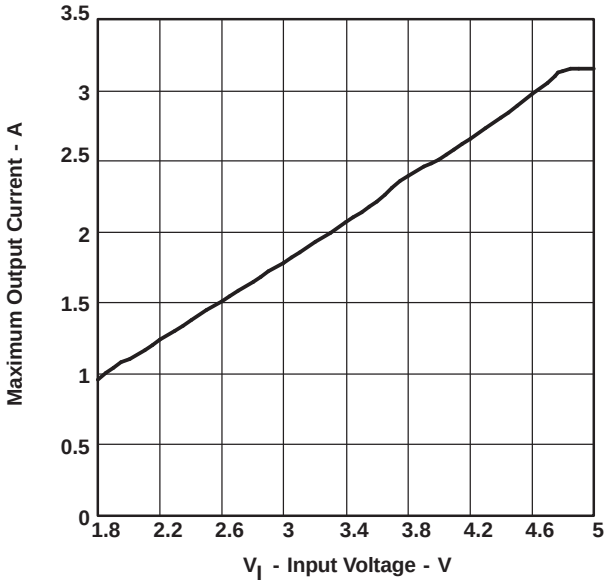


Figure 2.

TPS61030
EFFICIENCY
vs
OUTPUT CURRENT

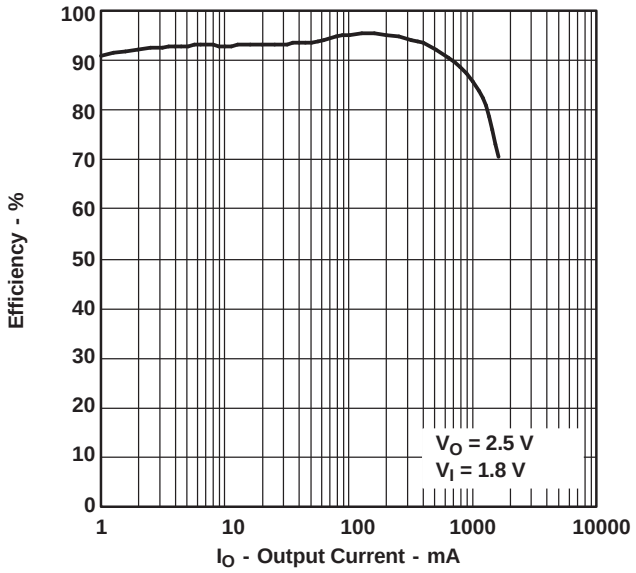


Figure 3.

TPS61031
EFFICIENCY
vs
OUTPUT CURRENT

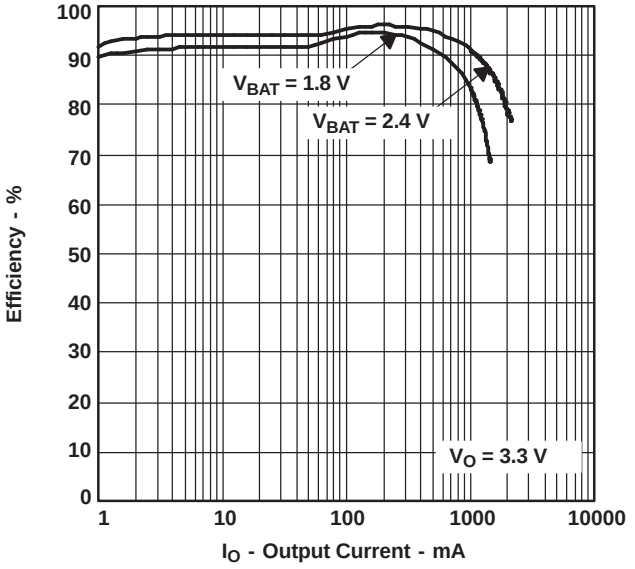


Figure 4.

TPS61032
EFFICIENCY
vs
OUTPUT CURRENT

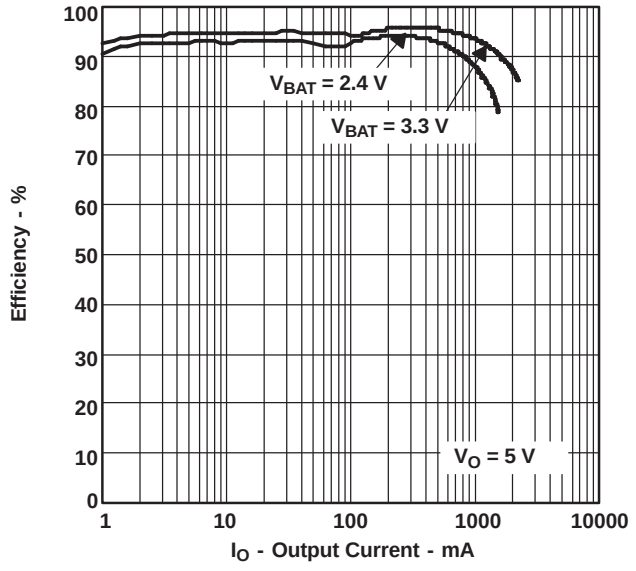


Figure 5.

TPS61031
EFFICIENCY
vs
INPUT VOLTAGE

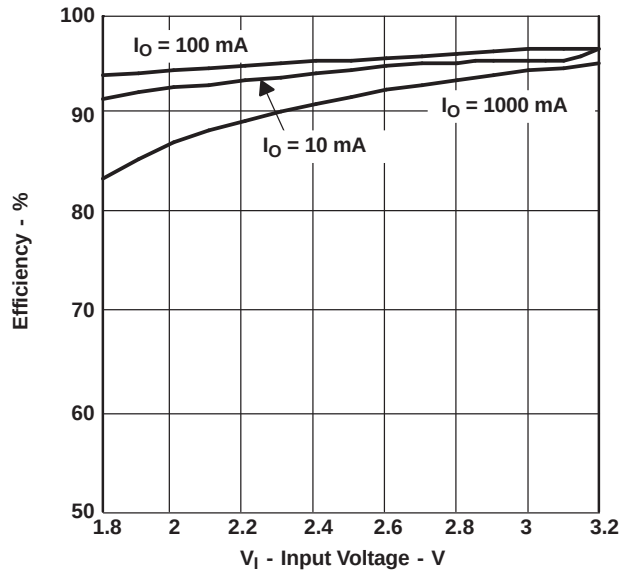


Figure 6.

TPS61032
EFFICIENCY
vs
INPUT VOLTAGE

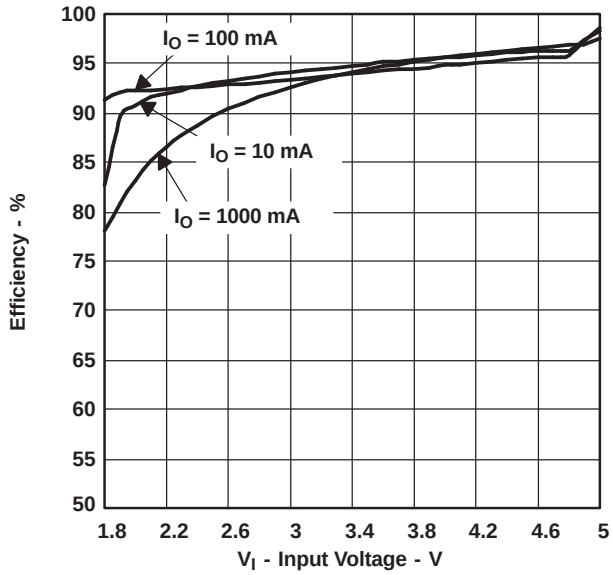


Figure 7.

TPS61031
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

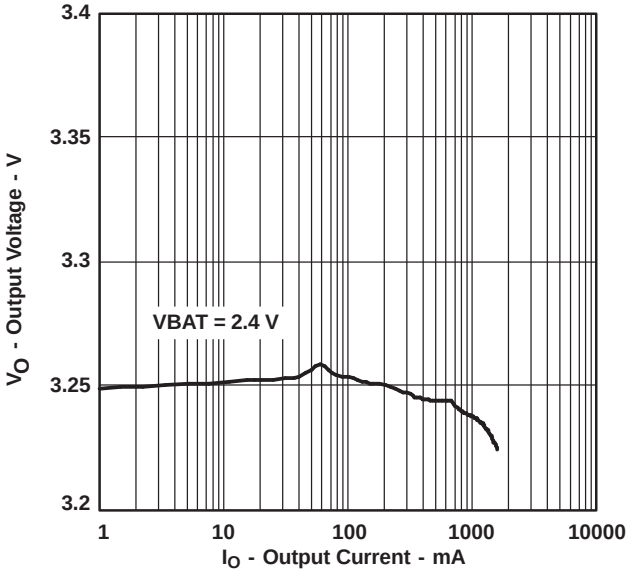


Figure 8.

TPS61032
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

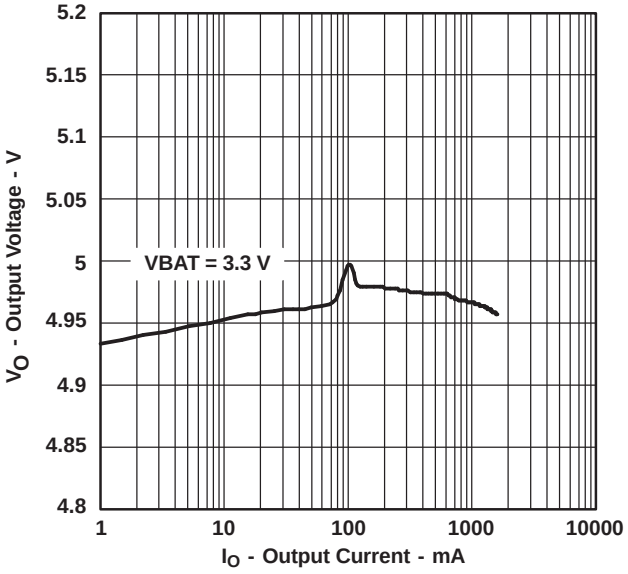


Figure 9.

TPS61032
NO-LOAD SUPPLY CURRENT INTO VBAT
vs
INPUT VOLTAGE

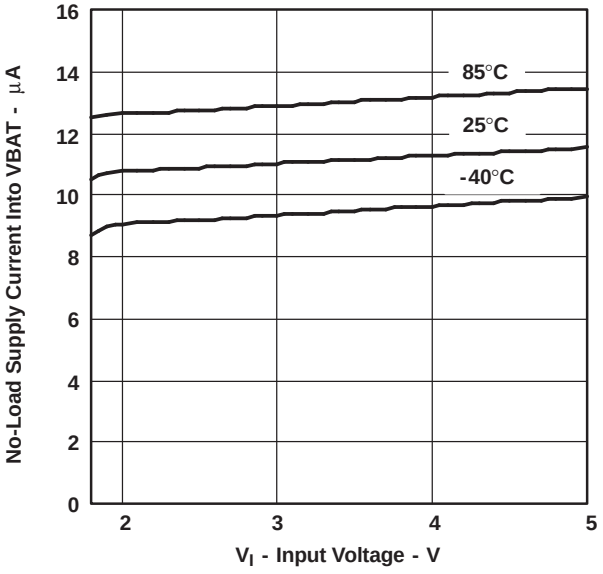


Figure 10.

TPS61032
NO-LOAD SUPPLY CURRENT INTO VOUT
vs
INPUT VOLTAGE

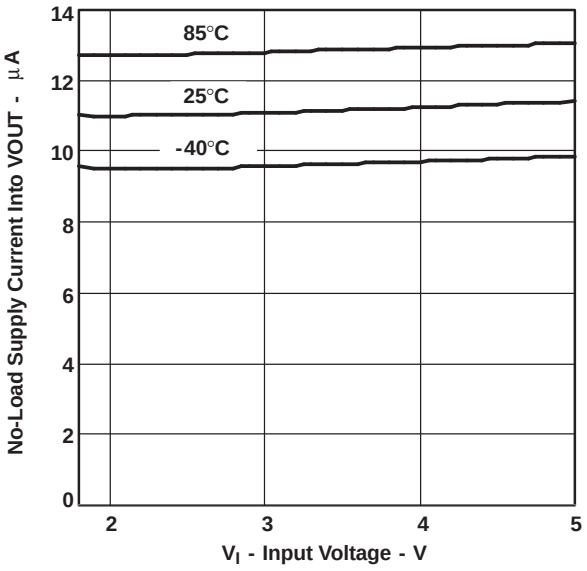


Figure 11.

MINIMUM LOAD RESISTANCE AT START-UP
vs
INPUT VOLTAGE

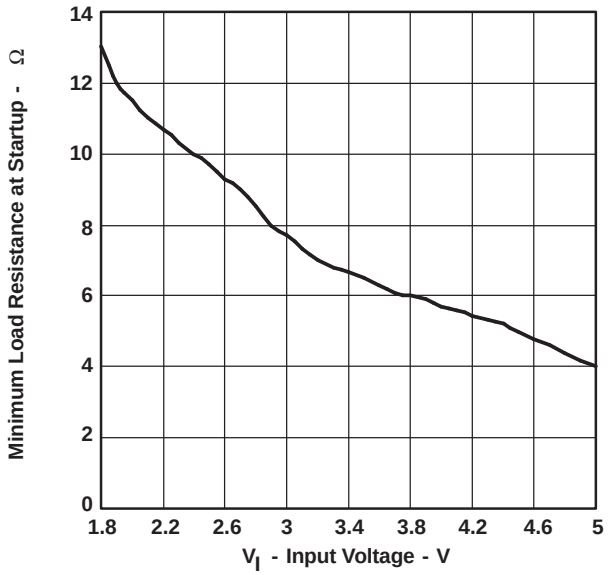


Figure 12.

TPS61032
OUTPUT VOLTAGE IN CONTINUOUS MODE

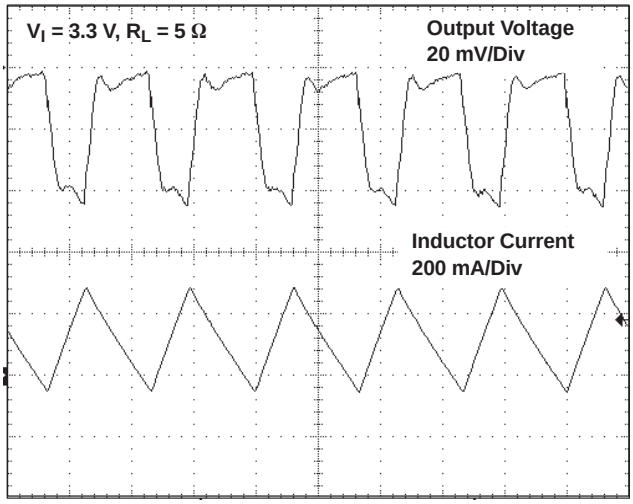


Figure 13.

TPS61032
OUTPUT VOLTAGE IN POWER SAVE MODE

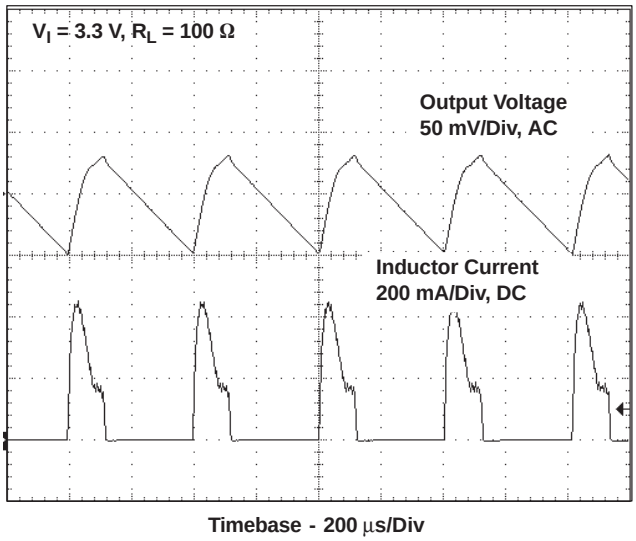
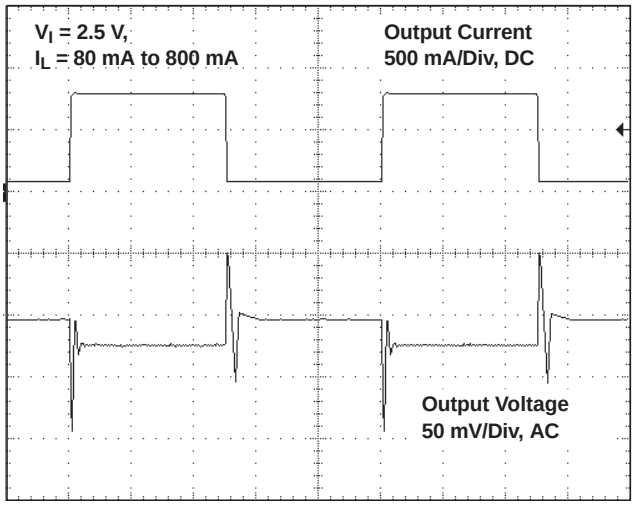


Figure 14.

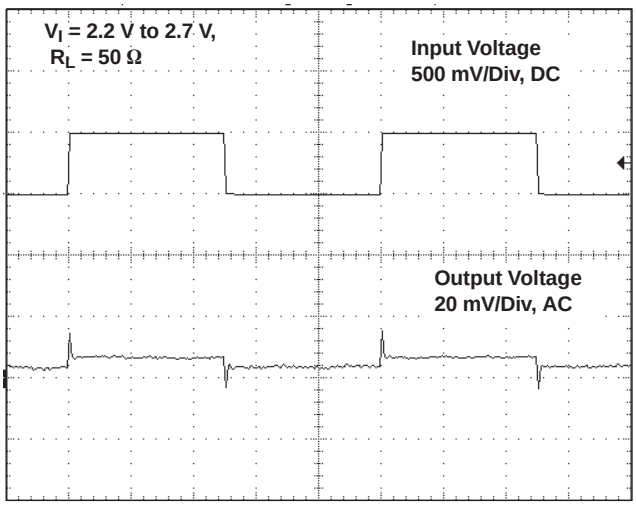
TPS61032
LOAD TRANSIENT RESPONSE



Timebase - 2 ms/Div

Figure 15.

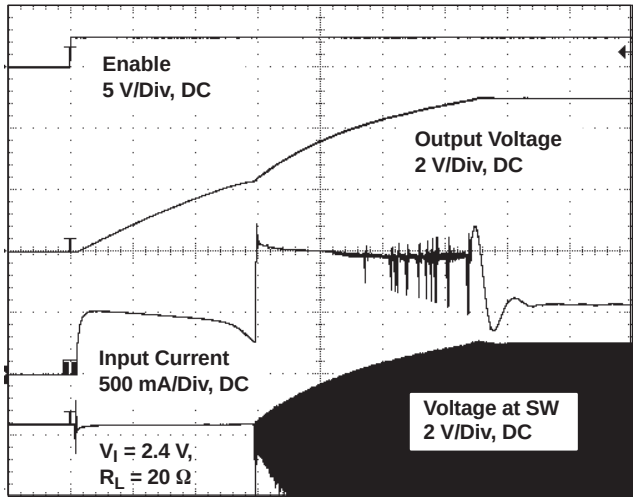
TPS61032
LINE TRANSIENT RESPONSE



Timebase - 2 ms/Div

Figure 16.

TPS61032
DC/DC CONVERTER START-UP AFTER ENABLE



Timebase - 400 μs/Div

Figure 17.

Detailed Description

Controller Circuit

The controller circuit of the device is based on a fixed frequency multiple feedforward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through the control loop and the error amplifier. The control loop, determined by the error amplifier, only has to handle small signal errors. The input for it is the feedback voltage on the FB pin or, at fixed output voltage versions, the voltage on the internal resistor divider. It is compared with the internal reference voltage to generate an accurate and stable output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to 4000 mA. An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

Synchronous Rectifier

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low RDS(ON) PMOS switch, the power conversion efficiency reaches 96%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the GND pin. A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device however uses a special circuit which takes the cathode of the backgate diode of the high-side PMOS and disconnects it from the source when the regulator is not enabled (EN = low).

The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components have to be added to the design to make sure that the battery is disconnected from the output of the converter.

Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the load is isolated from the input (as described in the Synchronous Rectifier Section). This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery.

Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VBAT is lower than approximately 1.6 V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VBAT drops below approximately 1.6 V. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

Softstart

When the device enables the internal start-up cycle starts with the first step, the precharge phase. During precharge, the rectifying switch is turned on until the output capacitor is charged to a value close to the input voltage. The rectifying switch current is limited in that phase. This also limits the output current under short-circuit conditions at the output. After charging the output capacitor to the input voltage the device starts switching. Until the output voltage is reached, the boost switch current limit is set to 40% of its nominal value to avoid high peak currents at the battery during startup. When the output voltage is reached, the regulator takes control and the switch current limit is set back to 100%.

Power Save Mode and Synchronization

The SYNC pin can be used to select different operation modes. To enable power save, SYNC must be set low. Power save mode is used to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and goes again into power save mode once the output voltage exceeds the set threshold voltage. This power save mode can be disabled by setting the SYNC to VBAT.

Applying an external clock with a duty cycle between 30% and 70% at the SYNC pin forces the converter to operate at the applied clock frequency. The external frequency has to be in the range of about ±20% of the nominal internal frequency. Detailed values are shown in the electrical characteristic section of the data sheet.

Low Battery Detector Circuit—LBI/LBO

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO pin is high-impedance. The switching threshold is 500 mV at LBI. During normal operation, LBO stays at high impedance when the voltage, applied at LBI, is above the threshold. It is active low when the voltage at LBI goes below 500 mV.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI threshold. If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to VBAT) and the LBO pin can be left unconnected. Do not let the LBI pin float.

Low-EMI Switch

The device integrates a circuit that removes the ringing that typically appears on the SW node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the SW pin is induced. The integrated antiringing switch clamps this voltage to VBAT and therefore dampens ringing.

APPLICATION INFORMATION

Design Procedure

The TPS6103x dc/dc converters are intended for systems powered by a dual or triple cell NiCd or NiMH battery with a typical terminal voltage between 1.8 V and 5.5 V. They can also be used in systems powered by one-cell Li-Ion with a typical stack voltage between 2.5 V and 4.2 V. Additionally, two or three primary and secondary alkaline battery cells can be the power source in systems where the TPS6103x is used.

Programming the Output Voltage

The output voltage of the TPS61030 dc/dc converter section can be adjusted with an external resistor divider. The typical value of the voltage on the FB pin is 500 mV. The maximum allowed value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA, and the voltage across R6 is typically 500 mV. Based on those two values, the recommended value for R4 should be lower than 500 kΩ, in order to set the divider current at 1 µA or higher. Because of internal compensation circuitry the value for this resistor should be in the range of 200 kΩ. From that, the value of resistor R3, depending on the needed output voltage (V_O), can be calculated using equation 1:

$$R3 = R4 \times \left(\frac{V_O}{V_{FB}} - 1 \right) = 180\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1 \right) \quad (1)$$

If as an example, an output voltage of 3.3 V is needed, a 1-MΩ resistor should be chosen for R3. If for any reason the value for R4 is chosen significantly lower than 200 kΩ additional capacitance in parallel to R3 is recommended. The required capacitance value can be easily calculated using Equation 2:

$$C_{parR3} = 10\ pF \times \left(\frac{200\ k\Omega}{R4} - 1 \right) \quad (2)$$

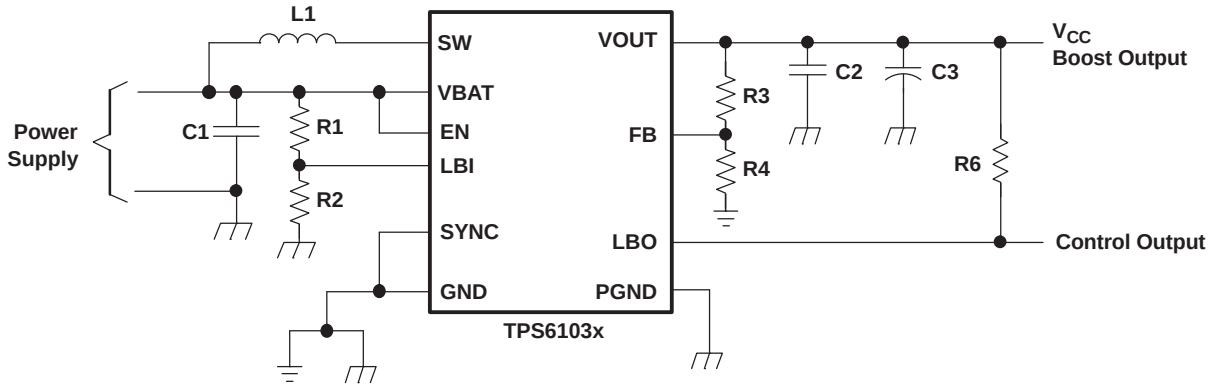


Figure 18. Typical Application Circuit for Adjustable Output Voltage Option

Programming the LBI/LBO Threshold Voltage

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The typical current into the LBI pin is 0.01 µA, and the voltage across R2 is equal to the LBI voltage threshold that is generated on-chip, which has a value of 500 mV. The recommended value for R2 is therefore in the range of 500 kΩ. From that, the value of resistor R1, depending on the desired minimum battery voltage V_{BAT}, can be calculated using Equation 3.

$$R1 = R2 \times \left(\frac{V_{BAT}}{V_{LBI-threshold}} - 1 \right) = 390\ k\Omega \times \left(\frac{V_{BAT}}{500\ mV} - 1 \right) \quad (3)$$

The output of the low battery supervisor is a simple open-drain output that goes active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1 MΩ. The maximum voltage which is used to pull up the LBO outputs should not exceed the output voltage of the dc/dc converter. If not used, the LBO pin can be left floating or tied to GND.

Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the TPS6103x's switch is 4500 mA at an output voltage of 5 V. The highest peak current through the inductor and the switch depends on the output load, the input (V_{BAT}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using Equation 4:

$$I_L = I_{OUT} \times \frac{V_{OUT}}{V_{BAT} \times 0.8} \quad (4)$$

For example, for an output current of 1000 mA at 5 V, at least 3500 mA of average current flows through the inductor at a minimum input voltage of 1.8 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system costs. With those parameters, it is possible to calculate the value for the inductor by using Equation 5:

$$L = \frac{V_{BAT} \times \left(V_{OUT} - V_{BAT}\right)}{\Delta I_L \times f \times V_{OUT}} \quad (5)$$

Parameter *f* is the switching frequency and ΔI_L is the ripple current in the inductor, i.e., 10% × I_L. In this example, the desired inductor has the value of 5.5 µH. In typical applications a 6.8 µH inductance is recommended. The minimum possible inductance value is 2.2 µH. With the calculated inductance and current values, it is possible to choose a suitable inductor. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in equation 4. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The following inductor series from different suppliers have been used with the TPS6103x converters:

List of Inductors

VENDOR	INDUCTOR SERIES
Sumida	CDRH124
	CDRH103R
	CDRH104R
Wurth Electronik	7447779___
	744771___
EPCOS	B82464G

Capacitor Selection

Input Capacitor

At least a 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel, placed close to the IC, is recommended.

Output Capacitor

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 6:

$$C_{min} = \frac{I_{OUT} \times \left(V_{OUT} - V_{BAT}\right)}{f \times \Delta V \times V_{OUT}} \quad (6)$$

Parameter *f* is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 10 mV, a minimum capacitance of 100 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 7:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (7)$$

An additional ripple of 80 mV is the result of using a tantalum capacitor with a low ESR of 80 mΩ. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 90 mV. Additional ripple is caused by load transients. This means that the output capacitance needs to be larger than calculated above to meet the total ripple requirements.

The output capacitor must completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change. With the calculated minimum value of 100 µF and load transient considerations, a recommended output capacitance value is in around 220 µF. For economical reasons this usually is a tantalum capacitor. Because of this the control loop has been optimized for using output capacitors with an ESR of above 30 mΩ. The minimum value for the output capacitor is 22 µF.

Small Signal Stability

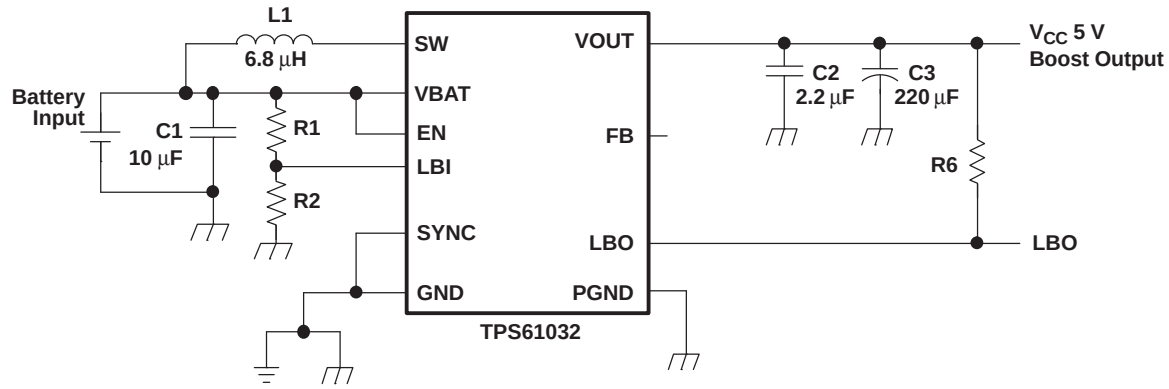
When using output capacitors with lower ESR, like ceramics, it is recommended to use the adjustable voltage version. The missing ESR can be easily compensated there in the feedback divider. Typically a capacitor in the range of 10 pF in parallel to R3 helps to obtain small signal stability with lowest ESR output capacitors. For more detailed analysis the small signal transfer function of the error amplifier and regulator, which is given in Equation 8, can be used.

$$A_{REG} = \frac{d}{V_{FB}} = \frac{5 \times (R3 + R4)}{R4 \times (1 + i \times \omega \times 2.3\,\mu s)} \quad (8)$$

Layout Considerations

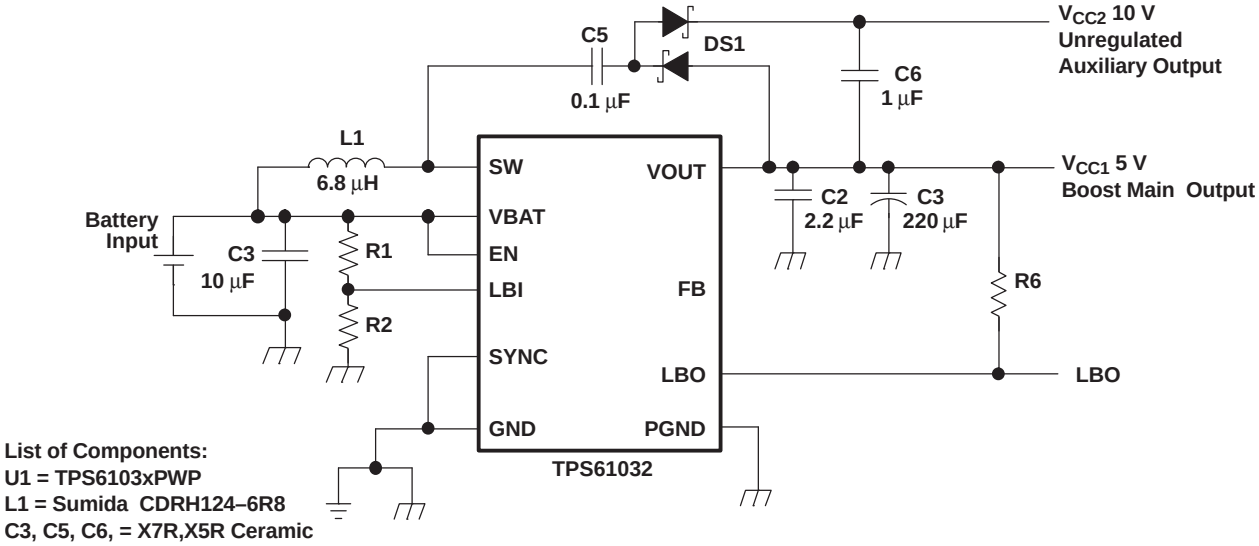
As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.



List of Components:
U1 = TPS6103xPWP
L1 = Sumida CDRH124–6R8
C1, C2 = X7R,X5R Ceramic
C3 = Low ESR Tantalum

Figure 19. Power Supply Solution for Maximum Output Power



List of Components:
U1 = TPS6103xPWP
L1 = Sumida CDRH124–6R8
C3, C5, C6, = X7R,X5R Ceramic
C3 = Low ESR Tantalum
DS1 = BAT54S

Figure 20. Power Supply Solution With Auxiliary Positive Output Voltage

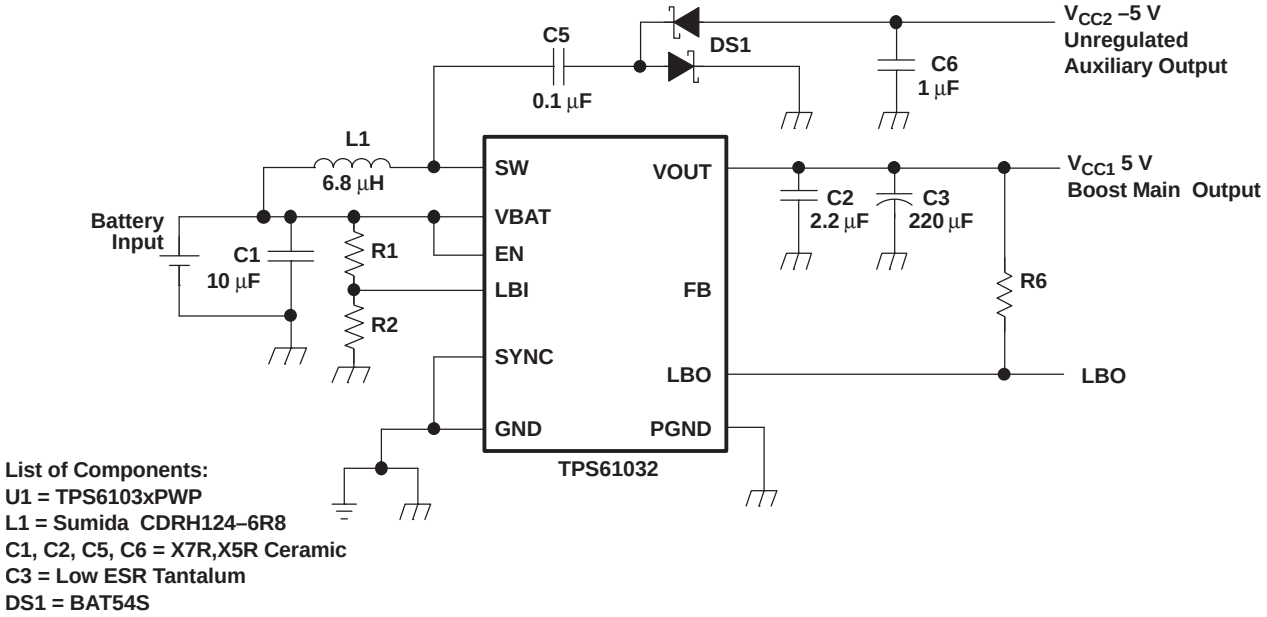


Figure 21. Power Supply Solution With Auxiliary Negative Output Voltage

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum junction temperature (T_J) of the TPS6103x devices is 125°C. The thermal resistance of the 16-pin TSSOP PowerPAD package (PWP) is $R_{\Theta JA}$ = 36.5 °C/W (QFN package, RSA, 38.1 °C/W), if the PowerPAD is soldered. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation for the PWP package is about 1096 mW, for the RSA package it is about 1050 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{125°C - 85°C}{36.5°C/W} \quad (9)$$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61030PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61030	Samples
TPS61030PWPG4	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61030	Samples
TPS61030PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61030	Samples
TPS61030PWPRG4	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61030	Samples
TPS61030RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS6 1030	Samples
TPS61030RSARG4	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS6 1030	Samples
TPS61031PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61031	Samples
TPS61031PWPG4	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61031	Samples
TPS61031PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61031	Samples
TPS61031PWPRG4	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61031	Samples
TPS61031RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS6 1031	Samples
TPS61031RSARG4	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS6 1031	Samples
TPS61032PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61032	Samples
TPS61032PWPG4	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61032	Samples
TPS61032PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61032	Samples
TPS61032PWPRG4	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61032	Samples
TPS61032RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS6 1032	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61032RSARG4	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS6 1032	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

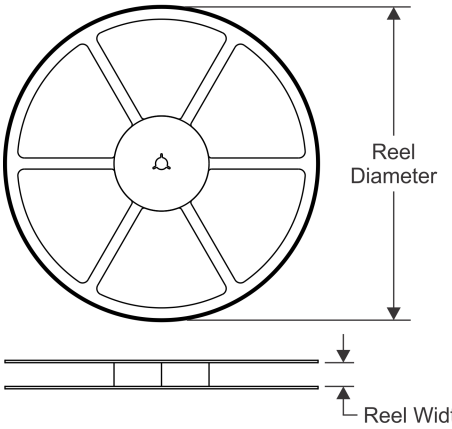
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

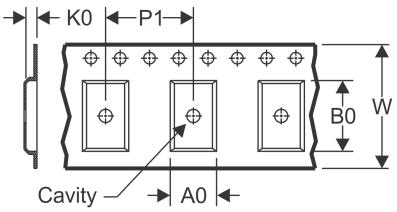
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

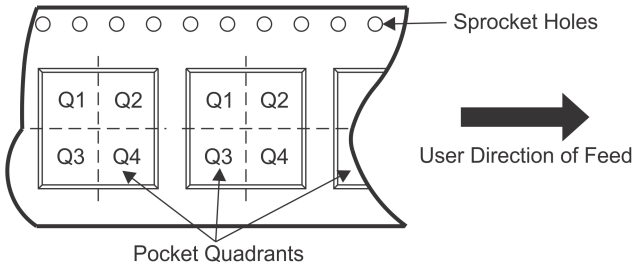


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

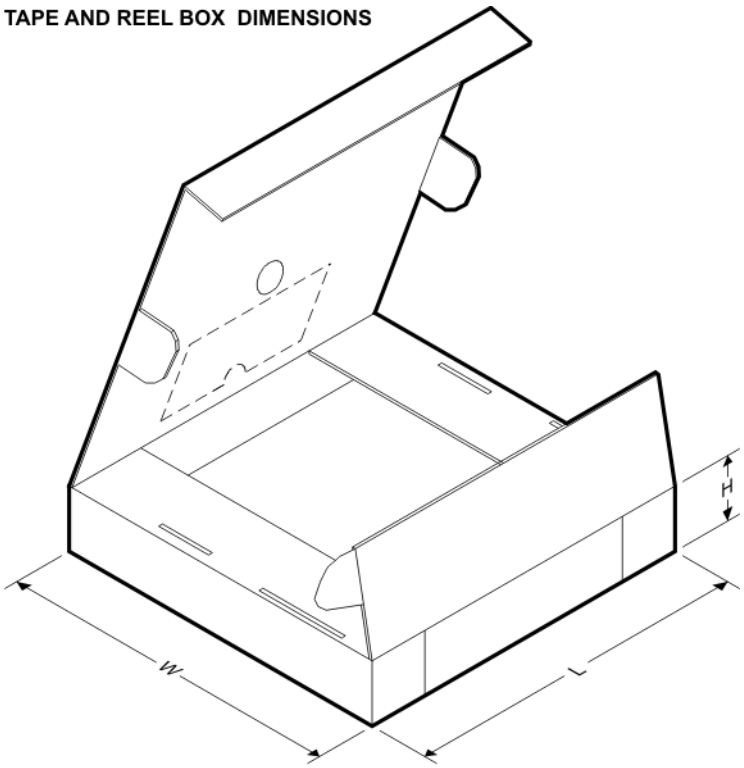
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61030PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS61030RSAR	QFN	RSA	16	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPS61031PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS61032PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS61032RSAR	QFN	RSA	16	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

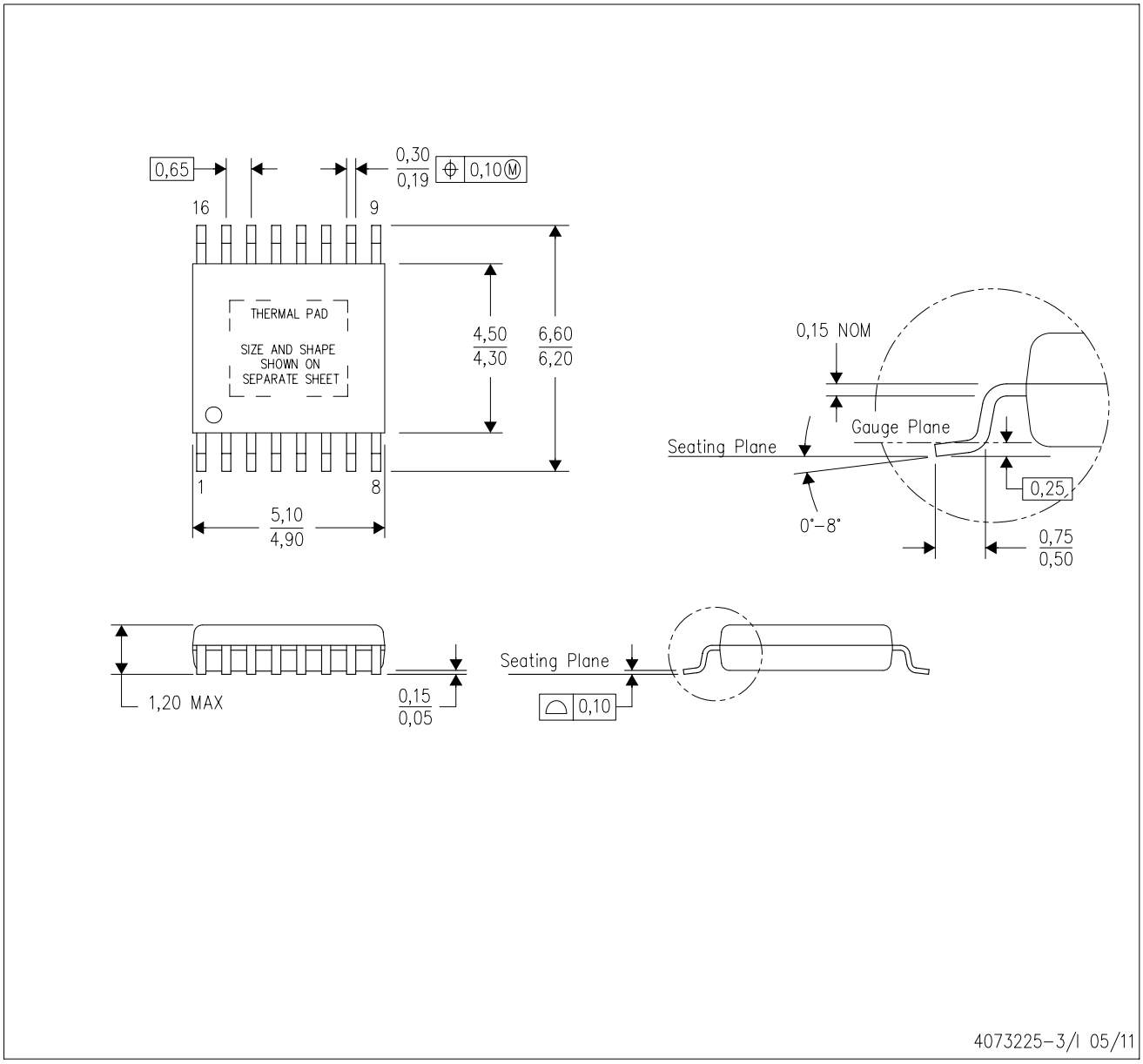
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61030PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0
TPS61030RSAR	QFN	RSA	16	3000	338.1	338.1	20.6
TPS61031PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0
TPS61032PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0
TPS61032RSAR	QFN	RSA	16	3000	338.1	338.1	20.6

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

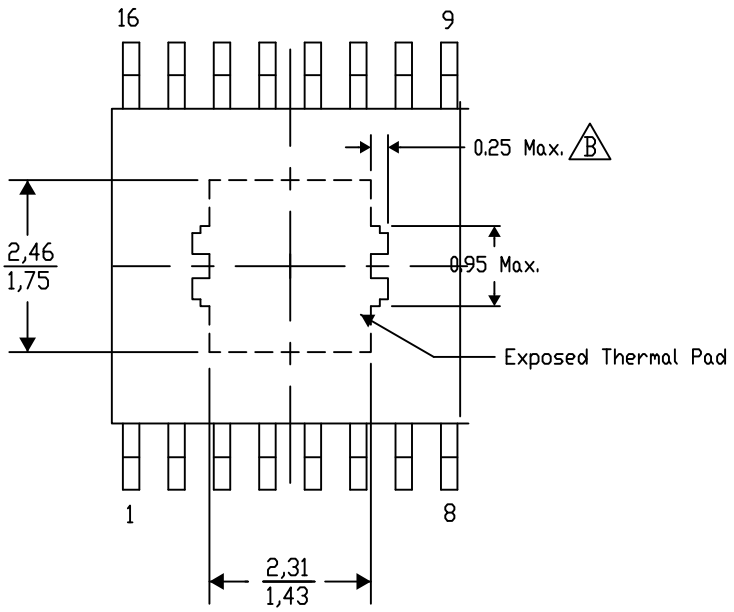
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

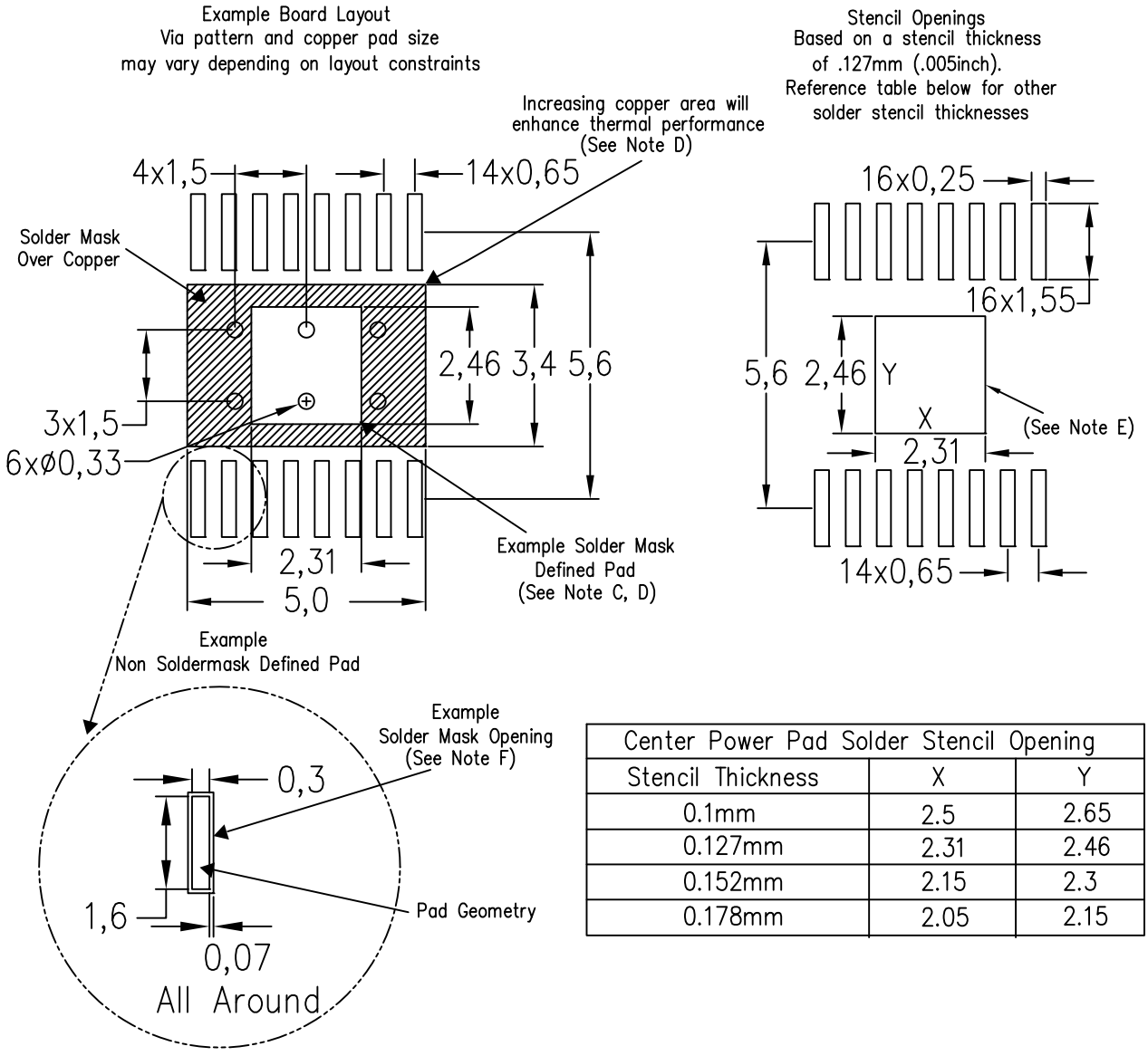
4206332–6/AG 08/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–3/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

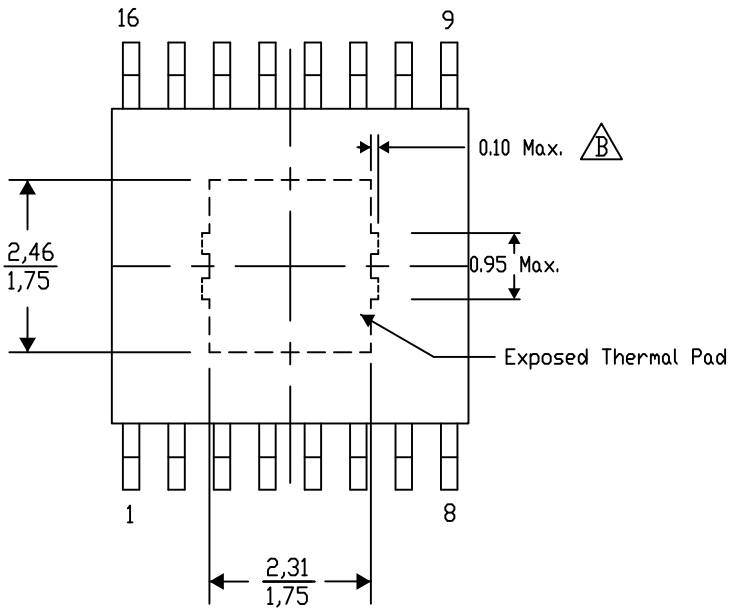
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

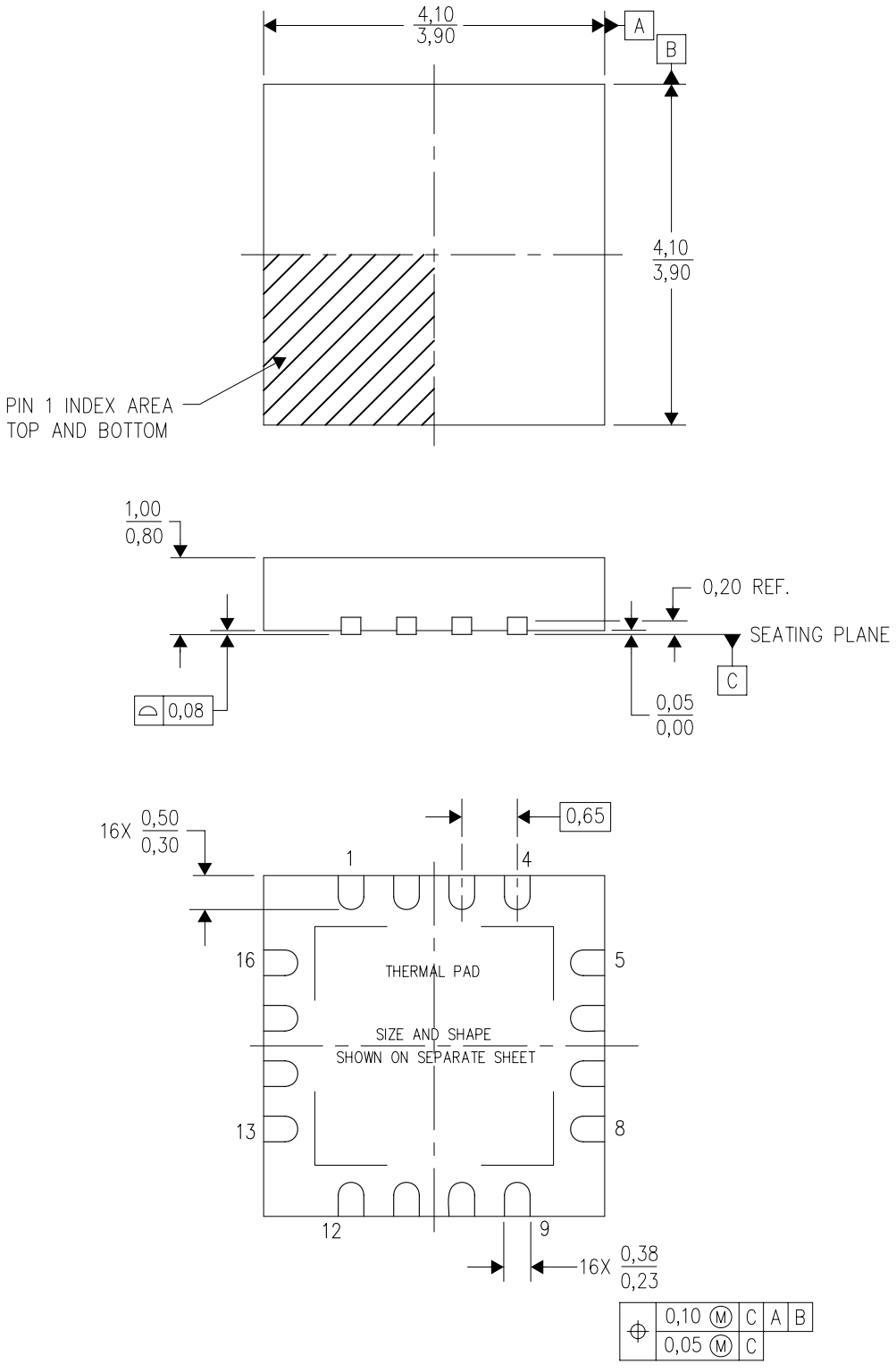
4206332–45/AG 08/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

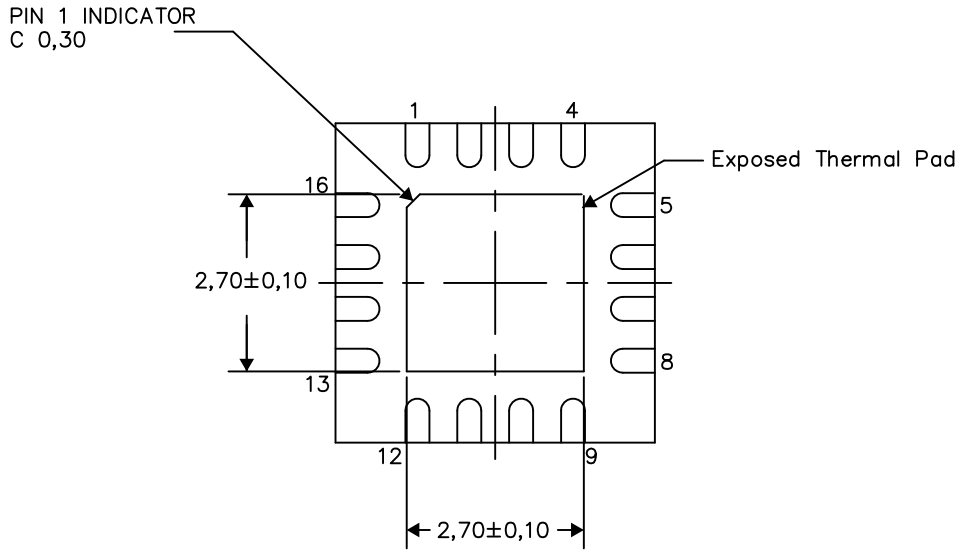
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206364/N 07/13

NOTES:
A. All linear dimensions are in millimeters

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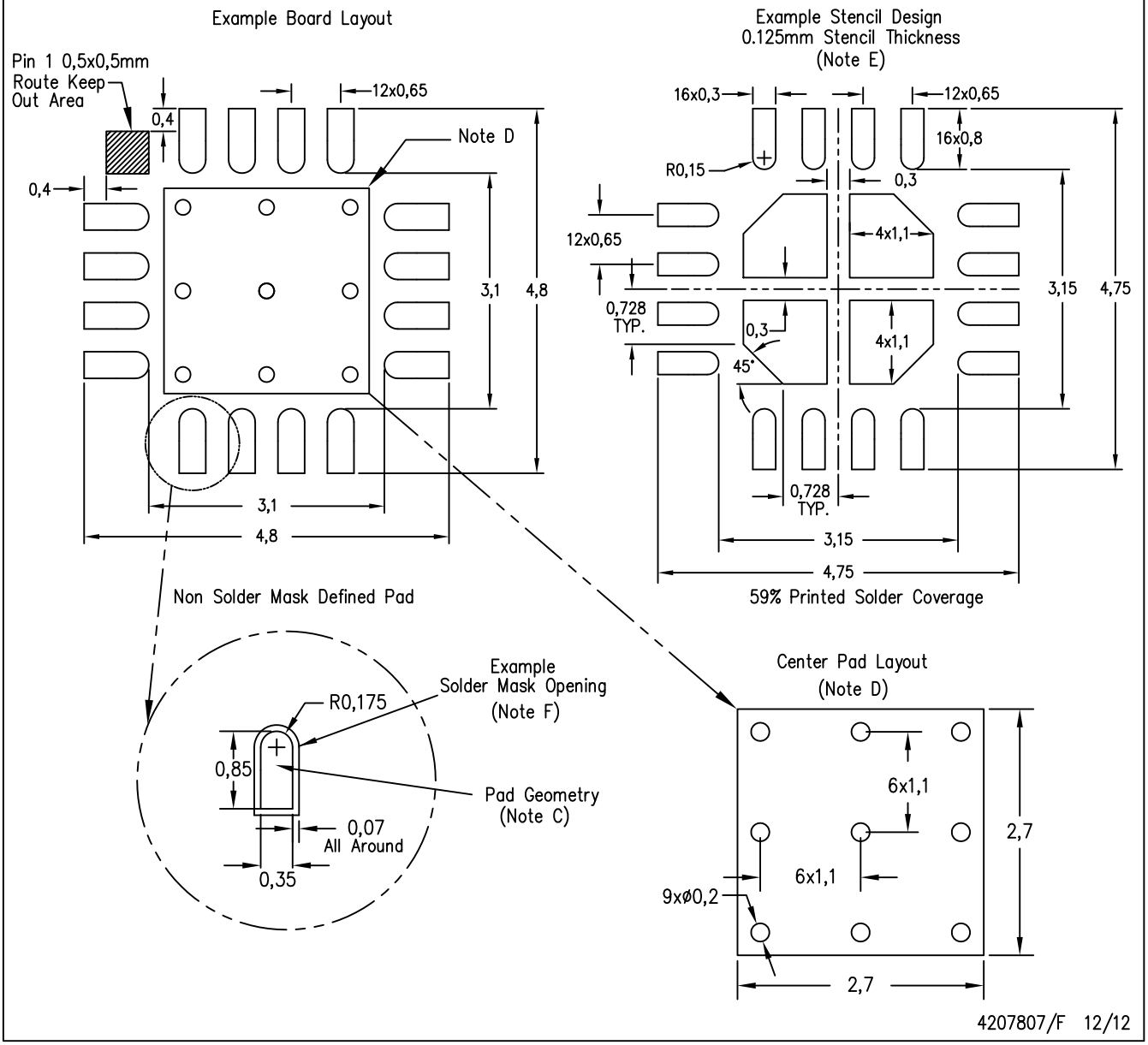

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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