1-A Step-Down Converter in 2-mm × 2-mm QFN Package

Check for Samples: TPS62590-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Output Current up to 1000 mA**
- **Input Voltage Range from 2.5 V to 6 V**
- **Output Voltage Accuracy in PWM mode ±2.5%**
- **Typ. 15-µA Quiescent Current**
- **100% Duty Cycle for Lowest Dropout**
- **Available in a 2-mm × 2-mm × 0,8-mm QFN Package**
- **For Improved Features Set, See TPS62290**

DESCRIPTION

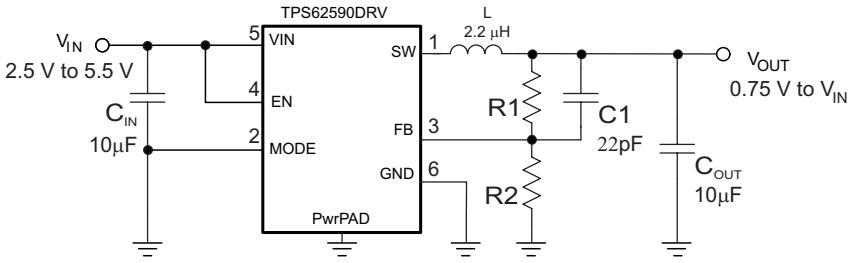
The TPS62590-Q1 device is a high-efficiency synchronous step-down converter, optimized for battery-powered portable applications. It provides up to 1000-mA output current from batteries, such as single Li-Ion or other common-chemistry AA and AAA cells.

With an input voltage range of 2.5 V to 6 V, the device is targeted to power a large variety of portable handheld equipment or POL applications.

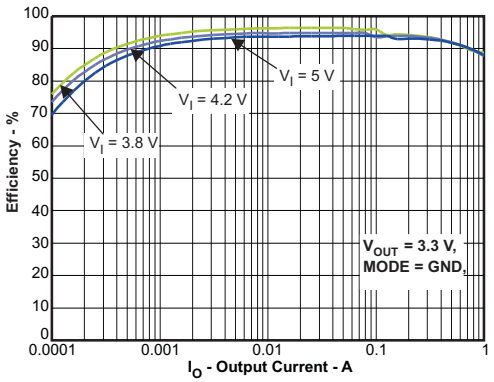
The TPS62590-Q1 family operates at a 2.25-MHz fixed switching frequency and enters a power-save mode at light load currents to maintain a high efficiency over the entire load current range.

The power-save mode is optimized for low output-voltage ripple. For low-noise applications, the device can be forced into fixed-frequency PWM mode by pulling the MODE pin high. In the shutdown mode, the current consumption is reduced to less than 1 µA. The TPS62590-Q1 allows the use of small inductors and capacitors to achieve a small solution size.

The TPS62590-Q1 is available in a 2-mm × 2-mm 6-pin QFN package.



Typical Application



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)

T_A	PACKAGE (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	QFN 2-mm × 2-mm	Reel of 3000	TPS62590TDRVRQ1	QWT

(1) The DRV (2-mm × 2-mm 6-terminal QFN) packages are available in tape on reel.
(2) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_I	Input voltage range(2)	–0.3 to 7	V
	Voltage range at EN, MODE	–0.3 to V_{IN} +0.3, ≤ 7	V
	Voltage on SW	–0.3 to 7	V
	Peak output current	Internally limited	A
T_J	Maximum operating junction temperature	–40 to 125	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS62590-Q1 DRV 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	101.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	80.9	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	71.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	71.6	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	43.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	2.5		6	V
	Output voltage range for adjustable voltage	0.75		V_{IN}	V
T_A	Operating ambient temperature	–40		105	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

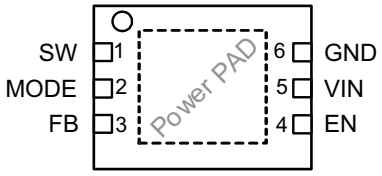
Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 10 µF 0603, C_{OUT} = 10 µF 0603, L = 2.2 µH; see parameter measurement information.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_I	Input voltage range		2.5		6	V
I_O	Output current(1)	V_{IN} 2.7 V to 6 V			1000	mA
		V_{IN} 2.5 V to 2.7 V			600	
I_Q	Operating quiescent current	I_O = 0 mA, PFM mode enabled (MODE = GND) device not switching, See (2)		15		µA
		I_O = 0 mA, switching with no load (MODE = V_{IN}) PWM mode, V_O = 1.8 V, V_{IN} = 3 V		3.8		mA
I_{SD}	Shutdown current	EN = GND		0.5		µA
UVLO	Undervoltage lockout threshold	Falling		1.85		V
		Rising		1.95		
ENABLE, MODE						
V_{IH}	High-level input voltage, EN, MODE	2.5 V ≤ V_{IN} ≤ 6 V	1		V_{IN}	V
V_{IL}	Low-level input voltage, EN, MODE	2.5 V ≤ V_{IN} ≤ 6 V	0		0.4	V
I_I	Input bias current, EN, MODE	EN, MODE = GND or V_{IN}		0.01	1	µA
POWER SWITCH						
$r_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V, T_A = 25°C		250		mΩ
	Low-side MOSFET on-resistance			190		
I_{LIMF}	Forward current limit MOSFET high-side and low-side	V_{IN} = V_{GS} = 3.6 V, T_A = 25°C	1.19	1.4	1.78	A
T_{SD}	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		
OSCILLATOR						
f_{SW}	Oscillator frequency	2.5 V ≤ V_{IN} ≤ 6 V		2.25		MHz
OUTPUT						
V_O	Adjustable output voltage range		0.75		V_I	V
V_{ref}	Reference voltage			600		mV
$V_{FB(PWM)}$	Feedback voltage	MODE = V_{IN}, PWM mode, 2.5 V ≤ V_{IN} ≤ 6 V, See (3)	–2.5%	0%	2.5%	
$V_{FB(PFM)}$	Feedback voltage, PFM mode	MODE = GND, device in PFM mode, 1% voltage positioning active, See (2)		1%		
	Load regulation			–1		%/A
$t_{Start\ Up}$	Start-up time	Time from active EN to reach 95% of V_O		500		µs
t_{Ramp}	V_O ramp-up time	Time to ramp from 5% to 95% of V_O		250		µs
I_{lkg}	Leakage current into SW pin	V_I = 3.6 V, V_I = V_O = V_{SW}, EN = GND, See (4)		0.1	1	µA

(1) Not production tested.
(2) In PFM mode, the internal reference voltage is set to typ. 1.01 × V_{ref} . See the parameter measurement information.
(3) For V_{IN} = V_O + 1 V
(4) In fixed output-voltage versions, the internal resistor divider network is disconnected from the FB pin.

PIN ASSIGNMENTS

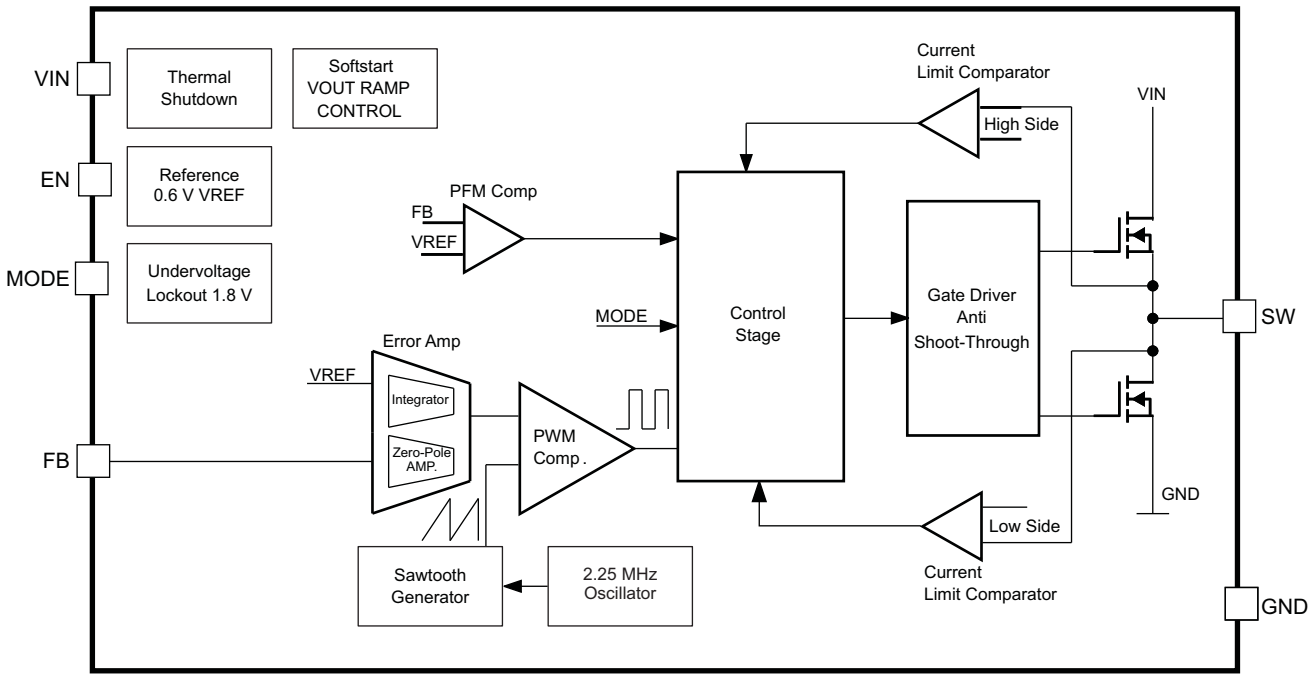
DRV PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VIN	5	PWR	VIN power supply pin
GND	6	PWR	GND supply pin
EN	4	I	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
SW	1	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
FB	3	I	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output-voltage option, connect this pin directly to the output capacitor.
MODE	2	I	MODE pin = high forces the device to operate in fixed-frequency PWM mode. Mode pin = low enables the power-save mode with automatic transition from PFM mode to fixed-frequency PWM mode.
Thermal pad			Must be soldered to achieve appropriate power dissipation. Should be connected to GND.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION

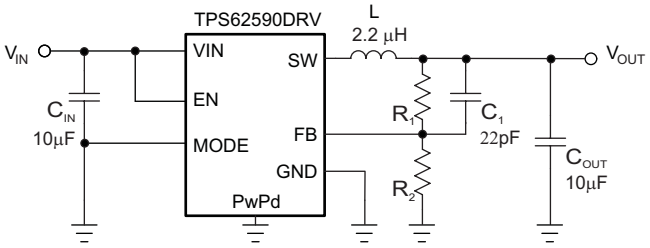


Table 2. List of Components:

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER	VALUE
C_{IN}	GRM188R60J106M	Murata	10-µF, 6.3-V. X5R ceramic
C_{OUT}	GRM188R60J106M	Murata	10-µF, 6.3-V. X5R ceramic
C_1		Murata	22-pF, ceramic
L_1	LPS3015	Coilcraft	2.2 µH, 110mΩ
R_1, R_2	Values depending on the programmed output voltage		

TYPICAL CHARACTERISTICS

Table 3. Table Of Graphs

		FIGURE
Efficiency	vs Output Current V_{OUT} = 1.8 V (Power-Save Mode)	Figure 1
	vs Output Current V_{OUT} = 1.8 V (Forced PWM Mode)	Figure 2
	vs Output Current V_{OUT} = 3.3 V (Power-Save Mode)	Figure 3
	vs Output Current V_{OUT} = 3.3 V (Forced PWM Mode)	Figure 4
Output Voltage	vs Output Current V_{OUT} = 1.8 V (Forced PWM Mode)	Figure 5
	vs Output Current V_{OUT} = 1.8 V (Power-Save Mode)	Figure 6
	vs Output Current V_{OUT} = 3.3 V (Forced PWM Mode)	Figure 7
	vs Output Current V_{OUT} = 3.3 V (Power-Save Mode)	Figure 8
Transient Behavior	PFM Load Transient	Figure 9
	PFM Line Transient	Figure 10
	PWM Load Transient	Figure 11
	PWM Line Transient	Figure 12
	Typical Performance – PFM Mode	Figure 13
	Typical Performance – PWM Mode	Figure 14
Shutdown Current	into VIN vs. Input Voltage	Figure 15
Quiescent Current	vs Input Voltage	Figure 16
Static Drain-Source On-State Resistance	vs Input Voltage	Figure 17
		Figure 18

EFFICIENCY vs OUTPUT CURRENT

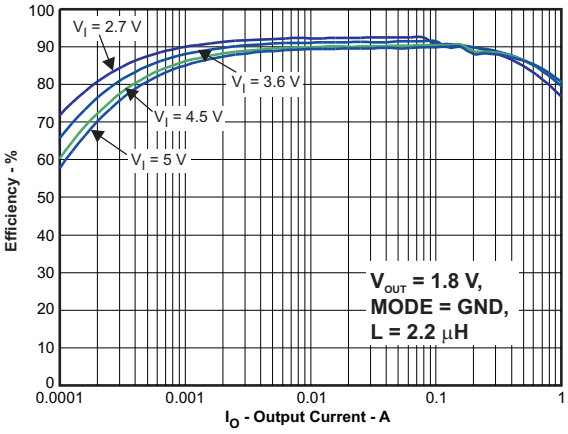


Figure 1.

EFFICIENCY vs OUTPUT CURRENT

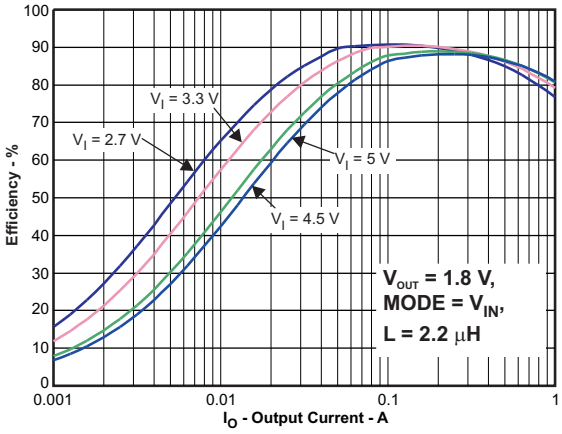


Figure 2.

EFFICIENCY vs OUTPUT CURRENT

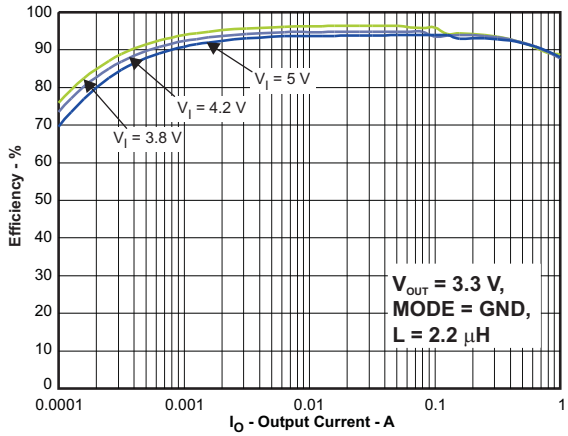


Figure 3.

EFFICIENCY vs OUTPUT CURRENT

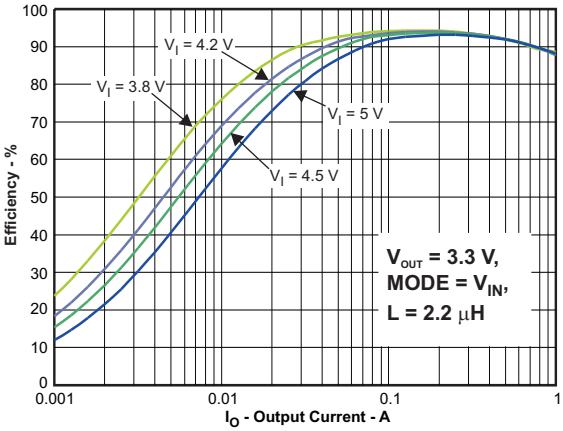


Figure 4.

OUTPUT VOLTAGE vs OUTPUT CURRENT

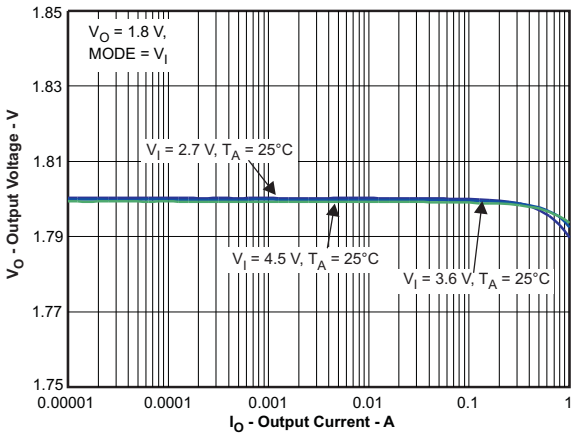


Figure 5.

OUTPUT VOLTAGE vs OUTPUT CURRENT

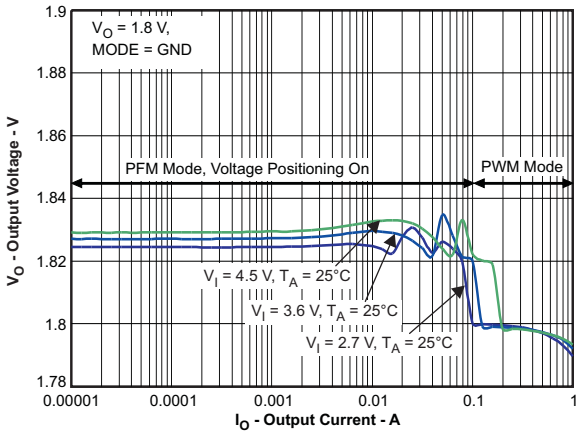


Figure 6.

OUTPUT VOLTAGE vs OUTPUT CURRENT

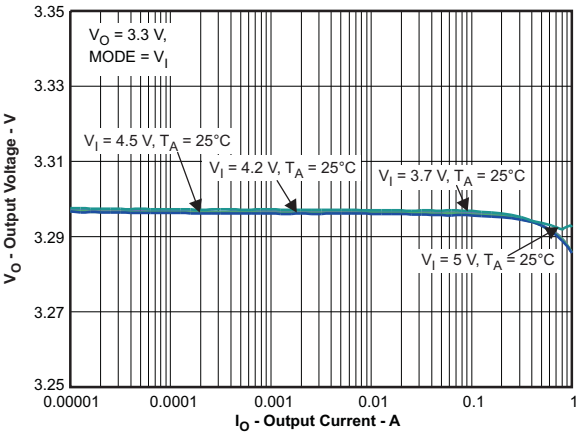


Figure 7.

OUTPUT VOLTAGE vs OUTPUT CURRENT

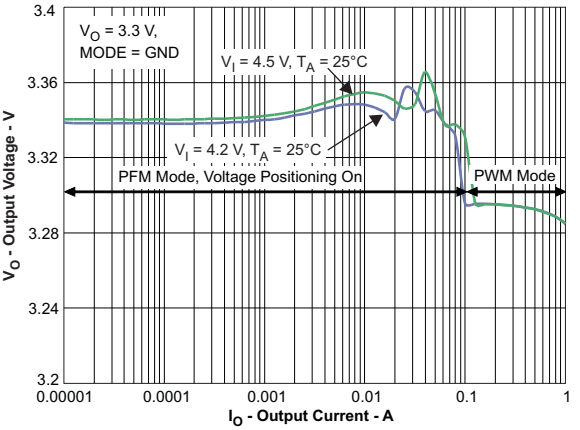
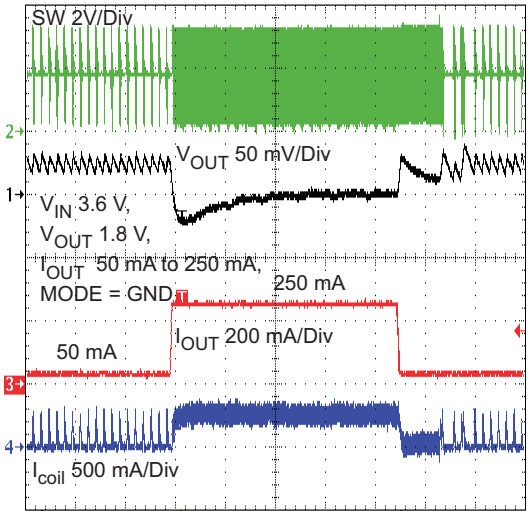


Figure 8.

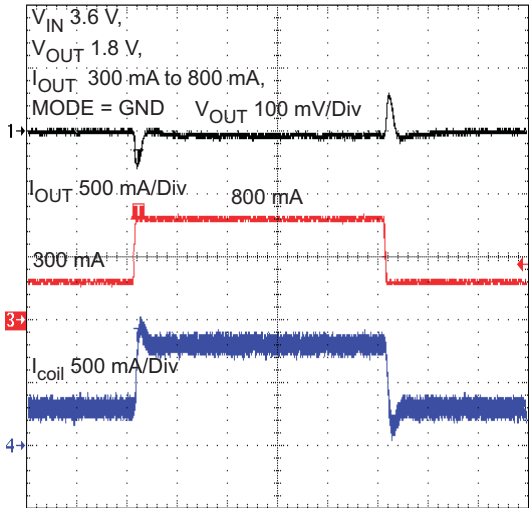
PFM LOAD TRANSIENT



Time Base - 20 µs/Div

Figure 9.

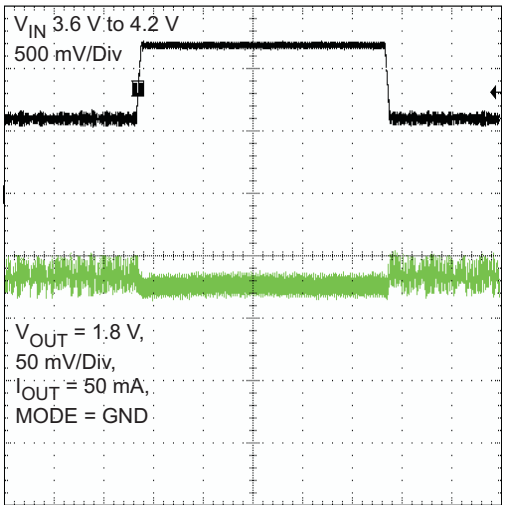
PFM LINE TRANSIENT



Time Base - 20 µs/Div

Figure 10.

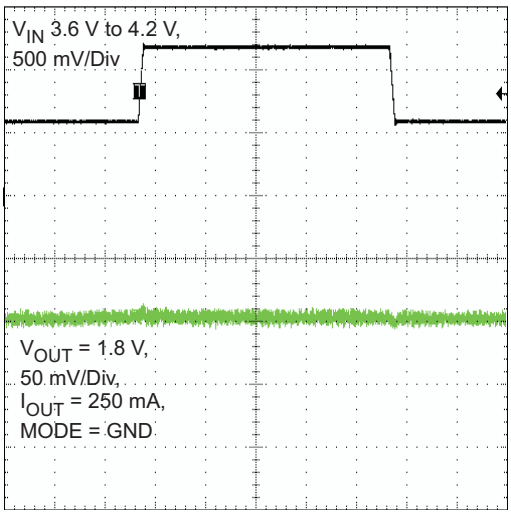
PWM LOAD TRANSIENT



Time Base - 100 µs/Div

Figure 11.

PWM LINE TRANSIENT



Time Base - 100 µs/Div

Figure 12.

TYPICAL PERFORMANCE – PFM MODE

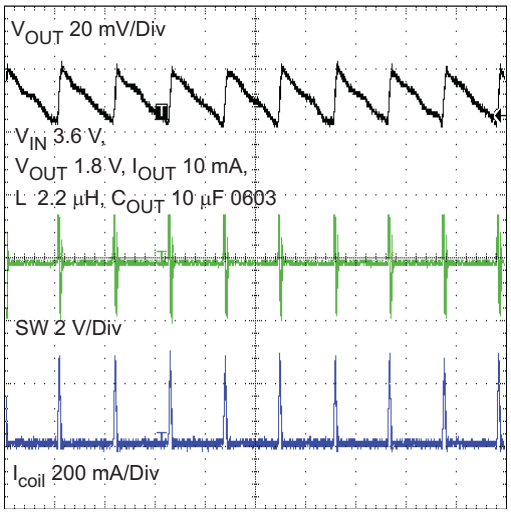


Figure 13.

TYPICAL PERFORMANCE – PWM MODE

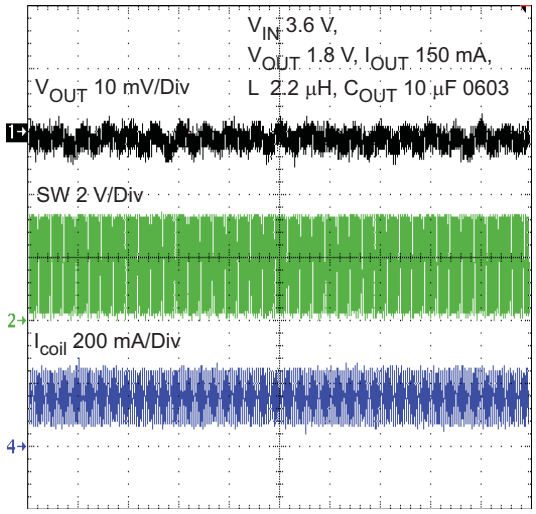


Figure 14.

SHUTDOWN CURRENT INTO VIN vs INPUT VOLTAGE

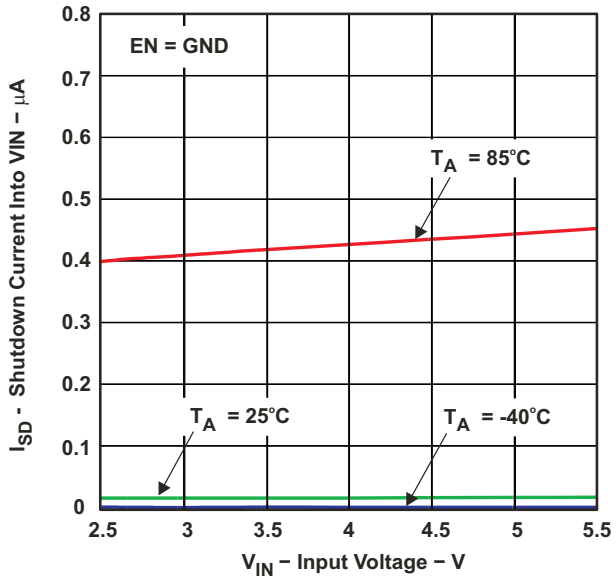


Figure 15.

QUIESCENT CURRENT vs INPUT VOLTAGE

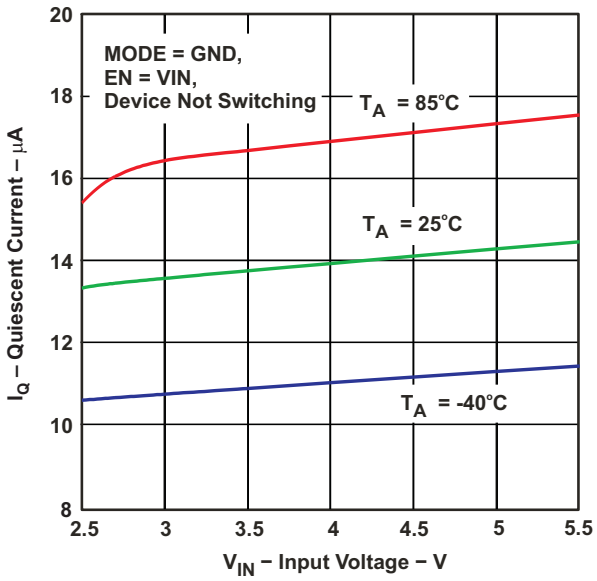


Figure 16.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

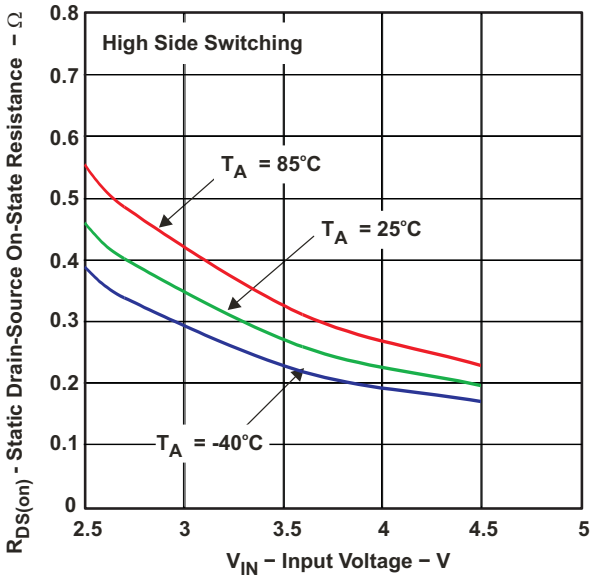


Figure 17.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

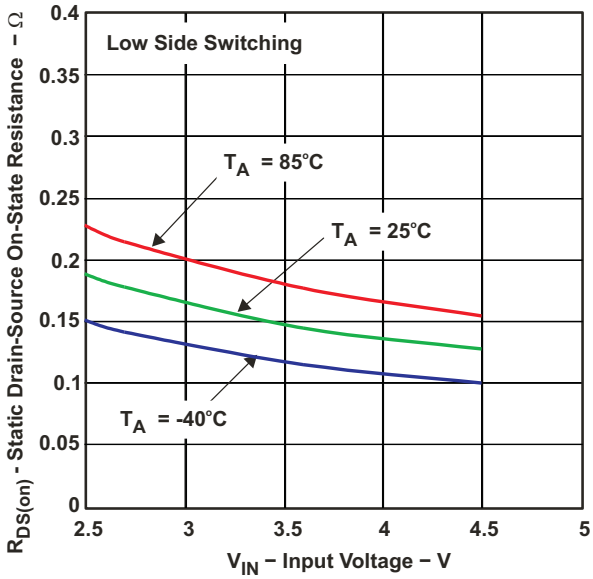


Figure 18.

DETAILED DESCRIPTION

OPERATION

The TPS62590-Q1 step-down converter operates with typically 2.25-MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter power-save mode and operates then in PFM mode.

During PWM mode, the converter uses a unique fast-response voltage-mode controller scheme with input-voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current flows now from the input capacitor via the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current-limit comparator also turns off the switch if the current limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current flows now from the inductor to the output capacitor and to the load. It returns to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the high-side MOSFET switch.

POWER-SAVE MODE

The power-save mode is enabled with the MODE pin set to low level. If the load current decreases, the converter enters power-save mode automatically. During power-save mode, the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage 1% above the nominal output voltage typically. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous-conduction mode.

During the power-save mode, the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of VOUT nominal + 1%, the device starts a PFM current pulse. For this, the high-side MOSFET switch turns on and the inductor current ramps up. After the on-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage rises. If the output voltage is equal to or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15-µA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses is generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a fast single-threshold comparator, the output voltage ripple during PFM mode can be kept small. The PFM pulse is time-controlled, which allows modifying the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values minimizes the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values.

The PFM mode is left and PWM mode entered in case the output current can no longer be supported in PFM mode. The power-save mode can be disabled by setting the MODE pin to high. The converter then operates in fixed-frequency PWM mode.

Dynamic Voltage Positioning

This feature reduces the voltage under- and overshoots at load steps from light to heavy load and vice versa. It is active in power-save mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

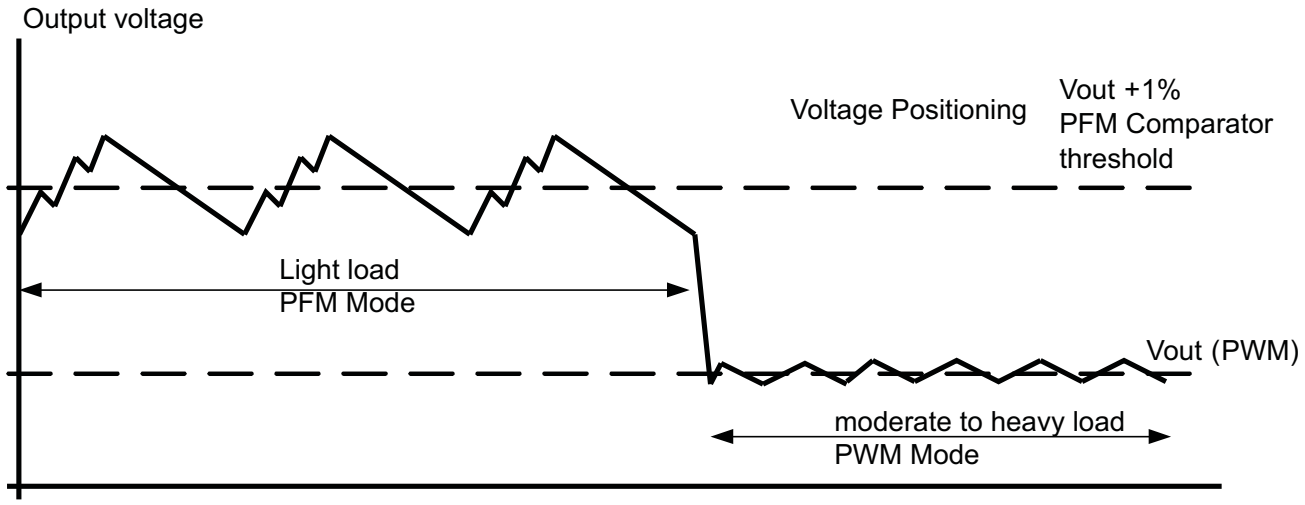


Figure 19. Operation in Power-Save Mode

100% Duty-Cycle Low-Dropout Mode

The device starts to enter 100% duty-cycle mode once the input voltage comes close the nominal output voltage. To maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing VIN, the high-side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_O max + I_O max \times r_{DS(on)} max + R_L)$$

with:

$I_O$max = maximum output current plus inductor ripple current

$r_{DS(on)}$max = maximum P-channel switch $r_{DS(on)}$.

R_L = dc resistance of the inductor

$V_O$max = nominal output voltage plus maximum output-voltage tolerance

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the output stage of the converter. The undervoltage lockout threshold is typically 1.85 V with falling V_{IN}.

MODE SELECTION

The MODE pin allows mode selection between forced PWM mode and power-save mode.

Connecting this pin to GND enables the power-save mode with automatic transition between PWM and PFM modes. Pulling the MODE pin high forces the converter to operate in fixed-frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

ENABLE

The device is enabled setting EN pin to high. During start-up time $t_{Start\ Up}$, the internal circuits are settled. Afterwards, the device activates the soft-start circuit. The EN input can be used to control power sequencing in a system with various dc/dc converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and get a sequencing of supply rails. With EN = GND, the device enters shutdown mode. In this mode, all circuits are disabled. In fixed-output-voltage versions, the internal resistor divider network is disconnected from the FB pin.

SOFT START

The TPS62590-Q1 has an internal soft-start circuit that controls the ramp-up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within typically 250 µs. This limits the inrush current in the converter during ramp-up and prevents possible input voltage drops when a battery or high-impedance power source is used. The soft-start circuit is enabled within start-up time $t_{Start\ Up}$.

SHORT-CIRCUIT PROTECTION

The high-side and low-side MOSFET switches are short-circuit protected with maximum switch current = I_{LIMF}. The current in the switches is monitored by current-limit comparators. Once the current in the high-side MOSFET switch exceeds the threshold of its current-limit comparator, it turns off and the low-side MOSFET switch is activated to ramp down the current in the inductor and high-side MOSFET switch. The high-side MOSFET switch can only turn on again once the current in the low-side MOSFET switch has decreased below the threshold of its current-limit comparator.

THERMAL SHUTDOWN

As soon as the junction temperature T_J exceeds 140°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

APPLICATION INFORMATION

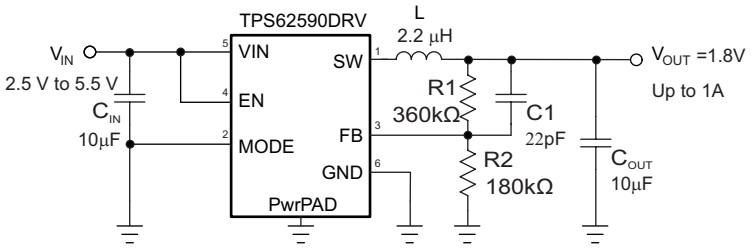


Figure 20. TPS62590-Q1DRV Adjustable 1.8 V

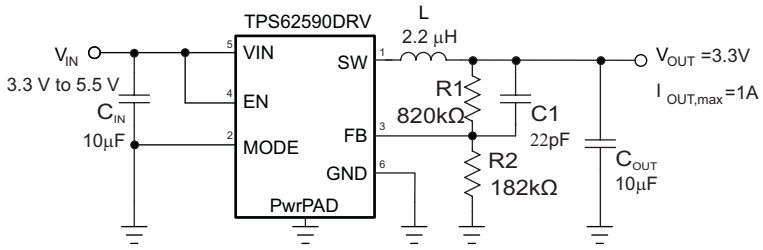


Figure 21. TPS62590-Q1DRV Adjustable 3.3 V

OUTPUT VOLTAGE SETTING

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

with the internal reference voltage V_{REF} = 0.6 V typically.

To minimize the current through the feedback divider network, R2 should be 180 kΩ or 360 kΩ. The sum of R1 and R2 should not exceed approximately 1 MΩ, to keep the network robust against noise. An external feed-forward capacitor C1 is required for optimum load-transient response. The value of C1 should be in the range between 22 pF and 33 pF.

Route the FB line away from noise sources, such as the inductor or the SW line.

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The TPS62590-Q1 is designed to operate with inductors in the range of 1.5 µH to 4.7 µH and with output capacitors in the range of 4.7 µF to 22 µF. The part is optimized for operation with a 2.2-µH inductor and 10-µF output capacitor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter may not fall below 1-µH effective inductance and 3.5-µF effective capacitance.

Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

The inductor selection also impacts the output-voltage ripple in PFM mode. Higher inductor values lead to lower output-voltage ripple and higher PFM frequency; lower inductor values lead to a higher output-voltage ripple but lower PFM frequency.

Equation 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 3. This is recommended because during heavy load transients the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad (2)$$

$$I_L max = I_{out} max + \frac{\Delta I_L}{2} \quad (3)$$

with:

f = Switching frequency (2.25 MHz, typical)

L = Inductor Value

ΔI_L = Peak-to-peak inductor ripple current

I_{Lmax} = Maximum inductor current

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter.

Accepting larger values of ripple current allows the use of low inductance values, but results in higher output voltage ripple, greater core losses, and lower output-current capability.

The total losses of the coil have a strong impact on the efficiency of the dc/dc conversion and consist of both the losses in the dc resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 4. List of Inductors

DIMENSIONS [mm]	INDUCTOR TYPE	SUPPLIER
3 × 3 × 1.5	LPS3015	Coilcraft
3 × 3 × 1.5	LQH3NPN2R2NM0	MURATA
3.2 × 2.6 × 1.2	MIPSA3226D2R2	FDK

Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the TPS62590-Q1 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output-voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode, and the RMS ripple current is calculated as:

$$I_{RMSC_{OUT}} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (4)$$

The overall output voltage ripple under the same conditions is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (5)$$

At light load currents, the converter operates in power-save mode, and the output-voltage ripple is dependent on the output capacitor and inductor values. Larger output capacitor and inductor values minimize the voltage ripple in PFM mode and tighten dc output accuracy in PFM mode.

Input Capacitor Selection

The buck converter has a natural pulsating input current; therefore, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 10-µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the V_{IN} pin. The ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 5. List of Capacitor

CAPACITANCE	TYPE	SIZE	SUPPLIER
10 µF	GRM188R60J106M69D	0603 1.6 mm × 0.8 mm × 0.8 mm	Murata

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues, and EMI problems. It is critical to provide a low-inductance, low-impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor, output capacitor, and inductor should be placed as close as possible to the IC pins.

Connect the GND pin of the device to the thermal pad of the PCB and use this pad as a star point. Use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Connect these ground nodes together to the thermal pad (star point) underneath the IC. Keep the common path to the GND pin, which returns the small-signal components and the high current of the output capacitors, as short as possible to avoid ground noise. The FB line should be connected directly to the output capacitor and routed away from noisy components and traces (for example, the SW line).

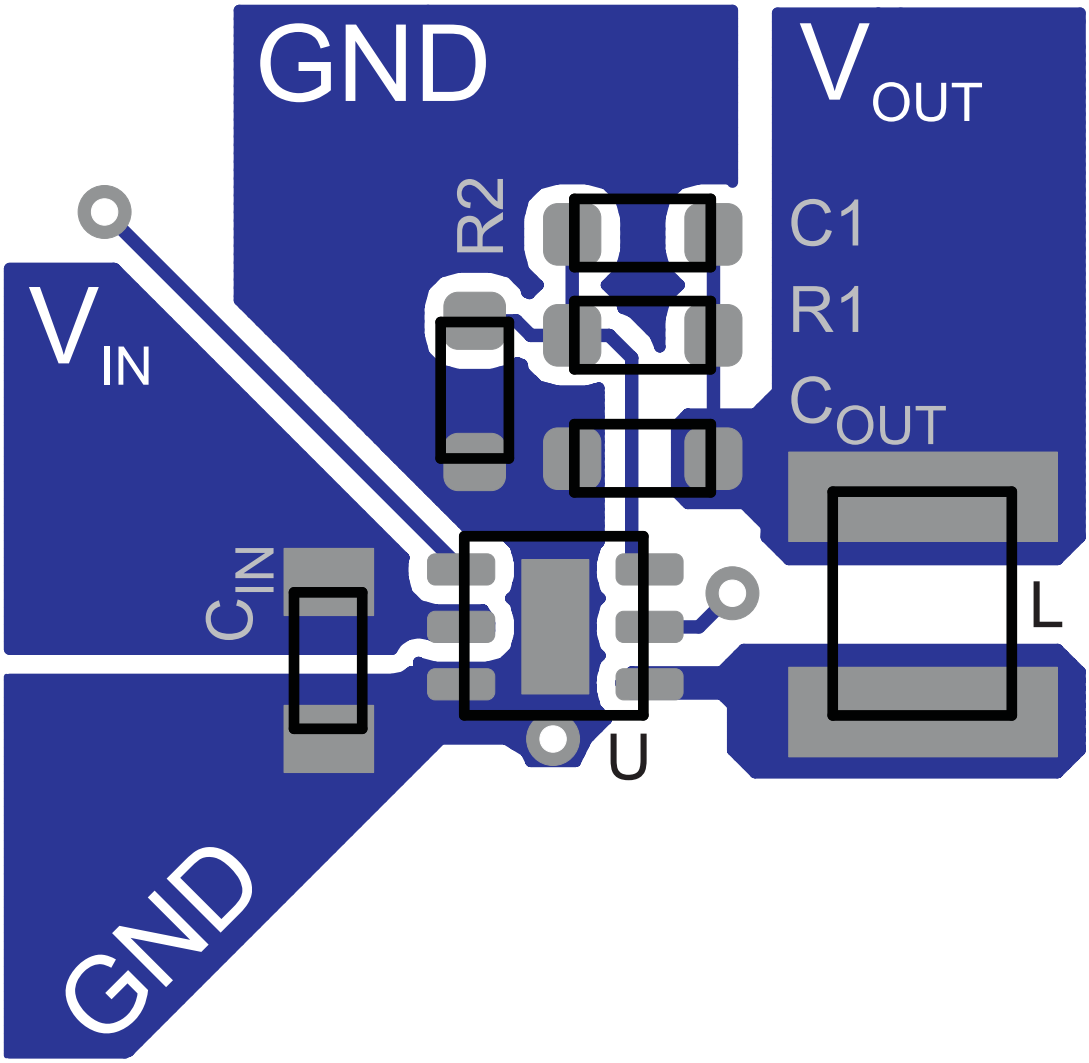


Figure 22. Layout

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62590TDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS62590-Q1 :

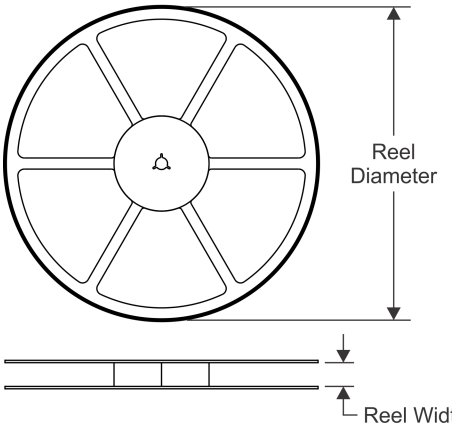
- Catalog: TPS62590

NOTE: Qualified Version Definitions:

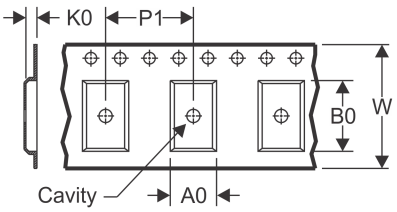
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

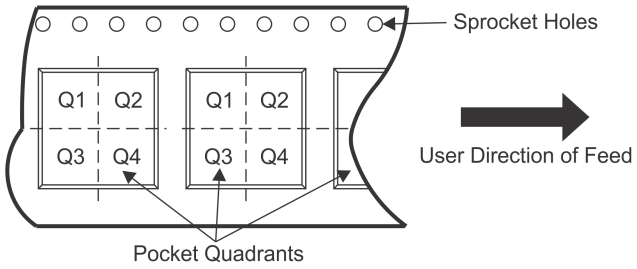


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

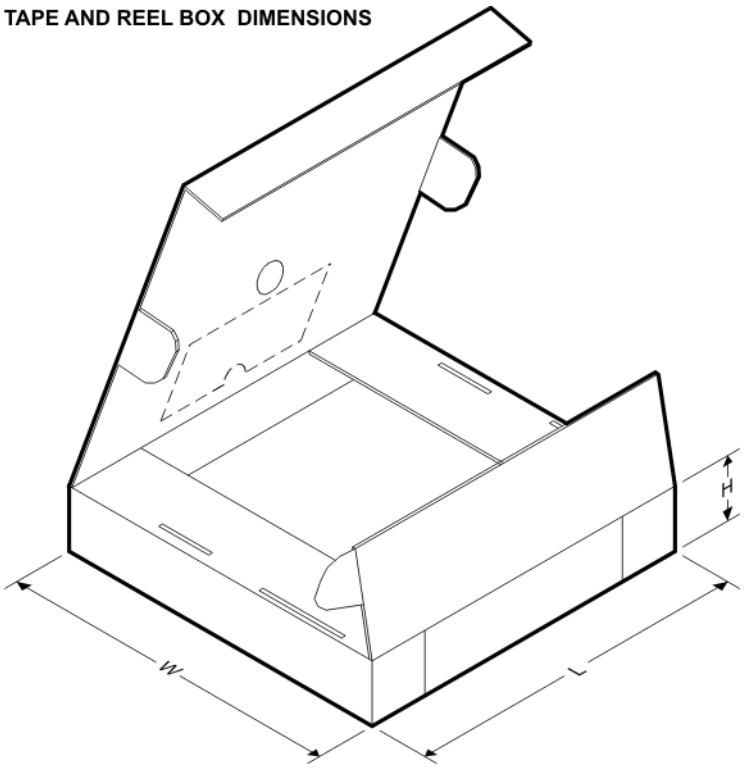
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62590TDRVRQ1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

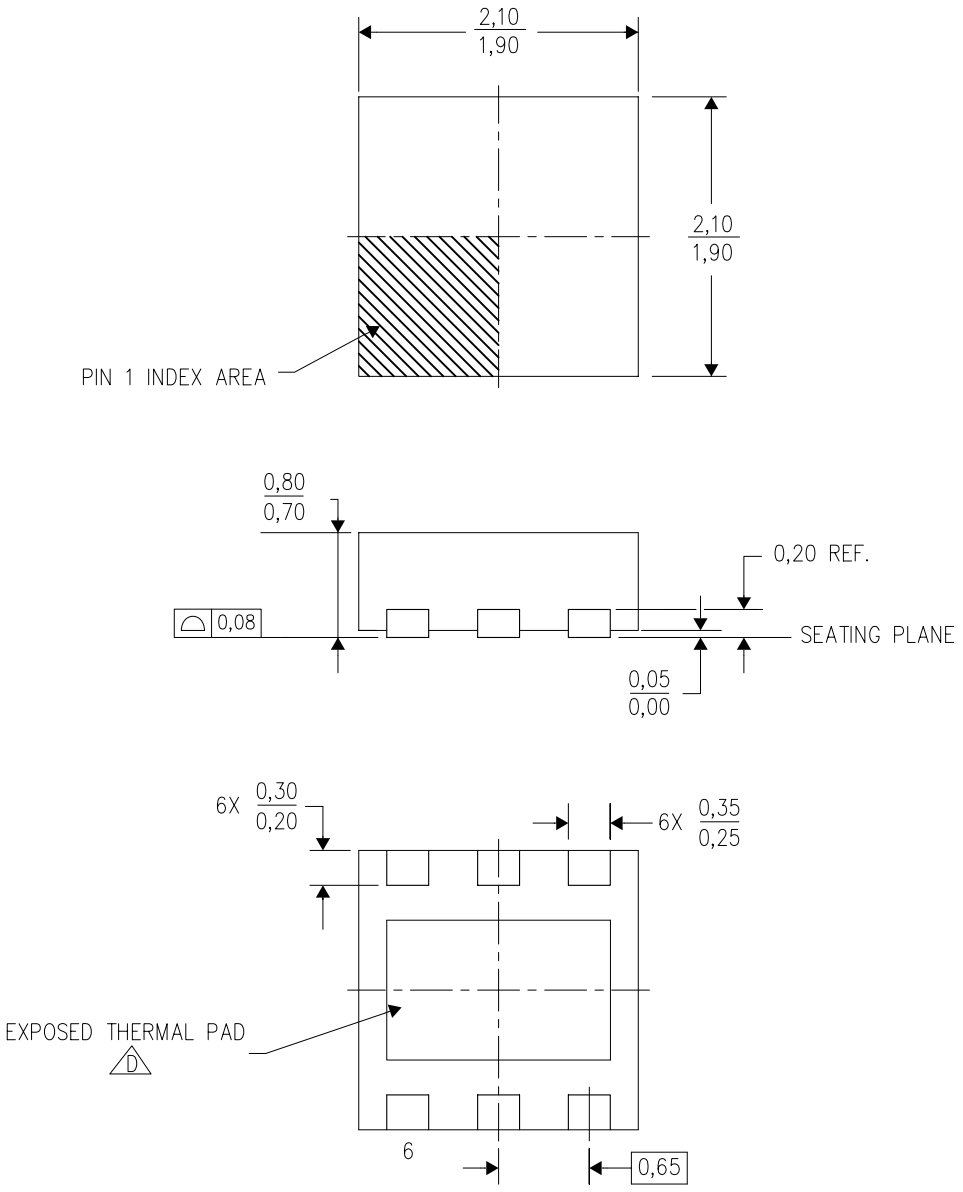
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62590TDRVRQ1	SON	DRV	6	3000	195.0	200.0	45.0

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

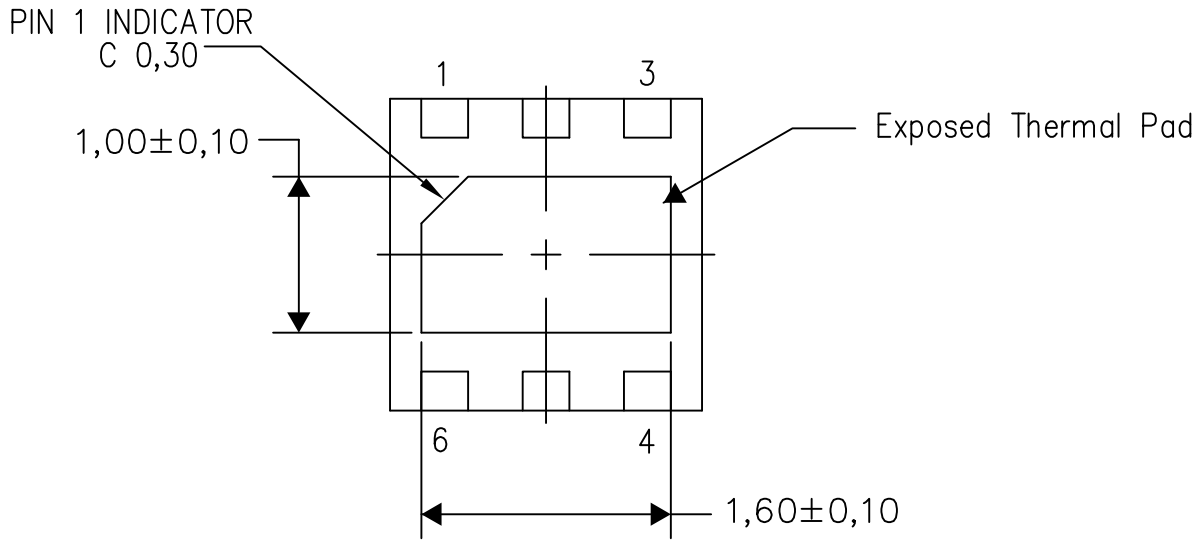
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



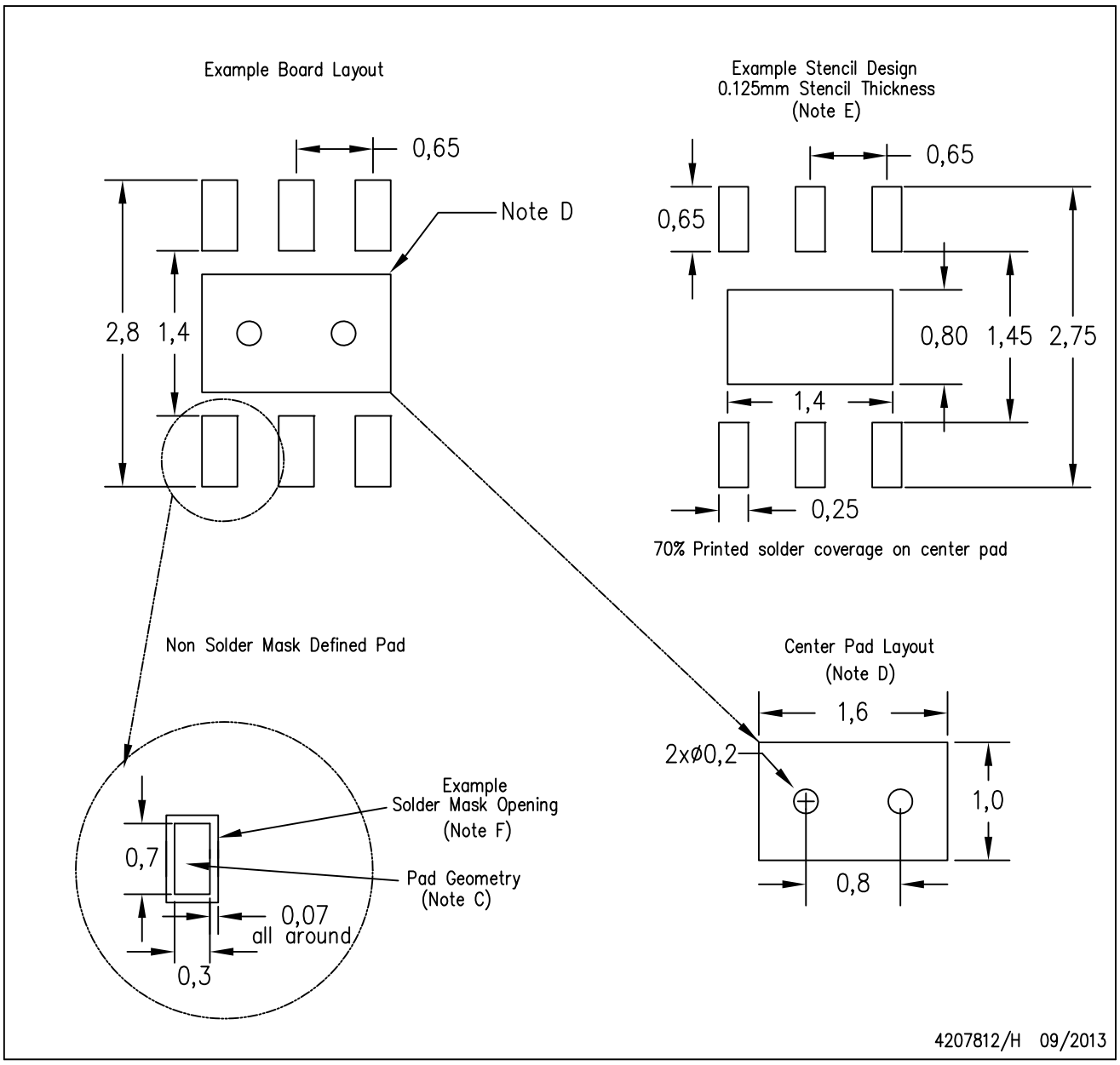
Bottom View

Exposed Thermal Pad Dimensions

4206926/N 03/13

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265