SINGLE INDUCTOR BUCK-BOOST WITH 1A SWITCHES AND ADJUSTABLE SOFT START

Check for Samples: TPS63051

FEATURES

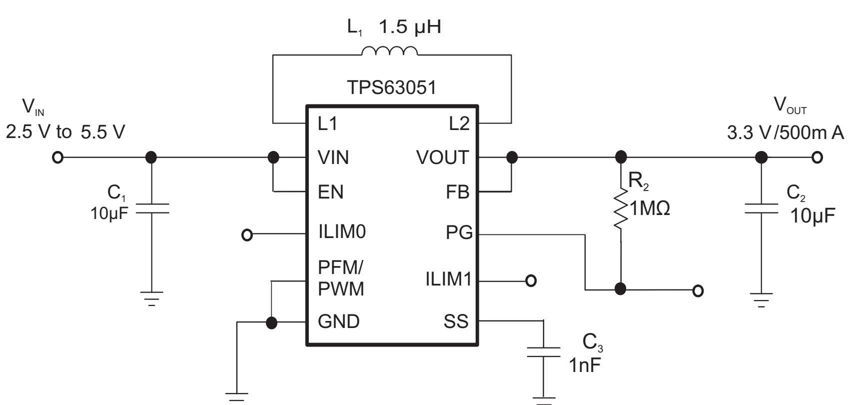
- **2.5V to 5.5V Input Voltage Range**
- **0.5A Continuous Output Current : V_{IN} ≥2.5V, V_{OUT} = 3.3V**
- **Real Buck or Boost Operation for Highest Efficiency**
- **Efficiency >90% in Boost Mode and >95% in Buck Mode**
- **Seamless Buck-Boost and PFM-PWM transition with the lowest Output Voltage Ripple**
- **2.5MHz Typical Switching Frequency**
- **Adjustable Average Input Current Limit**
- **Adjustable Soft Start**
- **Device Quiescent Current Less Than 50µA**
- **Power Save Mode**
- **Load Disconnect During Shutdown**
- **Over-Temperature Protection**
- **Small 1.6mm x 1.2mm, 12-pin WCSP package**

APPLICATIONS

- **Cellular Phones, Smart phones**
- **Tablet PCs**
- **PC and Smart Phone Accessories**
- **USB Powered Applications**

DESCRIPTION

The TPS63051 is high efficiency, low quiescent current buck-boost converter suitable for applications where the input voltage can be higher or lower than the output voltage . Output currents can go as high as 500mA in boost mode and as high as 1A in buck mode. The buck-boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters Power Save Mode to maintain high efficiency over a wide load current range. The maximum average input current in the switches is limited to a typical value of 1A. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery. The device is packaged in a 12-pin WCSP package measuring 1.6mm × 1.2mm.



ILIM0	ILIM1	Current LIMIT set
Low	Low	0.4*I_{IN_MAX}
High	Low	0.5*I_{IN_MAX}
Low	High	0.65*I_{IN_MAX}
High	High	I_{IN_MAX}

Figure 1. Typical Circuit

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	VOUT	PART NUMBER	PACKAGE	ORDERING	PACKAGE MARKING
–40°C to 85°C	3.3 V	TPS63051	WCSP	TPS63051YFF	63051

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE MIN	VALUE MAX	UNIT
Voltage range (1)	VIN, L1, L2, VOUT, EN, FB, PG, ILIM0, ILIM1	–0.3	7	V
	SS	-0.3	3	V
ESD rating (2)	Human Body Model		1.5	kV
	Charged Device Model		500	V
Operating junction temperature range, T_J		–40	150	°C
Storage temperature range T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC (1)		TPS63051 12 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	89.9	°C/W
$\theta_{JC(TOP)}$	Junction-to-case(top) thermal resistance	0.7	
θ_{JB}	Junction-to-board thermal resistance	43.9	
ψ_{JT}	Junction-to-top characterization parameter	2.9	
ψ_{JB}	Junction-to-board characterization parameter	43.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
VIN	Input Voltage Range	2.5		5.5	V
L	Inductor Value	1	1.5	2.2	µH
C_{out}	Output Capacitor value	10		120	µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

V_{IN}=3.6V, T_A=-40°C to 85°C, typical values are at T_A=25°C (unless otherwise noted)

PARAMETER$_{OUT}$			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply							
V_{IN}	Input voltage range			2.5		5.5	V
V_{IN_Min}	Minimum input voltage to turn on in to full load		I_{OUT}=500mA		2.7		V
I_{OUT}	Output Current (1)				500		mA
I_Q	Quiescent current	V_{IN}	I_{OUT}=0mA, PFM/PWM=GND, EN=V_{IN}=3.6V,V_{OUT}=3.3V		43	60	µA
		V_{OUT}				10	µA
I_{sd}	Shutdown current		EN=GND		0.1	1	µA
V_{UVLO}	Under voltage lockout threshold		V_{IN} falling	1.6	1.7	1.8	V
	Under voltage lockout hysteresis				200		mV
T_{SD}	Thermal shutdown		Temperature rising		140		°C
	Thermal Shutdown hysteresis				20		°C
Logic Signals EN, I_{LIM0}, I_{LIM1}							
V_{IH}	High Level Input voltage		V_{IN}=2.5V to 5.5V	1.2			V
V_{IL}	Low level Input Voltage		V_{IN}=2.5V to 5.5V			0.3	V
I_{lkg}	Input Leakage current		EN, I_{LIM0}, I_{LIM1}=GND or V_{IN}		0.01	0.1	µA
Power Good PG							
V_{OL}	Low level voltage		I_{sink}=100µA			0.3	V
I_{PG}	PG sinking current		V_{PG}=0.3V			0.1	mA
I_{lkg}	Input Leakage current		V_{PG}=3.6V		0.01	0.1	µA
Output							
V_{OUT}	Output Voltage range			2.5		5.5	V
V_{OUT}	TPS63051 Output voltage accuracy (2)		PWM mode	3.267	3.3	3.333	V
V_{OUT}	TPS63051 Output voltage accuracy(2)		PFM mode	3.267	3.3	3.399	V
$I_{PWM\text{->}PFM}$	Minimum output current to enter PFM mode(3)		V_{IN} =3V; V_{OUT} = 3.3V		150		mA
$R_{DS(on)}$	Input High side FET on-resistance		I_{SW}=500mA		145		mΩ
	Output High side FET on-resistance				95		mΩ
	Input Low side FET on-resistance				170		mΩ
	Output Low side FET on-resistance				115		mΩ
I_{IN_MAX}	Input current limit Boost Mode,(4)		I_{LIM0}=V_{IH}, I_{LIM1}= V_{IH},V_{IN}=2.7V to 3.3V, V_{OUT}=3.3V,	600		1400	mA
I_{SS_IN}	Soft Start programmable average input current limit (3)		I_{LIM0}=V_{IL}, I_{LIM1}= V_{IL},V_{IN}=3.0V,V_{OUT}=3.3V		0.4*I_{IN_MAX}		mA
			I_{LIM0}=V_{IL}, I_{LIM1}= V_{IH},V_{IN}=3.0V,V_{OUT}=3.3V		0.5*I_{IN_MAX}		mA
			I_{LIM0}=V_{IH}, I_{LIM1}= V_{IL},V_{IN}=3.0V,V_{OUT}=3.3V		0.65*I_{IN_MAX}		mA
			I_{LIM0}=V_{IH}, I_{LIM1}= V_{IH},V_{IN}=3.0V,V_{OUT}=3.3V		I_{IN_MAX}		mA
f_s	Switching Frequency				2.5		MHz
I_{SS}	Softstart Current				1		µA
t_{delay}	Start up delay		Time from EN=high to device starts switching		85		µs

(1) For minimum and maximum output current in a specific working point refer to Figure 3 , Figure 4 and Equation 1, Equation 2, Equation 3, and Equation 4 in the Adjustable Current Limit section
(2) Conditions: f=2.5MHz, L=1.5µH, C_{OUT}=10µF
(3) For variation of this parameter with Input voltage and temperature refer to Figure 5
(4) For variation of this parameter with temperature refer to Figure 6

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=3.6V, T_A=-40°C to 85°C, typical values are at T_A=25°C (unless otherwise noted)

PARAMETER$_{OUT}$		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SS}	Soft-start time	V_{OUT} with EN=low to high, SS=floating, Buck mode Vin=3.6V, Vout=3.3V, Iout=500mA		280		µs
		$V_{OUT}$with EN=low to high, SS=floating, Boost mode Vin=2.5V, Vout=3.3V, Iout=500mA		600		µs
	Line regulation PWM mode	V_{IN}=2.5V to 5.5V, I_{OUT}=500mA		0.000963		V/V
	Load regulation PWM mode	V_{IN}=3.6V, I_{OUT}=0mA to 500mA		0.004		V/A

PIN ASSIGNMENTS

(TOP VIEW)

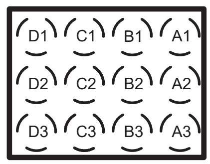
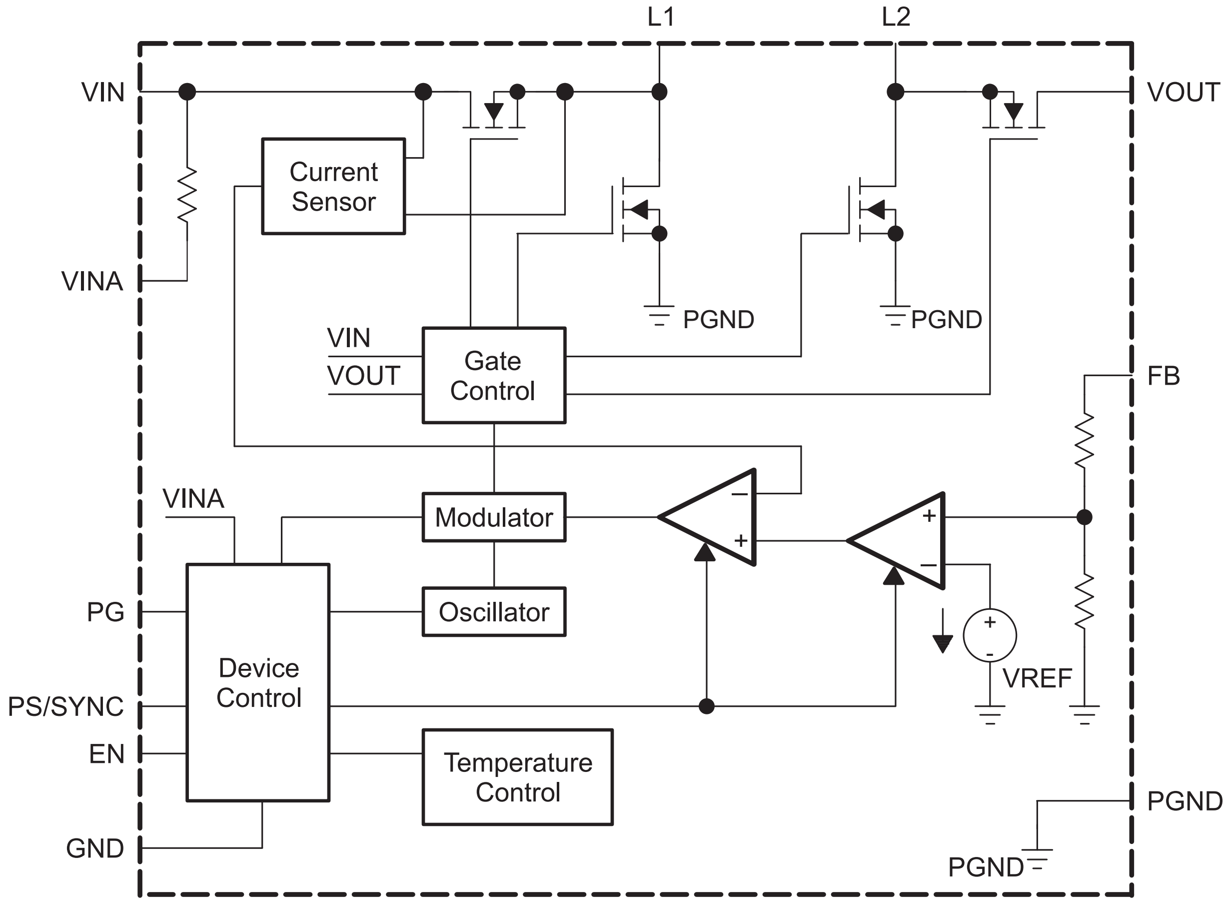


Figure 2.

Pin Functions

Pin NAME	Pin NO.	I/O	DESCRIPTION
ILIM0	B2	I	Adjustable current limit input, works together with I_{LIM1}. See table in Figure 1. It must not be left floating.
SS	D3	I	Adjustable Soft-Start. If connected to ground default soft-start time set.
PG	C3	O	Power good open drain output (See Power Good section for details)
FB	D2	I	Must be connected to VOUT
EN	A3	I	Enable input. (1 enabled, 0 disabled)
VOUT	D1	O	Buck-boost converter output
VIN	A2	I	Supply voltage for power stage and control stage
L1	A1		Connection for Inductor
GND	B1		Ground for Power stage and Control stage
ILIM1	B3	I	Adjustable current limit input, works together with I_{LIM0}. See table in Figure 1. It must not be left floating.
PFM/PWM	C2	I	0 for PFM mode, 1 for forced PWM. It must not be left open
L2	C1		Connection for Inductor

FUNCTIONAL BLOCK DIAGRAM (TPS63051)



TYPICAL CHARACTERISTICS

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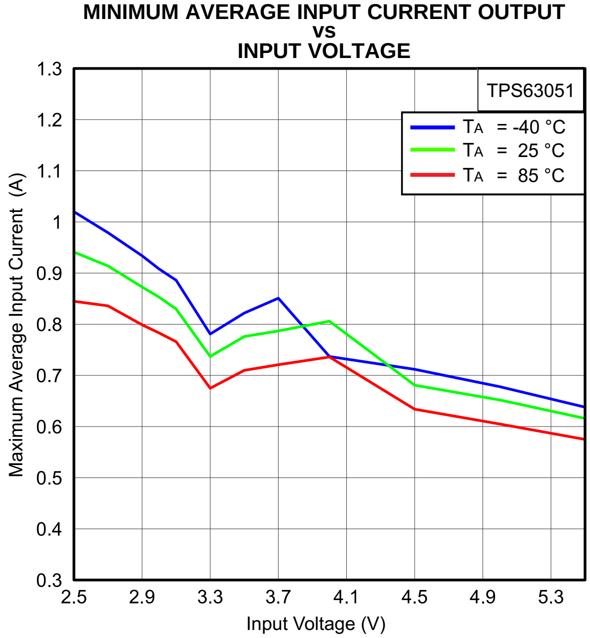


Figure 3.

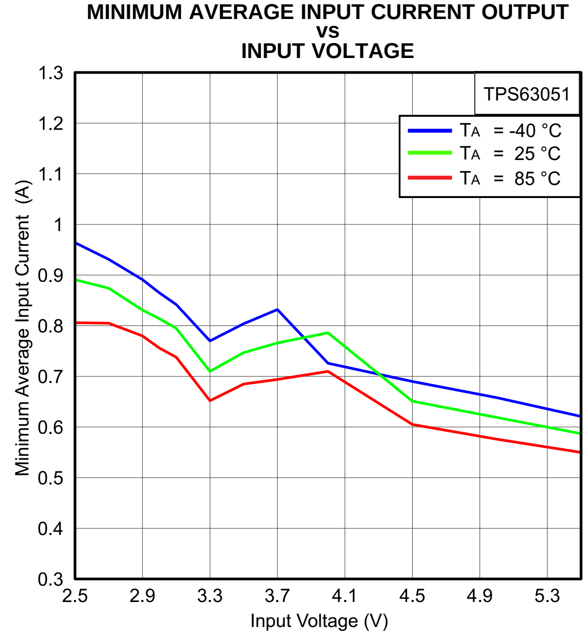


Figure 4.

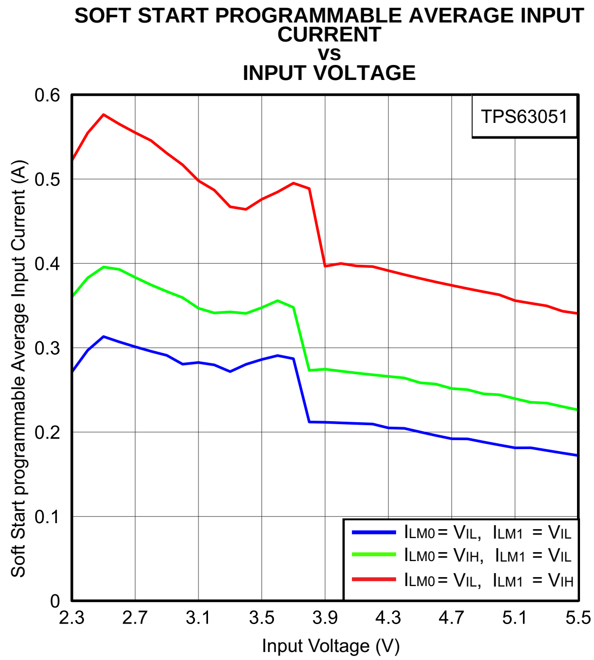


Figure 5.

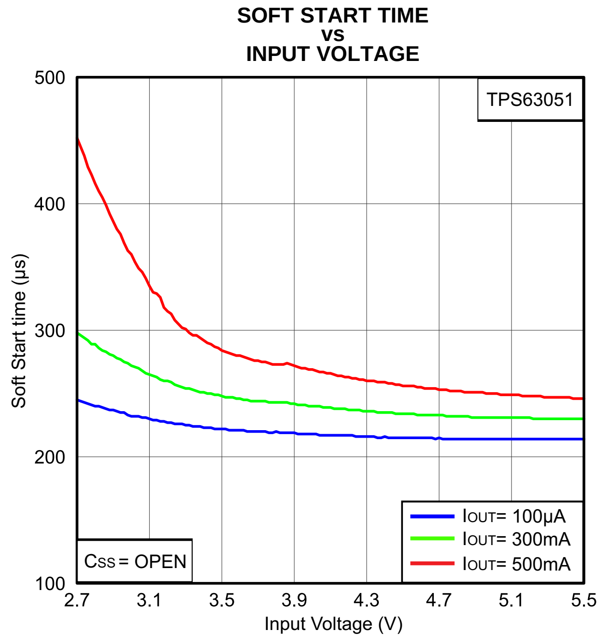


Figure 6.

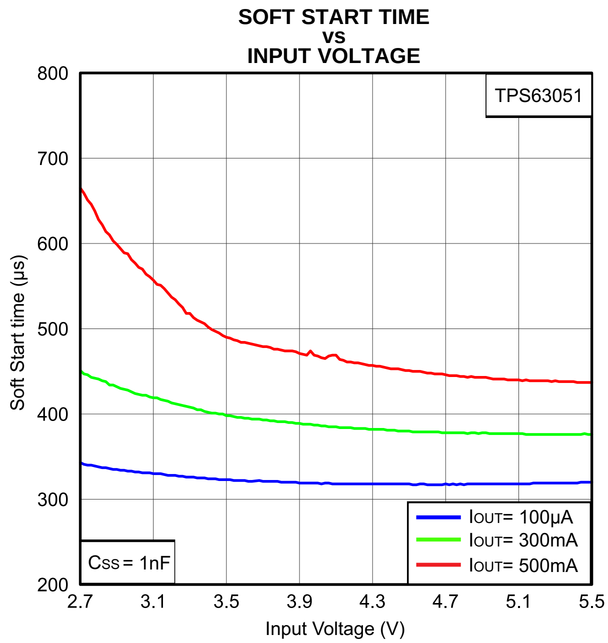


Figure 7.

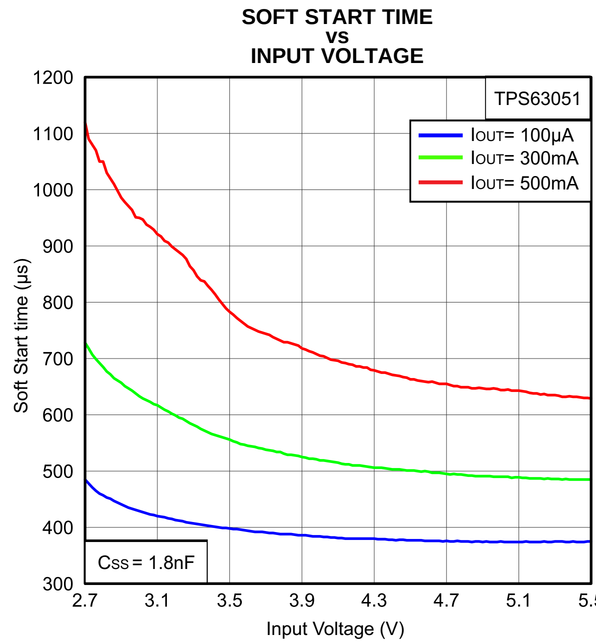


Figure 8.

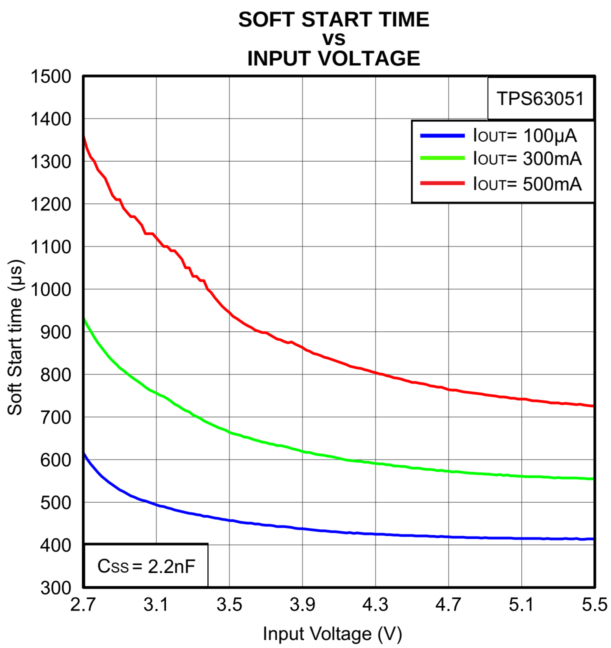


Figure 9.

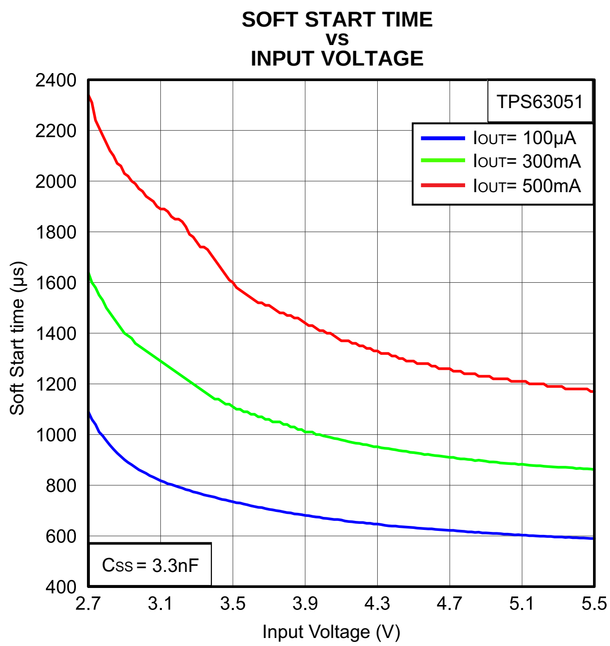


Figure 10.

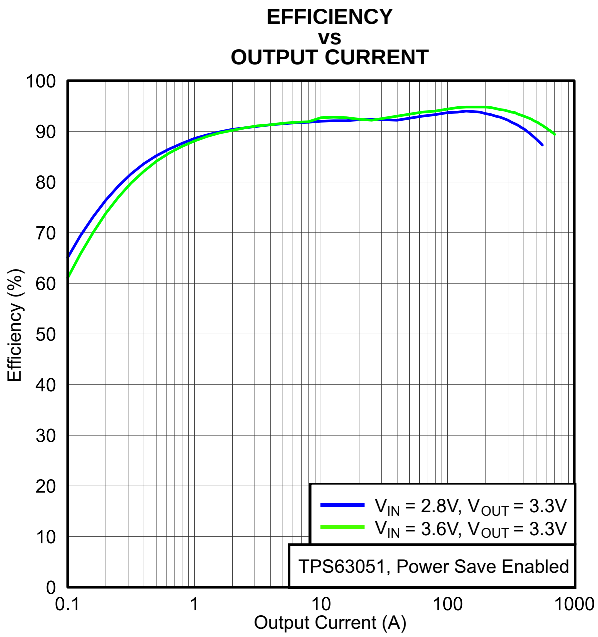
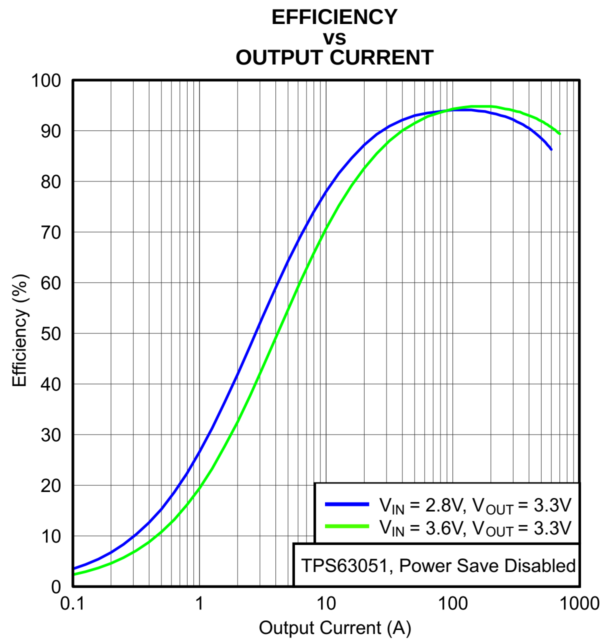


Figure 11.



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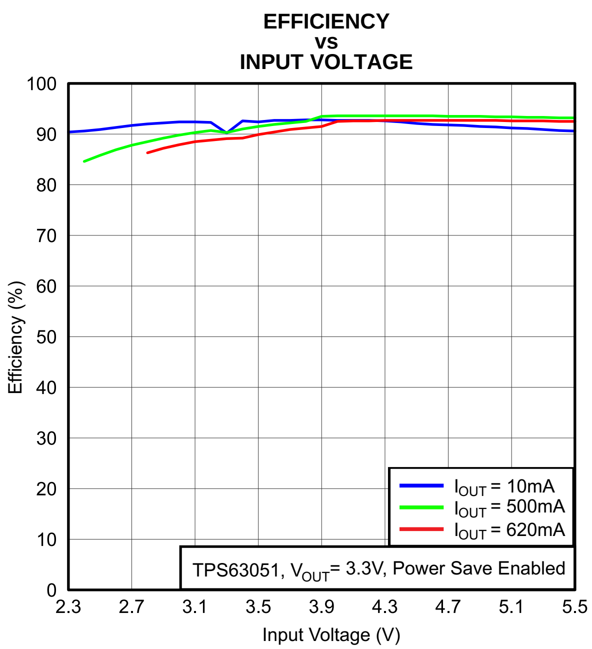

Figure 13.

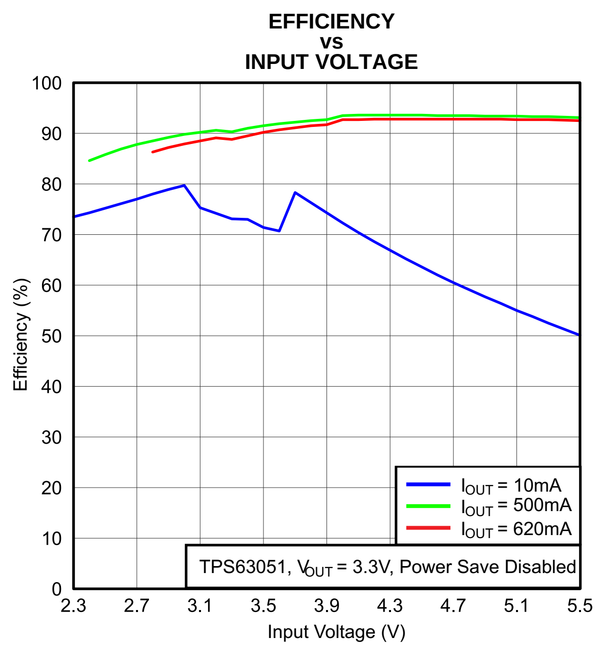

Figure 14.

OUTPUT VOLTAGE vs OUTPUT CURRENT

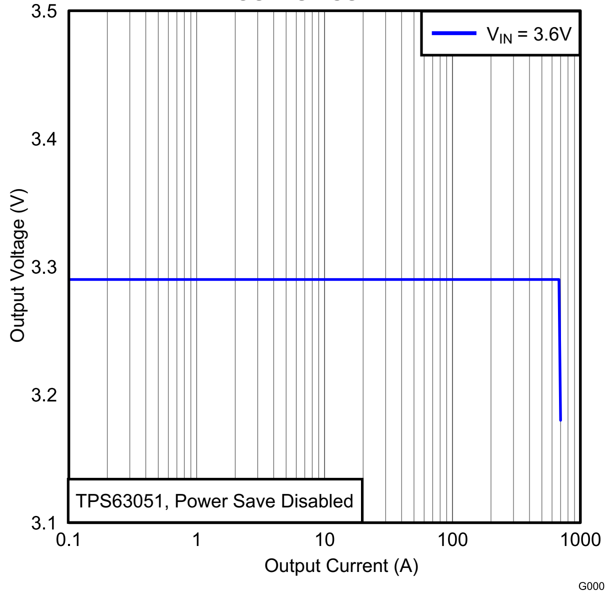

Figure 15.

OUTPUT VOLTAGE RIPPLE IN BUCK-BOOST MODE AND PFM TO PWM TRANSITION

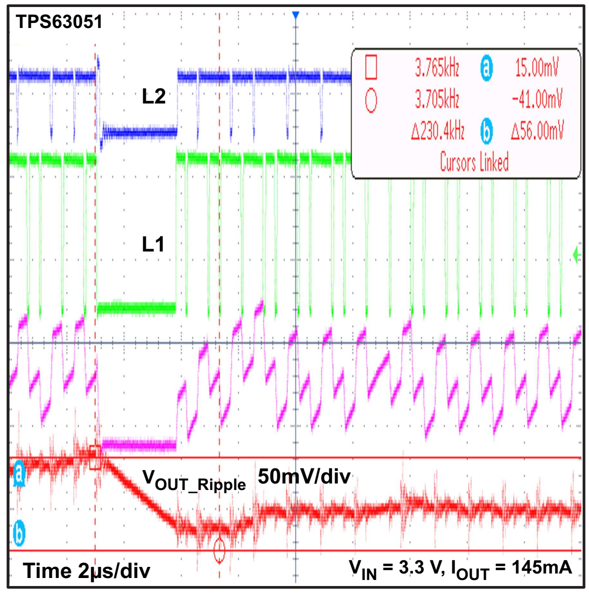

Figure 16.

OUTPUT VOLTAGE RIPPLE IN BOOST MODE AND PFM

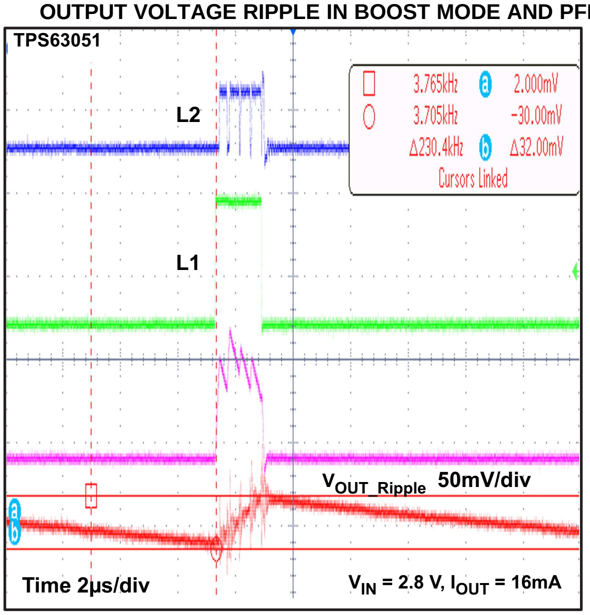

Figure 17.

OUTPUT VOLTAGE RIPPLE IN BUCK MODE AND PFM

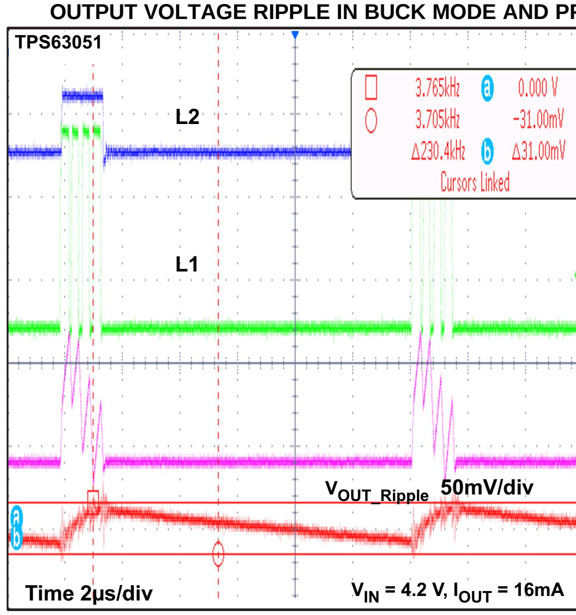

Figure 18.

SWITCHING WAVEFORMS BOOST MODE AND PWM

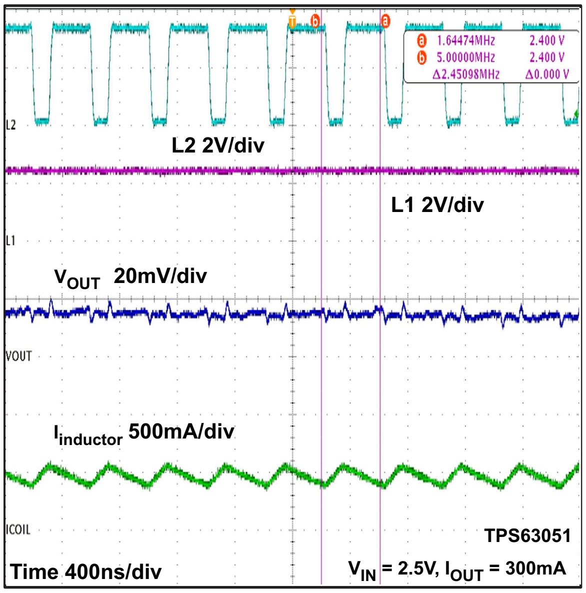

Figure 19.

SWITCHING WAVEFORMS BUCK MODE AND PWM

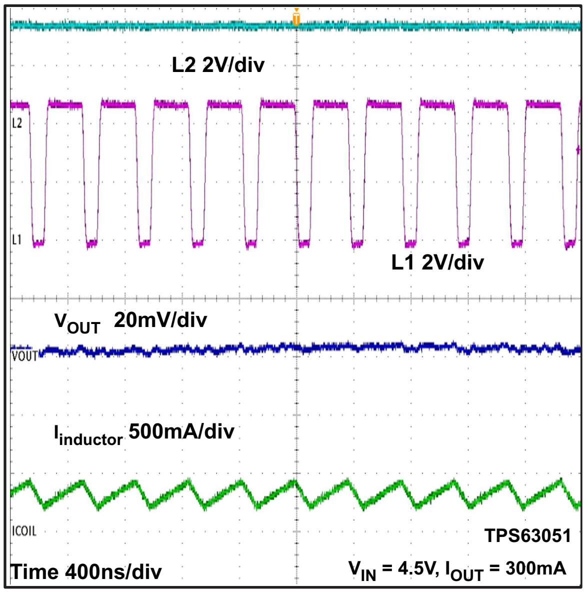

Figure 20.

SWITCHING WAVEFORMS BUCK-BOOST MODE AND PWM

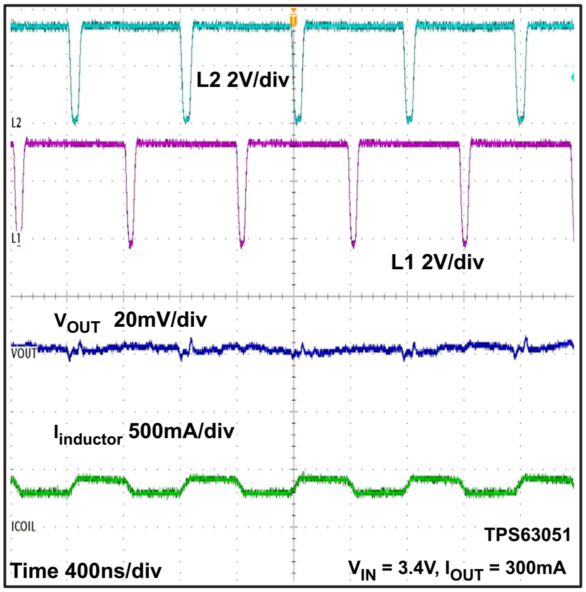

Figure 21.

LOAD TRANSIENT RESPONSE

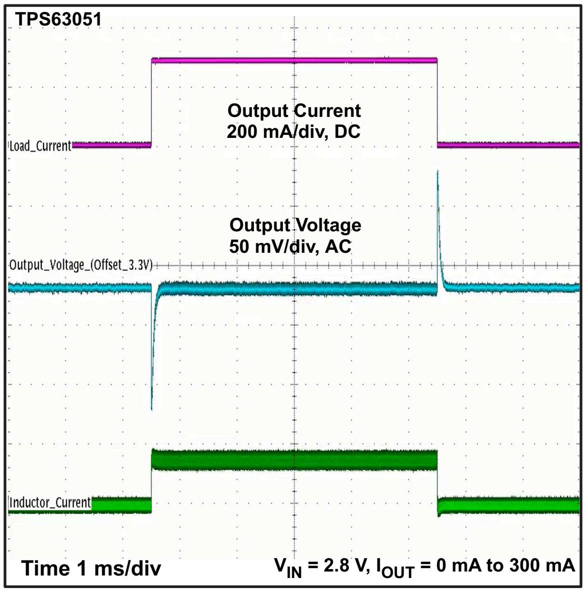

Figure 22.

LOAD TRANSIENT RESPONSE

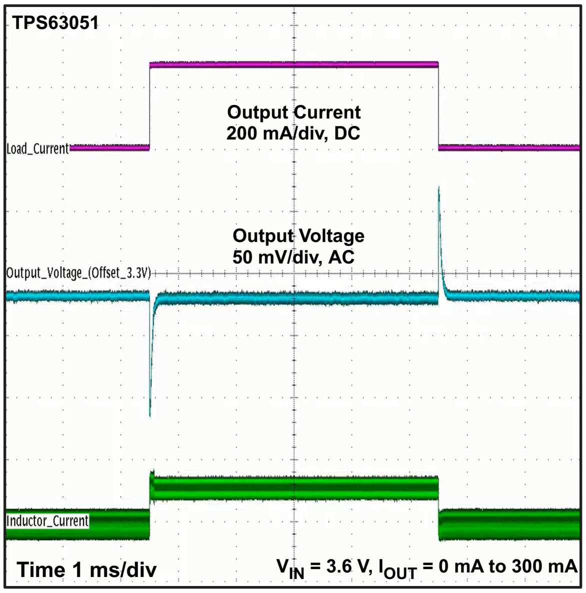

Figure 23.

LINE TRANSIENT RESPONSE

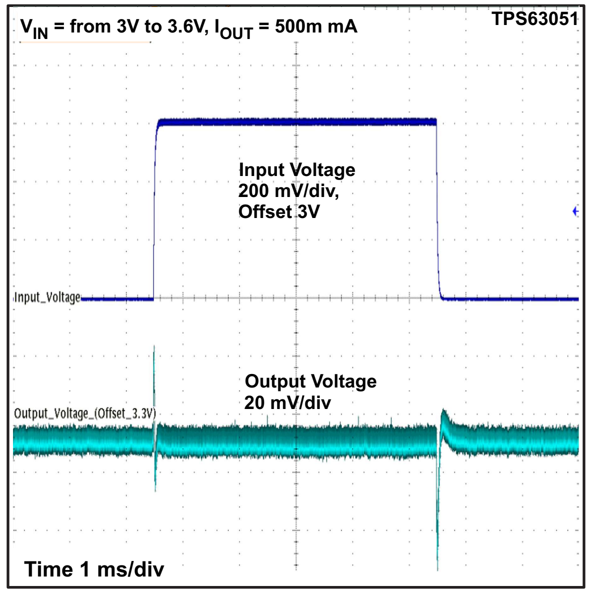

Figure 24.

START UP AFTER ENABLE

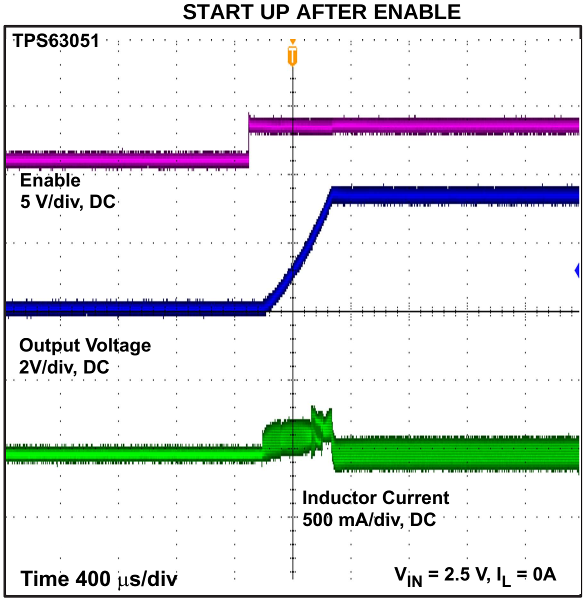

Figure 25.

START UP AFTER ENABLE

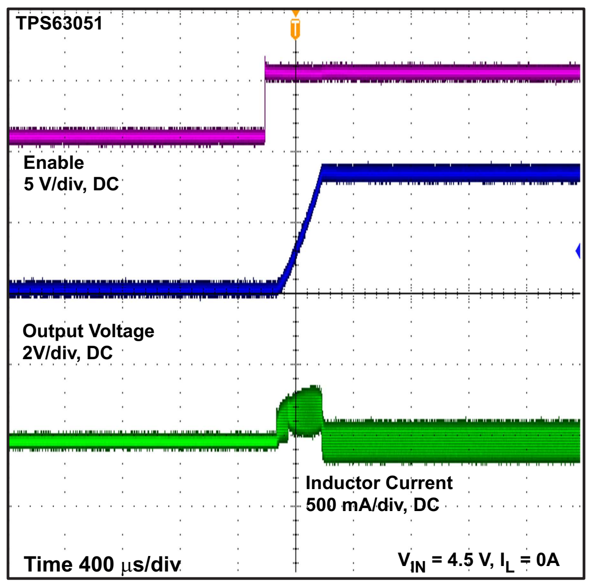

Figure 26.

PARAMETER MEASUREMENT INFORMATION

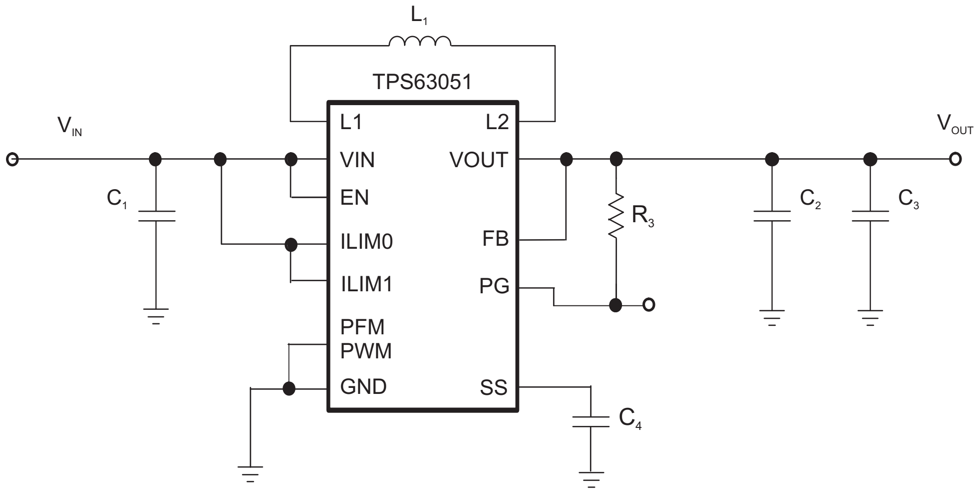

Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS63051	Texas Instruments
L1	1.5µH, 2.1A/108mΩ	1269AS-H-1R5M, TOKO
C1	10 µF 6.3V, 0603, X5R ceramic	GRM188R60J106ME84D, Murata
C2,C3	2 x 10 µF 6.3V, 0603, X5R ceramic	GRM188R60J106ME84D, Murata
R3	1 MΩ	

DETAILED DESCRIPTION

Buck-Boost Operation

The TPS63051 use 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range. To regulate the output voltage at all possible input voltage conditions, the device automatically switches from buck operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch on, and one switch held off. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are switching. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. For the remaining 2 switches, one is kept on and the other is kept off, thus causing no switching losses. Controlling the switches this way allows the converter to always keep high efficiency over the complete input voltage range. The device provides a seamless transition from buck to boost or from boost to buck operation.

Control Loop Description

The controller circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. Figure 27 shows the control loop.

The non inverting input of the transconductance amplifier Gmv can be assumed to be constant. The output of Gmv defines the average inductor current. The inductor current is reconstructed by measuring the current through the high side buck MOSFET. This current corresponds exactly to the inductor current in boost mode. In buck mode, the current is measured during the on time of the same MOSFET. During the off time, the current is reconstructed internally starting from the peak value reached at the end of the on time cycle. The average current is then compared to the desired value and the difference, or current error, is amplified and compared to the sawtooth ramp of either the Buck or the Boost. Depending on which of the two ramps is crossed by the signal, either the Buck MOSFETs or the Boost MOSFETs are activated. When the input voltage is close to the output voltage, one buck cycle is followed by a boost cycle. In this condition, not more than three cycle in a row of the same mode are allowed. This control method in the buck-boost region ensures a robust control and the highest efficiency.

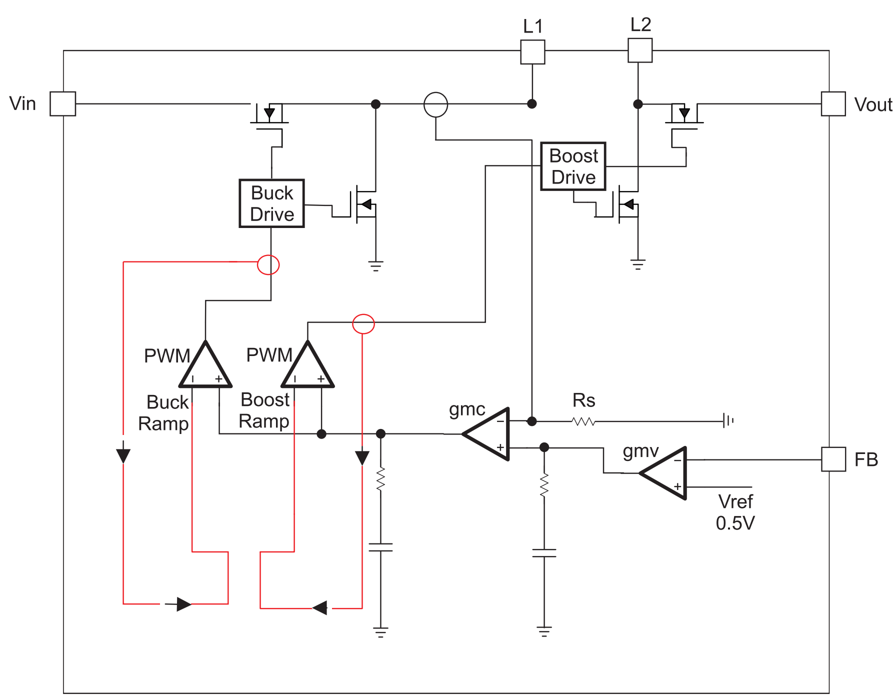

Figure 27. Average Current Mode Control

Power Save Mode

Depending on the load current, in order to provide the best efficiency over the complete load range, the device works in PWM mode at load current of approximately 150mA or higher. At lighter load, the device switches automatically in to Power Save Mode to reduce power consumption and extend battery life. The PFM/PWM pin can be used to select between the two different operation modes. To enable Power Save Mode, the PFM/PWM pin must be set low.

During Power Save Mode, the part operates with a reduced switching frequency and supply current to maintain high efficiency. The output voltage is monitored with a comparator by the threshold comp low and comp high at every clock cycle. When the device enters Power Save Mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the value of output capacitance. When the output voltage reaches the comp low threshold, at the next clock cycle the device ramps up the output voltage again, by starting operation. Operation can last for one or several pulses until the comp high threshold is reached. At the next clock cycle, if the output current is still lower than about 150mA, the device switches off again and the same operation is repeated. Instead, if at the next clock cycle, the load is above 150mA , the device automatically switches to PWM mode.

In order to keep high efficiency in PFM mode, there is only a comparator active to keep the output voltage regulated. The AC ripple in this condition is increased, compared to the voltage in PWM mode. The amplitude of this voltage ripple in the worst case scenario is 50mV pk-pk, (typically 30mV pk-pk), with 10µF effective capacitance. In order to avoid a critical voltage drop when switching from 0A to full load, the output voltage in PFM is typically 1.5% above the nominal value in PWM. This allows the converter to operate with a small output capacitor and still have a low absolute voltage drop during heavy load transients.

Power Save Mode can be disabled by programming the PFM/PWM pin high.

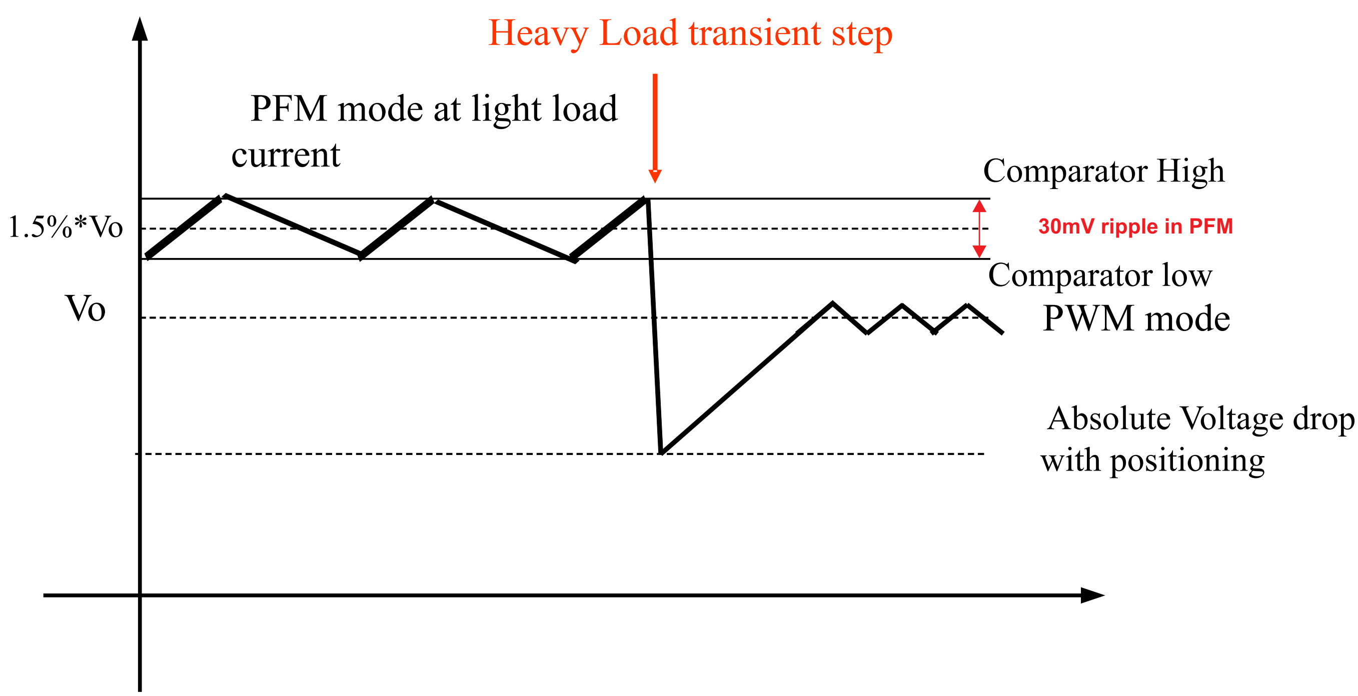

Figure 28. Dynamic Voltage Positioning

Adjustable Current Limit

The TPS63051 has an internal soft-start circuit that controls the ramp-up of the current during start-up and prevents high inrush current that exceeds the set current limit, protecting the device and the application. During start-up the input current does not exceed the current limit set by the I_{LIM0} pin and I_{LIM1} pin. Depending on the voltage applied at these two pins, it's possible to switch between 4 different current levels, as described in the table below. The variation of these values over input voltage and temperature is described in Figure 3, Figure 4, Figure 5, and Figure 6.

It's possible to further adjust, at turn on, the ramp up time of the current and the output voltage using the Soft-Start capacitor.

The combination allowed using I_{LIM0} and I_{LIM1}, which will lead to the different current level, is described in the Current Settings table below.

Current Settings

ILIM0	ILIM1	Current LIMIT set
Low	Low	$0.4 \cdot I_{IN\_MAX}$
High	Low	$0.5 \cdot I_{IN\_MAX}$
Low	High	$0.65 \cdot I_{IN\_MAX}$
High	High	I_{IN_MAX}

The I_{LIM0}, I_{LIM1} pins may be changed during operation.

The current limit varies depending on the input voltage. The maximum value of average input current is obtained at the lowest input voltage.

Given the curves provided in Figure 3, Figure 4, Figure 5, and Figure 6 it is possible to calculate the output current in the different conditions in boost mode using Equation 1 and Equation 2 and in buck mode using Equation 3 and Equation 4.

Duty Cycle Boost
$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (1)$$

Output Current Boost
$$I_{OUT} = \eta \times I_{IN} (1-D) \quad (2)$$

Duty Cycle Buck
$$D = \frac{V_{OUT}}{V_{IN}} \quad (3)$$

Output Current Buck
$$I_{OUT} = (\eta \times I_{IN}) / D \quad (4)$$

With,

η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)
f = Converter switching frequency (typical 2.5MHz)
L = Selected inductor value
I_{IN}=Minimum average input current (Figure 5, Figure 6, Figure 7 and Figure 8)

Soft Start

To minimize inrush current during start up, the device implements a soft start. At turn on, the input current is raised in a controlled manner until the output voltage reaches regulation. The device ramps up the output voltage in a controlled manner, even if a large capacitor is connected at the output. The input current is prevented from rising above the level set by the I_{LIM0}, I_{LIM1} pins.

The TPS63051 charges the soft start capacitor, at the SS pin, with a constant current of typically 1µA. The input current follows the current used to charge the capacitor connected at the SS pin. The soft start operation is completed once the voltage at the SS pin has reached typically 1.3V. Figure 6 through Figure 10 list the value of soft start capacitor needed to obtain a specific soft start time. The soft start time listed in the table below is measured as the time from when the EN pin is asserted to when the output voltage has reached 90% of it's nominal value. This time depends on the load current also, measurements were taken on the schematic described on page 13. If the amount of output capacitor is different, then the soft start time will be different from the one shown in the plots.

Thanks to its innovative soft start circuit the device ramps up the output voltage even if a large capacitor is connected at the output at the same time as the load current. This specific case is never confused with a short circuit condition. The inductor current is able to decrease and guarantee always soft start unless a real short circuit is applied at the output terminals.

Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents flowing from the input.

Power Good

The device has a built in power good function to indicate whether the output voltage operates above appropriate levels. By monitoring the status of the current control loop, the power good output provides the earliest indication possible for an output voltage break down and leaves the connected application a maximum time to safely react. The power good is operable as long as the converter is enabled and VIN is present.

If the device is in current limit and the output voltage has not reached the regulated condition, the PG pin is held low. If the regulated condition is reached, PG is open drain.

When PG is open drain, its logic function can be adjusted to any voltage level the connected logic is using, via a pull up resistor to the supply voltage of the logic. PG follows the voltage which it is connected to, which can be the output of the TPS63051 or another external voltage.

If EN is pulled low and one of the pins I_{LIM0} or I_{LIM1} is high, then the PG pin is low. If both pins, I_{LIM0} and I_{LIM1} are low, the PG is open drain. In this case PG, follows its pull-up voltage. If this is not desired one of the two pins I_{LIM0} or I_{LIM1} must be set high. The power good settings table describes the PG functionality.

Power Good Settings

EN	ILIM1	ILIM0	PG
1	X	X	0 or Open Drain
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	Open Drain

Short Circuit Protection

The TPS63051 provides short circuit protection to protect itself and the application. When the output voltage does not increase above 1.2V, the device assumes a short circuit at the output and keeps the current limit low to protect itself and the application. In short circuit the current limit is kept low at maximum 1.5A

Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage does not work anymore. Therefore, overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. The implemented overvoltage protection circuit monitors the output voltage internally. In case it reaches the overvoltage threshold (typically 6.7V) the voltage amplifier regulates the output voltage to this value.

Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VIN is lower than V_{UVLO} (see electrical characteristics table). When in operation, the device automatically enters the shutdown mode if the voltage on VIN drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers above the hysteresis amount.

Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table), the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again.

APPLICATION INFORMATION

DESIGN PROCEDURE

The TPS63051 series of buck-boost converter has internal loop compensation. Therefore, the external L-C filter has to be selected according to the internal compensation. Nevertheless, it's important to consider that the effective inductance, due to inductor tolerance and current derating can vary between 20% and -30%. The same for the capacitance of the output filter: the effective capacitance can vary between +20% and -50% of the specified datasheet value, due to capacitor tolerance and bias voltage. For this reason, Output Filter Selection shows the nominal capacitance and inductance value allowed.

Table 2. Output Filter Selection

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)				
	10	20	44	66	100
1.0	√	√	√	√	√
1.5	√(3)	√	√	√	√
2.2			√	√	√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) Typical application. Other check marks indicates recommended filter combinations

Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using Equation 6. Only the equation which defines the switch current in boost mode is shown, because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{5}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{6}$$

Where,

D =Duty Cycle in Boost mode
f = Converter switching frequency (typical 2.5MHz)
L = Selected inductor value
η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)
Note: The calculation must be done for the minimum input voltage which is possible to have in boost mode

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to choose an inductor with a saturation current 20% higher than the value calculated from Equation 6. The following inductors are recommended for use:

Table 3. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	Isat/DCR
1 µH	TOKO 1286AS-H-1R0M	2x1.6x1.2	2.5A/78mΩ
1.5µH	TOKO, 1286AS-H-1R5M	2x1.6x1.2	4.4A/ 14.40mΩ
1.5µH	TOKO, 1269AS-H-1R5M	2.5x2x1	2.1A/108mΩ
2.2µH	TOKO D1286AS-H-2R2M	2x1.6x1.2	1.6A/192mΩ

The inductor value also affects the stability of the feedback loop. In particular the boost transfer function exhibits a right half-plane zero, whose frequency is inverse proportional to the inductor value and the load current. This means the higher the value of inductance and load current, the more possibilities that the right half plane zero is moved to a lower frequency. This could degrade the phase margin of the feedback loop. It is recommended to choose the inductor's value in order to have the frequency of the right half plane zero >400kHz. The frequency of the RHPZ is calculated using Equation 7.

$$f_{RHPZ} = \frac{(1 - D)^2 \times Vout}{2\pi \times Iout \times L} \tag{7}$$

With,

D =Duty Cycle in Boost mode

Note: The calculation must be done for the minimum input voltage which is possible to have in boost mode

If the operating conditions results in a frequency of the RHPZ of less than 400kHz, then more output capacitance should be added to reduce the cross over frequency.

Capacitor selection

Input Capacitor

At least a 10µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

Output Capacitor

For the output capacitor, use of a small X5R or X7R ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC is recommended. The recommended typical output capacitor value is 10µF with a variance as outlined in Output Filter Selection.

There is also no upper limit for the output capacitance value. Larger capacitors will cause lower output voltage ripple as well as lower output voltage drop during load transients.

LAYOUT CONSIDERATIONS

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC.

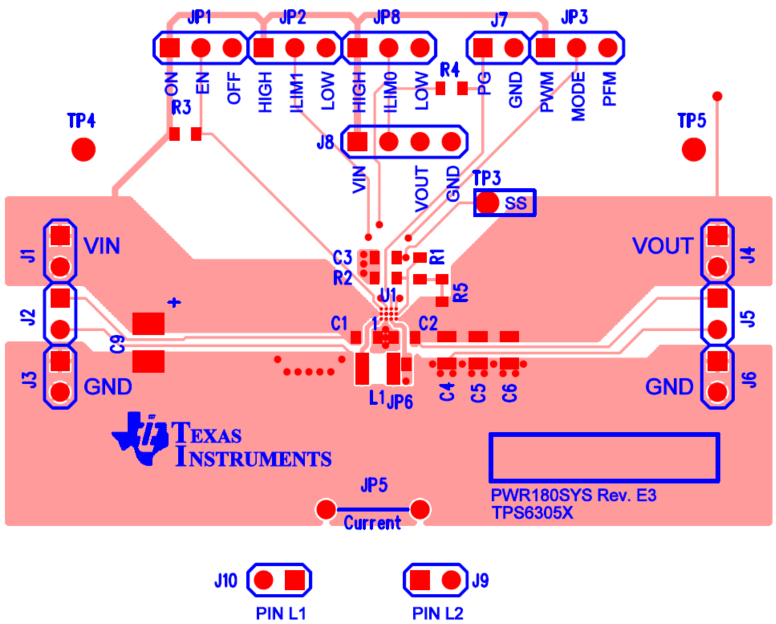

Figure 29. PCB Layout Suggestion

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note (SZZA017), and IC Package Thermal Metrics Application Note (SPRA953).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63050YFFR	PREVIEW	DSBGA	YFF	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	63050	
TPS63050YFFT	PREVIEW	DSBGA	YFF	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	63050	
TPS63051YFFR	ACTIVE	DSBGA	YFF	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	63051	Samples
TPS63051YFFT	ACTIVE	DSBGA	YFF	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	63051	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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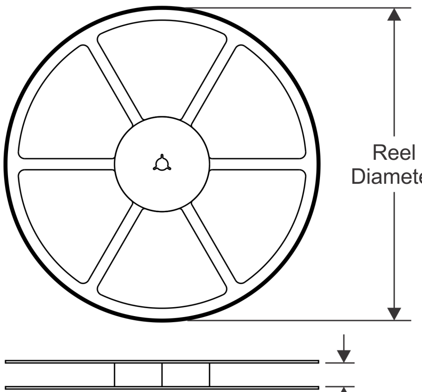
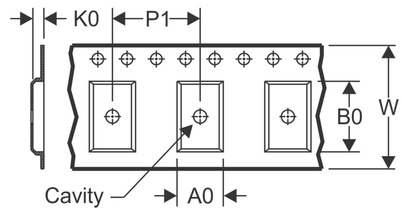
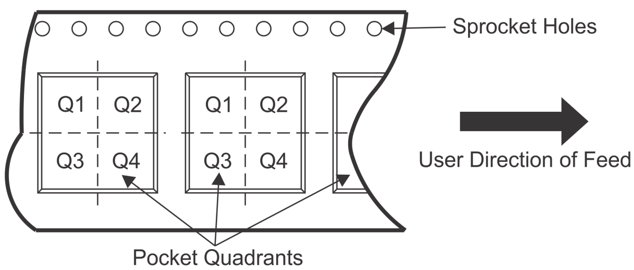


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

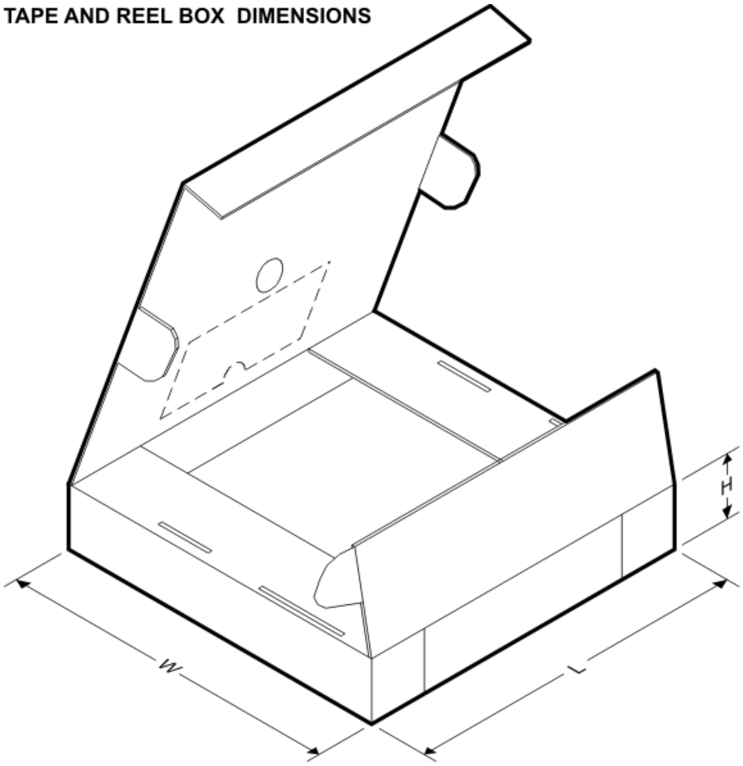
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63051YFFR	DSBGA	YFF	12	3000	180.0	8.4	1.39	1.79	0.7	4.0	8.0	Q1
TPS63051YFFT	DSBGA	YFF	12	250	180.0	8.4	1.39	1.79	0.7	4.0	8.0	Q1

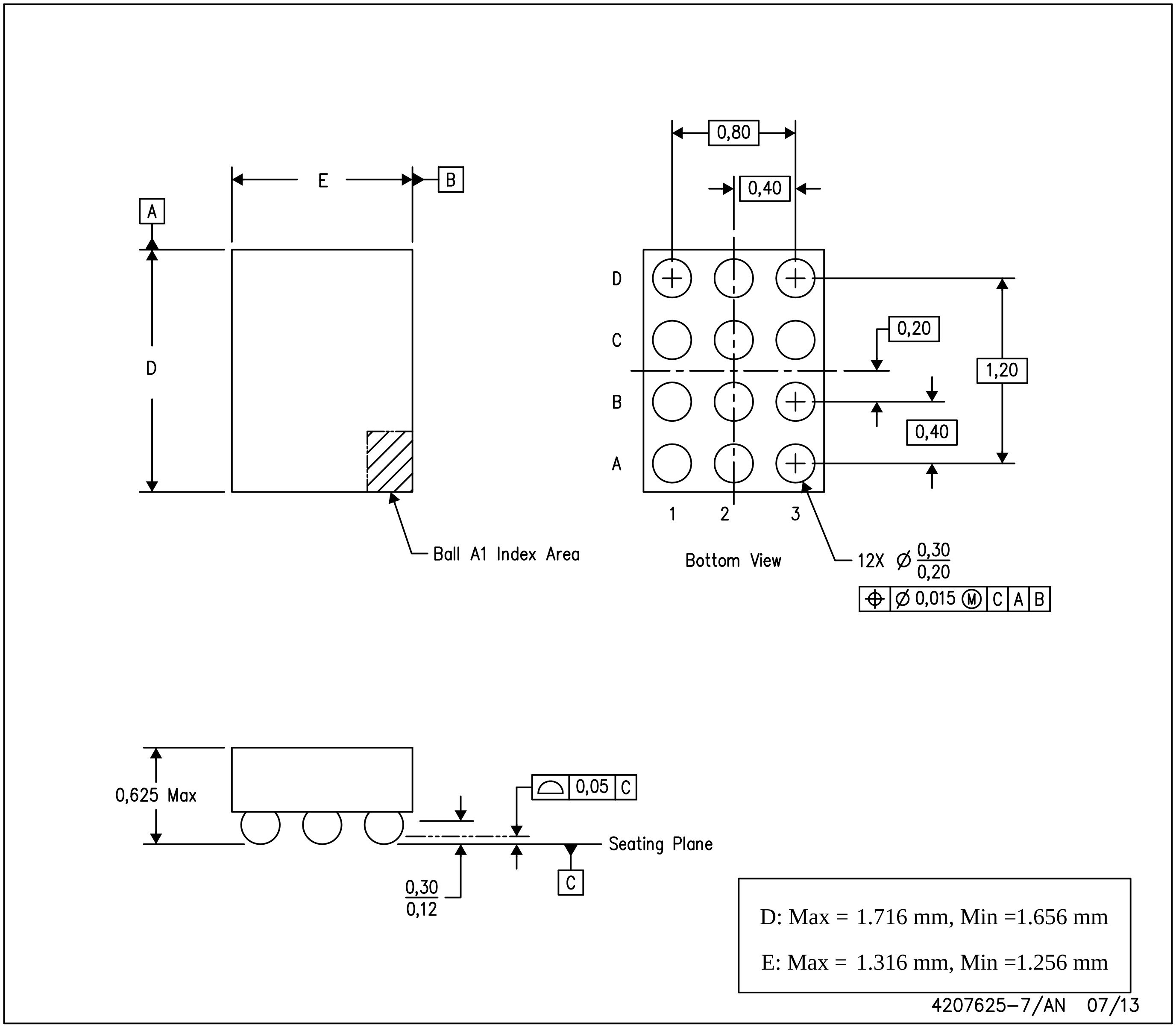
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63051YFFR	DSBGA	YFF	12	3000	182.0	182.0	17.0
TPS63051YFFT	DSBGA	YFF	12	250	182.0	182.0	17.0

YFF (R–XBGA–N12) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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