Low Noise, High-Bandwidth PSRR Low-Dropout 150-mA Linear Regulator

Check for Samples: TPS71750-Q1 , TPS71709-Q1, TPS71745-Q1

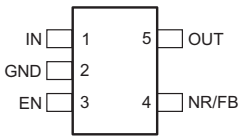
FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified with the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device HBM ESD Classification Level C4B**
- **150-mA Low-Dropout Regulator with Enable**
- **Low I_Q: 45 µA (typical)**
- **Available in Multiple Output Versions:**
  - **Fixed Output with Voltages from 0.9 V to 5 V Using Innovative Factory EEPROM Programming**
  - **Adjustable Output Voltage from 0.9 V to 6.2 V**
- **Ultra-High PSRR:**
  - **70 dB at 1 kHz, 67 dB at 100 kHz and 45 dB at 1 MHz**
- **Low Noise: 30-µV typical (100 Hz to 100 kHz)**
- **Stable with a 1-µF Ceramic Capacitor**
- **Excellent Load/Line Transient Response**
- **3% Overall Accuracy (Over Load, Line, or Temp)**
- **Overcurrent and Overtemperature Protection**
- **Very Low Dropout: 170-mV Typical at 150 mA**
- **Small SC70-5, 2-mm x 2-mm SON-6, and 1.5-mm × 1.5-mm SON-6 Packages**

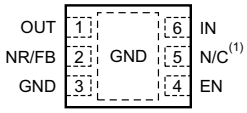
APPLICATIONS

- **Wireless LAN, *Bluetooth*®**

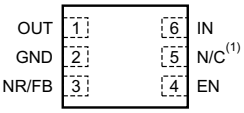
TPS717xx-Q1 DCK
SC70-5 PACKAGE
(TOP VIEW)



TPS717xx-Q1 DRV
2-mm x 2-mm SON
(TOP VIEW)



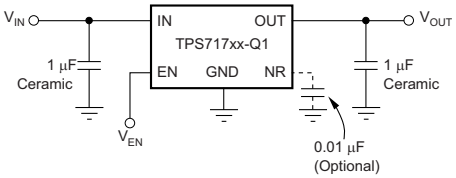
TPS717xx-Q1 DSE
1.5-mm x 1.5-mm SON
(TOP VIEW)



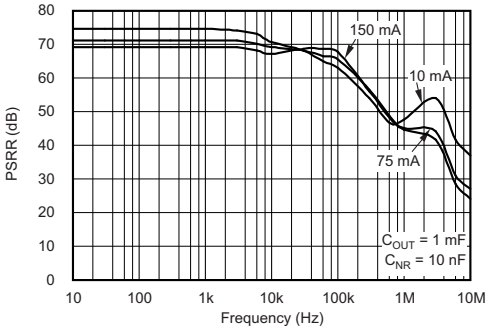
NOTE: (1) N/C = Not connected.

DESCRIPTION

The TPS717xx-Q1 family of low-dropout (LDO), low-power linear regulators offers very high power supply rejection (PSRR) while maintaining very low 45-µA ground current in an ultra-small, five-pin SC70 package. The family uses an advanced BiCMOS process and a PMOSFET pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance. The TPS717xx-Q1 is stable with a 1-µF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations. It is fully specified from T_A = –40°C to 125°C and is offered in a small SC70-5 package, a 2-mm × 2-mm SON-6 package with a thermal pad, and a 1.5-mm × 1.5-mm SON package, which are ideal for small form factor portable equipment such as wireless handsets and PDAs.



Typical Application Circuit for Fixed Voltage Versions



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted). All voltages are with respect to GND.

PARAMETER		VALUE		UNIT
		MIN	MAX	
Input voltage range, V_{IN}		–0.3	7	V
Feedback input voltage range, V_{FB}, V_{NR}		–0.3	3.6	V
Enable voltage range, V_{EN}		–0.3	V_{IN} + 0.3 V(2)	V
Output voltage range, V_{OUT}		–0.3	7	V
Maximum output current, I_{OUT}		Internally limited		
Continuous total power dissipation, P_{DISS}		See THERMAL INFORMATION Table		
Ambient temperature range, T_A		–40	125	°C
Junction temperature range, T_J		–55	150	°C
Storage junction temperature range, T_{STG}		–55	150	°C
ESD Ratings	Human body model (HBM) AEC-Q100 Classification Level H2		2	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C4B		750	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) V_{EN} absolute maximum rating is V_{IN} + 0.3 V or 7 V, whichever is greater.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS717xx-Q1			UNIT
		DCK (5 PINS)	DRV (6 PINS)	DSE (6 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	279.2	71.1	190.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	57.5	96.5	94.9	
θ_{JB}	Junction-to-board thermal resistance	74.1	40.5	149.3	
ψ_{JT}	Junction-to-top characterization parameter	0.8	2.7	6.4	
ψ_{JB}	Junction-to-board characterization parameter	73.1	40.9	152.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	10.7	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_A = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.5 V, whichever is greater; I_{OUT} = 0.5 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{NR} = 0.01 µF, unless otherwise noted. For TPS71701-Q1, V_{OUT} = 2.8 V. Typical values are at T_A = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			2.5		6.5	V
V_{FB}	Internal reference (TPS71701-Q1)			0.790	0.800	0.810	V
V_{OUT}	Output voltage range (TPS717xx-Q1)			0.9		5	V
	Output voltage range (TPS71701-Q1)			0.9		6.5 – V_{DO}	V
V_{OUT}	Output accuracy	Nominal	T_A = 25°C		±2.5		mV
	Output accuracy (V_{OUT} < 1 V)	Over V_{IN}, I_{OUT}, Temp(2)	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.5 V 0 mA ≤ I_{OUT} ≤ 150 mA	–30		30	mV
	Output accuracy (V_{OUT} ≥ 1 V)	Over V_{IN}, I_{OUT}, Temp(2)	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.5 V 0 mA ≤ I_{OUT} ≤ 150 mA	–3		3	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation (1)		$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 6.5 V, I_{OUT} = 5 mA		125		µV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation		0 mA ≤ I_{OUT} ≤ 150 mA		120		µV/mA
V_{DO}	Dropout voltage(3) (V_{IN} = $V_{OUT(NOM)}$ – 0.1 V)		I_{OUT} = 150 mA		170	300	mV
I_{CL} (Fixed)	Output current limit (fixed output)		V_{OUT} = 0.9 × $V_{OUT(NOM)}$	200	325	575	mA
I_{CL} (Adjustable)	Output current limit (TPS71701-Q1)		V_{OUT} = 0.9 × $V_{OUT(NOM)}$	200	325	575	mA
I_{GND}	Ground pin current		I_{OUT} = 0.1 mA		45	80	µA
			I_{OUT} = 150 mA		100		µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4 V, 2.5 V ≤ V_{IN} < 4.5 V, T_A = –40°C to 125°C		0.20	1.5	µA
			V_{EN} ≤ 0.4 V, 4.5 V ≤ V_{IN} ≤ 6.5 V, T_A = –40°C to 125°C		0.90		µA
I_{FB}	Feedback pin current (TPS71701-Q1)				0.02	1	µA
PSRR	Power-supply rejection ratio V_{IN} = 3.8 V, V_{OUT} = 2.8 V, I_{OUT} = 150 mA		f = 100 Hz		70		dB
			f = 1 kHz		70		dB
			f = 10 kHz		67		dB
			f = 100 kHz		67		dB
			f = 1 MHz		45		dB
V_N	Output noise voltage BW = 100 Hz to 100 kHz, V_{IN} = 3.8 V, V_{OUT} = 2.8 V, I_{OUT} = 10 mA		C_{NR} = none (fixed output, TPS71701-Q1)		95 × V_{OUT}		μV_{RMS}
			C_{NR} = 0.001 µF		25 × V_{OUT}		μV_{RMS}
			C_{NR} = 0.01 µF		12.5 × V_{OUT}		μV_{RMS}
			C_{NR} = 0.1 µF		11.5 × V_{OUT}		μV_{RMS}
T_{STR}	Startup time V_{OUT} = 90% $V_{OUT(NOM)}$, R_L = 19 Ω, C_{OUT} = 1 µF		0.9 V ≤ V_{OUT} ≤ 1.6 V, C_{NR} = 0.001 µF		0.700		ms
			1.6 V < V_{OUT} < V_{MAX}, C_{NR} = 0.01 µF		0.160		ms
$V_{EN(HI)}$	Enable high (enabled)		V_{IN} ≤ 5.5 V	1.2		6.5(4)	V
			5.5 V < V_{IN} ≤ 6.5 V	1.25		6.5	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled		EN = 6.5 V		0.02	1	µA
UVLO	Under-voltage lockout		V_{IN} rising	2.41	2.45	2.49	V
	Hysteresis		V_{IN} falling		150		mV
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		160		°C
			Reset, temperature decreasing		140		°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.5 V, whichever is greater.
(2) Does not include external resistor tolerances.
(3) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ < 2.6 V because minimum V_{IN} = 2.5 V.
(4) Maximum $V_{EN(HI)}$ = V_{IN} + 0.3 or 6.5 V, whichever is smaller.

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DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAMS

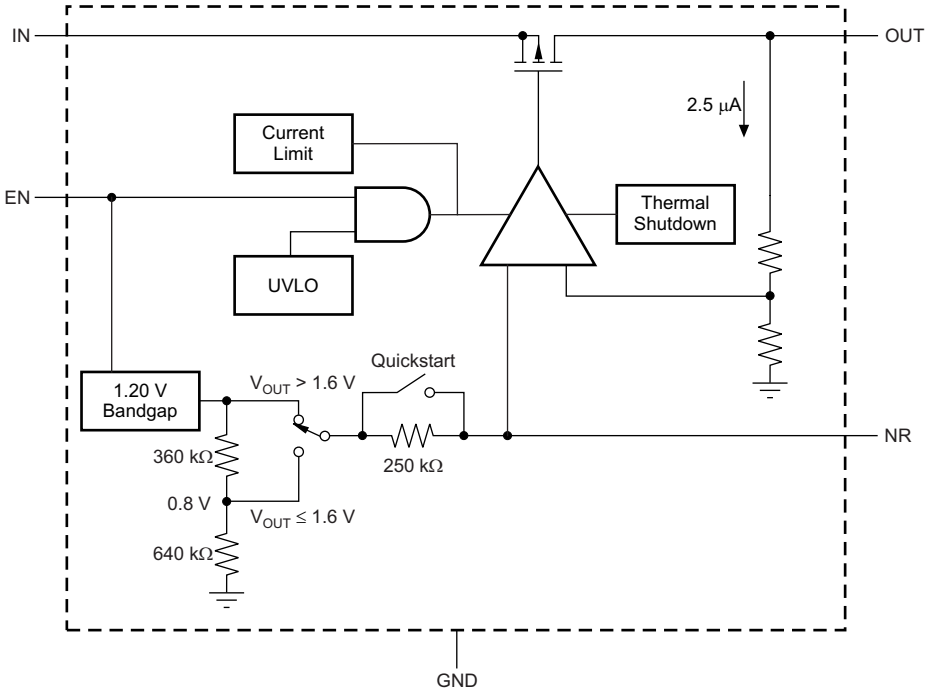

Figure 1. Fixed Voltage Versions

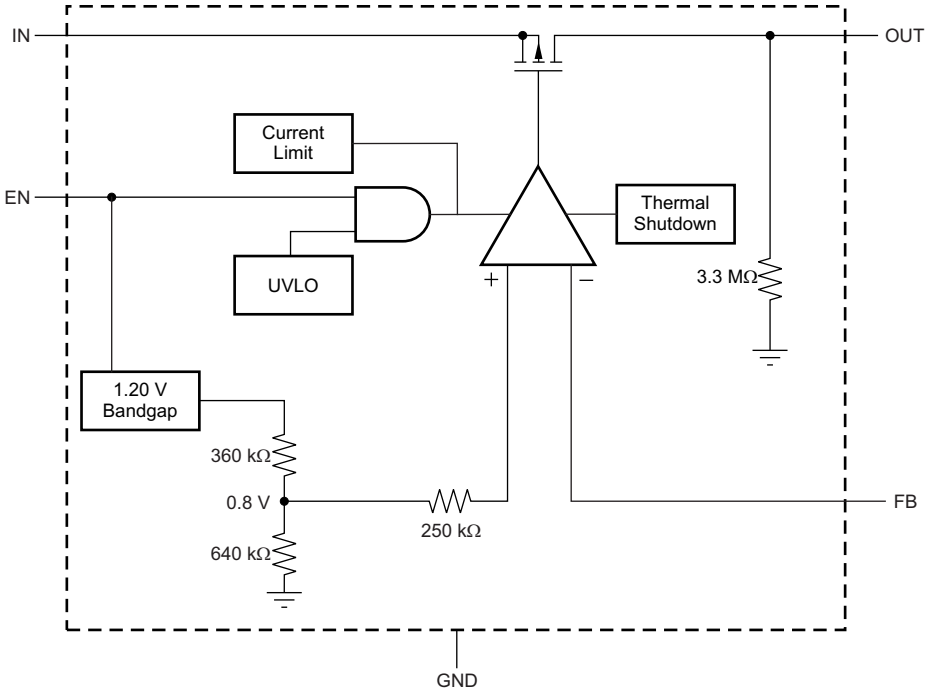

Figure 2. Adjustable Voltage Version

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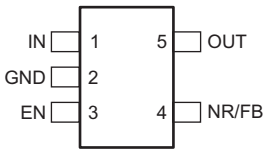
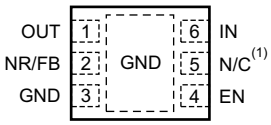
PIN CONFIGURATIONS

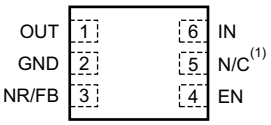
TPS717xx-Q1 DCK
SC70-5 PACKAGE
(TOP VIEW)



TPS717xx-Q1 DRV
2-mm x 2-mm SON
(TOP VIEW)



TPS717xx-Q1 DSE
1.5-mm x 1.5-mm SON
(TOP VIEW)



NOTE: (1) N/C = Not connected.

Table 1. PIN DESCRIPTIONS

TPS717xx-Q1				DESCRIPTION
NAME	SC70 (DCK)	2 × 2 SON (DRV)	1.5 × 1.5 SON (DSE)	
IN	1	6	6	Input to the device.
GND	2	3	2	Ground.
EN	3	4	4	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into standby mode, thereby reducing operating current.
NR	4	2	3	Fixed voltage versions only. An external capacitor connected to this terminal bypasses noise generated by the internal bandgap, lowering output noise.
FB	4	2	3	Adjustable voltage version only. The voltage at this pin is fed to the error amplifier. A resistor divider from OUT to FB sets the output voltage when in regulation.
OUT	5	1	1	This is the regulated output voltage. A small capacitor is needed from this pin to ground to assure stability; a 1-µF ceramic capacitor is adequate.
NC	–	5	5	Not connected. This pin can be tied to ground to improve thermal dissipation.

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TYPICAL CHARACTERISTICS

Over operating temperature range (T_A = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.5 V, whichever is greater; I_{OUT} = 0.5 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{NR} = 0.01 µF, unless otherwise noted. For TPS71701-Q1, V_{OUT} = 2.8 V.
Typical values are at T_A = 25°C.

LOAD REGULATION

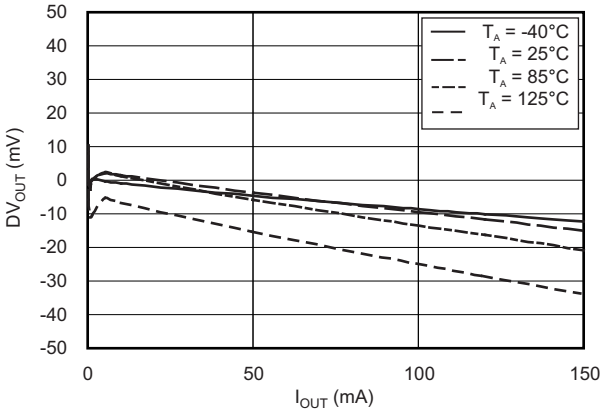

Figure 3.

LOAD REGULATION UNDER LIGHT LOADS

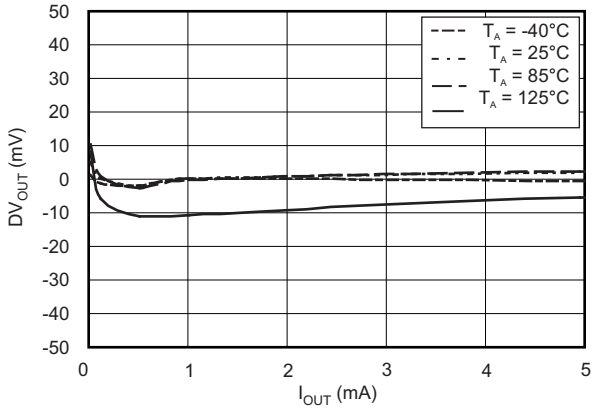

Figure 4.

LINE REGULATION
I_{OUT} = 5mA

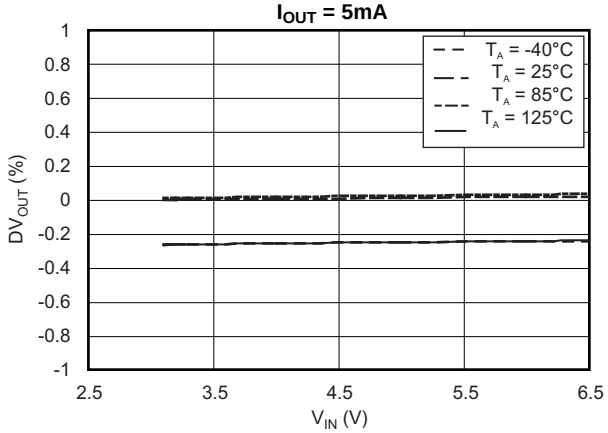

Figure 5.

LINE REGULATION
I_{OUT} = 150mA

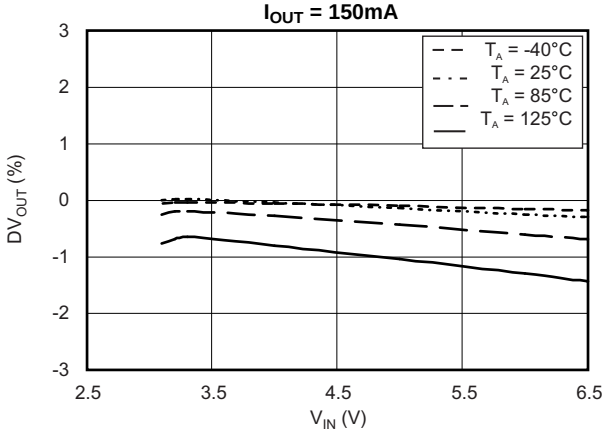

Figure 6.

OUTPUT VOLTAGE
vs
TEMPERATURE

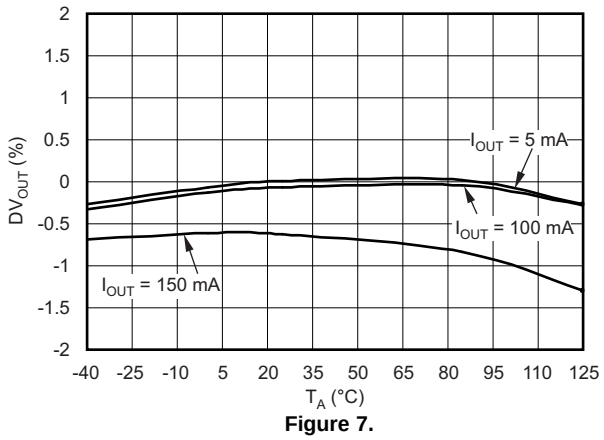

Figure 7.

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

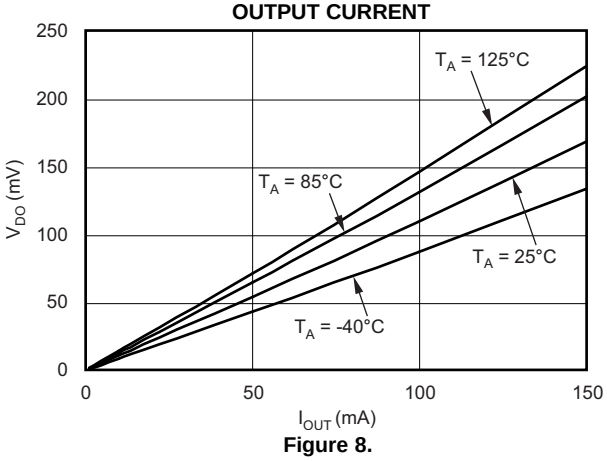

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_A = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.5 V, whichever is greater; I_{OUT} = 0.5 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{NR} = 0.01 µF, unless otherwise noted. For TPS71701-Q1, V_{OUT} = 2.8 V.

Typical values are at T_A = 25°C.

DROPOUT VOLTAGE vs TEMPERATURE

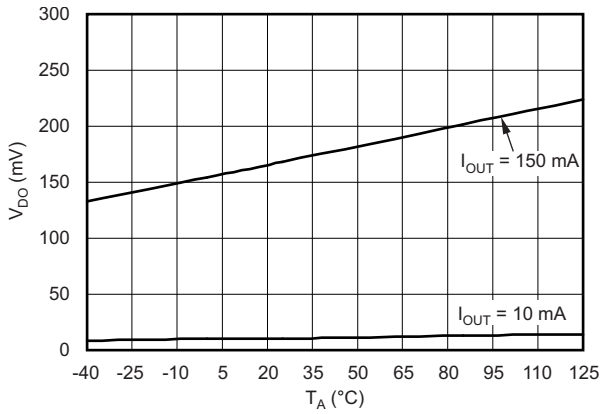

Figure 9.

GROUND PIN CURRENT vs INPUT VOLTAGE

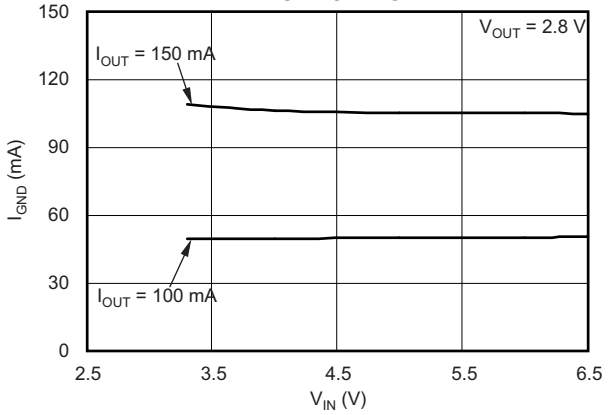

Figure 10.

GROUND PIN CURRENT vs OUTPUT CURRENT

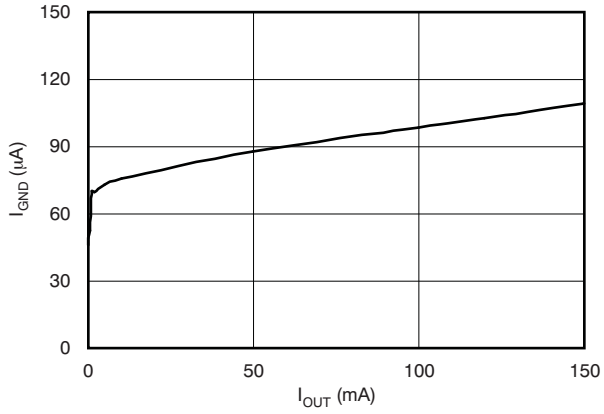

Figure 11.

GROUND PIN CURRENT vs TEMPERATURE (ENABLED)

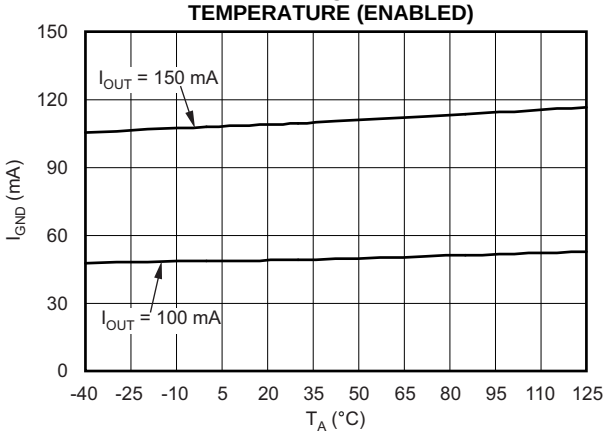

Figure 12.

GROUND PIN CURRENT vs TEMPERATURE (DISABLED)

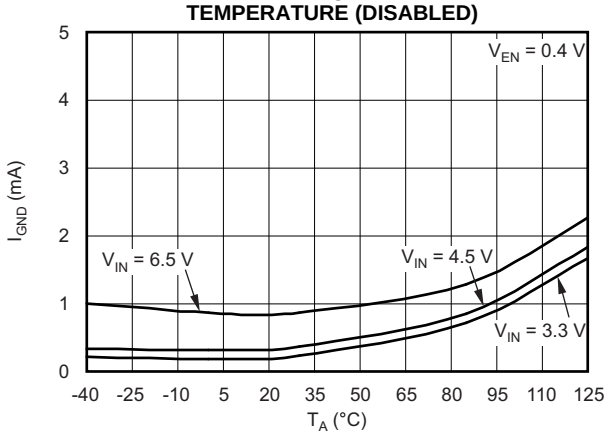

Figure 13.

CURRENT LIMIT vs INPUT VOLTAGE

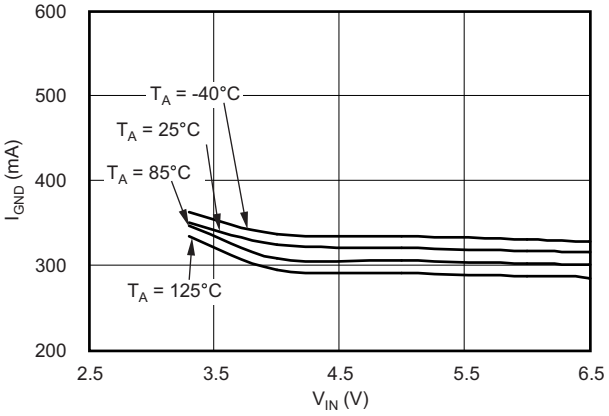

Figure 14.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_A = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.5 V, whichever is greater; I_{OUT} = 0.5 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{NR} = 0.01 µF, unless otherwise noted. For TPS71701-Q1, V_{OUT} = 2.8 V.

Typical values are at T_A = 25°C.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 1 V)

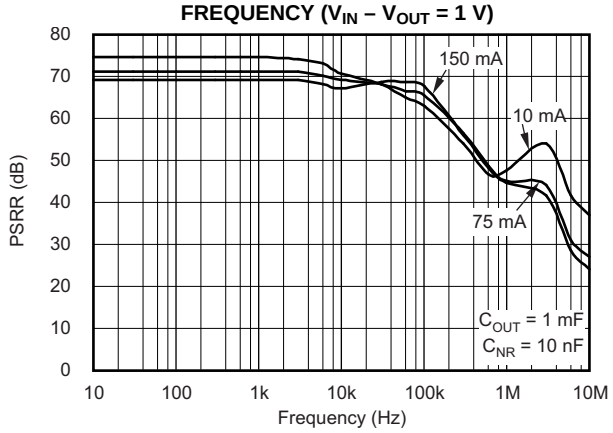

Figure 15.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.5 V)

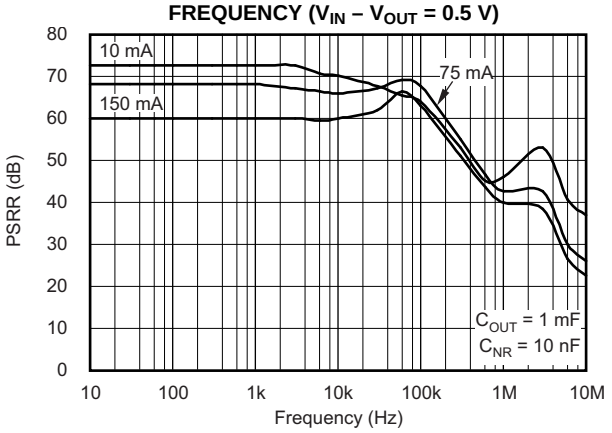

Figure 16.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.25 V)

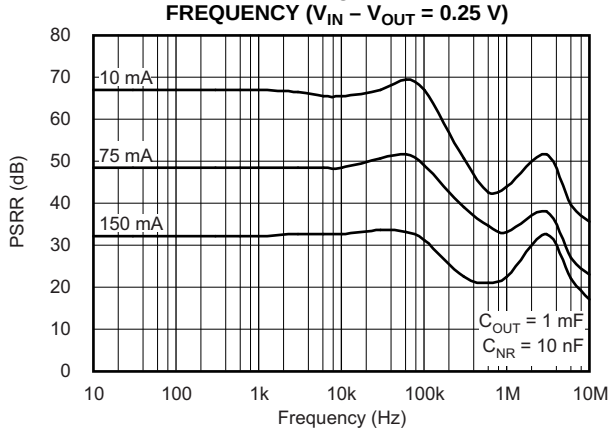

Figure 17.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 1 V)

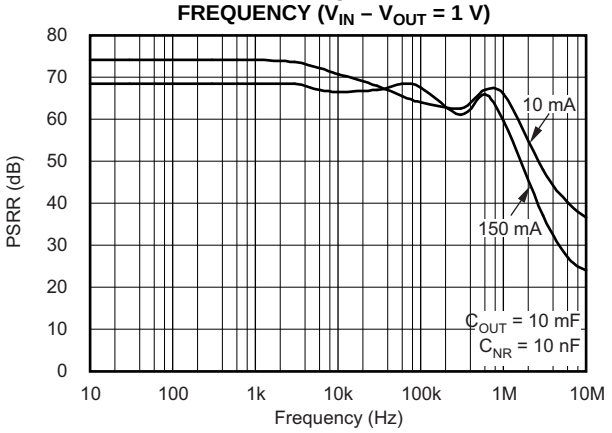

Figure 18.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.25 V)

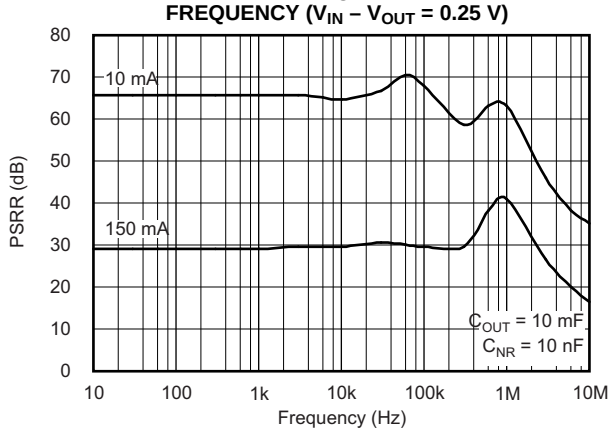

Figure 19.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 1 V)

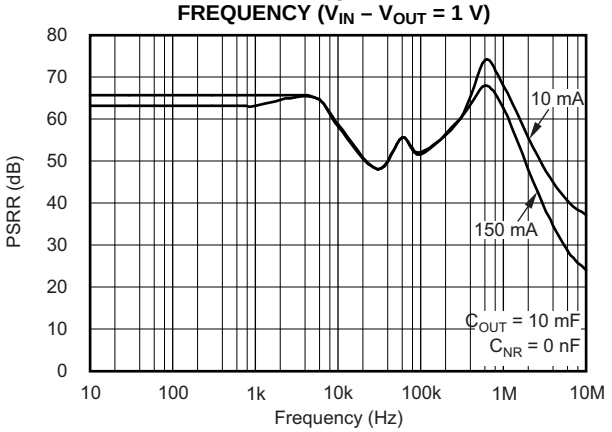

Figure 20.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_A = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.5 V, whichever is greater; I_{OUT} = 0.5 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{NR} = 0.01 µF, unless otherwise noted. For TPS71701-Q1, V_{OUT} = 2.8 V.

Typical values are at T_A = 25°C.

POWER-SUPPLY RIPPLE REJECTION vs (V_{IN} – V_{OUT})

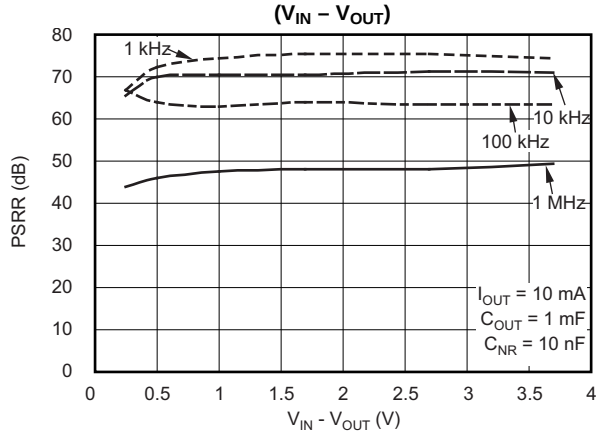

Figure 21.

POWER-SUPPLY RIPPLE REJECTION vs (V_{IN} – V_{OUT})

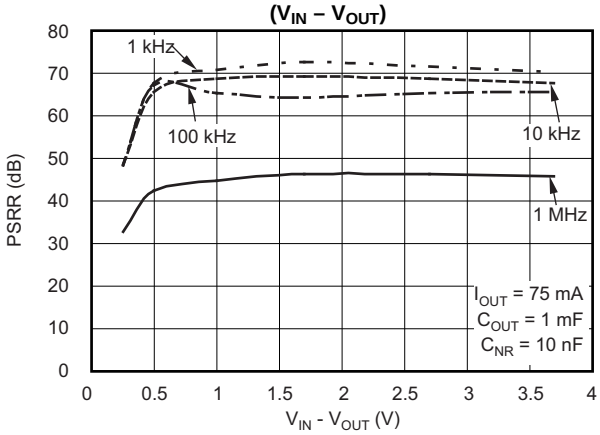

Figure 22.

POWER-SUPPLY RIPPLE REJECTION vs (V_{IN} – V_{OUT})

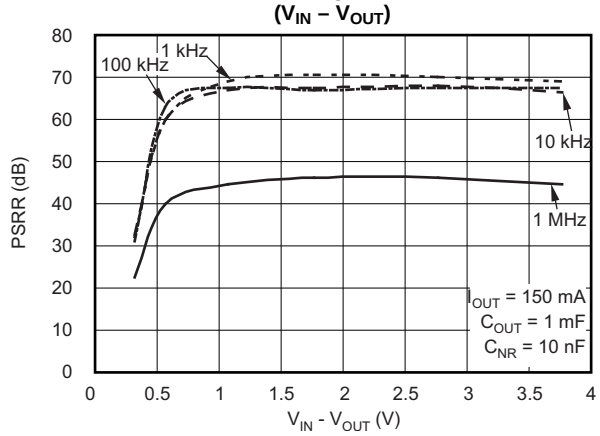

Figure 23.

OUTPUT SPECTRAL NOISE DENSITY vs OUTPUT CURRENT

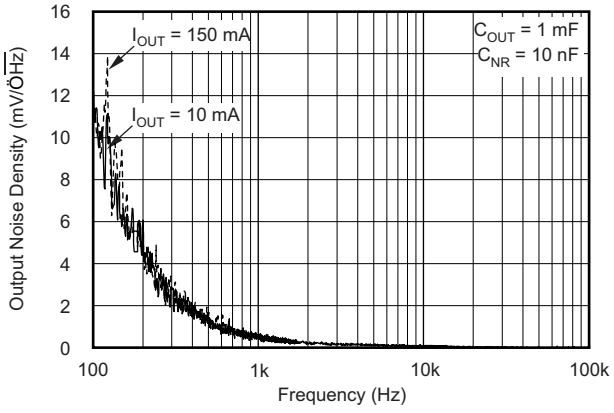

Figure 24.

OUTPUT SPECTRAL NOISE DENSITY vs OUTPUT CAPACITANCE

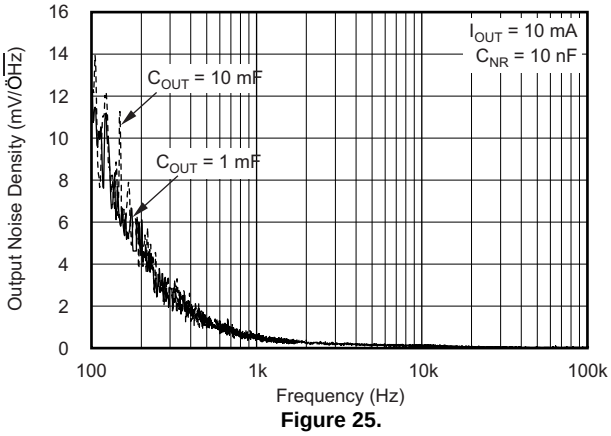

Figure 25.

OUTPUT SPECTRAL NOISE DENSITY vs NOISE REDUCTION

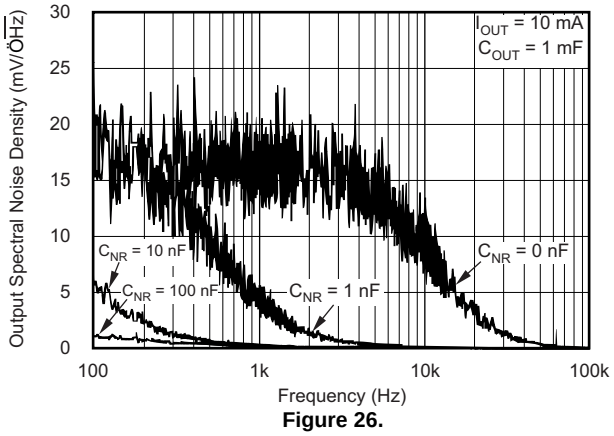

Figure 26.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_A = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.5 V, whichever is greater; I_{OUT} = 0.5 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{NR} = 0.01 µF, unless otherwise noted. For TPS71701-Q1, V_{OUT} = 2.8 V.

Typical values are at T_A = 25°C.

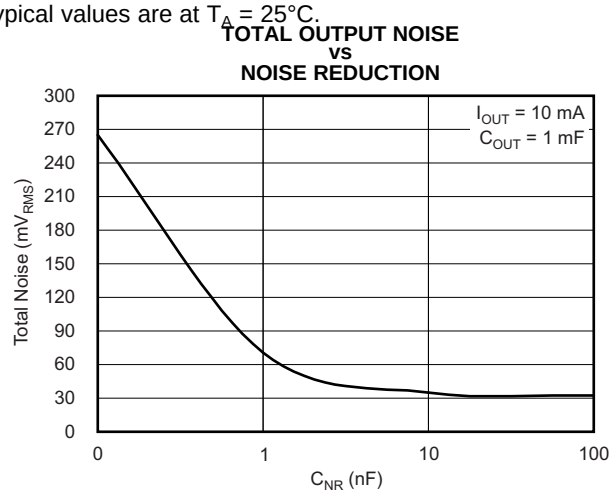

Figure 27.

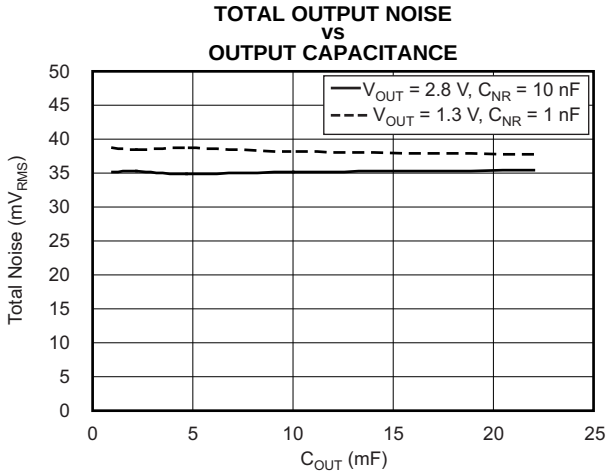

Figure 28.

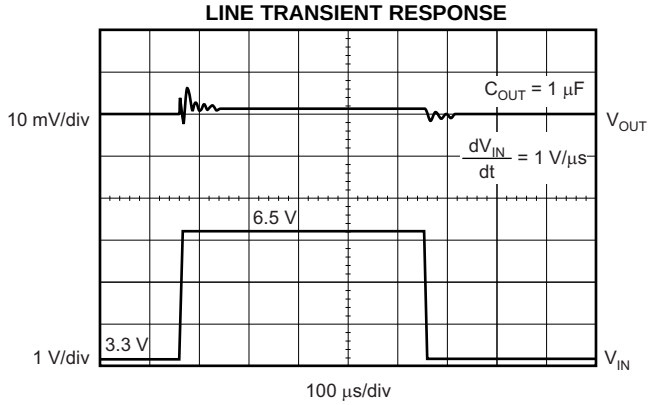

Figure 29.

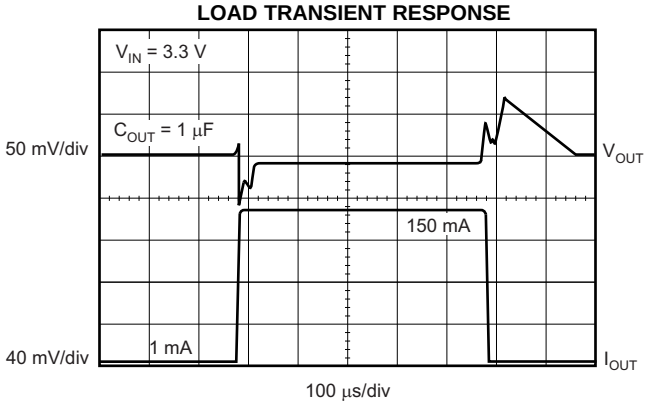

Figure 30.

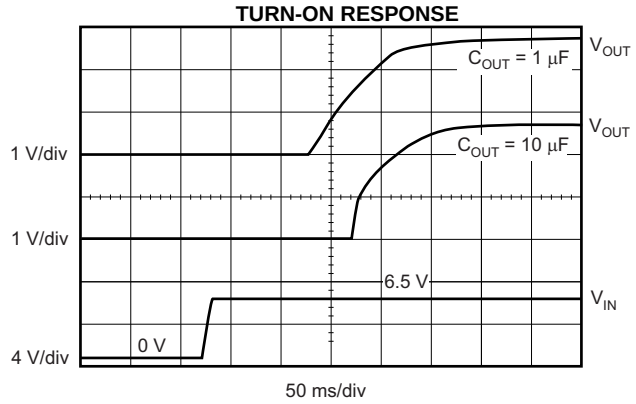

Figure 31.

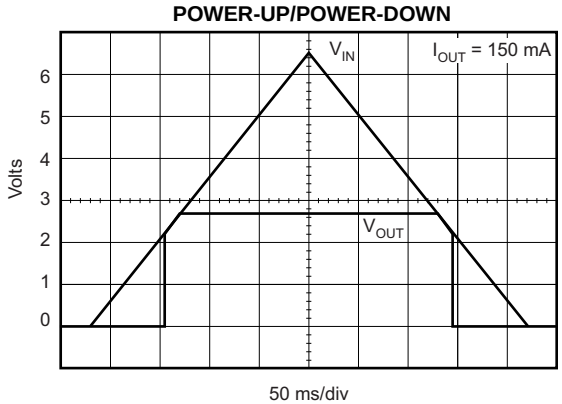

Figure 32.

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APPLICATION INFORMATION

The TPS717xx-Q1 belongs to a family of new generation LDO regulators that use innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR (up to 1 MHz) at very low headroom (V_{IN} – V_{OUT}). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the bandgap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor. These features, combined with low noise, enable, low ground pin current, and ultra-small packaging, make this part ideal for portable applications. This family of regulators offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from –40°C to 125°C.

Figure 33 shows the basic circuit connections for the fixed voltage options. Figure 34 gives the connections for the adjustable output version (TPS71701-Q1). **Note that the NR pin is not available on the adjustable version**.

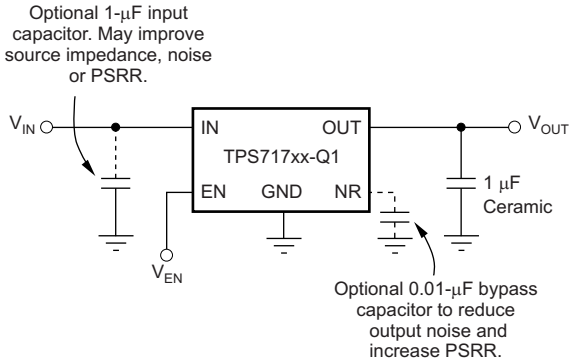

Figure 33. Typical Application Circuit (Fixed Voltage Versions)

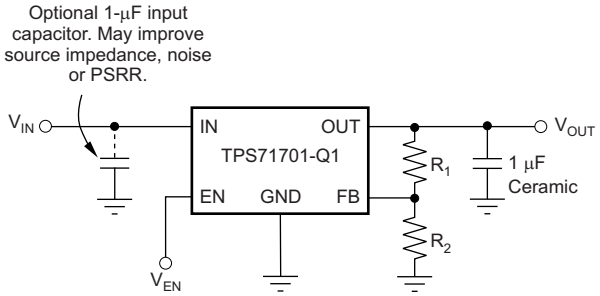

Figure 34. Typical Application Circuit (Adjustable Voltage Version)

For the adjustable version (TPS71701-Q1), the NR pin is replaced with a feedback (FB) pin. The voltage on this pin sets the output voltage and is determined by the values of R_1 and R_2. The values of R_1 and R_2 can be calculated for any voltage using the formula given in Equation 1:

$$V_{OUT} = \frac{(R_1 + R_2)}{R_2} \times 0.800,\ R_2 \sim 320k\Omega \quad (1)$$

The value of R_2 directly impacts the stability of the device and should be chosen at approximately 160 kΩ or 320 kΩ. Sample resistor values for common output voltages are shown in Table 2.

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Table 2. Sample 1% Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
1	80.6 kΩ	324 kΩ
1.2	162 kΩ	324 kΩ
1.5	294 kΩ	332 kΩ
1.8	402 kΩ	324 kΩ
2.5	665 kΩ	316 kΩ
3.3	1.02 MΩ	324 kΩ
5	1.74 MΩ	332 kΩ

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor will counteract reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

The TPS717xx-Q1 is designed to be stable with standard ceramic capacitors of values 1 µF or larger. The X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be < 1 Ω.

The TPS717xx-Q1 implements an innovative internal compensation circuit that does not require a feedback capacitor across R_2 for stability. A feedback capacitor should not be used for this device.

Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor (C_{NR}) is used with the TPS717xx-Q1, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-µF (minimum) noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2.5 µA of divider current has the same noise performance as a fixed voltage version.

Equation 2 approximates the total noise referred to the feedback point (FB pin) when C_{NR} = 0.01 µF, total noise is approximately given by Equation 2:

$$V_N = 11.5 \frac{\mu V_{RMS}}{V} \times V_{OUT} \quad (2)$$

Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TPS717xx-Q1 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TPS717xx-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

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Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

Dropout Voltage

The TPS717xx-Q1 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} will approximately scale with output current because the PMOS device behaves like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 21 through Figure 23 in the Typical Characteristics section.

Startup

Fixed voltage versions of the TPS717xx-Q1 use a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR}, if present (see Functional Block Diagrams, Figure 1). This circuit allows the combination of very low output noise and fast start-up times. The NR pin is high impedance, so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, V_{IN} should be applied first, then the enable pin (EN) driven high. If EN is tied to IN, startup will be somewhat slower. Refer to Figure 31 in the Typical Characteristics section. The quick-start switch is closed for approximately 135 µs. To ensure that C_{NR} is fully charged during the quick-start time, a 0.01 µF or smaller capacitor should be used.

For output voltages below 1.6 V, a voltage divider on the bandgap reference voltage is employed to optimize output regulation performance for lower output voltages. This configuration results in an additional resistor in the quick-start path and combined with the noise reduction capacitor (C_{NR}) results in slower start-up times for output voltages below 1.6 V.

Equation 3 approximates the start-up time as a function of C_{NR} for output voltages below 1.6 V:

$$t_{START} = 160\mu s + \left(540 \frac{\mu s}{nF} \times C_{NR} nF\right)\mu s \quad (3)$$

Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot or undershoot magnitude but increases duration of the transient response.

Under-Voltage Lock-Out (UVLO)

The TPS717xx-Q1 utilizes an under-voltage lock-out circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it typically ignores undershoot transients on the input if they are less than 50-µs duration.

Minimum Load

The TPS717xx-Q1 is stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS717xx-Q1 employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

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Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS717xx-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS717xx-Q1 into thermal shutdown will degrade device reliability.

Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *THERMAL INFORMATION* table. Using heavier copper will increase the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Package Mounting

Solder pad footprint recommendations for the TPS717xx-Q1 are available from the Texas Instruments web site at www.ti.com.

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REVISION HISTORY

Changes from Original (September 2012) to Revision A **Page**

- Changed front page to two-column format. 1
- Added part number TPS71745-Q1. 1
- Changed C3B to C4B in Features. 1
- Removed Ordering Information table. 2
- Added Junction Temperature to Absolute Maximum Ratings table. 2
- Changed C3B to C4B in Absolute Maximum Ratings table. 2
- Changed Application Information section to one-column format. 11

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS71709QDSERQ1	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD	Samples
TPS71745QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHF	Samples
TPS71750QDSERQ1	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		AV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS71709-Q1, TPS71745-Q1, TPS71750-Q1 :

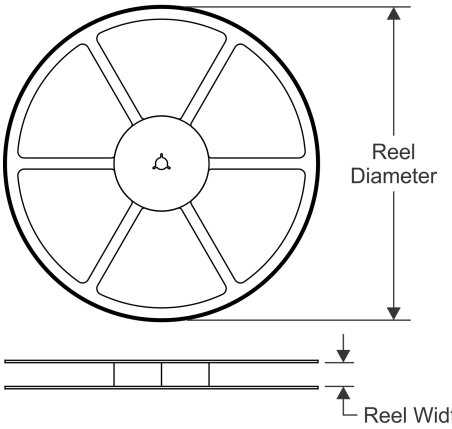
- Catalog: TPS71709, TPS71745, TPS71750

NOTE: Qualified Version Definitions:

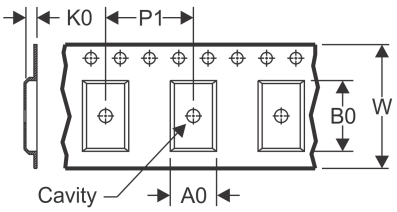
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

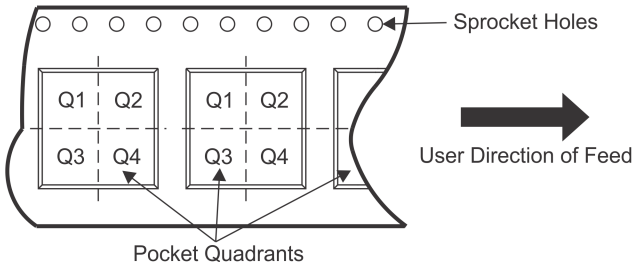


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

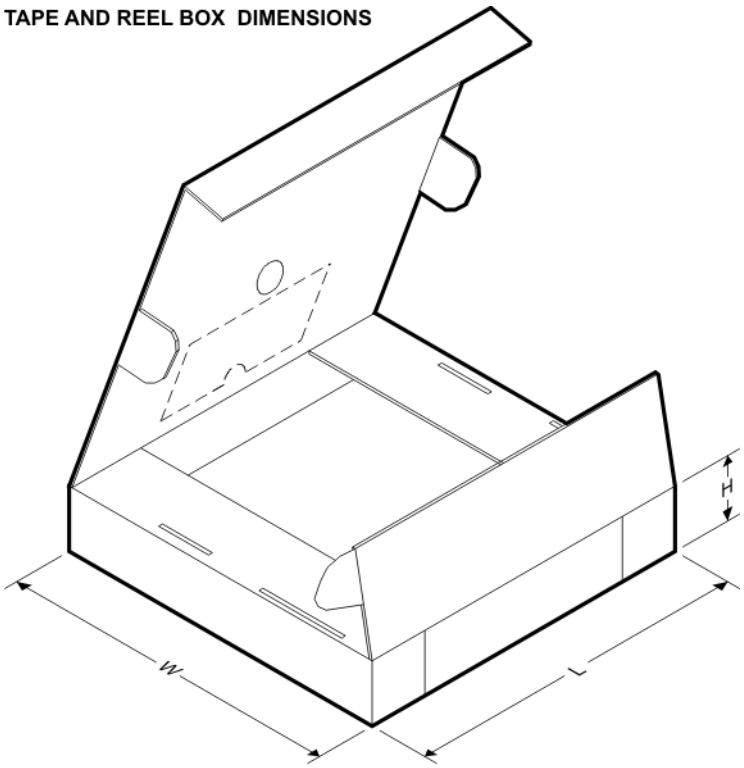
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS71709QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS71745QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71750QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

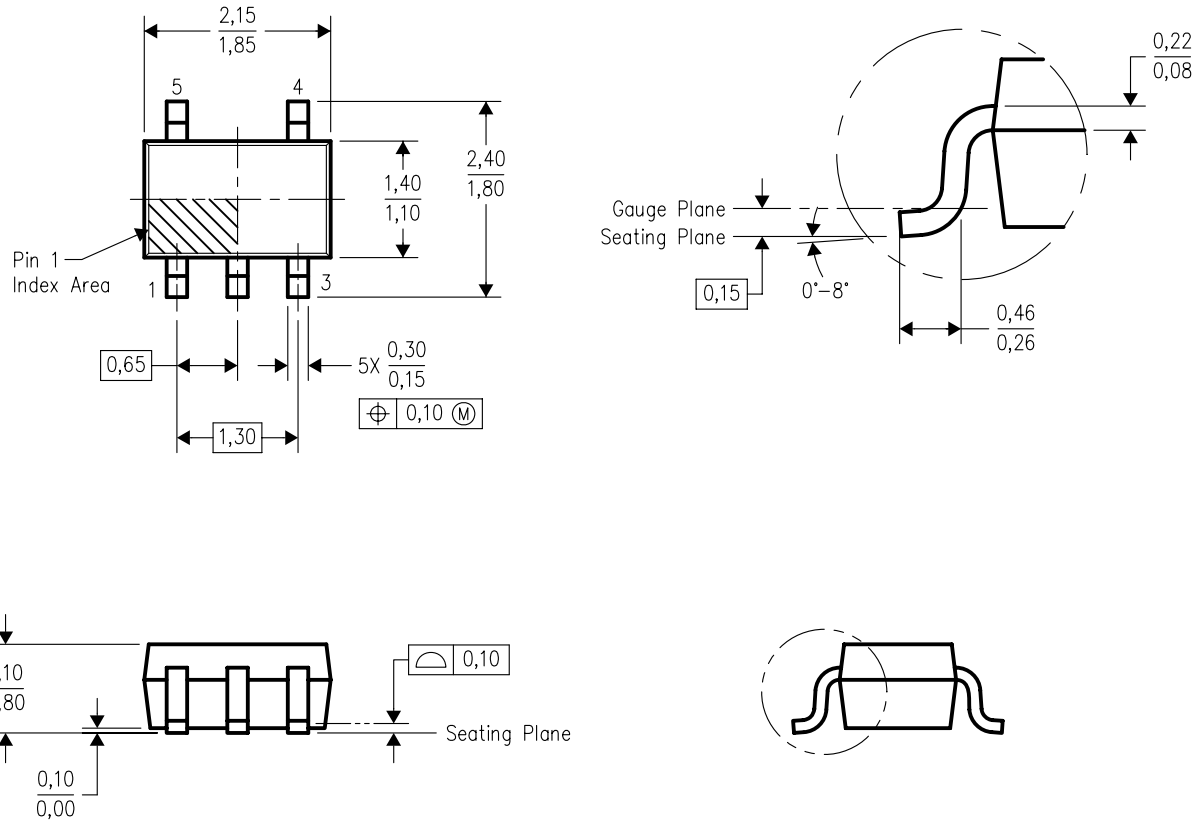
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS71709QDSERQ1	WSON	DSE	6	3000	203.0	203.0	35.0
TPS71745QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71750QDSERQ1	WSON	DSE	6	3000	203.0	203.0	35.0

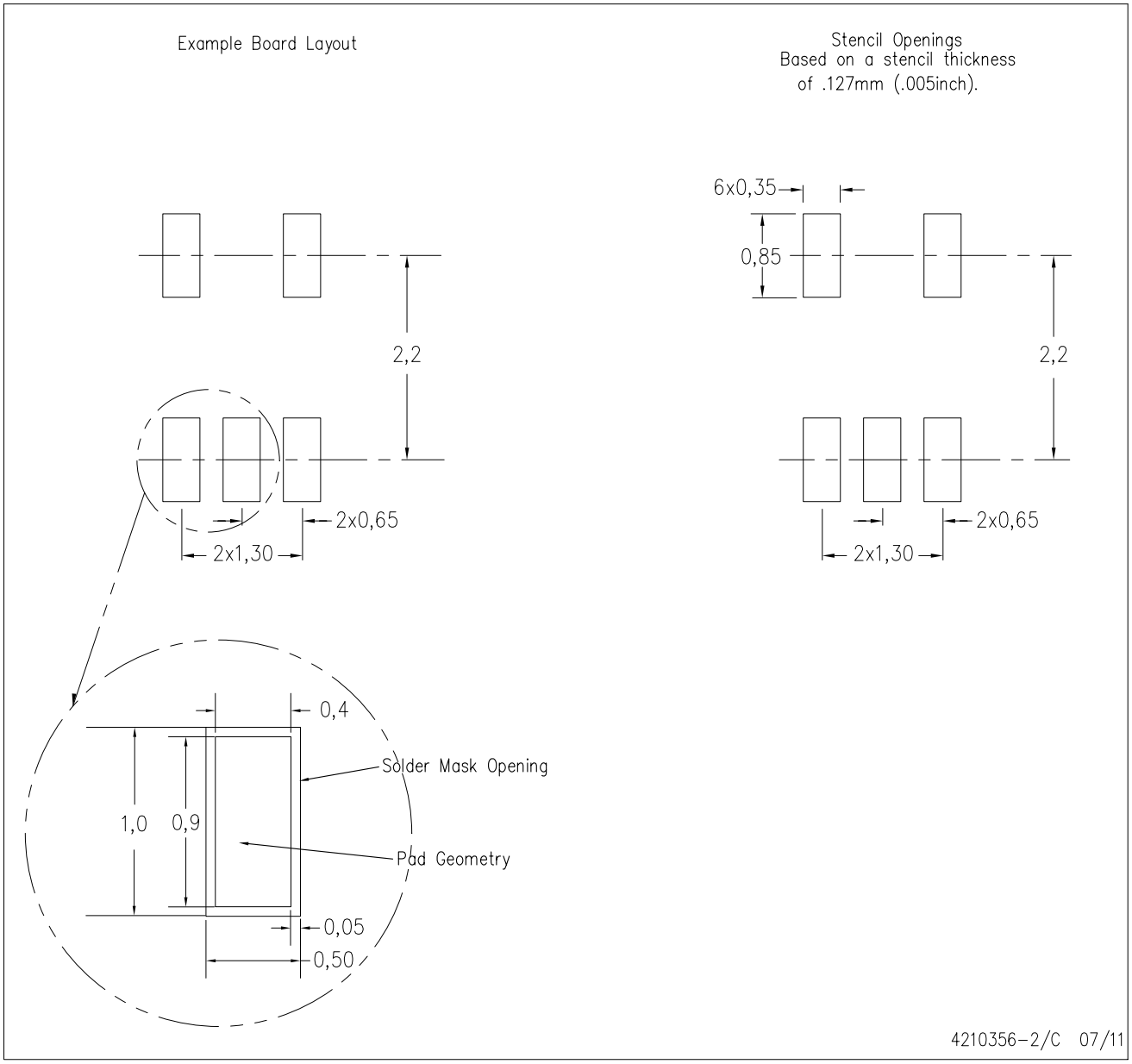
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

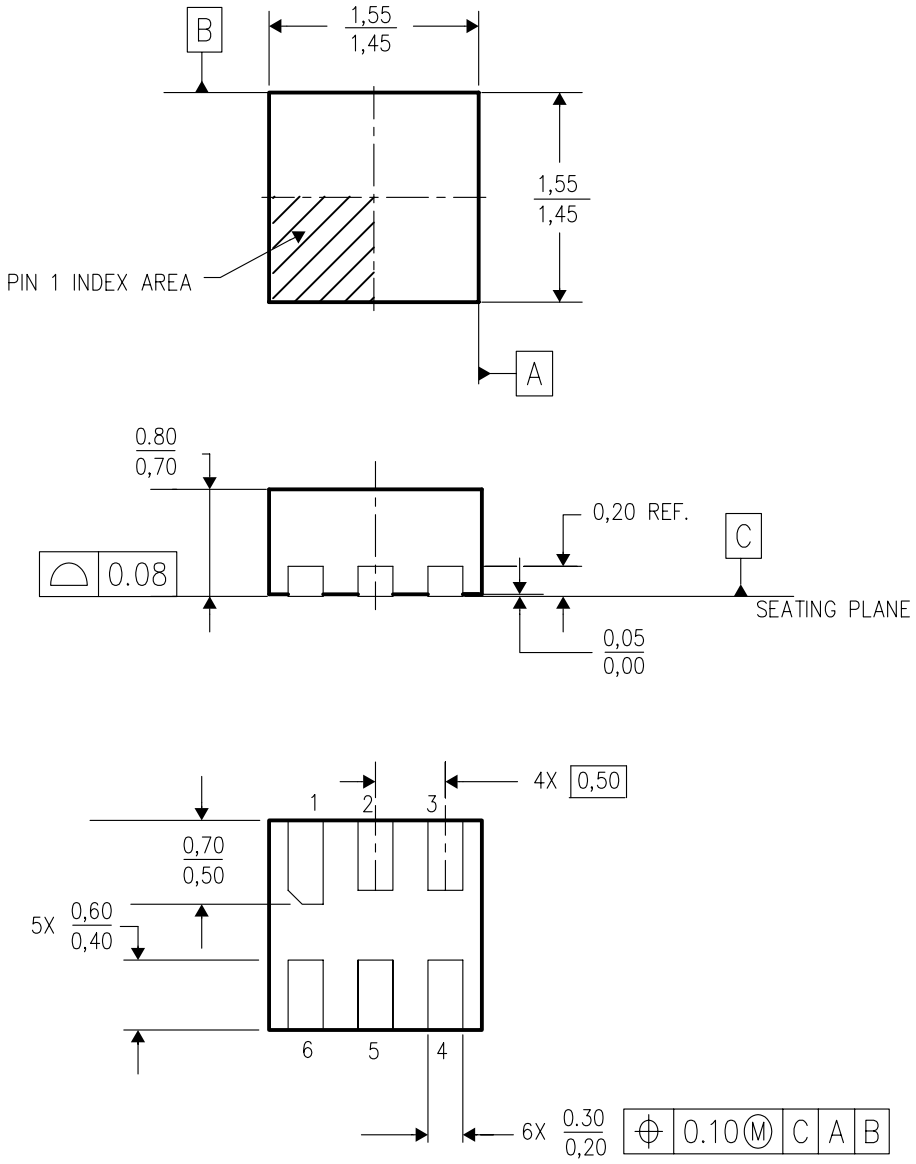
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



4207810/A 03/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

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