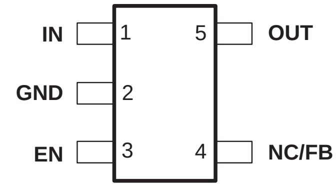
TPS76301-Q1, TPS76316-Q1, TPS76318-Q1, TPS76325-Q1, TPS76327-Q1 TPS76328-Q1, TPS76330-Q1, TPS76333-Q1, TPS76338-Q1, TPS76350-Q1 LOW-POWER 150-mA LOW-DROPOUT LINEAR REGULATORS

SGLS247A − JUNE 2004 − REVISED JUNE 2008

- **Qualified for Automotive Applications**
- **150-mA Low-Dropout Regulator**
- **Output Voltage: 5 V, 3.8 V, 3.3 V, 3 V, 2.8 V, 2.7 V, 2.5 V, 1.8 V, 1.6 V and Variable**
- **Dropout Voltage, Typically 300 mV at 150 mA**
- **Thermal Protection**
- **Overcurrent Limitation**
- **Less Than 2-μA Quiescent Current in Shutdown Mode**
- **−40°C to 125°C Operating Junction Temperature Range**
- **5-Pin SOT-23 (DBV) Package**

DBV PACKAGE
(TOP VIEW)



description

The TPS763xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, low-power operation, and miniaturized packaging. These regulators feature low dropout voltages and quiescent currents compared to conventional LDO regulators. Offered in a 5-terminal, small outline integrated-circuit SOT-23 package, the TPS763xx series devices are ideal for cost-sensitive designs and for applications where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual pnp pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is low—typically 300 mV at 150 mA of load current (TPS76333)—and is directly proportional to the load current. Since the PMOS pass element is a voltage-driven device, the quiescent current is low (140 μA maximum) and is stable over the entire range of output load current (0 mA to 150 mA). Intended for use in portable systems such as laptops and cellular phones, the low-dropout voltage feature and low-power operation result in a significant increase in system battery operating life.

The TPS763xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μA maximum at T_J = 25°C.The TPS763xx is offered in 1.6-V,1.8-V, 2.5-V, 2.7-V, 2.8-V, 3-V, 3.3-V, 3.8-V, and 5-V fixed-voltage versions and in a variable version (programmable over the range of 1.5 V to 6.5 V).

AVAILABLE OPTIONS†

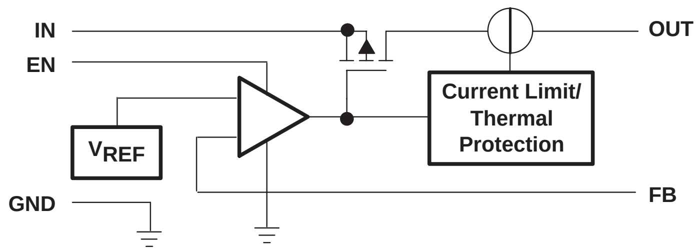
T_J	VOLTAGE	PACKAGE‡	PART NUMBER	SYMBOL
−40°C to 125°C	Variable	SOT-23 (DBV)	TPS76301QDBVRQ1	BAN
	1.6 V		TPS76316QDBVRQ1	BAD
	1.8 V		TPS76318QDBVRQ1	BAP
	2.5 V		TPS76325QDBVRQ1	BAQ
	2.7 V		TPS76327QDBVRQ1§	
	2.8 V		TPS76328QDBVRQ1§	
	3 V		TPS76330QDBVRQ1	BAT
	3.3 V		TPS76333QDBVRQ1	BAU
	3.8 V		TPS76338QDBVRQ1§	
	5.0 V		TPS76350QDBVRQ1	BAW

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.
§ Product Preview. Contact Texas Instruments for availability.

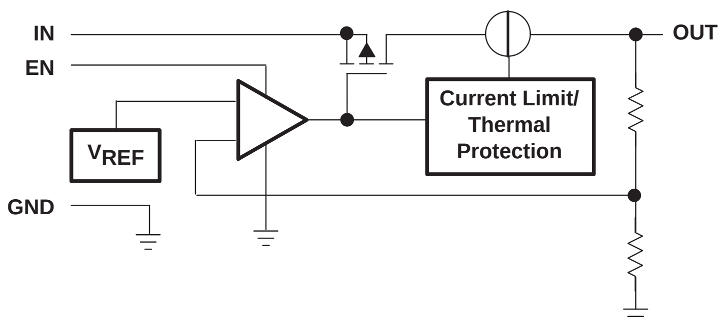
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram

TPS76301



TPS76316/ 18/ 25/ 27/ 28/ 30/ 33/ 38/ 50



Terminal Functions

TERMINAL NAME	DESCRIPTION
GND	Ground
EN	Enable input
FB	Feedback voltage (TPS76301 only)
IN	Input supply voltage
NC	No connection (fixed-voltage option only)
OUT	Regulated output voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[1]

Input voltage range[2]	−0.3 V to 10 V
Voltage range at EN	−0.3 V to V_I + 0.3 V
Voltage on OUT, FB	7 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
Continuous total power dissipation	See Dissipation Rating Tables
Operating junction temperature range, T_J	−40°C to 150°C
Storage temperature range, T_{stg}	−65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le$ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low K[1]	DBV	65.8°C/W	259°C/W	3.9 mW/°C	386 mW	212 mW	154 mW
High K[2]	DBV	65.8°C/W	180°C/W	5.6 mW/°C	555 mW	305 mW	222 mW

(1) The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.
(2) The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, V_I[1]	2.7		10	V
Continuous output current, I_O	0		150	mA
Operating junction temperature, T_J	−40		125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following equation:
$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$

electrical characteristics over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, EN = IN, $C_o = 4.7$ μF (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	TPS76301	3.25 V > V_I ≥ 2.7 V, 2.5 V ≥ V_O ≥ 1.5 V,	I_O = 1 mA to 75 mA, T_J = 25°C	0.98 V_O	V_O	1.02 V_O	V
			3.25 V > V_I ≥ 2.7 V, 2.5 V ≥ V_O ≥ 1.5 V	I_O = 1 mA to 75 mA,	0.97 V_O	V_O	1.03 V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V	I_O = 1 mA to 100 mA, T_J = 25°C	0.98 V_O	V_O	1.02 V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V	I_O = 1 mA to 100 mA,	0.97 V_O	V_O	1.03 V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V	I_O = 1 mA to 150 mA, T_J = 25°C	0.975 V_O	V_O	1.025 V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V	I_O = 1 mA to 150 mA,	0.9625 V_O	V_O	1.0375 V_O	
		TPS76316	V_I = 2.7 V,	1 mA< I_O < 75 mA, T_J = 25°C	1.568	1.6	1.632	V
			V_I = 2.7 V,	1 mA< I_O < 75 mA	1.552	1.6	1.648	
			V_I = 3.25 V,	1 mA < I_O < 100 mA, T_J = 25°C	1.568	1.6	1.632	
			V_I = 3.25 V,	1 mA < I_O < 100 mA	1.552	1.6	1.648	
			V_I = 3.25 V,	1 mA < I_O < 150 mA, T_J = 25°C	1.56	1.6	1.640	
			V_I = 3.25 V,	1 mA < I_O < 150 mA	1.536	1.6	1.664	
		TPS76318	V_I = 2.7 V,	1 mA< I_O < 75 mA, T_J = 25°C	1.764	1.8	1.836	V
			V_I = 2.7 V,	1 mA< I_O < 75 mA	1.746	1.8	1.854	
			V_I = 3.25 V,	1 mA < I_O < 100 mA, T_J = 25°C	1.764	1.8	1.836	
			V_I = 3.25 V,	1 mA < I_O < 100 mA	1.746	1.8	1.854	
			V_I = 3.25 V,	1 mA < I_O < 150 mA, T_J = 25°C	1.755	1.8	1.845	
			V_I = 3.25 V,	1 mA < I_O < 150 mA	1.733	1.8	1.867	
		TPS76325	I_O = 1 mA to 100 mA,	T_J = 25°C	2.45	2.5	2.55	V
			I_O = 1 mA to 100 mA		2.425	2.5	2.575	
			I_O = 1 mA to 150 mA,	T_J = 25°C	2.438	2.5	2.562	
			I_O = 1 mA to 150 mA		2.407	2.5	2.593	
		TPS76327	I_O = 1 mA to 100 mA,	T_J = 25°C	2.646	2.7	2.754	V
			I_O = 1 mA to 100 mA		2.619	2.7	2.781	
			I_O = 1 mA to 150 mA,	T_J = 25°C	2.632	2.7	2.767	
			I_O = 1 mA to 150 mA		2.599	2.7	2.801	
		TPS76328	I_O = 1 mA to 100 mA,	T_J = 25°C	2.744	2.8	2.856	V
			I_O = 1 mA to 100 mA		2.716	2.8	2.884	
			I_O = 1 mA to 150 mA,	T_J = 25°C	2.73	2.8	2.87	
			I_O = 1 mA to 150 mA		2.695	2.8	2.905	
		TPS76330	I_O = 1 mA to 100 mA,	T_J = 25°C	2.94	3	3.06	V
			I_O = 1 mA to 100 mA		2.91	3	3.09	
			I_O = 1 mA to 150 mA,	T_J = 25°C	2.925	3	3.075	
			I_O = 1 mA to 150 mA		2.888	3	3.112	

electrical characteristics over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, EN = IN, $C_o = 4.7$ µF (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	TPS76333	I_O = 1 mA to 100 mA,	T_J = 25°C	3.234	3.3	3.366	V
			I_O = 1 mA to 100 mA		3.201	3.3	3.399	
			I_O = 1 mA to 150 mA,	T_J = 25°C	3.218	3.3	3.382	
			I_O = 1 mA to 150 mA		3.177	3.3	3.423	
		TPS76338	I_O = 1 mA to 100 mA,	T_J = 25°C	3.724	3.8	3.876	V
			I_O = 1 mA to 100 mA		3.705	3.8	3.895	
			I_O = 1 mA to 150 mA,	T_J = 25°C	3.686	3.8	3.914	
			I_O = 1 mA to 150 mA		3.667	3.8	3.933	
		TPS76350	I_O = 1 mA to 100 mA,	T_J = 25°C	4.875	5	5.125	V
			I_O = 1 mA to 100 mA		4.825	5	5.175	
			I_O = 1 mA to 150 mA,	T_J = 25°C	4.750	5	5.15	
			I_O = 1 mA to 150 mA		4.80	5	5.20	
$I_{(Q)}$	Quiescent current (GND terminal current)		I_O = 0 to 150 mA,	T_J = 25°C (1)		85	100	µA
			I_O = 0 to 150 mA see (2)				140	
	Standby current		EN < 0.5 V,	T_J = 25°C		0.5	1	
			EN < 0.5 V				2	
V_n	Output noise voltage		BW = 300 Hz to 50 kHz, T_J = 25°C,	C_o = 10 µF (2)		140		µV
PSRR	Ripple rejection		f = 1 kHz, C_o = 10 µF,	T_J = 25°C (2)		60		dB
	Current limit		T_J = 25°C, see (3)		0.5	0.8	1.5	A
	Output voltage line regulation ($\Delta V_O/V_O$), (see (3))		$V_O + 1\text{ V} < V_I \le 10$ V,	$V_I \ge 3.5$ V, T_J = 25°C		0.04	0.07	%/V
			$V_O + 1\text{ V} < V_I \le 10$ V,	$V_I \ge 3.5$ V			0.1	
V_{IH}	EN high level input		See (2)			1.4	2	V
V_{IL}	EN low level input		See (2)		0.5	1.2		
I_I	EN input current		EN = 0 V			−0.01	−0.5	µA
			EN = IN			−0.01	−0.5	

(1) Minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater.
(2) Test condition includes: output voltage V_O = 0 V (for variable device FB is shorted to V_O) and pulse duration = 10 ms.
(3) If V_O < 2.5 V and V_{Imax} = 10 V, V_{Imin} = 3.5 V:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O\left(V_{Imax} - 3.5\text{ V}\right)}{100} \times 1000$$

If V_O > 2.5 V and V_{Imax} = 10 V, $V_{Imin} = V_O + 1$ V:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O\left(V_{Imax} - \left(V_O + 1\right)\right)}{100} \times 1000$$

electrical characteristics over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, EN = IN, $C_o = 4.7$ μF (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage	TPS76325	I_O = 0 mA,	T_J = 25°C		0.2		mV
			I_O = 1 mA,	T_J = 25°C		3		
			I_O = 50 mA,	T_J = 25°C		120	150	
			I_O = 50 mA				200	
			I_O = 75 mA,	T_J = 25°C		180	225	
			I_O = 75 mA				300	
			I_O = 100 mA,	T_J = 25°C		240	300	
			I_O = 100 mA				400	
			I_O = 150 mA,	T_J = 25°C		360	450	
			I_O = 150 mA				600	
		TPS76333	I_O = 0 mA,	T_J = 25°C		0.2		mV
			I_O = 1 mA,	T_J = 25°C		3		
			I_O = 50 mA,	T_J = 25°C		100	125	
			I_O = 50 mA				166	
			I_O = 75 mA,	T_J = 25°C		150	188	
			I_O = 75 mA				250	
			I_O = 100 mA,	T_J = 25°C		200	250	
			I_O = 100 mA				333	
			I_O = 150 mA,	T_J = 25°C		300	375	
			I_O = 150 mA				500	
		TPS76350	I_O = 0 mA,	T_J = 25°C		0.2		mV
			I_O = 1 mA,	T_J = 25°C		2		
			I_O = 50 mA,	T_J = 25°C		60	75	
			I_O = 50 mA				100	
			I_O = 75 mA,	T_J = 25°C		90	113	
			I_O = 75 mA				150	
			I_O = 100 mA,	T_J = 25°C		120	150	
			I_O = 100 mA				200	
			I_O = 150 mA,	T_J = 25°C		180	225	
			I_O = 150 mA				300	

TYPICAL CHARACTERISTICS

TPS76325
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

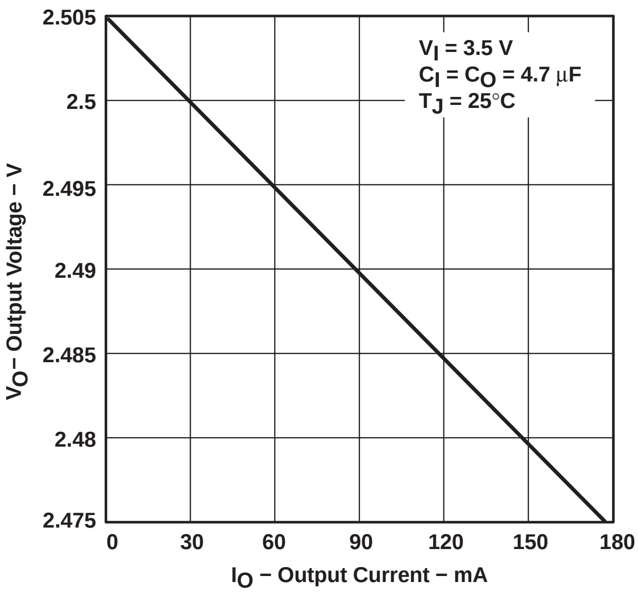


Figure 1

TPS76318
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

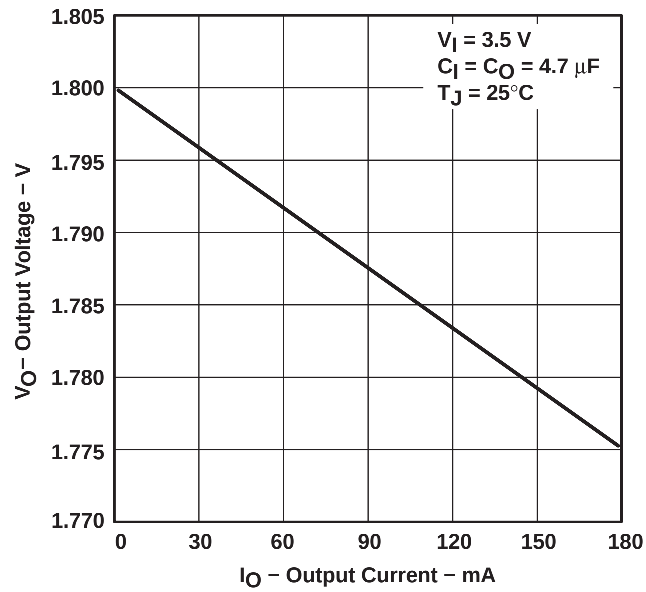


Figure 2

TPS76350
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

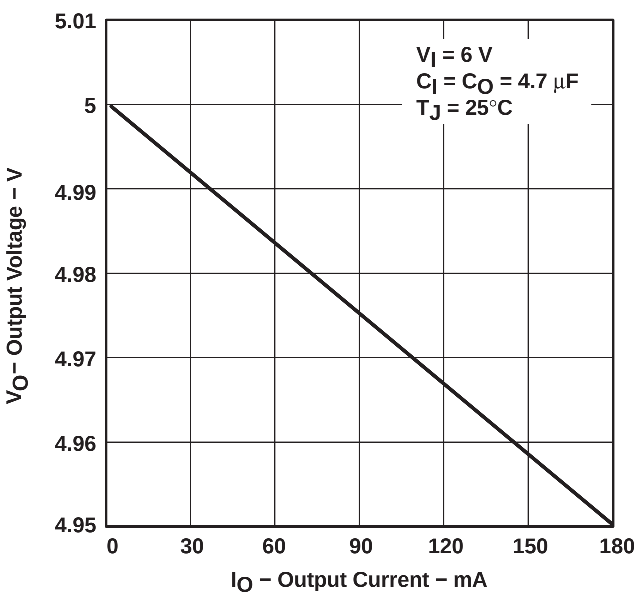


Figure 3

TPS76325
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

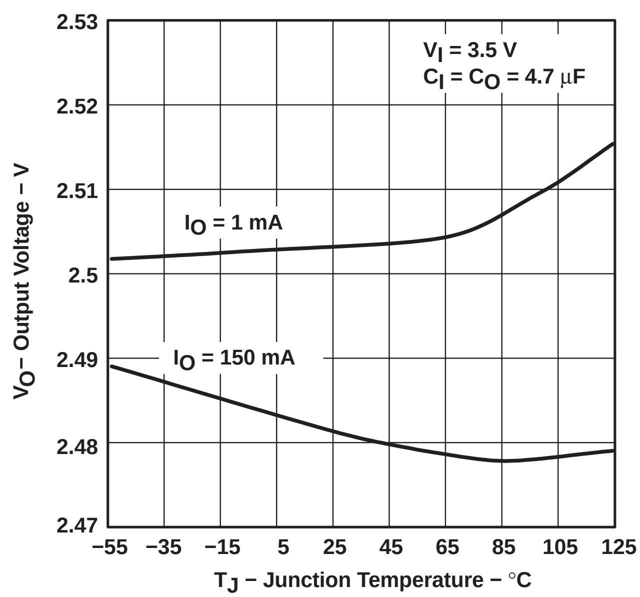


Figure 4

TYPICAL CHARACTERISTICS

TPS76318
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

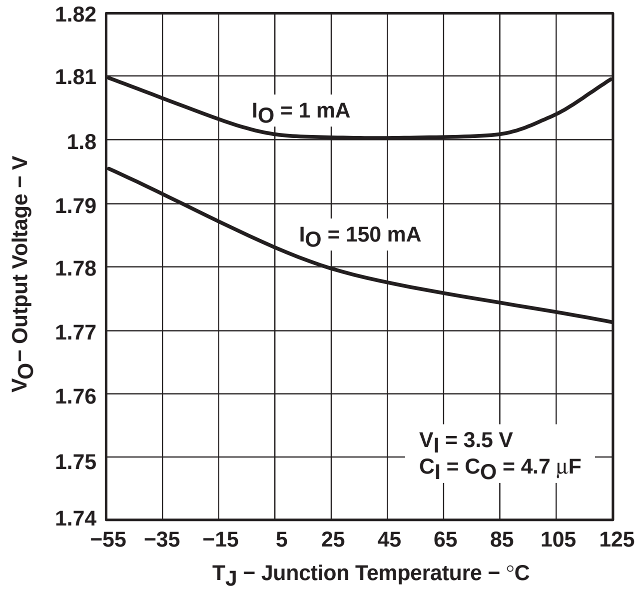


Figure 5

TPS76350
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

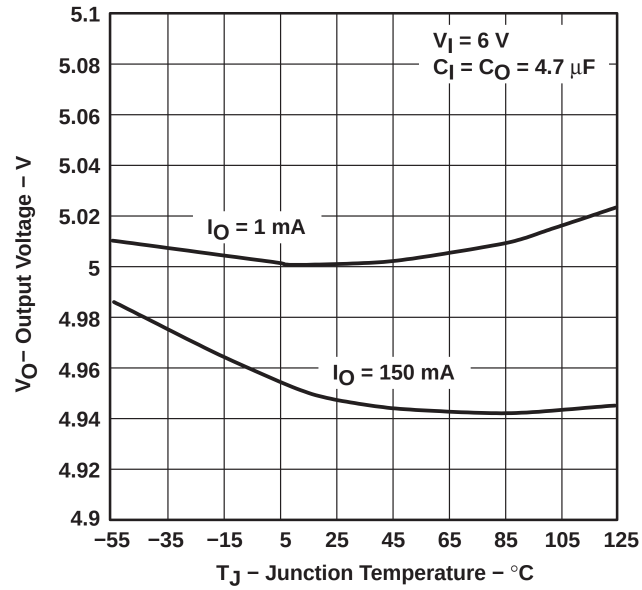


Figure 6

TPS76350
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

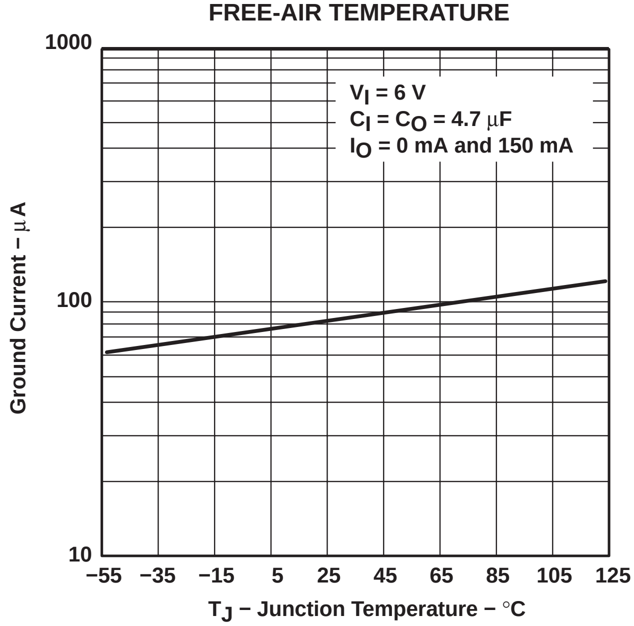


Figure 7

OUTPUT NOISE
vs
FREQUENCY

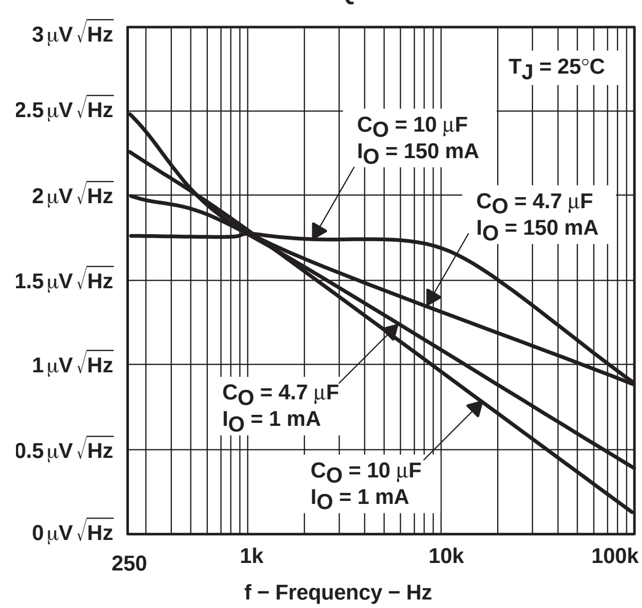


Figure 8

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs FREQUENCY

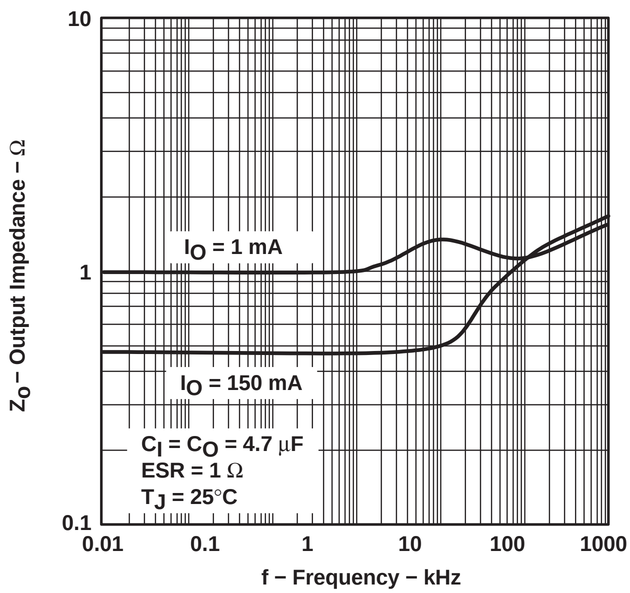


Figure 9

TPS76325 DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

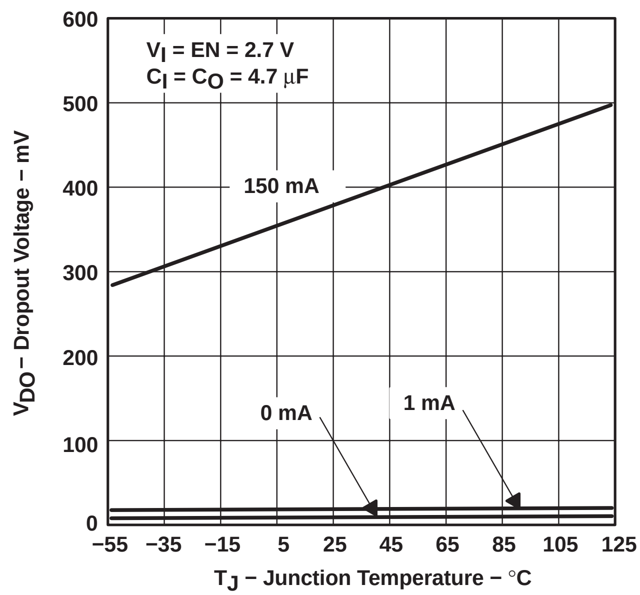


Figure 10

TPS76325 RIPPLE REJECTION vs FREQUENCY

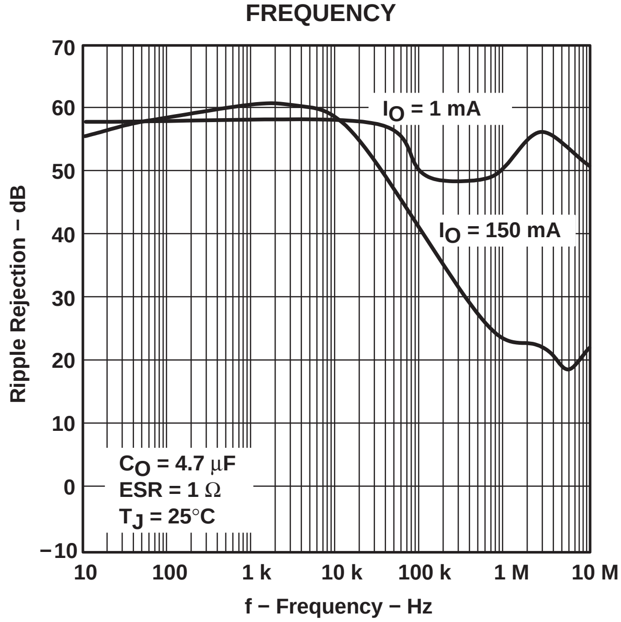


Figure 11

TYPICAL CHARACTERISTICS

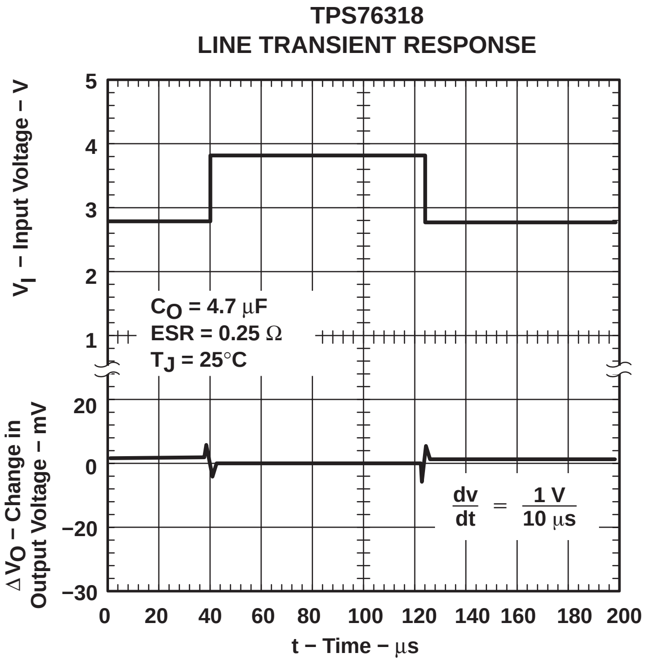


Figure 12

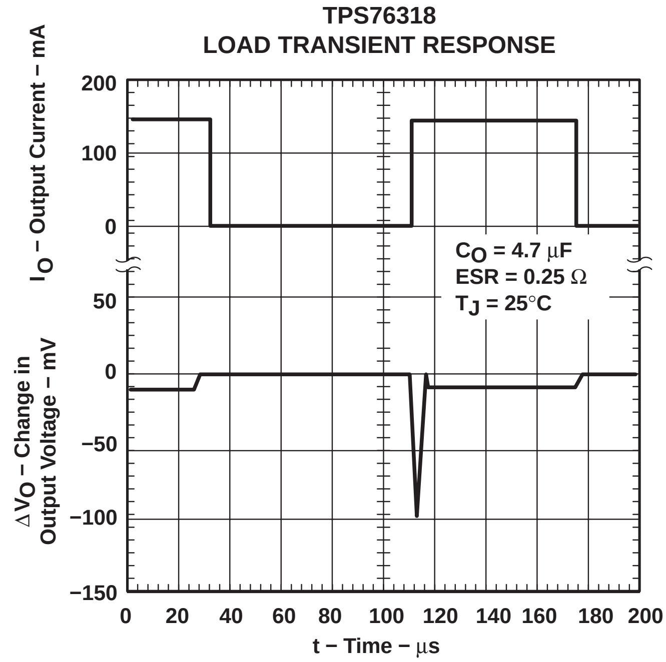


Figure 13

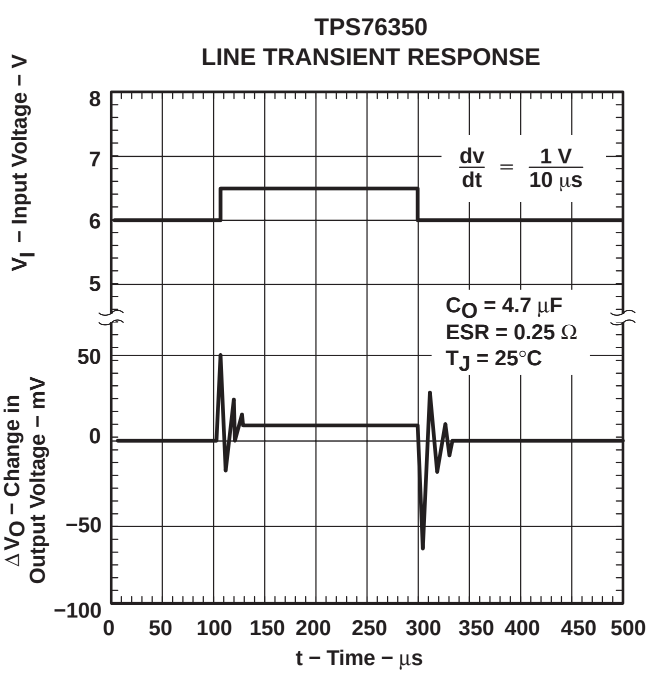


Figure 14

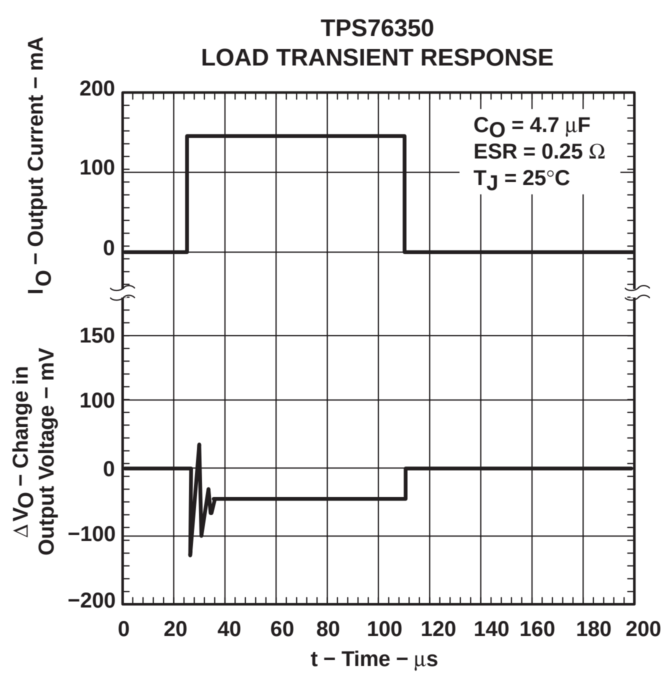


Figure 15

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)(1)
vs
OUTPUT CURRENT

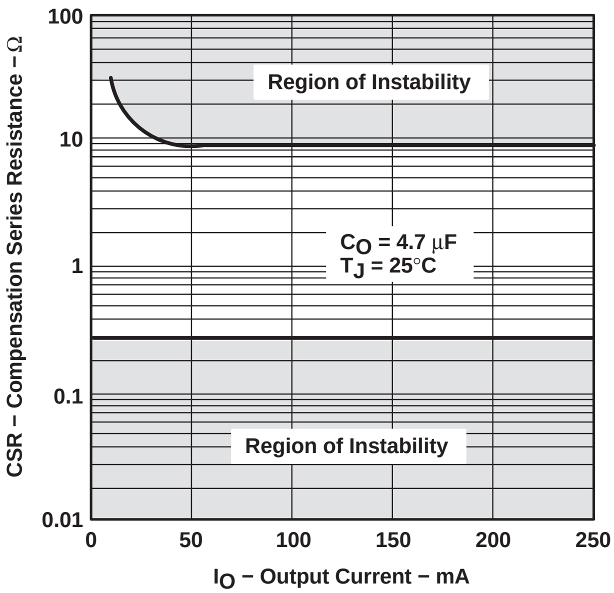


Figure 16

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)(1)
vs
ADDED CERAMIC CAPACITANCE

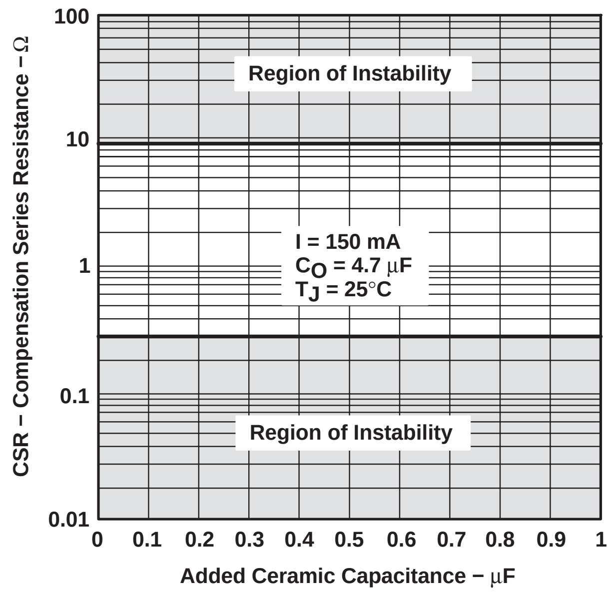


Figure 17

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)(1)
vs
OUTPUT CURRENT

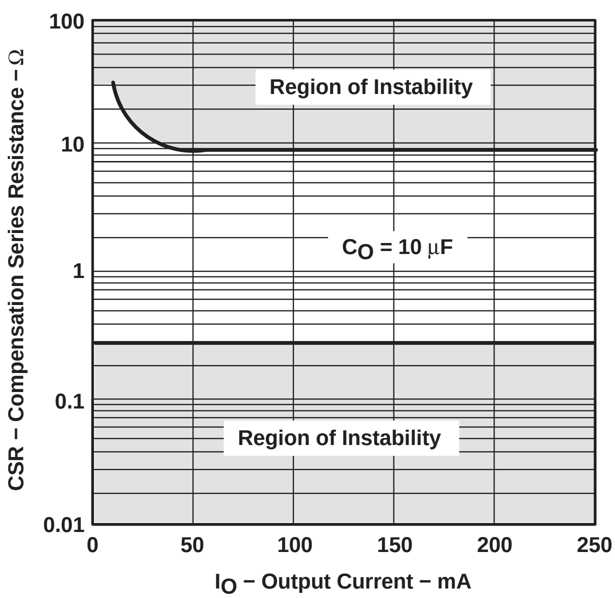


Figure 18

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)(1)
vs
ADDED CERAMIC CAPACITANCE

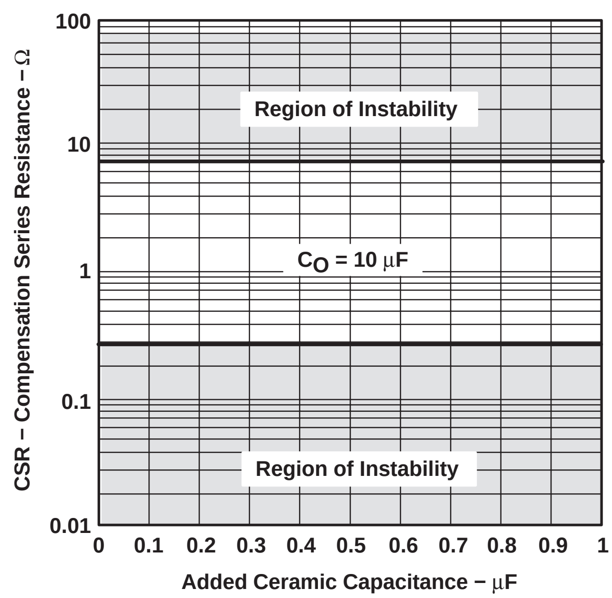


Figure 19

(1) CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

APPLICATION INFORMATION

The TPS763xx low-dropout (LDO) regulators are new families of regulators which have been optimized for use in battery-operated equipment and feature low dropout voltages, low quiescent current (140 μA), and an enable input to reduce supply currents to less than 2 μA when the regulator is turned off.

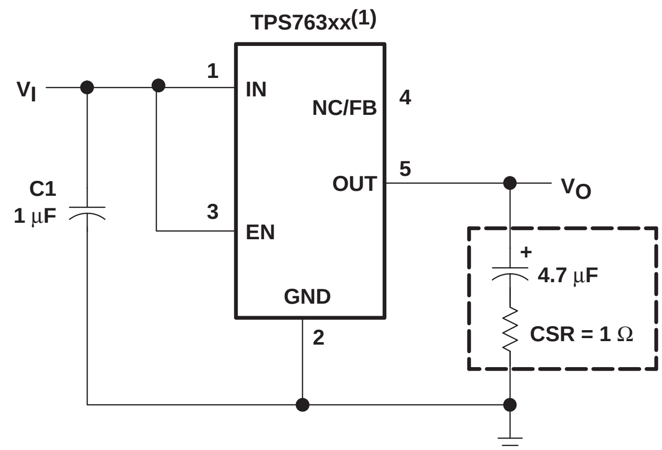
device operation

The TPS763xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP pass element LDO designs. The PMOS pass element is a voltage-controlled device that, unlike a PNP transistor, does not require increased drive current as output current increases. Supply current in the TPS763xx is essentially constant from no-load to maximum load.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 1 A; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

A logic low on the enable input, EN shuts off the output and reduces the supply current to less than 2 μA. EN should be tied high in applications where the shutdown feature is not used.

A typical application circuit is shown in Figure 20.



(1) TPS76316, TPS76318, TPS76325, TPS76327, TPS76328, TPS7630 TPS76333, TPS76338, TPS76350 (fixed-voltage options).

Figure 20. Typical Application Circuit

APPLICATION INFORMATION

external capacitor requirements

Although not required, a 0.047 µF or larger ceramic bypass input capacitor, connected between IN and GND and located close to the TPS763xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS763xx requires an output capacitor connected between OUT and GND to stabilize the internal loop control. The minimum recommended capacitance value is 4.7 µF and the ESR (equivalent series resistance) must be between 0.3 Ω and 10 Ω. Capacitor values of 4.7 µF or larger are acceptable, provided the ESR is less than 10 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7-µF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above.

CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR(1)	SIZE (H ⎮ L ⎮ W)†
T494B475K016AS	KEMET	4.7 µF	1.5 Ω	1.9 × 3.5 × 2.8
195D106x0016x2T	SPRAGUE	10 µF	1.5 Ω	1.3 × 7.0 × 2.7
695D106x003562T	SPRAGUE	10 µF	1.3 Ω	2.5 × 7.6 × 2.5
TPSC475K035R0600	AVX	4.7 µF	0.6 Ω	2.6 × 6.0 × 3.2

(1) Size is in mm. ESR is maximum resistance in ohms at 100 kHz and T_A = 25°C. Listings are sorted by height.

output voltage programming

The output voltage of the TPS76301 adjustable regulator is programmed using an external resistor divider as shown in Figure 21. The output voltage is calculated using:

$$V_O = 0.995 \times V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where:

V_{ref} = 1.192 V typ (the internal reference voltage)

0.995 is a constant used to center the load regulator (1%)

Resistors R1 and R2 should be chosen for approximately 7-µA divider current. Lower value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{0.995 \times V_{ref}} - 1\right) \times R2 \tag{2}$$

APPLICATION INFORMATION

OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (kΩ)(1)	
	R1	R2
2.5	187	169
3.3	301	169
3.6	348	169
4	402	169
5	549	169
6.45	750	169

(1) 1% values shown.

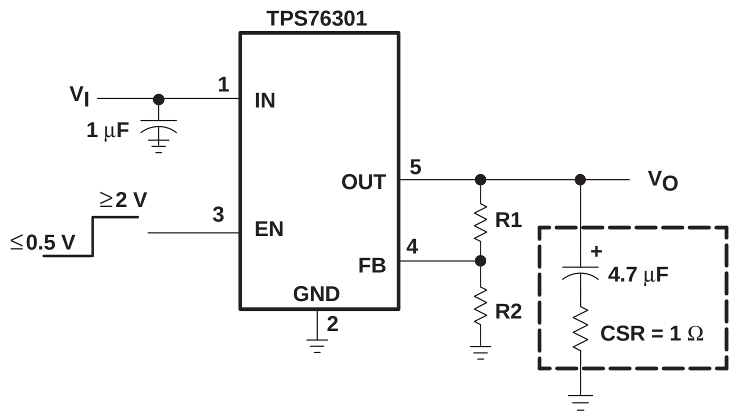


Figure 21. TPS76301 Adjustable LDO Regulator Programming

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature allowable to avoid damaging the device is 150°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$ and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J$max is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible.

regulator protection

The TPS763xx pass element has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS763xx also features internal current limiting and thermal protection. During normal operation, the TPS763xx limits output current to approximately 800 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below 140°C, the regulator operation resumes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76301QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAN	Samples
TPS76301QDBVRQ1	ACTIVE	SOT-23	DBV	5		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAN	Samples
TPS76316QDBVRQ1	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125		
TPS76318QDBVRG4Q1	ACTIVE	SOT-23	DBV	5		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAP	Samples
TPS76318QDBVRQ1	ACTIVE	SOT-23	DBV	5		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAP	Samples
TPS76325QDBVRG4Q1	ACTIVE	SOT-23	DBV	5		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAQ	Samples
TPS76325QDBVRQ1	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125		
TPS76330QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAT	Samples
TPS76330QDBVRQ1	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125		
TPS76333QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAU	Samples
TPS76333QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAU	Samples
TPS76350QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAW	Samples
TPS76350QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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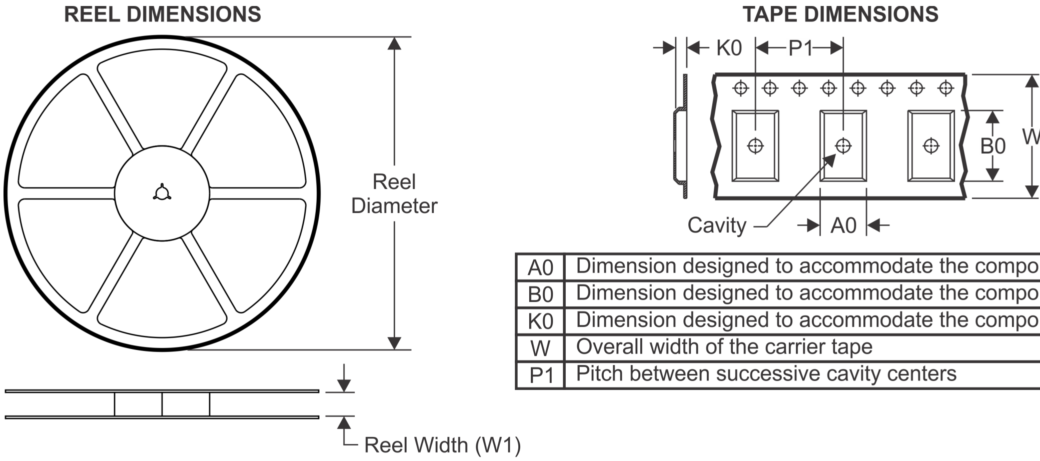
- Catalog: TPS76301, TPS76316, TPS76318, TPS76325, TPS76330, TPS76333, TPS76350

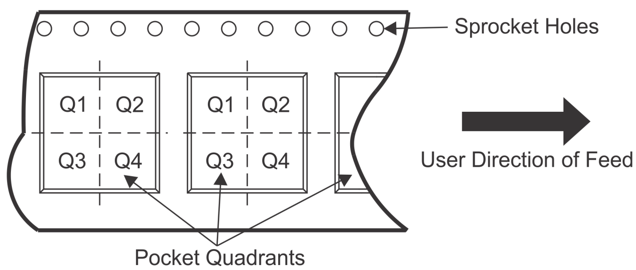
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



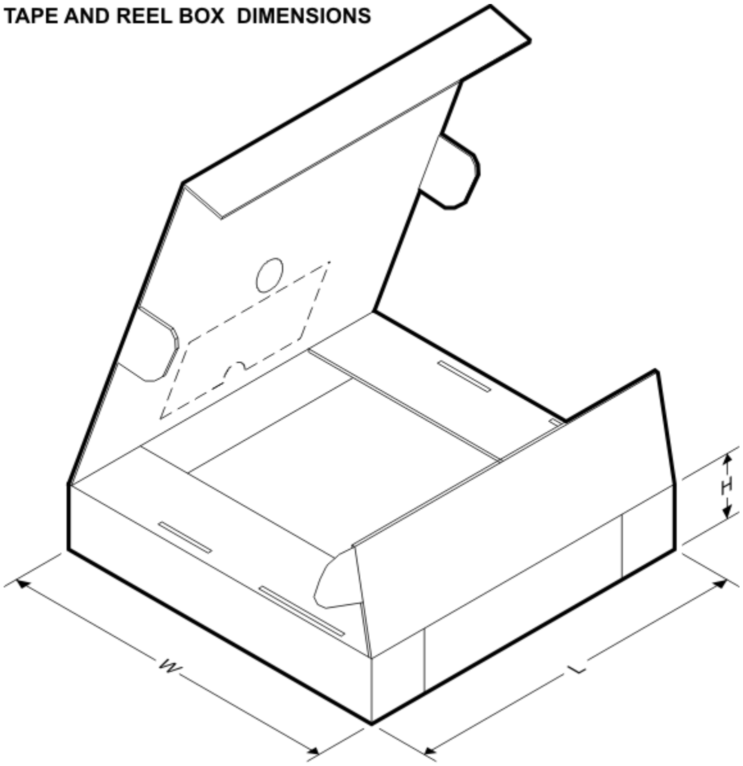
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76301QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76301QDBVRQ1	SOT-23	DBV	5	0	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76318QDBVRG4Q1	SOT-23	DBV	5	0	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76318QDBVRQ1	SOT-23	DBV	5	0	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76325QDBVRG4Q1	SOT-23	DBV	5	0	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76330QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76333QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76333QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76350QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76350QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

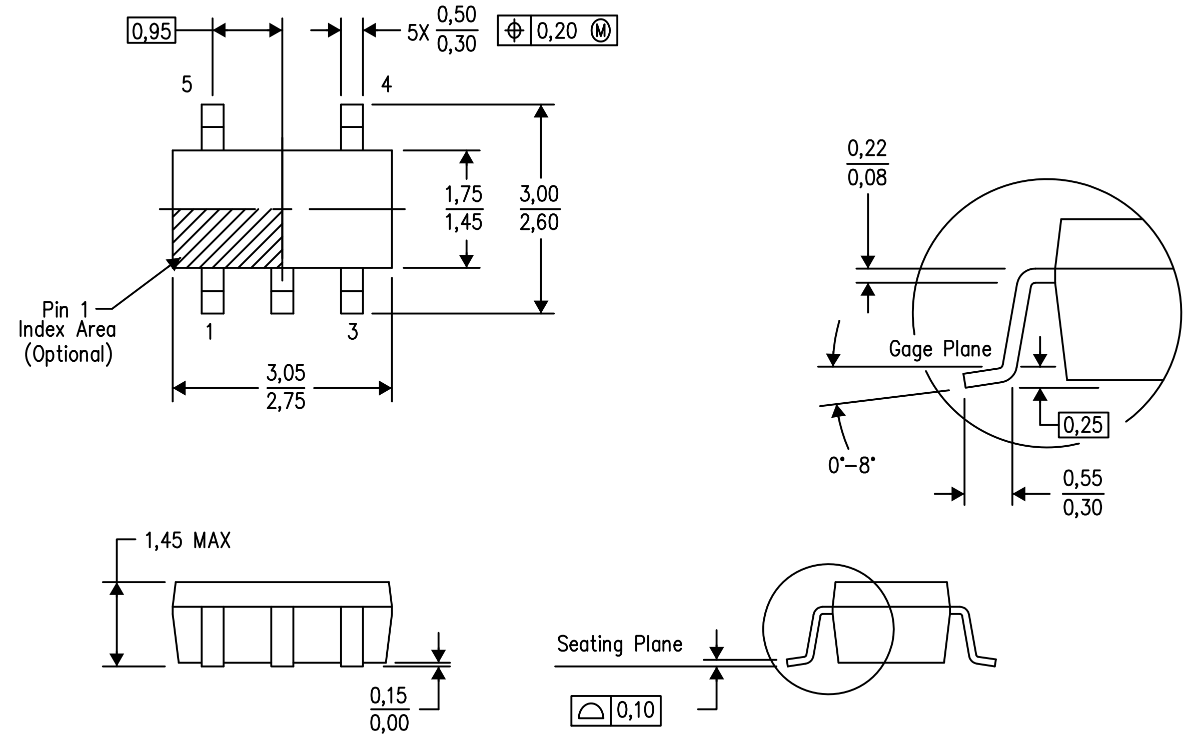
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76301QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76301QDBVRQ1	SOT-23	DBV	5	0	182.0	182.0	20.0
TPS76318QDBVRG4Q1	SOT-23	DBV	5	0	182.0	182.0	20.0
TPS76318QDBVRQ1	SOT-23	DBV	5	0	182.0	182.0	20.0
TPS76325QDBVRG4Q1	SOT-23	DBV	5	0	182.0	182.0	20.0
TPS76330QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76333QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76333QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76350QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76350QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



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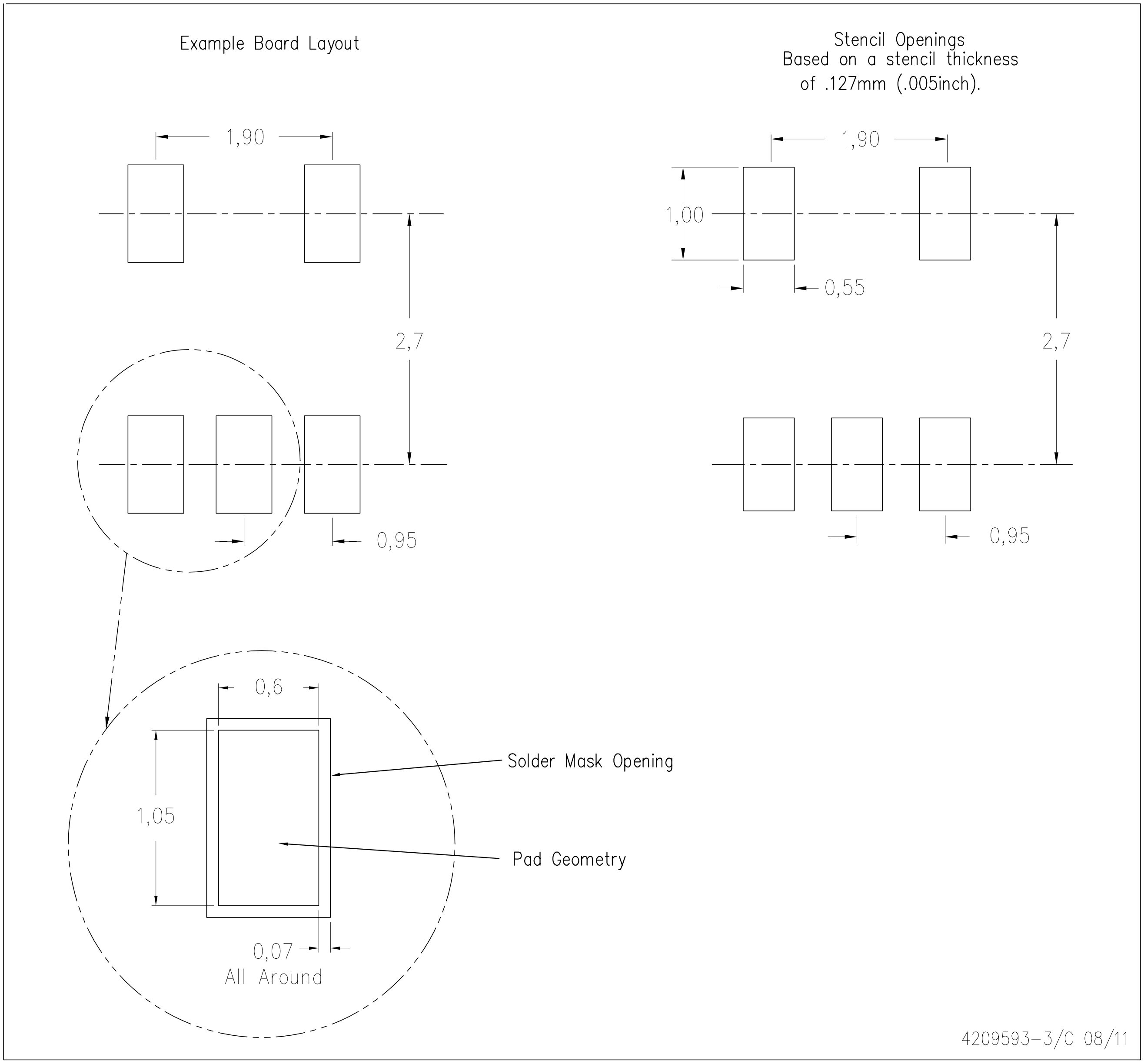
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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