200-mA, Low-Dropout Linear Regulator with Built-In Inrush Current Protection

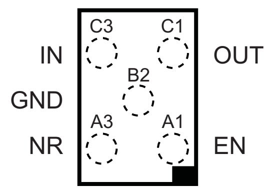
FEATURES

- **200mA Low-Dropout Regulator with EN**
- **Multiple Output Voltage Versions Available:**
  - **TPS799L: Fixed Outputs of 5.2 V to 6.2 V Using Innovative Factory EEPROM Programming**
  - **TPS799L57 : 5.7-V Output**
  - **TPS799: Output Options Less Than 5.2 V**
- **Inrush current Protection with EN Toggle**
- **Low I_Q: 40 μA**
- **High PSRR: 66 dB at 1 kHz**
- **Stable with a Low-ESR, 2.0-μF Typical Output Capacitance**
- **Excellent Load/Line Transient Response**
- **2% Overall Accuracy (Load, Line, and Temp)**
- **Very Low Dropout: 100 mV**
- **Package: 5-Bump, Thin, 1-mm × 1.37-mm WCSP**

APPLICATIONS

- **Cellular Phones**
- **Wireless LAN, Bluetooth®**
- **VCOs, RF**
- **Handheld Organizers, PDAs**

TPS799LxxYZY
WCSP
(TOP VIEW)



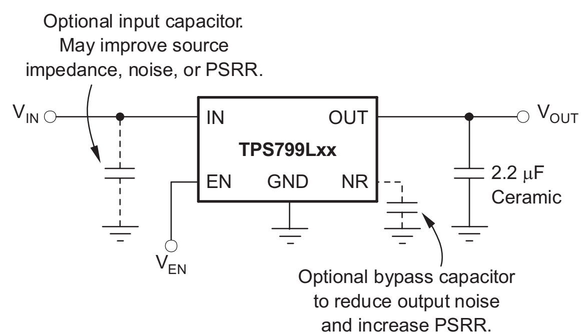
DESCRIPTION

The TPS799L family of low-dropout (LDO), low-power linear regulators offers excellent ac performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response are provided while consuming a very low 40 μA (typical) ground current.

The TPS799Lxx is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a dropout voltage of typically 100 mV at a 200 mA output. The TPS799L uses a precision voltage reference and feedback loop to achieve an overall accuracy of 2% over all load, line, process, and temperature variations. The TPS799L features inrush current protection when the EN toggle is used to start the device, immediately clamping the current.

All devices are fully specified over the temperature range of T_J = –40°C to +125°C, and offered in a low-profile, wafer chip-scale (WCSP) package, ideal for wireless handsets and WLAN cards.

TYPICAL APPLICATION CIRCUIT



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All other trademarks are the property of their respective owners.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}
TPS799L**xx** ***yyy z***	**XX** is nominal output voltage (for example, 57 = 5.7V). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	IN	–0.3	+7.0	V
	EN	–0.3	V_{IN} + 0.3	V
	OUT	–0.3	V_{IN} + 0.3	V
Current	OUT	Internally limited		mA
Temperature	Operating virtual junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic discharge ratings(3)	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charge device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPS799L YZY (WCSP) 5 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	143.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	1.1	
θ_{JB}	Junction-to-board thermal resistance	84.7	
ψ_{JT}	Junction-to-top characterization parameter	3.8	
ψ_{JB}	Junction-to-board characterization parameter	84.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF, unless otherwise noted.
Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range (1)			2.7		6.5	V
V_{OUT}	Output voltage range			5.2		6.2	V
	Output accuracy, nominal	T_J = +25°C		–1.0		+1.0	%
	Output accuracy (1) Over V_{IN}, I_{OUT}, temperature	V_{OUT} + 0.3 V ≤ V_{IN} ≤ 6.5 V 500 µA ≤ I_{OUT} ≤ 200 mA		–2.0	±1.0	+2.0	%
$\Delta V_{O(\Delta VI)}$	Line regulation (1)	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 6.5 V			0.02		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	500 µA ≤ I_{OUT} ≤ 200 mA			0.002		%/mA
V_{DO}	Dropout voltage (V_{IN} = $V_{OUT(NOM)}$ – 0.1V)	V_{OUT} ≥ 3.3 V, I_{OUT} = 200 mA			90	160	mV
I_{LIM}	Output current limit (2)	V_{OUT} = 0.9 × $V_{OUT(NOM)}$		220	340	600	mA
I_{GND}	Ground pin current	500 µA ≤ I_{OUT} ≤ 200 mA			40	60	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.4 V, 2.7 V ≤ V_{IN} ≤ 6.5 V			0.15	1.0	µA
PSRR	Power-supply rejection ratio	V_{IN} = 6.5 V, V_{OUT} = 2.85 V, C_{NR} = 0.01 µF, I_{OUT} = 100 mA	f = 100 Hz		70		dB
			f = 1 kHz		66		dB
			f = 10 kHz		51		dB
			f = 100 kHz		38		dB
V_N	Output noise voltage	BW = 10 Hz to 100 kHz	C_{NR} = 0.01 µF		10.5 x V_{OUT}		μV_{RMS}
			C_{NR} = none		94 x V_{OUT}		μV_{RMS}
T_{STR}	Start-up time	V_{OUT} = 5.7 V, R_L = 28 Ω, C_{OUT} = 2.2 µF	C_{NR} = 0.01 µF		90		µs
			C_{NR} = none		95		µs
$V_{EN(HI)}$	Enable high (enabled)			1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	V_{EN} = V_{IN} = 6.5 V			0.03	1.0	µA
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing			165		°C
		Reset, temperature decreasing			145		°C
T_J	Operating junction temperature			–40		+125	°C
UVLO	Undervoltage lockout	V_{IN} rising		1.90	2.20	2.65	V
	Hysteresis	V_{IN} falling			70		mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7V, whichever is greater.
(2) TPS799Lxx has peak current clamp during EN toggle start-up.

FUNCTIONAL BLOCK DIAGRAM

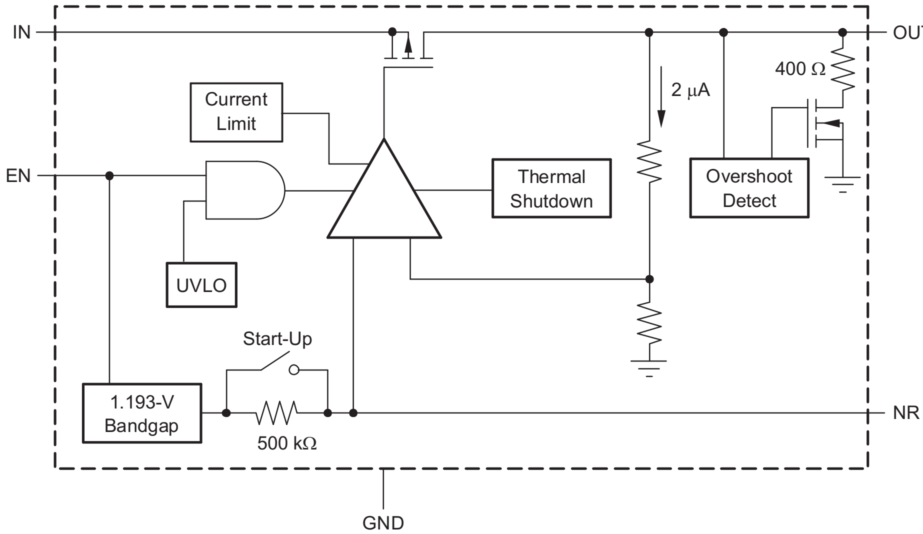
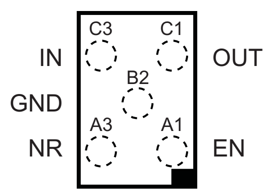


Figure 1. Functional Block Diagram

PIN CONFIGURATION

YZY PACKAGE
WCSP-5
(TOP VIEW)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	NO.	
EN	A1	Driving this pin high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
GND	B2	Ground.
IN	C3	Input supply.
NR	A3	Noise reduction; connecting this pin to an external capacitor bypasses noise generated by the internal bandgap. This capacitor allows output noise to be reduced to very low levels.
OUT	C1	Output of the regulator. To assure stability, a small ceramic capacitor (total typical capacitance ≥ 2.0 µF) is required from this pin to ground.

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J= –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 μF, C_{NR} = 0.01μF, unless otherwise noted. Typical values are at T_J = +25°C.

LOAD REGULATION (V_{IN} = 6.5 V)

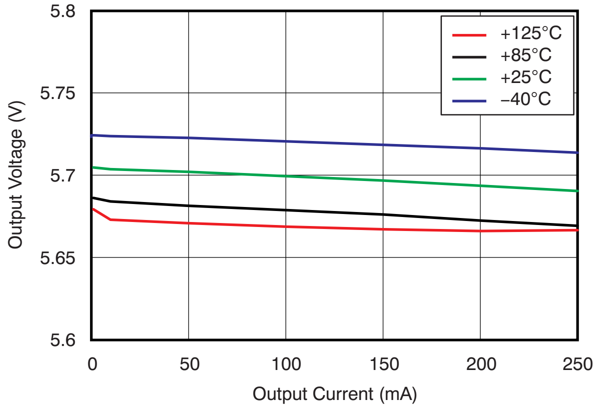


Figure 2.

OUTPUT VOLTAGE vs JUNCTION TEMPERATURE (TPS799Axx)

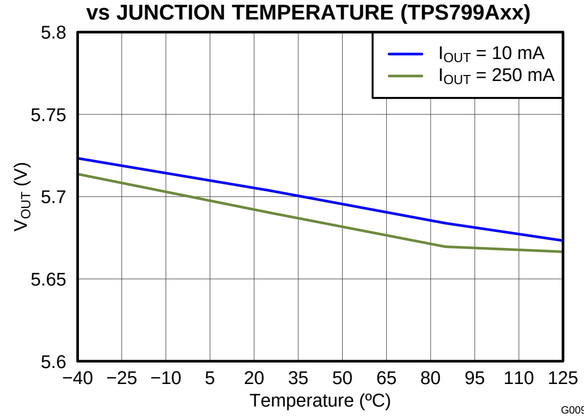


Figure 3.

DROPOUT VOLTAGE vs OUTPUT CURRENT

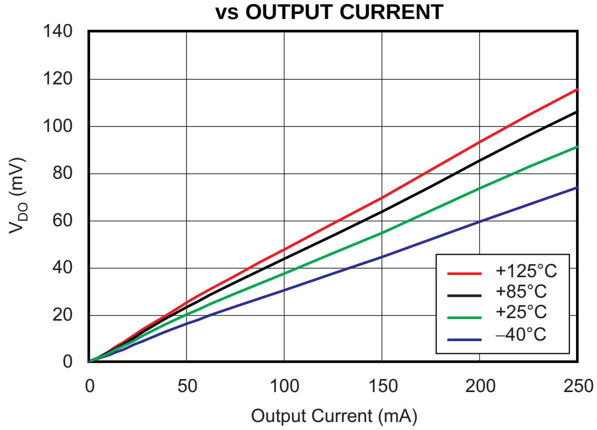


Figure 4.

DROPOUT VOLTAGE vs INPUT VOLTAGE, I_{OUT} = 250mA

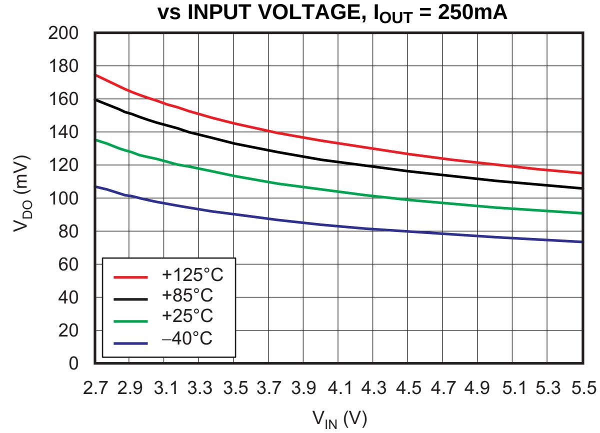


Figure 5.

GROUND PIN CURRENT vs INPUT VOLTAGE

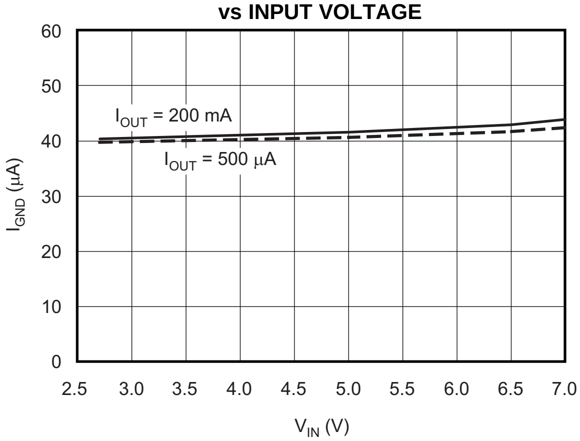


Figure 6.

GROUND PIN CURRENT vs OUTPUT CURRENT (V_{IN} = 6.5 V)

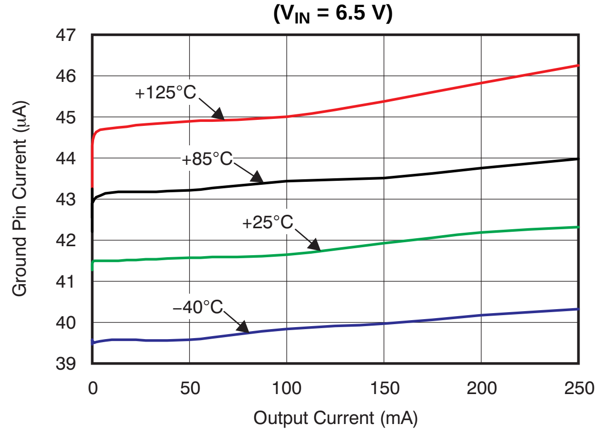


Figure 7.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01µF, unless otherwise noted. Typical values are at T_J = +25°C.

GROUND PIN CURRENT (DISABLED) vs JUNCTION TEMPERATURE

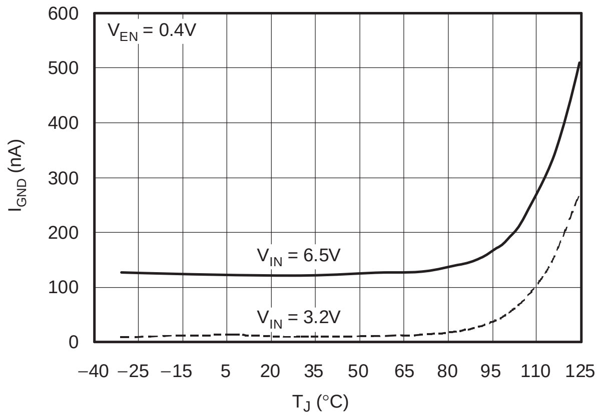


Figure 8.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY (V_{IN} = 6.5 V)

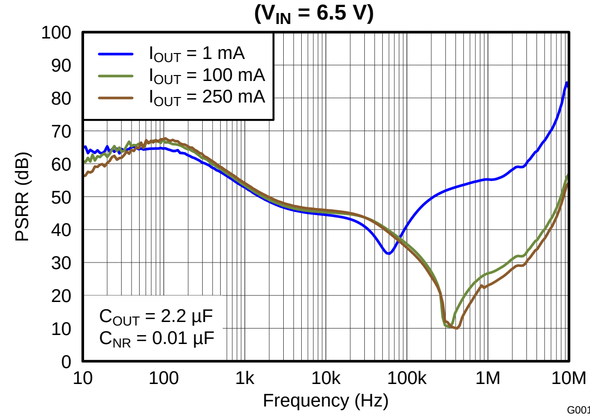


Figure 9.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY (V_{IN} = 6.2 V)

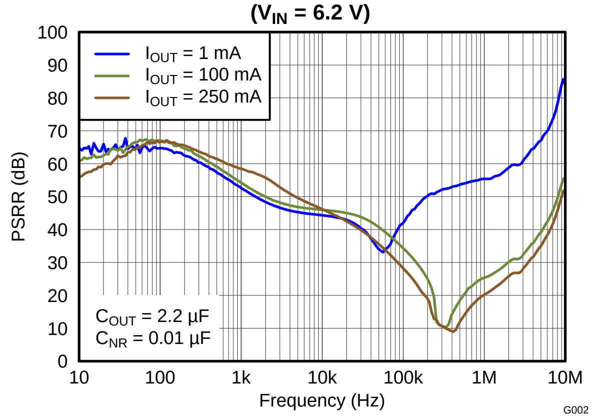


Figure 10.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY (V_{IN} = 5.95 V)

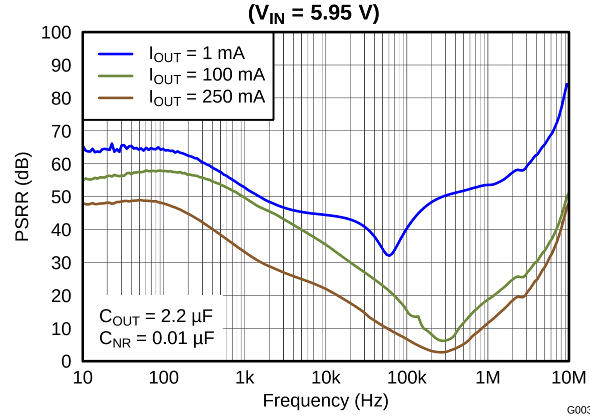


Figure 11.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY (V_{IN} = 6.5 V)

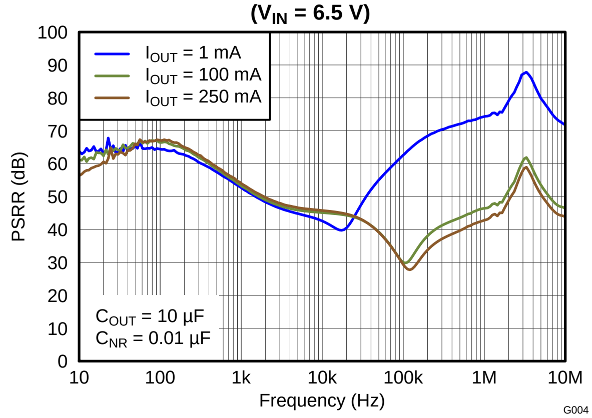


Figure 12.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY (V_{IN} = 6.2 V)

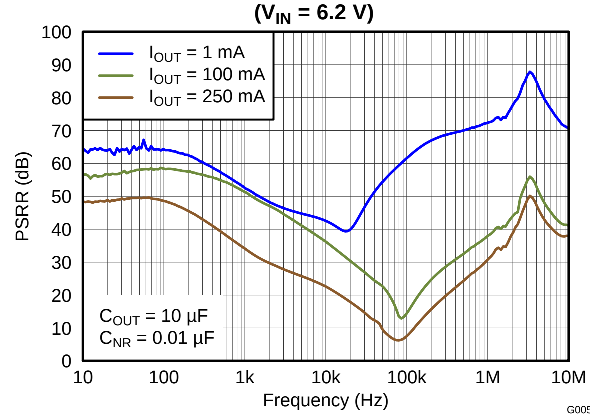


Figure 13.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01µF, unless otherwise noted. Typical values are at T_J = +25°C.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY (V_{IN} = 5.95 V)

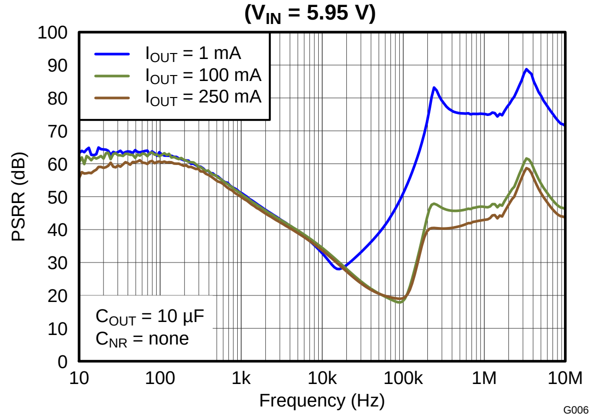


Figure 14.

TOTAL NOISE vs C_{NR} (V_{IN} = 6 V)

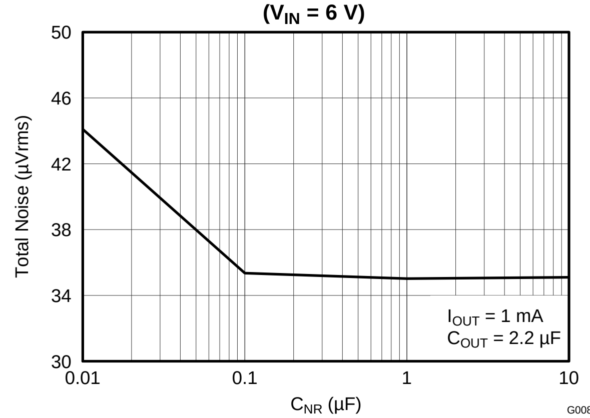


Figure 15.

TOTAL NOISE vs C_{OUT} (V_{IN} = 6 V)

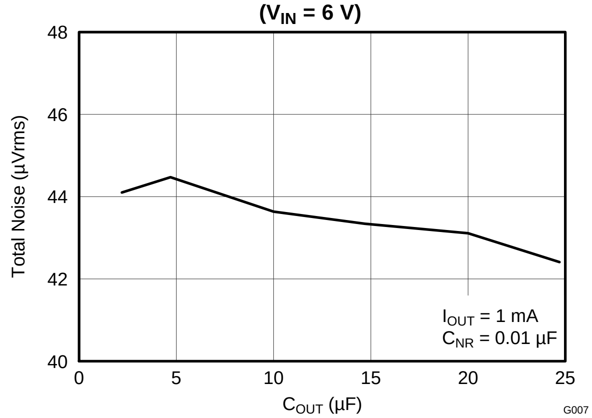


Figure 16.

INRUSH CURRENT AT EN TURN-ON (C_{IN} = C_{OUT} = 20 µF, I_{OUT} = 47 mA)

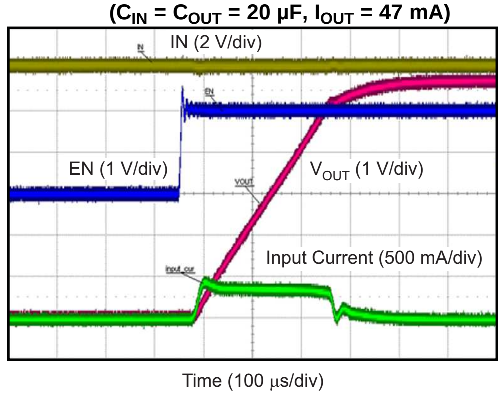


Figure 17.

APPLICATION INFORMATION

The TPS799Lxx family of LDO regulators combines the high performance required of many RF and precision analog applications with ultralow current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom ($V_{IN} – V_{OUT}$). A noise-reduction pin is provided to bypass noise generated by the bandgap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. The combination of high performance and low ground current also make these devices an excellent choice for portable applications. All versions have thermal and overcurrent protection, and are fully specified from –40°C to +125°C.

The TPS799Lxx family also features inrush current protection with an EN toggle start-up, and overshoot detection at the output. When the EN toggle is used to start the device, current limit protection is immediately activated, restricting the inrush current to the device (see Figure 17). If voltage at the output overshoots 5% from the nominal value, a pull-down resistor reduces the voltage to normal operating conditions (see Figure 1).

Figure 18 shows the basic circuit connections.

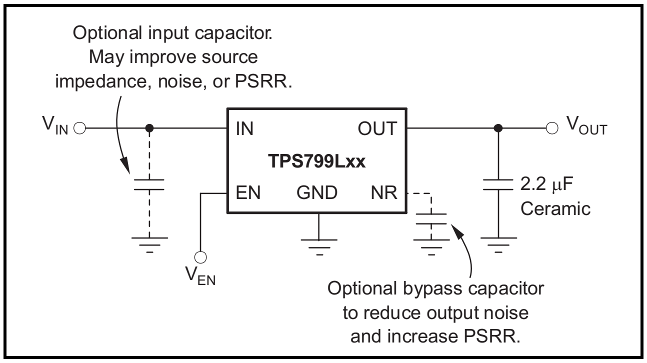


Figure 18. Typical Application Circuit

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-μF to 1-μF low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor may be necessary to ensure stability.

The TPS799Lxx is designed to be stable with standard ceramic capacitors with values of 2.2 μF or greater. X5R and X7R type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be < 1.0 Ω.

OUTPUT NOISE

In most LDOs, the bandgap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS799Lxx, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-μF noise reduction capacitor. To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point; with C_{NR} = 0.01 μF total noise is approximately given by Equation 1:

$$V_N = \frac{10.5\mu V_{RMS}}{V} \times V_{OUT} \tag{1}$$

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, connect the bypass capacitor directly to the GND pin of the device.

INTERNAL CURRENT LIMIT

The TPS799Lxx internal current limit helps protect the regulator during fault conditions. In current limit mode, the output sources a fixed amount of current that is largely independent of the output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

The PMOS pass element in the TPS799Lxx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited; therefore, if extended reverse voltage operation is anticipated, external limiting may be required.

SHUTDOWN

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

DROPOUT VOLTAGE

The TPS799Lxx uses a PMOS pass transistor to achieve a low dropout voltage. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and $r_{DS(on)}$ of the PMOS pass element is the input-to-output resistance. Because the PMOS device behaves like a resistor in dropout, V_{DO} approximately scales with the output current.

As with any linear regulator, PSRR degrades as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 9 through Figure 14 in the *Typical Characteristics* section.

START-UP

The TPS799Lxx uses a start-up circuit to quickly charge the noise reduction capacitor, C_{NR}, if present (see *Functional Block Diagrams*, Figure 1). This circuit allows for the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate for this configuration.

Note that for fastest start-up, apply V_{IN} first, and then drive the enable pin (EN) high. If EN is tied to IN, start-up is somewhat slower. The start-up switch is closed for approximately 135 μs. To ensure that C_{NR} is fully charged during start-up, use a 0.01-μF or smaller capacitor.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude, but increases the duration of the transient response. The transient response of the TPS799Lxx is enhanced by an active pull-down device that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pull-down device behaves like a 350-Ω resistor to ground.

UNDERVOLTAGE LOCKOUT (UVLO)

The TPS799Lxx uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that it typically ignores undershoot transients on the input if they are less than 50 μs in duration.

MINIMUM LOAD

The TPS799Lxx is stable with no output load. To meet the specified accuracy, a minimum load of 500 μA is required. With loads less than 500 μA at junction temperatures near +125°C, the output can drift up enough to cause the output pull-down device to turn on. The output pull-down device limits voltage drift to 5% typically; however, ground current can increase by approximately 50 μA. In typical applications, the junction cannot reach high temperatures at light loads because there is no noticeable dissipated power. The specified ground current is then valid at no load in most applications.

THERMAL INFORMATION

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS799Lxx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the device into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the head from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table near the front of this data sheet. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current time the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = \left(V_{IN} - V_{OUT}\right) \cdot I_{OUT} \quad (2)$$

PACKAGE MOUNTING

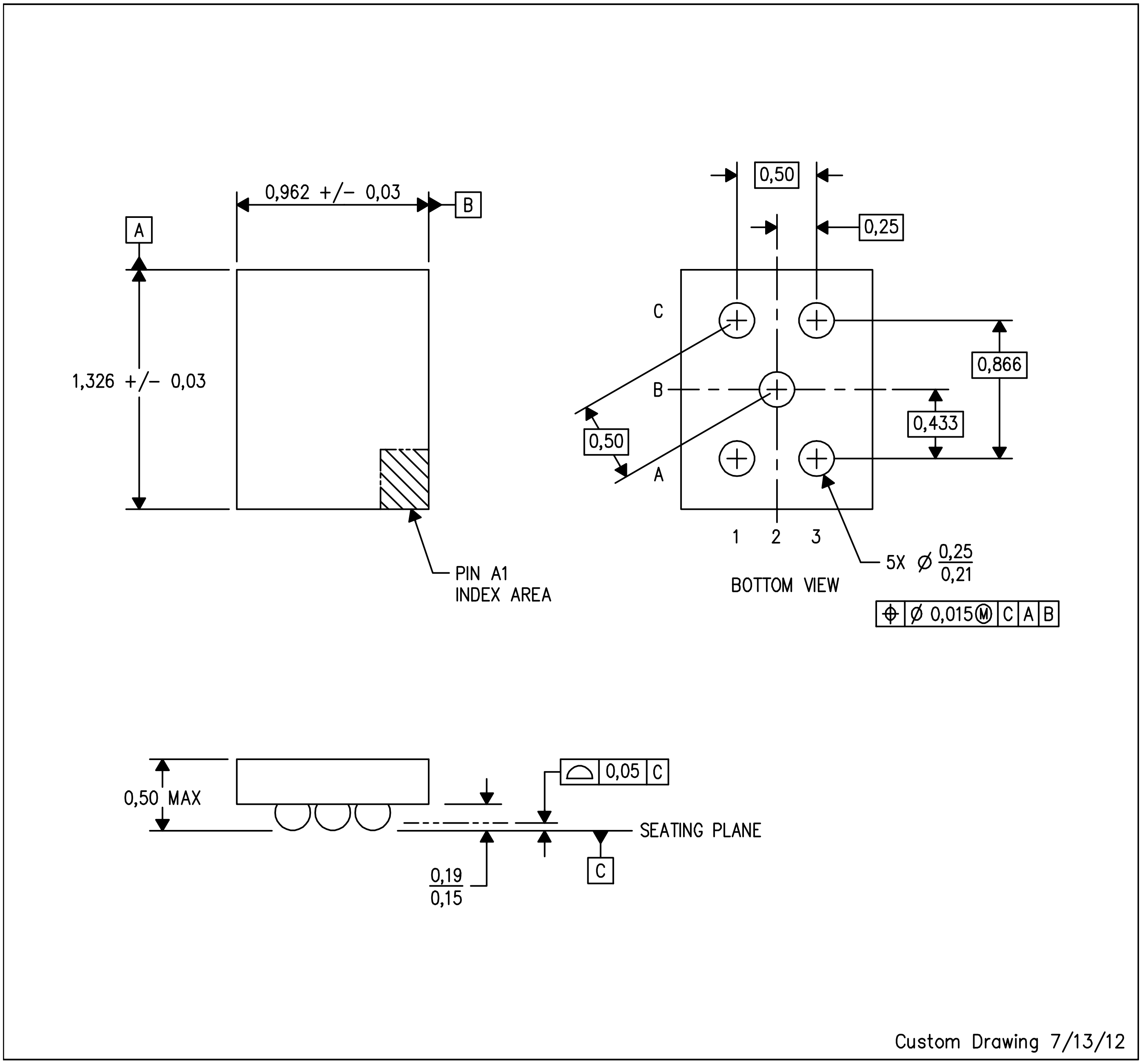
Solder pad footprint recommendations for the TPS799Lxx are available from the Texas Instruments' web site at www.ti.com.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from the poage numbers in this version.

Changes from Original (April 2012) to Revision A **Page**

TPS799L57YZY (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. This package contains Pb–free balls.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS799L57YZYR	ACTIVE	DSBGA	YZY	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	YF	Samples
TPS799L57YZYT	ACTIVE	DSBGA	YZY	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	YF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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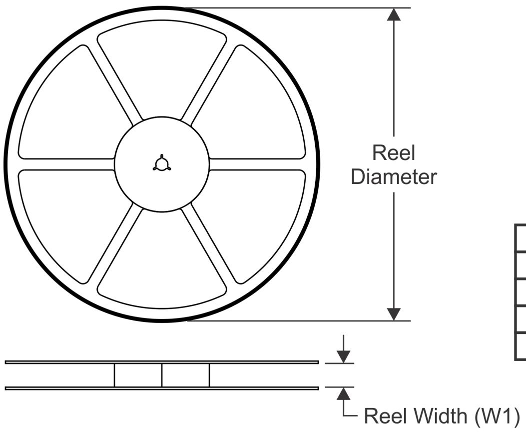
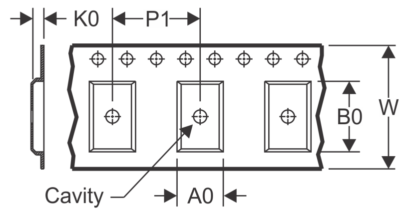
TAPE AND REEL INFORMATION

REEL DIMENSIONS

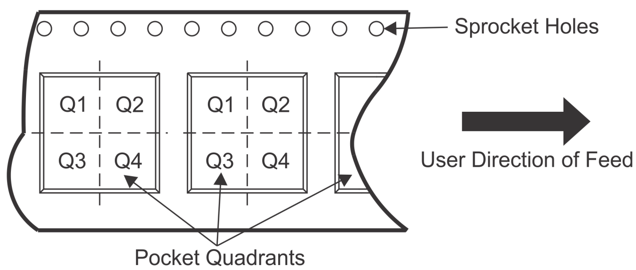


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

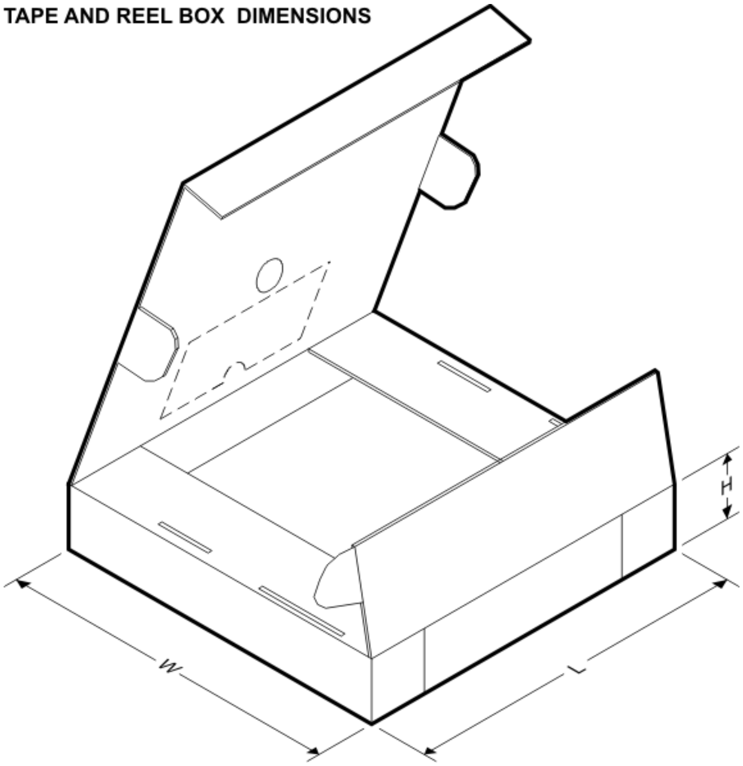
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS799L57YZYR	DSBGA	YZY	5	3000	180.0	8.4	1.08	1.45	0.61	4.0	8.0	Q1
TPS799L57YZYT	DSBGA	YZY	5	250	180.0	8.4	1.08	1.45	0.61	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS799L57YZYR	DSBGA	YZY	5	3000	182.0	182.0	17.0
TPS799L57YZYT	DSBGA	YZY	5	250	182.0	182.0	17.0

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