–20-V, –200-mA, Low-Noise NEGATIVE VOLTAGE REGULATOR

Check for Samples: TPS7A3401

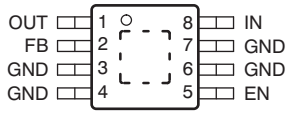
FEATURES

- **Input Voltage Range: –3 V to –20 V**
- **Noise:**
  - **80 μV_{RMS} (10 Hz to 100 kHz)**
- **Power-Supply Ripple Rejection:**
  - **50 dB (1 kHz)**
  - **≥ 27 dB (10 Hz to 1 MHz)**
- **Adjustable Output: ~ –1.18 V to –18 V**
- **Maximum Output Current: 200 mA**
- **Dropout Voltage: 500 mV at 100 mA**
- **Stable with Ceramic Capacitors ≥ 2.2 µF**
- **CMOS Logic-Level-Compatible Enable Pin**
- **Built-In, Fixed, Current-Limit and Thermal Shutdown Protection**
- **Available in High Thermal Performance MSOP-8 PowerPAD™ Package**
- **Operating Tempature Range: –40°C to +125°C**

APPLICATIONS

- **Cost-Effective Supply Rails for Op Amps, DACs, ADCs, and Other High-Precision Analog Circuitry**
- **Cost-Effective Post DC/DC Converter Regulation and Ripple Filtering**

DGN PACKAGE
3mm × 5mm MSOP-8 PowerPAD
(TOP VIEW)



DESCRIPTION

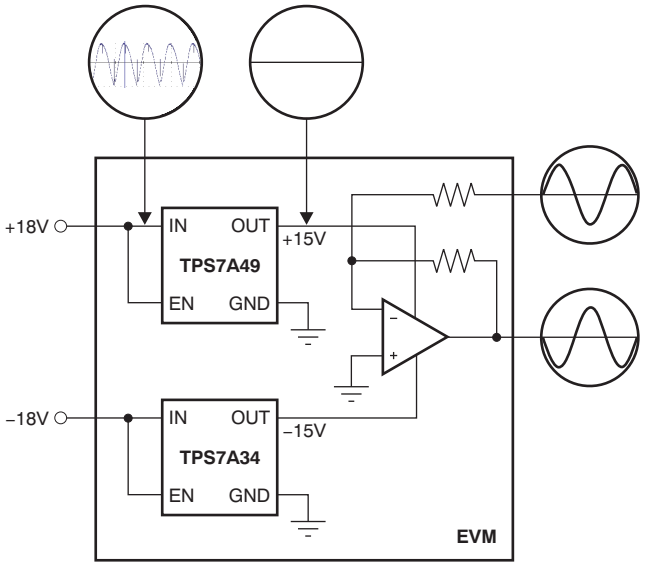
The TPS7A3401 is a negative, high-voltage (–20 V), low-noise linear regulator capable of sourcing a maximum load of 200 mA.

These linear regulators include a CMOS logic-level-compatible enable pin. Other features available include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A3401 is designed using bipolar technology, and is ideal for instrumentation applications where clean voltage rails are critical to improve system performance. This design makes it a cost-effective choice to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other analog circuitry.

In addition, the TPS7A3401 linear regulator is suitable for cost-effective, post dc/dc converter regulation. By filtering out the output voltage ripple inherent to dc/dc switching conversion, increased system performance is provided in instrumentation applications.

Typical Application



Post DC/DC Converter Regulation

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}
TPS7A34**xx** ***yyy*** **z**	**XX** is nominal output voltage (01 = Adjustable).(2) **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) For fixed -1.2-V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage	IN pin to GND pin	–22	+0.3	V
	OUT pin to GND pin	–22	+0.3	V
	OUT pin to IN pin	–0.3	+22	V
	FB pin to GND pin	–2	+0.3	V
	FB pin to IN pin	–0.3	+22	V
	EN pin to IN pin	–0.3	+22	V
	EN pin to GND pin	–22	+22	V
	NR/SS pin to IN pin	–0.3	+22	V
	NR/SS pin to GND pin	–2	+0.3	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–40	+125	°C
	Storage, T_{stg}	–65	+150	°C
Electrostatic discharge rating	Human body model (HBM)		1500	V
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS7A3401 DGN 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	55.09	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	8.47	
θ_{JB}	Junction-to-board thermal resistance	—	
ψ_{JT}	Junction-to-top characterization parameter	0.36	
ψ_{JB}	Junction-to-board characterization parameter	14.6	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS(1)

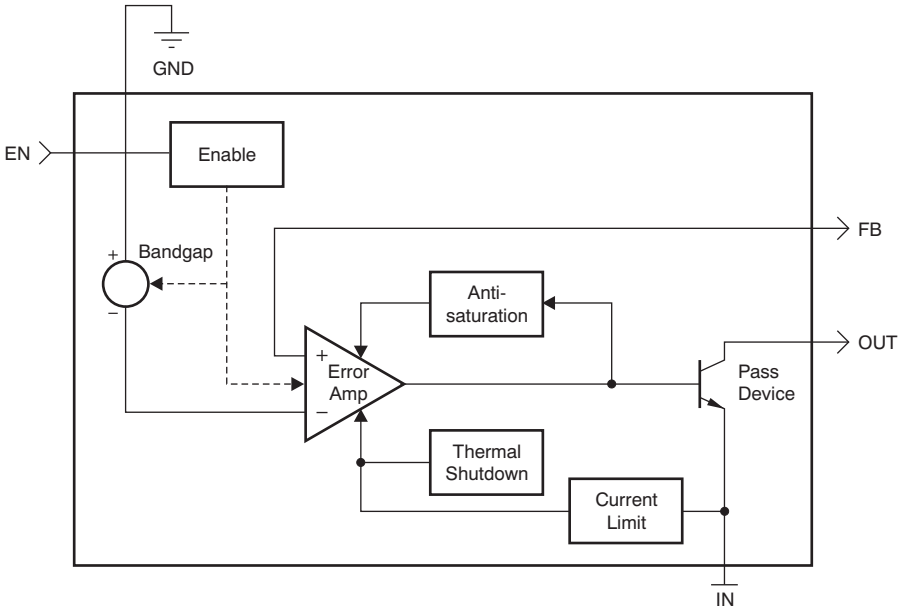
At T_J = –40°C to +125°C, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0$ V or $|V_{IN}| = 3.0$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and the FB pin tied to OUT, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TPS7A3401			UNIT
			MIN	TYP	MAX	
V_{IN}	Input voltage range		–20.0		–3.0	V
V_{REF}	Internal reference	T_J = +25°C, $V_{FB} = V_{REF}$	–1.202	–1.184	–1.166	V
V_{OUT}	Output voltage range(2)	$\|V_{IN}\| \geq \|V_{OUT(NOM)}\| + 1.0$ V	–18.0		V_{REF}	V
	Nominal accuracy	T_J = +25°C, $\|V_{IN}\| = \|V_{OUT(NOM)}\| + 0.5$ V	–1.5		+1.5	$\%V_{OUT}$
	Overall accuracy	$\|V_{OUT(NOM)}\| + 1.0$ V ≤ $\|V_{IN}\|$ ≤ 20 V 1 mA ≤ I_{OUT} ≤ 200 mA	–2.5		+2.5	$\%V_{OUT}$
$\left\|\frac{\Delta V_{OUT}(\Delta V_{IN})}{V_{OUT(NOM)}}\right\|$	Line regulation	T_J = +25°C, $\|V_{OUT(NOM)}\| + 1.0$ V ≤ $\|V_{IN}\|$ ≤ 20 V		0.14		$\%V_{OUT}$
$\left\|\frac{\Delta V_{OUT}(\Delta I_{OUT})}{V_{OUT(NOM)}}\right\|$	Load regulation	T_J = +25°C, 1 mA ≤ I_{OUT} ≤ 200 mA		0.04		$\%V_{OUT}$
$\|V_{DO}\|$	Dropout voltage	V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 100 mA		216		mV
		V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 200 mA		500	800	mV
I_{LIM}	Current limit	V_{OUT} = 90% $V_{OUT(NOM)}$	200	330	500	mA
I_{GND}	Ground current	I_{OUT} = 0 mA		55	100	µA
		I_{OUT} = 100 mA		950		µA
$\|I_{SHDN}\|$	Shutdown supply current	V_{EN} = +0.4 V		1.0	5.0	µA
		V_{EN} = –0.4 V		1.0	5.0	µA
I_{FB}	Feedback current(3)			14	100	nA
$\|I_{EN}\|$	Enable current	$V_{EN} = \|V_{IN}\| = \|V_{OUT(NOM)}\| + 1.0$ V		0.48	1.0	µA
		$V_{IN} = V_{EN}$ = –20 V		0.51	1.0	µA
		V_{IN} = –20 V, V_{EN} = +15 V		0.50	1.0	µA
V_{+EN_HI}	Positive enable high-level voltage	T_J = –40°C to +125°C	+2.0		+15	V
		T_J = –40°C to +85°C	+1.8		+15	
V_{+EN_LO}	Positive enable low- level voltage		0		+0.4	V
$V_{–EN\_HI}$	Negative enable high-level voltage		V_{IN}		–2.0	V
$V_{–EN\_LO}$	Negative enable low- level voltage		–0.4		0	V
V_{NOISE}	Output noise voltage	V_{IN} = –3 V, $V_{OUT(NOM)} = V_{REF}$, C_{OUT} = 10 µF, BW = 10 Hz to 100 kHz		80		μV_{RMS}
PSRR	Power-supply rejection ratio	V_{IN} = –6.2 V, $V_{OUT(NOM)}$ = –5 V, C_{OUT} = 10 µF, f = 1 kHz		50		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+170		°C
		Reset, temperature decreasing		+150		°C
T_J	Operating junction temperature range		–40		+125	°C

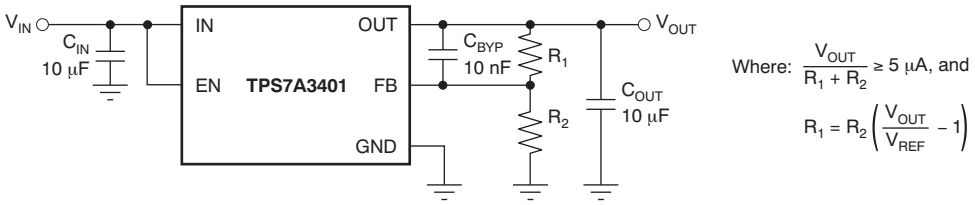
(1) At operating conditions, $V_{IN} \leq 0$ V, $V_{OUT(NOM)} \leq V_{REF} \leq 0$ V. At regulation, $V_{IN} \leq V_{OUT(NOM)} - |V_{DO}|$. $I_{OUT} > 0$ flows from OUT to IN.
(2) To ensure stability at no load conditions, a current from the feedback resistive network equal to or greater than 5 µA is required.
(3) $I_{FB} > 0$ flows into the device.

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



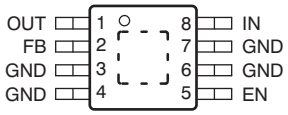
TYPICAL APPLICATION CIRCUIT



Maximize PSRR Performance and Minimize RMS Noise

PIN CONFIGURATION

DGN PACKAGE
MSOP-8
(TOP VIEW)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NO.	NAME	
1	OUT	Regulator output. A capacitor ≥ 10 µF must be tied from this pin to ground to assure stability.
2	FB	This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device.
3, 4, 6, 7	GND	Ground
5	EN	This pin turns the regulator on or off. If $V_{EN} \geq V_{+EN\_HI}$ or $V_{EN} \leq V_{-EN\_HI}$, the regulator is enabled. If $V_{+EN\_LO} \geq V_{EN} \geq V_{-EN\_LO}$, the regulator is disabled. The EN pin can be connected to IN, if not used. $\lvert V_{EN} \rvert \leq \lvert V_{IN} \rvert$.
8	IN	Input supply
PowerPAD		Must either be left open or tied to GND. Solder to printed circuit board (PCB) plane to enhance thermal performance.

TYPICAL CHARACTERISTICS

At T_J = –40°C to +125°C, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0$ V or $|V_{IN}| = 3.0$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and the FB pin tied to OUT, unless otherwise noted.

FEEDBACK VOLTAGE vs INPUT VOLTAGE

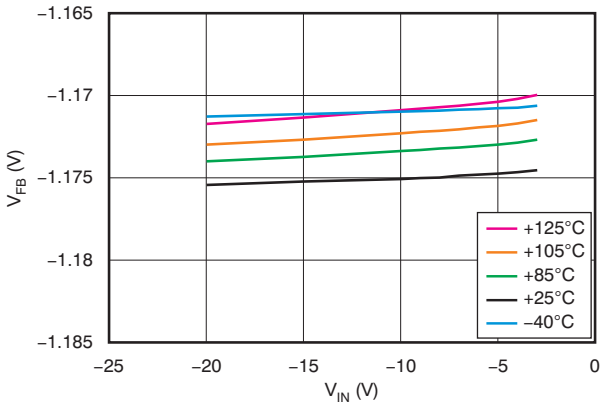


Figure 1.

FEEDBACK CURRENT vs TEMPERATURE

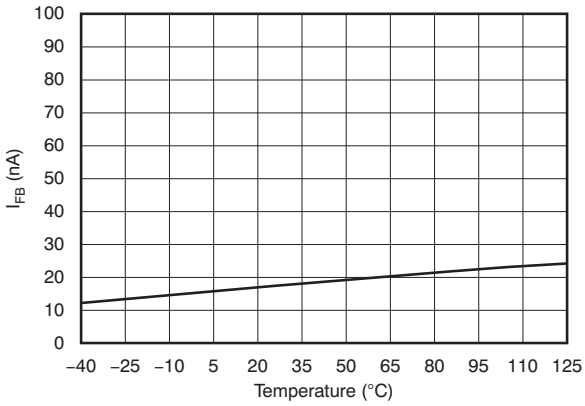


Figure 2.

GROUND CURRENT vs INPUT VOLTAGE

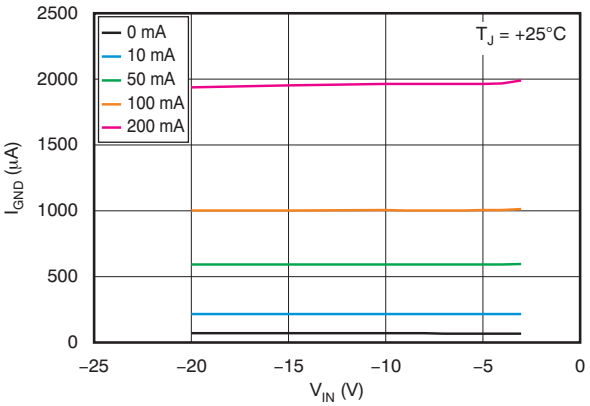


Figure 3.

GROUND CURRENT vs INPUT VOLTAGE

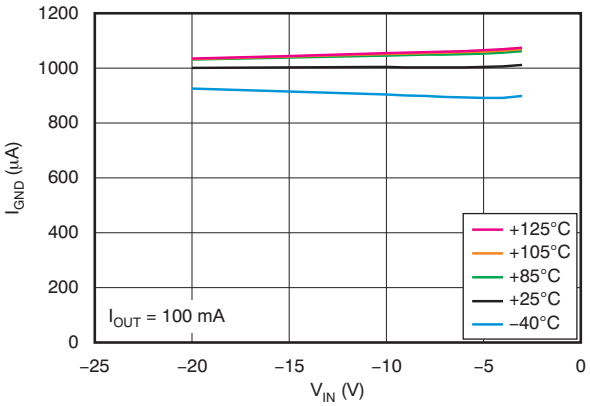


Figure 4.

GROUND CURRENT vs OUTPUT CURRENT

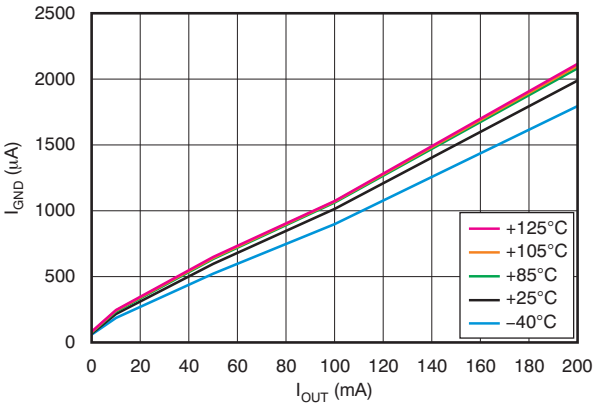


Figure 5.

ENABLE CURRENT vs ENABLE VOLTAGE

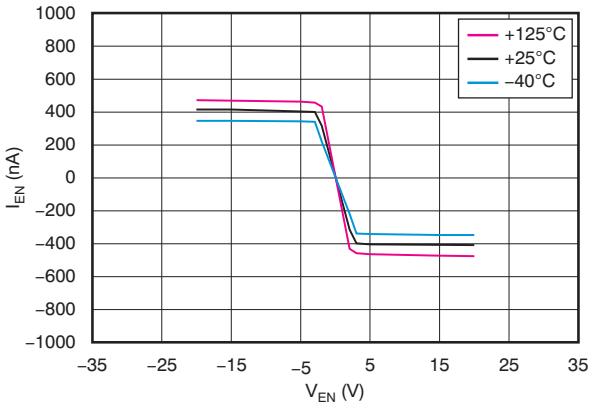


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_J = –40°C to +125°C, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0$ V or $|V_{IN}| = 3.0$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and the FB pin tied to OUT, unless otherwise noted.

QUIESCENT CURRENT vs INPUT VOLTAGE

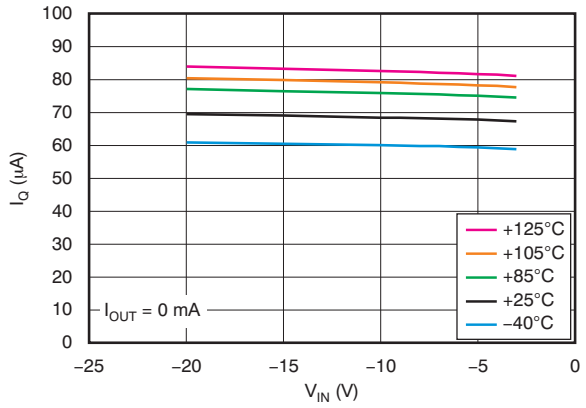


Figure 7.

SHUTDOWN CURRENT vs INPUT VOLTAGE

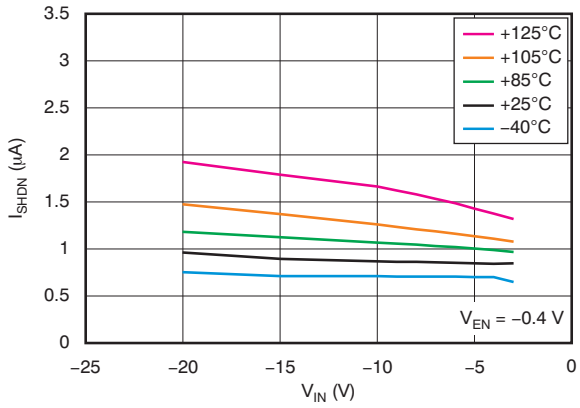


Figure 8.

DROPOUT VOLTAGE vs OUTPUT CURRENT

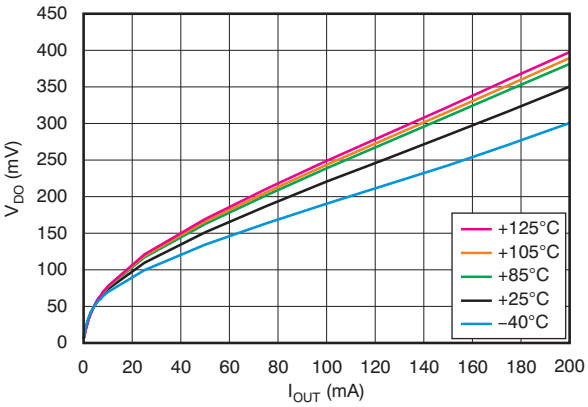


Figure 9.

DROPOUT VOLTAGE vs TEMPERATURE

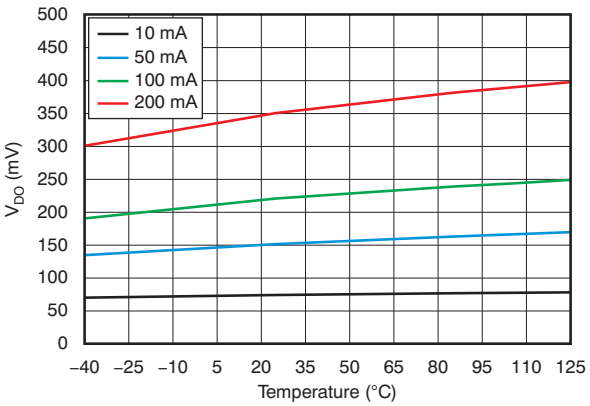


Figure 10.

CURRENT LIMIT vs INPUT VOLTAGE

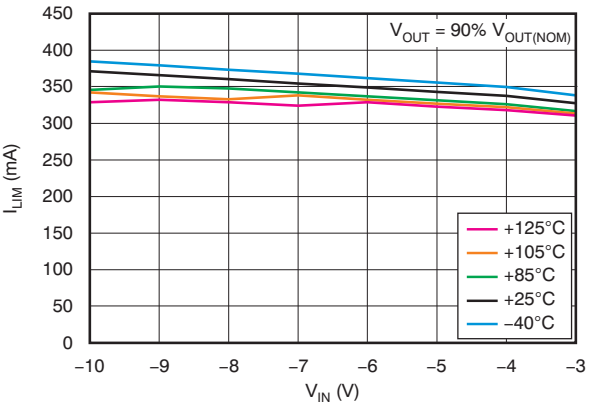


Figure 11.

CURRENT LIMIT vs TEMPERATURE

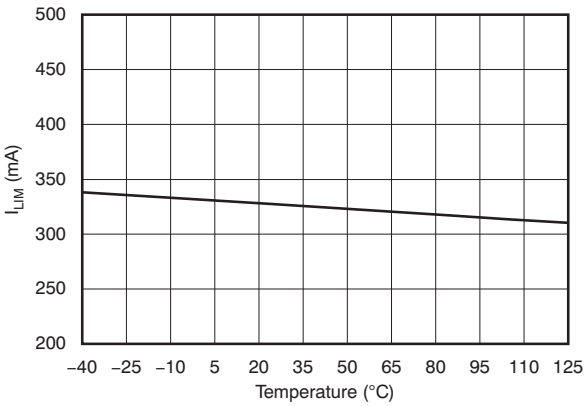


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_J = –40°C to +125°C, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0$ V or $|V_{IN}| = 3.0$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and the FB pin tied to OUT, unless otherwise noted.

ENABLE THRESHOLD VOLTAGE vs TEMPERATURE

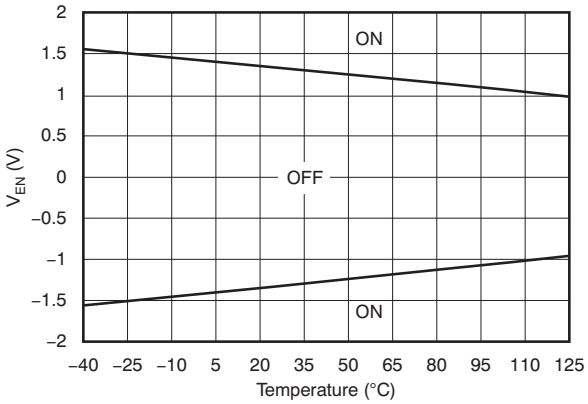


Figure 13.

LINE REGULATION

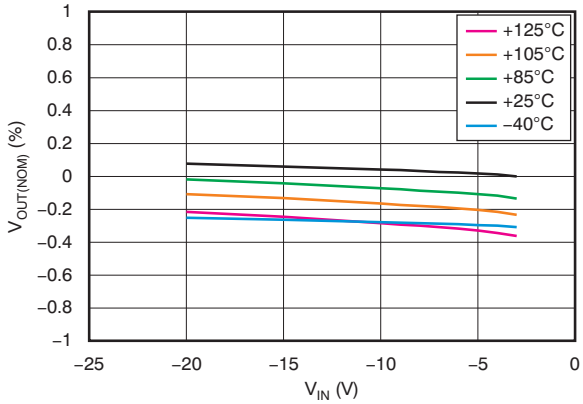


Figure 14.

POWER-SUPPLY REJECTION RATIO

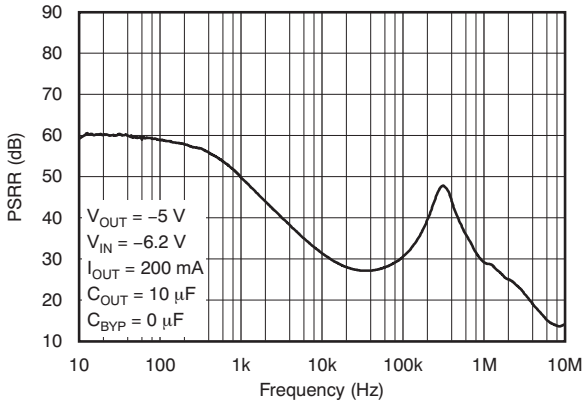


Figure 15.

LOAD REGULATION

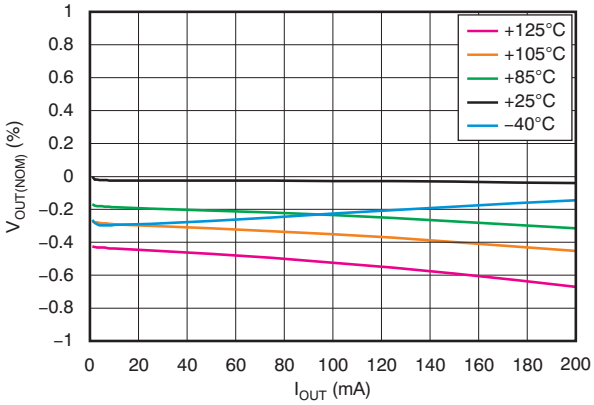


Figure 16.

OUTPUT SPECTRAL NOISE DENSITY

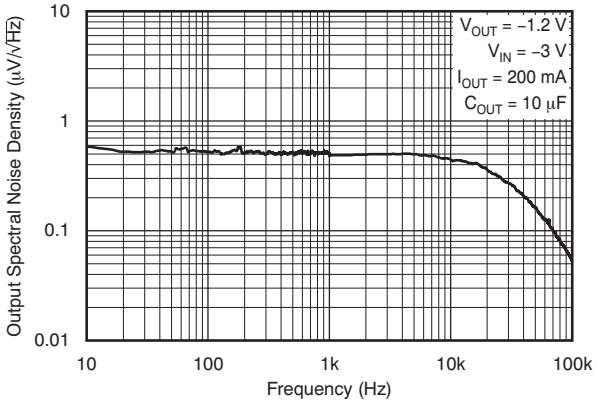


Figure 17.

THEORY OF OPERATION

GENERAL DESCRIPTION

The TPS7A3401 belongs to a new generation of linear regulators that use an innovative bipolar process to achieve low noise and high PSRR levels at a wide input voltage range. These features, combined with a high thermal performance MSOP-8 with PowerPAD package, make this device ideal for analog applications.

ADJUSTABLE OPERATION

The TPS7A3001 has an output voltage range of –1.184 V to –17 V. The nominal output voltage of the device is set by two external resistors, as shown in Figure 18.

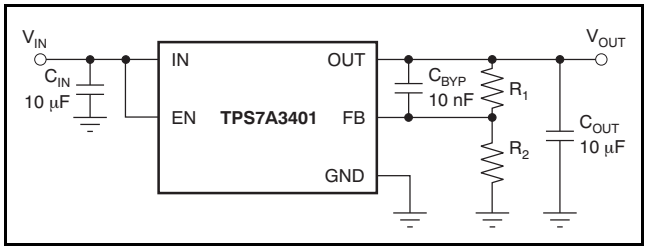


Figure 18. Adjustable Operation for Maximum AC Performance

R_1 and R_2 can be calculated for any output voltage range using the formula shown in Equation 1. To ensure stability under no load conditions, this resistive network must provide a current equal to or greater than 5 µA.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right), \quad \text{where} \quad \frac{V_{OUT}}{R_1 + R_2} \geq 5\ \mu A \tag{1}$$

If greater voltage accuracy is required, take into account the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

ENABLE PIN OPERATION

The TPS7A3401 provides a dual polarity enable pin (EN) that turns on the regulator when $|V_{EN}| > 2.0$ V, whether the voltage is positive or negative, as shown in Figure 19.

This functionality allows for different system power management topologies:

- Connecting the EN pin directly to a negative voltage, such as V_{IN}, or
- Connecting the EN pin directly to a positive voltage, such as the output of digital logic circuitry.

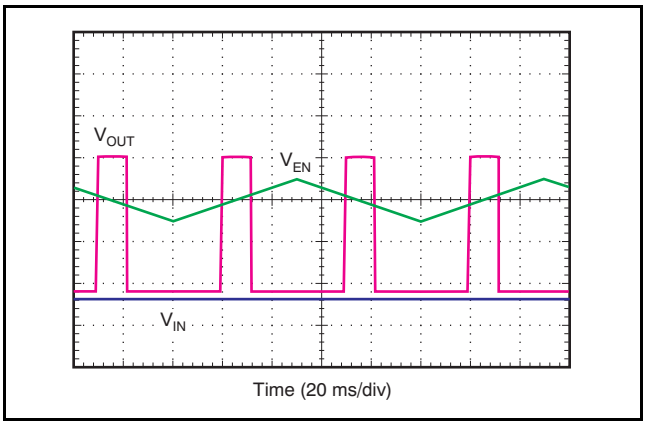


Figure 19. Enable Pin Positive/Negative Threshold

CAPACITOR RECOMMENDATIONS

Low equivalent series resistance (ESR) capacitors should be used for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are more cost-effective and are available in higher values.

Note that high ESR capacitors may degrade PSRR.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

The TPS7A3401 negative, high-voltage linear regulator achieves stability with a minimum input and output capacitance of 2.2 µF.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

APPLICATION INFORMATION

POWER FOR PRECISION ANALOG

One of the primary TPS7A3401 applications is to provide low-noise voltage rails to analog circuitry in order to improve system accuracy and precision.

The TPS7A3401 negative high-voltage linear regulator provides a low-noise voltage rail to analog circuitry, such as operational amplifiers, ADCs, and DACs.

Because of the low noise levels at high voltages, analog circuitry with high-voltage input supplies can be used. This characteristic allows for analog solutions to optimize the voltage range, thereby maximizing system accuracy.

POST DC/DC CONVERTER FILTERING

Most of the time, the voltage rails available in a system do not match the voltage specifications demanded by one or more of its circuits; these rails must be stepped up or down, depending on specific voltage requirements.

DC/DC converters are generally the preferred solution to step up or down a voltage rail when current consumption is not negligible. They offer high efficiency with minimum heat generation, but they have one primary disadvantage: they introduce a high-frequency component, and the associated harmonics, on top of the dc output signal.

This high-frequency component, if not filtered properly, degrades analog circuitry performance, reducing overall system accuracy and precision.

The TPS7A3401 offers a wide-bandwidth, high power-supply rejection ratio (PSRR). It is highly recommended to use the maximum performance schematic shown in Figure 18. Also, verify that the fundamental frequency (and its first harmonic, if possible) is within the bandwidth of the regulator PSRR, shown in Figure 15.

LAYOUT

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS7A3401 are available at the end of this product datasheet and at www.ti.com.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized in order to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, C_{BYP}) must be placed as close as possible to the device and on the same side of the printed circuit board (PCB) as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for the TPS7A30 evaluation board, available at www.ti.com.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +170°C, allowing the device to cool. When the junction temperature cools to approximately +150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of +125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A3401 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A3401 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT})\, I_{OUT} \quad (2)$$

SUGGESTED LAYOUT AND SCHEMATIC

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

The GND pin should be tied directly to the PowerPAD under the IC. The PowerPAD should be connected to any internal PCB ground planes using multiple vias directly under the IC.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS7A3401DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPKQ	Samples
TPS7A3401DGNT	ACTIVE	MSOP-PowerPAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPKQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

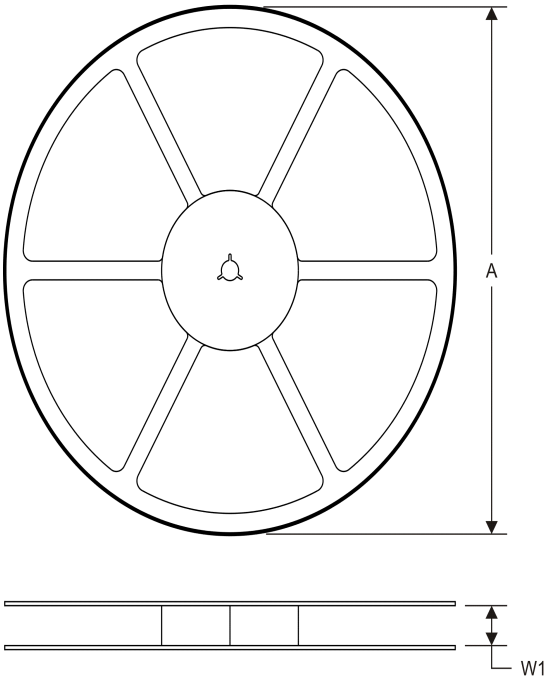
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

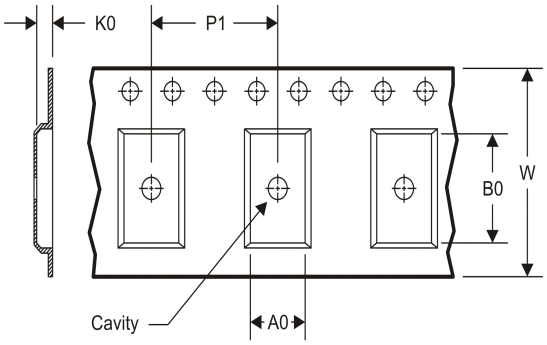
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



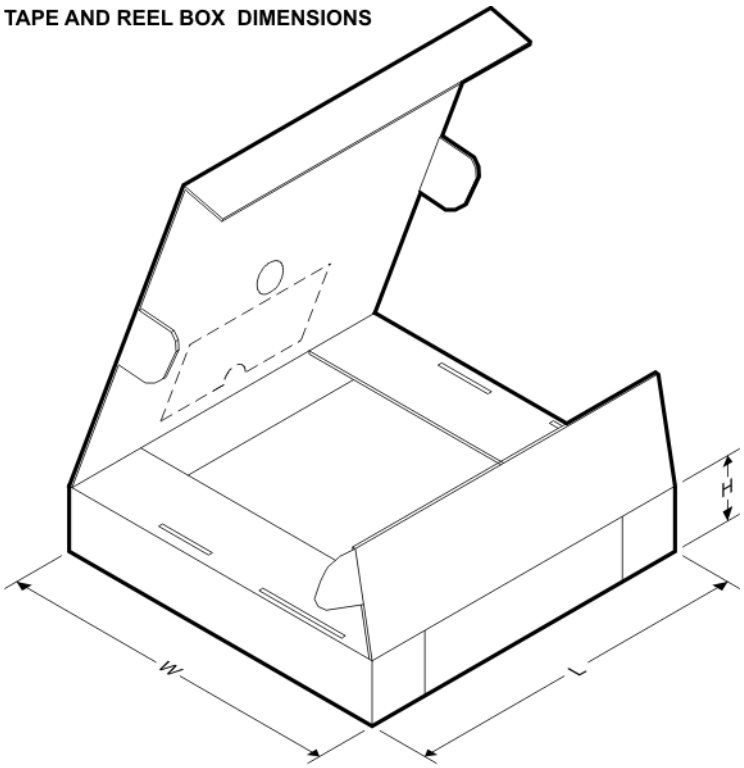
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A3401DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A3401DGNT	MSOP-Power PAD	DGN	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

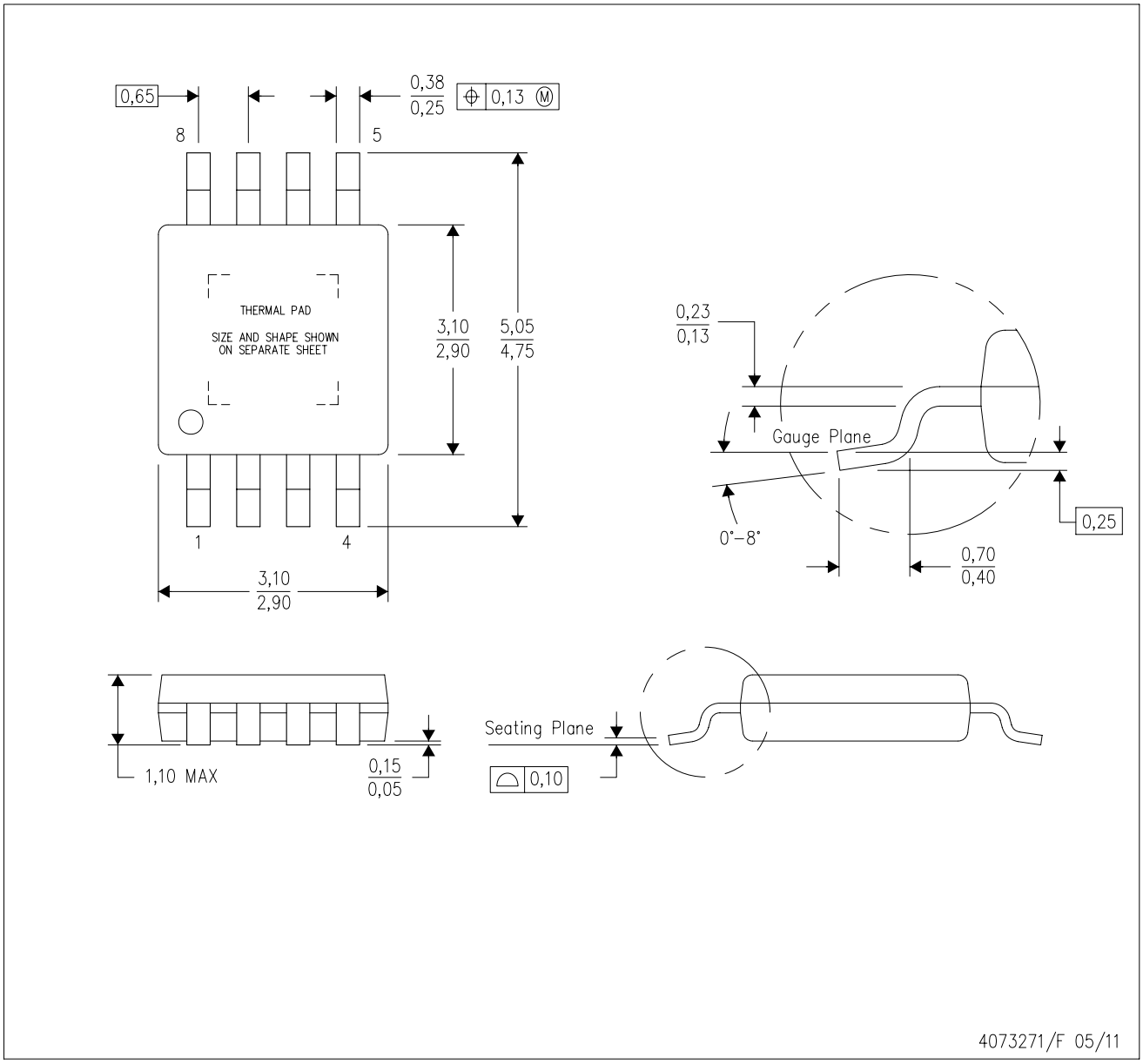
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A3401DGNR	MSOP-PowerPAD	DGN	8	2500	367.0	367.0	35.0
TPS7A3401DGNT	MSOP-PowerPAD	DGN	8	250	210.0	185.0	35.0

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

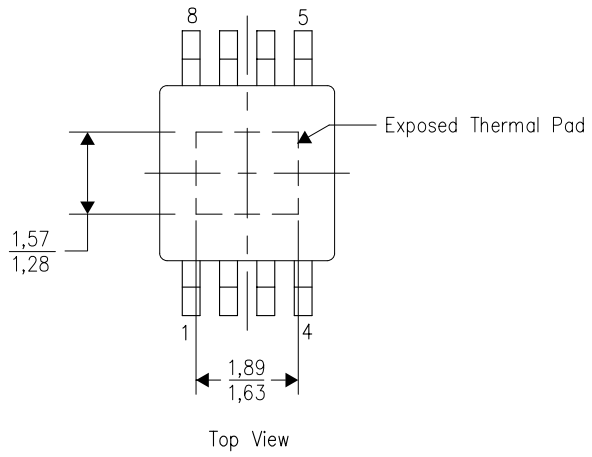
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

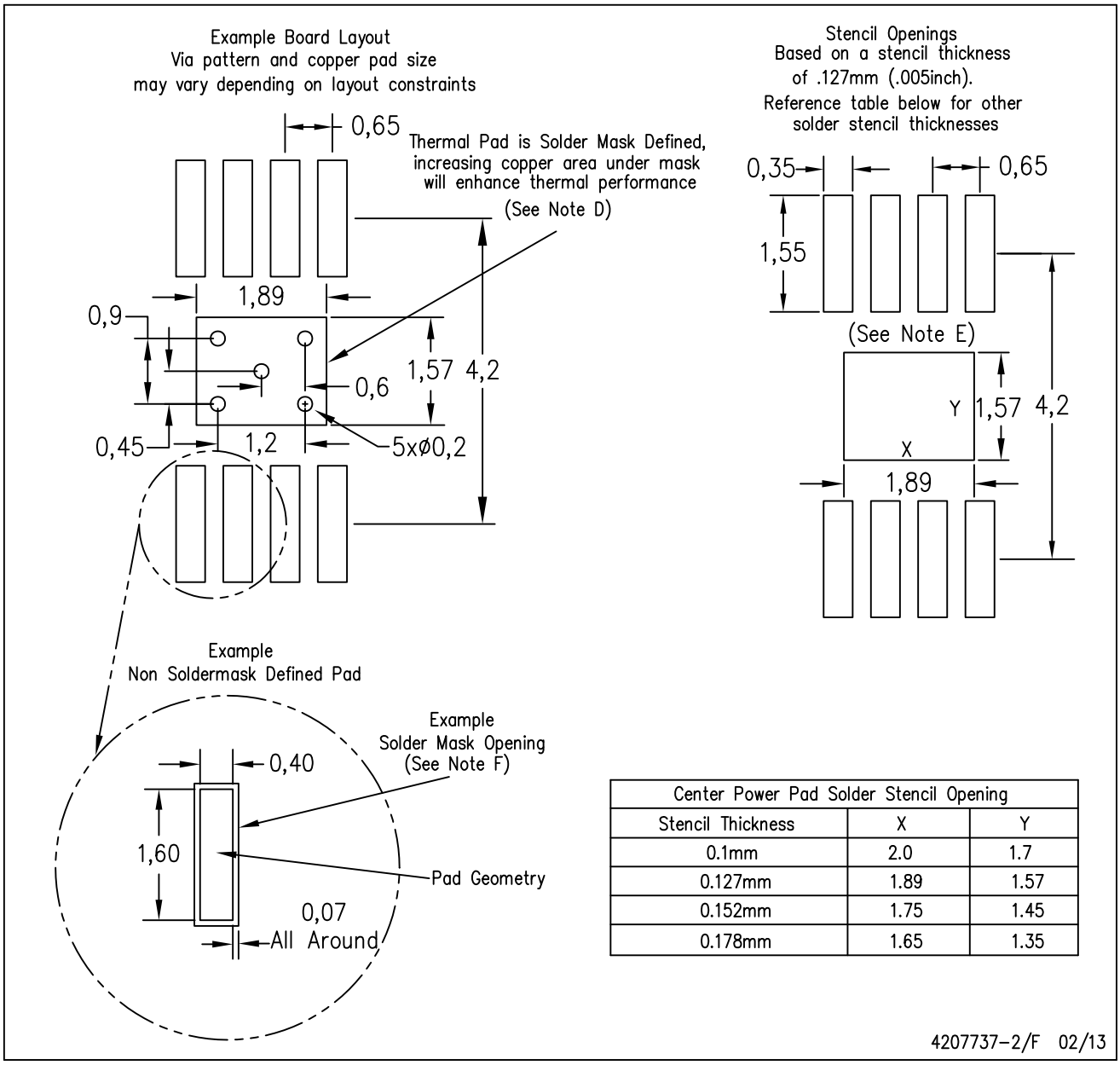
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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