

## Very Low Input, Very Low Dropout 3-Amp Regulator With Enable

Check for Samples: [TPS7A7002](#)

### FEATURES

- Input Voltage as Low as 1.425 V
- 380-mV Maximum Dropout at 2 A
- 600-mV Maximum Dropout at 3 A
- Adjustable Output from 0.5 V
- Protections: Current Limit and Thermal Shutdown
- Enable Pin
- 1-μA Quiescent Current in Shutdown Mode
- Full Industrial Temperature Range
- Available in an SOIC-8, Fully RoHS-Compliant Package

### APPLICATIONS

- Telecom/Networking Cards
- Motherboards/Peripheral Cards
- Industrial
- Wireless Infrastructure
- Set-Top Boxes
- Medical Equipment
- Notebook Computers
- Battery-Powered Systems

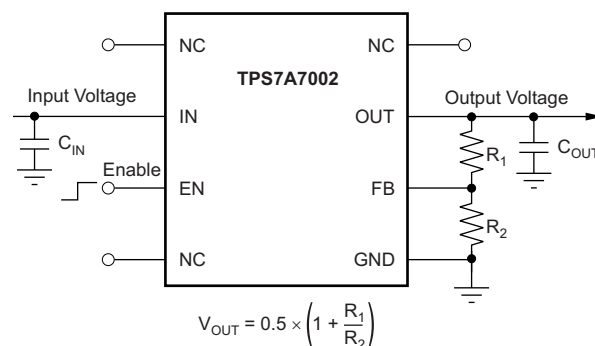
### DESCRIPTION

The TPS7A7002 is a high-performance, positive-voltage, low-dropout (LDO) regulator designed for use in applications requiring very-low input voltage and very-low dropout voltage at up to 3 A. The device operates with a single input voltage as low as 1.425 V, and with an output voltage programmable to as low as 0.5 V. The output voltage can be set using an external divider.

The TPS7A7002 features ultralow dropout, ideal for applications where  $V_{OUT}$  is very close to  $V_{IN}$ . Additionally, the TPS7A7002 has an enable pin for further reduced power dissipation while in Shutdown mode. The TPS7A7002 provides excellent regulation over variations in line, load, and temperature.

The TPS7A7002 is available in an SOIC-8 PowerPAD™ package.

### TYPICAL APPLICATION



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	V <sub>OUT</sub>
TPS7A7002yyyz	YYY is package designator. Z is package quantity.

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage	IN, OUT	–0.3	+7.0	V
	EN, FB	–0.3	V <sub>IN</sub> + 0.3 <sup>(2)</sup>	V
Current	OUT	Internally limited		A
Temperature	Operating virtual junction, T <sub>J</sub>	–55	+150	°C
	Storage, T <sub>stg</sub>	–55	+150	°C
Electrostatic discharge (ESD) ratings <sup>(3)</sup>	Human body model (HBM, JESD22-A114A)		2	kV
	Charged device model (CDM, JESD22-C101B.01)		500	V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The absolute maximum rating is V<sub>IN</sub> + 0.3 V or +7.0 V, whichever is smaller.
- (3) ESD testing is performed according to the respective JESD22 JEDEC standard.

### RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage	1.425		6.5	V
Ambient temperature range	–40		+105	°C
Junction temperature range	–40		+125	°C
Maximum output current			3	A

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS7A7002	UNITS
		DDA (SOIC)	
		8 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	46.4	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	54.2	
θ <sub>JB</sub>	Junction-to-board thermal resistance	29.9	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	10.2	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	29.8	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	6.8	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953A](http://www.ti.com/lit/an/spra953a).

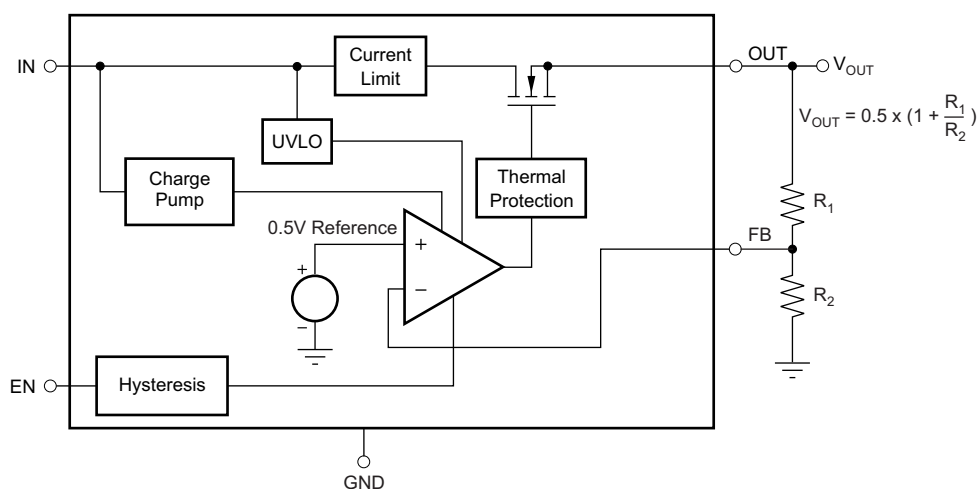
## ELECTRICAL CHARACTERISTICS

Over the full operating temperature range (see [Recommended Operating Conditions](#)),  $V_{EN} = 1.1\text{ V}$ ,  $V_{FB} = V_{OUT}^{(1)}$ ,  $1.425\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ ,  $10\text{ }\mu\text{A} \leq I_{OUT} \leq 3\text{ A}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TPS7A7002			UNIT
			MIN	TYP	MAX	
INPUT VOLTAGE						
I <sub>GND</sub>	GND pin current (small)	V <sub>IN</sub> = 3.3 V, 50-Ω load resistor between OUT and GND			3	mA
	GND pin current (shutdown)	V <sub>IN</sub> = 6.5 V, V <sub>EN</sub> = 0 V			5	μA
OUTPUT VOLTAGE						
V <sub>OUT</sub>	Output voltage accuracy <sup>(2)(3)</sup>	V <sub>IN</sub> = V <sub>OUT</sub> + 0.5 V <sup>(4)</sup> , I <sub>OUT</sub> = 10 mA	−2.0		+2.0	%
		V <sub>IN</sub> = 1.8 V, I <sub>OUT</sub> = 0.8 A, 0°C ≤ T <sub>J</sub> = T <sub>A</sub> ≤ +85°C				
		I <sub>OUT</sub> = 10 mA	−3.0		+3.0	
ΔV <sub>O(ΔVI)</sub>	Line regulation	I <sub>OUT</sub> = 10 mA		0.2	0.4	%/V
ΔV <sub>O(ΔIO)</sub>	Load regulation <sup>(3)</sup>	10 mA ≤ I <sub>OUT</sub> ≤ 3 A		0.25	0.75	%/A
V <sub>DO</sub>	Dropout voltage <sup>(5)</sup>	I <sub>OUT</sub> = 1.0 A, 0.5 V ≤ V <sub>OUT</sub> ≤ 5.0 V			200	mV
		I <sub>OUT</sub> = 2.0 A, 0.5 V ≤ V <sub>OUT</sub> ≤ 5.0 V			380	
		I <sub>OUT</sub> = 3.0 A, 0.5 V ≤ V <sub>OUT</sub> ≤ 4.8 V			600	
I <sub>LIM</sub>	Output current limit	V <sub>IN</sub> = 1.425 V, V <sub>OUT</sub> = 0.9 × V <sub>OUT(NOM)</sub>	3.36			A
FEEDBACK						
V <sub>REF</sub>	Reference voltage accuracy	V <sub>IN</sub> = 3.3 V, V <sub>FB</sub> = V <sub>OUT</sub> , I <sub>OUT</sub> = 10 mA	0.490	0.500	0.510	V
I <sub>FB</sub>	FB pin current	V <sub>FB</sub> = 0.5 V			1	μA
ENABLE						
I <sub>EN</sub>	EN pin current	V <sub>EN</sub> = 0 V, V <sub>IN</sub> = 3.3 V			0.2	μA
V <sub>IL<sub>EN</sub></sub>	EN pin input low (disable)	V <sub>IN</sub> = 3.3 V	0		0.5	V
V <sub>IH<sub>EN</sub></sub>	EN pin input high (enable)	V <sub>IN</sub> = 3.3 V	1.1		V <sub>IN</sub>	V
TEMPERATURE						
T <sub>SD</sub>	Thermal shutdown temperature	Shutdown, temperature increasing		+160		°C
		Reset, temperature decreasing		+140		°C

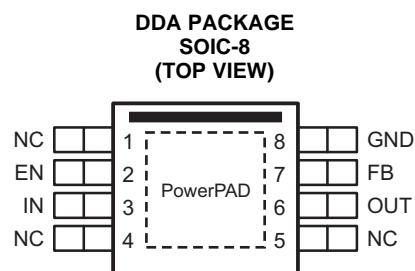
- (1) When setting  $V_{OUT}$  to a value other than 0.5 V, connect  $R_1$  and  $R_2$  to the FB pin using  $10\text{ k}\Omega \leq R_2 \leq 50\text{ k}\Omega$  resistors. See [Figure 1](#) for details of  $R_1$  and  $R_2$ .
- (2) Accuracy does not include error on feedback resistors  $R_1$  and  $R_2$ .
- (3) TPS7A7002 is not tested at  $V_{OUT} = 0.5\text{ V}$ ,  $2.3\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ , and  $500\text{ mA} \leq I_{OUT} \leq 3\text{ A}$  because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply to any application condition that exceeds the power dissipation limit of the package.
- (4)  $V_{IN} = V_{OUT} + 0.5\text{ V}$  or  $1.425\text{ V}$ , whichever is greater.
- (5)  $V_{DO} = V_{IN} - V_{OUT}$  with  $V_{FB} = \text{GND}$  configuration.

## FUNCTIONAL BLOCK DIAGRAM



**Figure 1. Adjustable Output Voltage Version**

## PIN CONFIGURATIONS



## PIN DESCRIPTIONS

NAME	PIN #	DESCRIPTION
EN	2	Enable input. Pulling this pin below 0.5 V turns the regulator off. Connect to $V_{IN}$ if not being used.
FB	7	This pin is the output voltage feedback input through voltage dividers. See <a href="#">Table 1</a> for more details.
GND	8	Ground pin
IN	3	Unregulated supply voltage pin. It is recommended to connect an input capacitor to this pin.
NC	1, 4, 5	Not internally connected. The NC pins are not connected to any electrical node. It is recommended to connect the NC pins to large-area planes.
OUT	6	Regulated output pin. A 4.7- $\mu$ F or larger capacitor of any type is required for stability.
PowerPAD		It is strongly recommended to connect the thermal pad to a large-area ground plane. If an electrically floating, dedicated thermal plane is available, the thermal pad can also be connected to it.

## TYPICAL CHARACTERISTICS

For all fixed voltage versions and an adjustable version at  $T_J = +25^\circ\text{C}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 10\ \mu\text{F}$ ,  $C_{OUT} = 10\ \mu\text{F}$ , and using the component values in Table 1, unless otherwise noted.

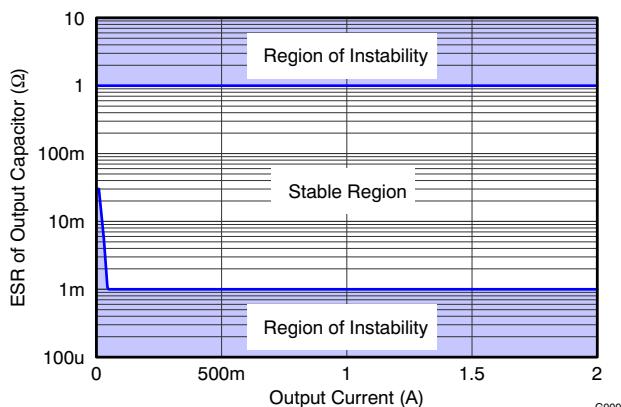


Figure 2. STABILITY CURVE ( $C_{OUT} = 10\ \mu\text{F}$ )

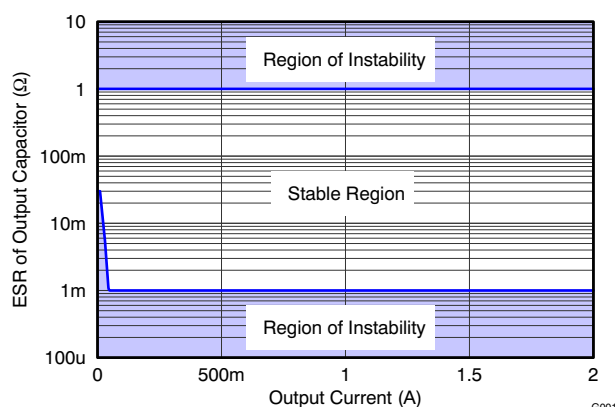


Figure 3. STABILITY CURVE ( $C_{OUT} = 100\ \mu\text{F}$ )

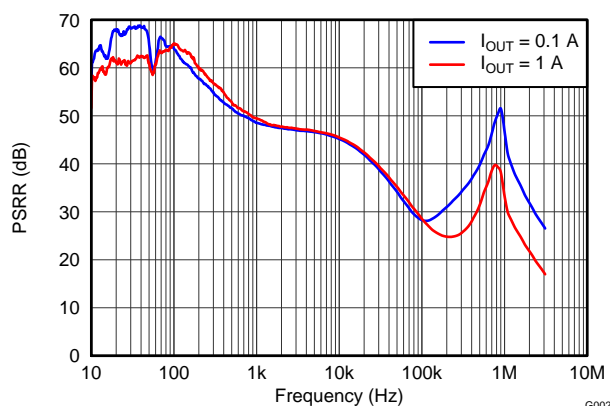


Figure 4. POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY  
( $V_{IN} = 5.0\ \text{V}$ ,  $V_{OUT} = 3.3\ \text{V}$ )

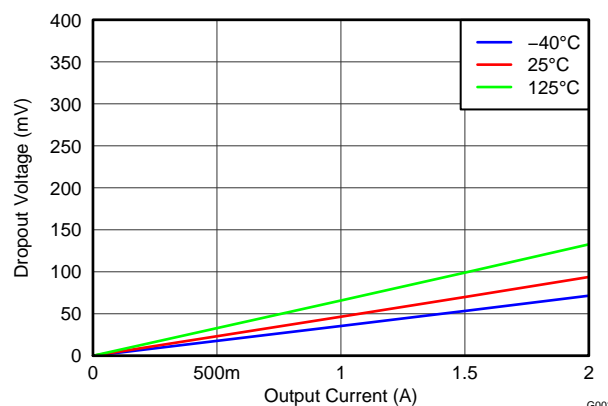


Figure 5. DROPOUT VOLTAGE vs OUTPUT CURRENT  
( $V_{OUT} = 3.3\ \text{V}$ )

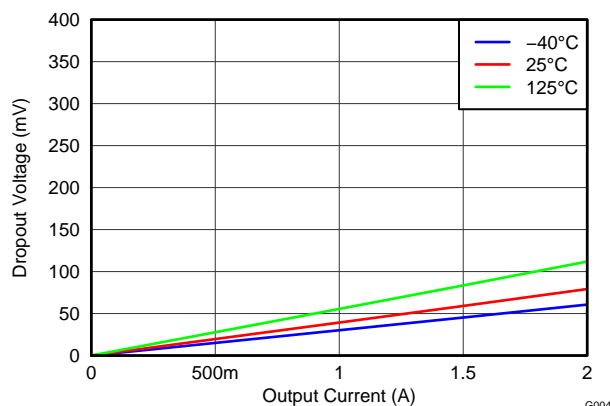


Figure 6. DROPOUT VOLTAGE vs OUTPUT CURRENT  
( $V_{OUT} = 1.6\ \text{V}$ )

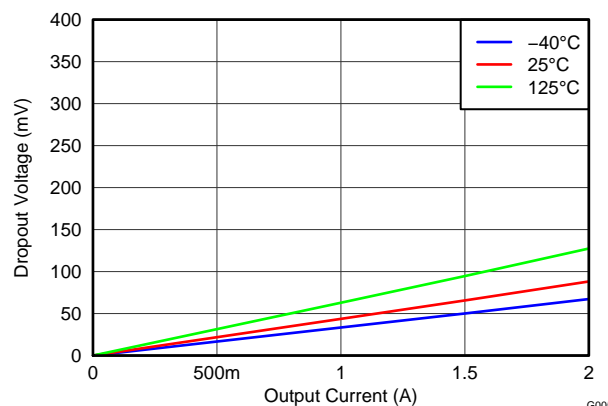


Figure 7. DROPOUT VOLTAGE vs OUTPUT CURRENT  
( $V_{OUT} = 1.4\ \text{V}$ )

## APPLICATION INFORMATION

### OVERVIEW

The TPS7A7002 offers a high current supply with very-low dropout voltage. The TPS7A7002 is designed to minimize the required component count for a simple, small-size, and low-cost solution.

### INPUT CAPACITOR (IN)

When designing your printed circuit board (PCB), an input capacitor is not required for stability; however, it is recommended to connect a 1-μF to 10-μF low equivalent series resistance (ESR) capacitor across IN and GND as close as possible to the device.

### OUTPUT CAPACITOR (OUT)

The device is designed to be stable with an output capacitance of 4.7 μF or larger. For a good load transient response, a 10-μF or larger ceramic capacitor is recommended. Connect the output capacitor across OUT and GND as close as possible to the device.

### FEEDBACK RESISTORS (FB)

The voltage on the FB pin sets the output voltage and is determined by the values of  $R_1$  and  $R_2$ . The values of  $R_1$  and  $R_2$  can be calculated for any voltage using the formula given in [Equation 1](#):

$$V_{OUT} = \frac{(R_1 + R_2)}{R_2} \times 0.500 \quad (1)$$

[Table 1](#) shows the recommended resistor values for the best performance of the TPS7A7002. In [Table 1](#), E96 series resistors are used. For the actual design, pay attention to any resistor error factors.

**Table 1. Sample Resistor Values for Common Output Voltages**

$V_{OUT}$	$R_1$	$R_2$
1.0 V	30.1 kΩ	30.1 kΩ
1.2 V	42.2 kΩ	30.1 kΩ
1.5 V	60.4 kΩ	30.1 kΩ
1.8 V	78.7 kΩ	30.1 kΩ
2.5 V	121 kΩ	30.1 kΩ
3.0 V	150 kΩ	30.1 kΩ
3.3 V	169 kΩ	30.1 kΩ
5.0 V	274 kΩ	30.1 kΩ

### ENABLE (EN)

The enable pin (EN) is an active-high logic input. When it is logic low, the device turns off, and the consumption current is less than 1 μA. When it is logic high, the device turns on. The EN pin is required to be connected to a logic high or logic low level.

When the enable function is not required, connect EN to VIN.

### INTERNAL CURRENT LIMIT

The TPS7A7002 internal current limit helps protect the regulator during fault conditions. During a current-limit condition, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

Powering on the device with the enable pin, or increasing the input voltage above the minimum operating voltage while a low-impedance short exists on the output of the device, may result in a sequence of high-current pulses from the input to the output of the device. The energy consumed by the device is minimal during these events; therefore, there is no failure risk. Additional input capacitance helps to mitigate the load transient requirement of the upstream supply during these events.

## THERMAL INFORMATION

### Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is enabled again.

The internal protection circuitry of the TPS7A7002 is designed to protect against overload conditions. It is not intended to replace proper heat sinking. Continuously running the TPS7A7002 into thermal shutdown degrades device reliability.

### Power Dissipation

Power dissipation of the device depends on the input voltage and load conditions and can be calculated using [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the SOIC (DDA) package, the primary conduction path for heat is through the exposed pad to the PCB. The pad can either be connected to ground or left floating; however, to prevent overheating, attach the device to an appropriate amount of copper PCB area. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device, and can be calculated using [Equation 3](#):

$$R_{\theta JA} = \left( \frac{+125^{\circ}\text{C} - T_A}{P_D} \right) \quad (3)$$

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2013) to Revision B	Page
<ul style="list-style-type: none"><li>Changed data sheet status from product preview to production data .....</li></ul>	1
<ul style="list-style-type: none"><li>Added pin 1 identifier (black bar) to pinout diagram .....</li></ul>	4
<hr/>	
Changes from Original (May 2013) to Revision A	Page
<ul style="list-style-type: none"><li>Changed product preview data sheet; added new text to <i>Internal Current Limit</i> section .....</li></ul>	6



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A7002DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SJA	<a href="#">Samples</a>
TPS7A7002DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SJA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A7002DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A7002DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - This package complies to JEDEC MS-012 variation BA

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DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

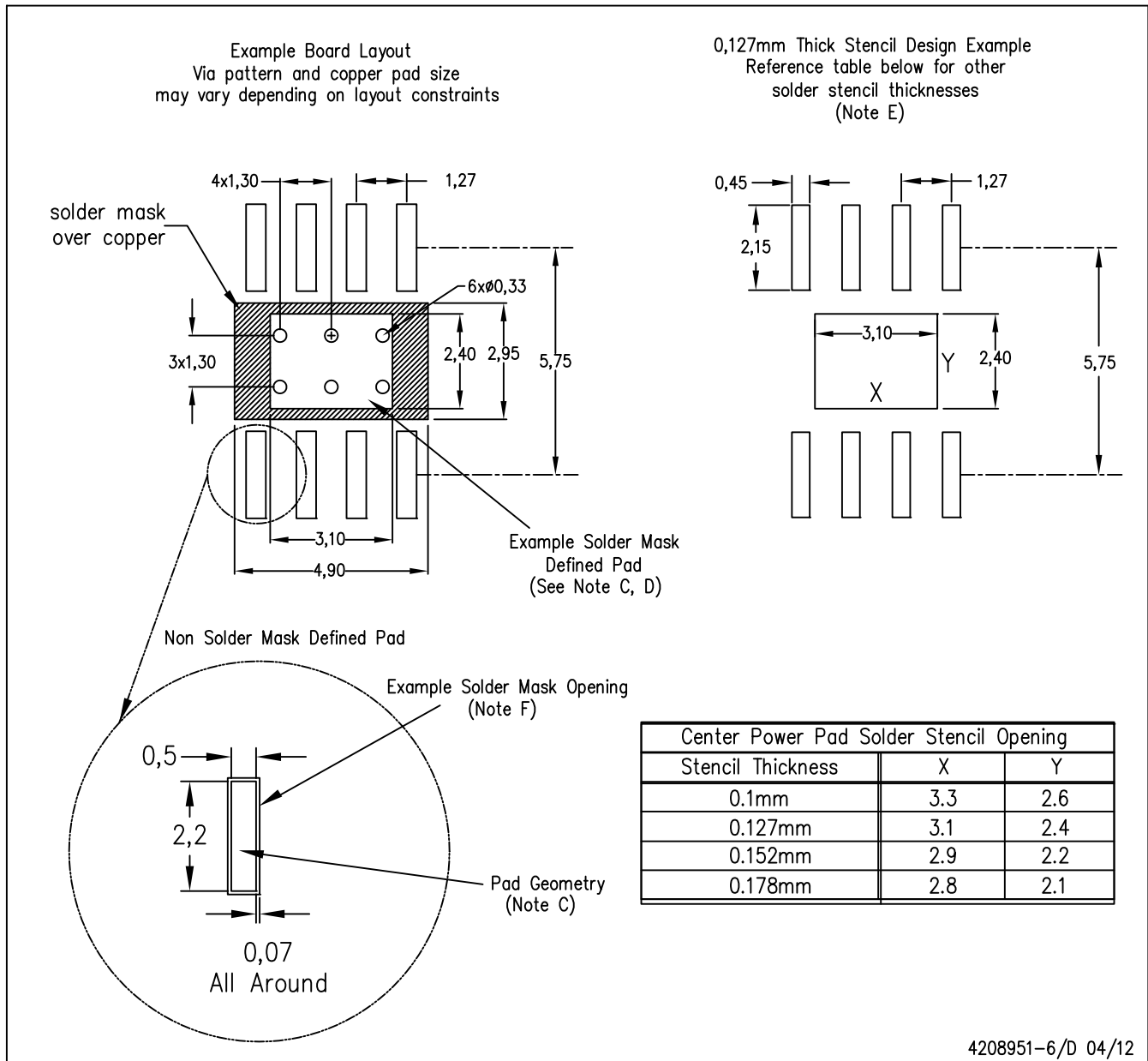
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NOTE: A. All linear dimensions are in millimeters

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DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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