Floating Switch for Offline AC Linear Direct Drive of LEDs with Low Ripple Current

Check for Samples: TPS92411, TPS92411P

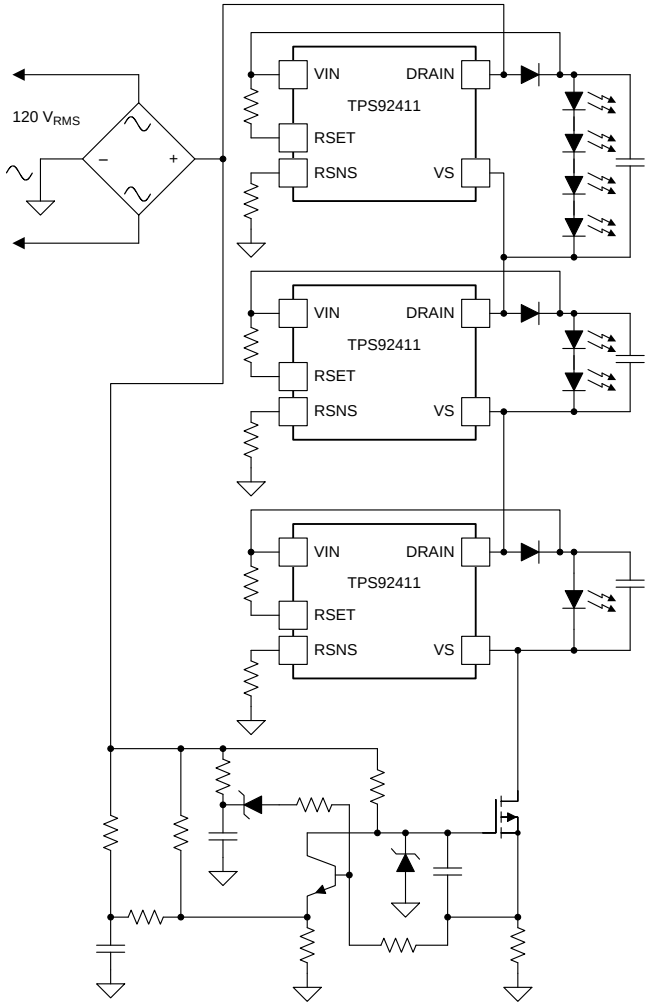
FEATURES

- **High-Performance Solution for Driving LEDs from AC Mains**
- **Simplifies Design of Phase Dimmable LED Driver with High Power Factor, Low Total Harmonic Distortion, and Low Current Ripple**
- **Suitable for LED Lamp and Luminaires up to 70 W**
- **Input Voltage Range: 7.5 V to 100 V**
- **Stackable 100V, 2-Ω MOSFET Building Block**
- **Up to 350 mA Current Capability (PSOP package)**
- **Controlled Switch Open and Close Transitions Minimize EMI**
- **Input Undervoltage Protection**
- **Output Overvoltage Protection (TPS92411P)**
- **Low I_Q: 200 µA (typ)**

APPLICATIONS

- **LED Lamps and Light Bulbs**
- **LED Luminaires**
- **Downlights**

SIMPLIFIED APPLICATION DIAGRAM



DESCRIPTION

The TPS92411 is a 100-V floating MOSFET switch for use in offline LED lighting applications. It is used in conjunction with a current regulator that can achieve greater than 0.9 power factor to create a LED drive solution with low-ripple current. When properly designed, solution performance is comparable to traditional flyback, buck or boost based AC/DC LED drivers. The approach requires no inductive components saving size and cost. Slew controlled low frequency operation of the TPS92411 switches creates very little EMI. Detailed operation is described in the *APPLICATION INFORMATION* section.

Package options include SOT23-5 and PSOP-8 allowing the user to optimize for small size or scale for high power. Using the PSOP-8 package, design of LED luminaires up to 70 W is possible. Other features include a UVLO circuit to monitor when the device has sufficient voltage to operate properly and over-voltage protection (TPS92411P).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

All voltages are with respect to VS, –40°C < T_J = T_A ≤150°C. All currents are positive into and negative out of the specified terminal (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Supply voltage	VIN	–0.3	105	V
Switch voltage	DRAIN	-0.3	105	
Junction temperature	T_J	-40	165	°C
Storage temperature range	T_{stg}	-65	150	
Electrostatic Discharge	(HBM) QSS 009-105 (JESD22-A114A)		1	kV
	Field Induced Charged Device Model (FIDCM)		250	V

THERMAL INFORMATION

THERMAL METRIC(1)		TPS92411		UNITS
		SOT-23	PSOP	
		5 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	209.8	58.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	125.2	72	
θ_{JB}	Junction-to-board thermal resistance(4)	38	39.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	15.6	21.6	
ψ_{JB}	Junction-to-board characterization parameter(6)	37.1	39.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	15	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, θ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, θ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
VIN	Input voltage	TPS92411P	7.5		94	V
		TPS92411	7.5		100	
T_J	Operating junction temperature		–40	25	150	°C
I_{SW}	Switch drain (DRAIN) to source (VS) current	DBV (SOT23-5)		100	200	mA
		DDA (SO-8 Power-Pad)		175	350	

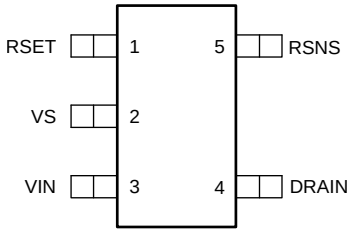
ELECTRICAL CHARACTERISTICS

Unless otherwise specified –40°C ≤ T_J = T_A ≤ 150°C, (V_{VIN} – V_{VS}) = 30 V, R_{RSET} = R_{RSNS} = Open, all voltages are with respect to VS.

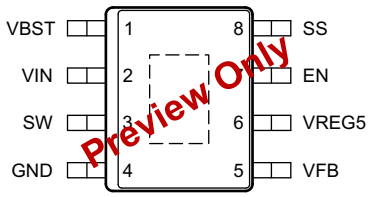
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VIN)							
$V_{IN(ovp)}$	Input overvoltage protection	TPS92411P	Rising threshold	95	100		V
			Falling threshold		96		
			Hysteresis		4		
I_Q	Bias current				200	400	µA
$V_{IN(uvlo)}$	Input undervoltage lockout		Rising threshold		6.5	7	V
$V_{IN(hys)}$	Input UVLO hysteresis				370		mV
SWITCH CONTROL (RSNS, RSET)							
I_{RSNS}	RSNS threshold current			–3.3	–4	–4.9	µA
V_{RSNS_OS}	RSNS offset voltage			165	210	255	mV
V_{RSET}	RSET threshold voltage			1.2	1.25	1.3	V
I_{RSET}	RSET current		I_{RSNS} = –20 µA, (V_{RSET} – V_{VS}) = 1.5 V	–9.3	–10	–10.7	µA
			I_{RSNS} = –40 µA, (V_{RSET} – V_{VS}) = 1.5 V	–19	–20	–21	
			I_{RSNS} = –100 µA, (V_{RSET} – V_{VS}) = 1.5 V	–47.9	–50	–52.1	
SWITCH (DRAIN, VS)							
$R_{DS(on)}$	On-resistance		I_{DRAIN} = 100 mA, T_J = 25°C	1	2	2.5	Ω
$dv/dt_{(ON)}$	Switch ON slew rate		(V_{DRAIN} – V_{VS}) falling 36 V to 4 V, I_{SW} = 100 mA		1		V/µs
$dv/dt_{(OFF)}$	Switch OFF slew rate		(V_{DRAIN} – V_{VS}) = rising 4 V to 36 V, I_{SW} = 100 mA		0.5		

DEVICE INFORMATION

DBV (SOT23-5) PACKAGE
5 PIN
(TOP VIEW)



DDA (SO-8 Power-Pad) PACKAGE
8 PIN
(TOP VIEW)

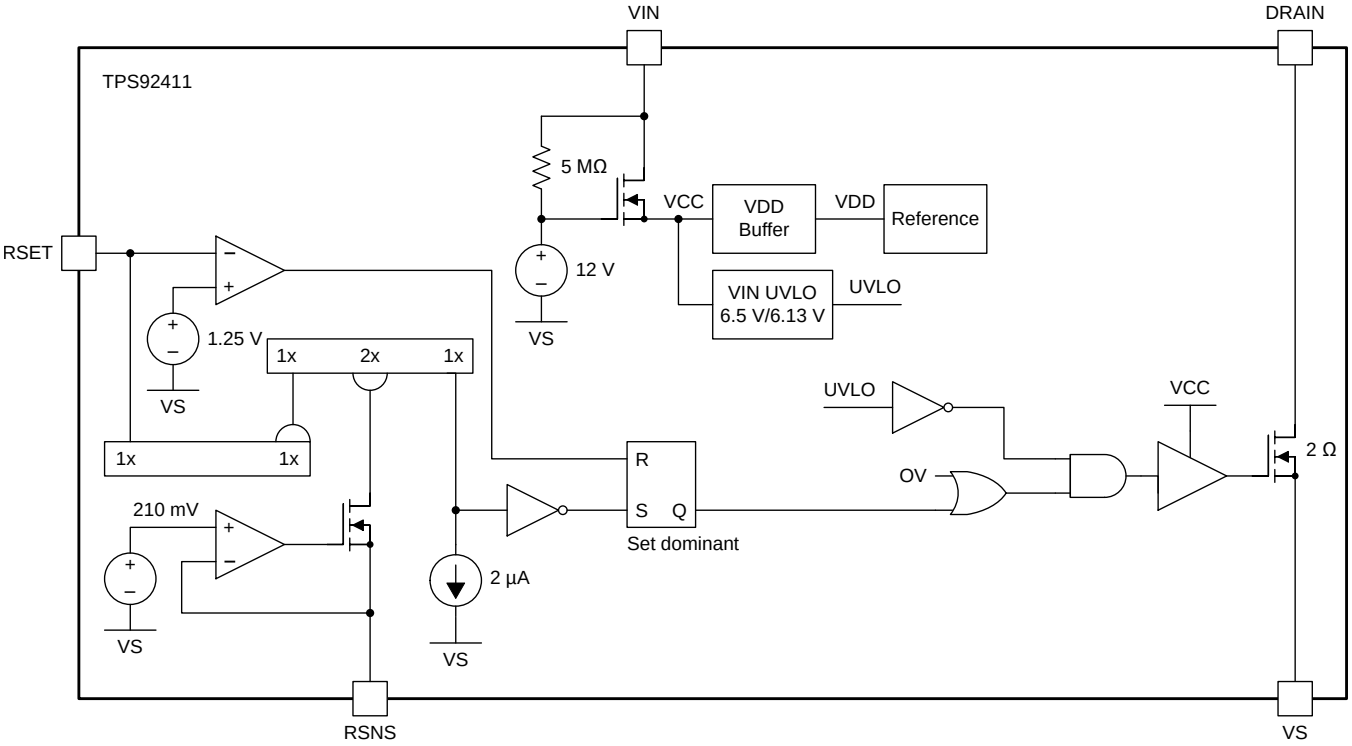


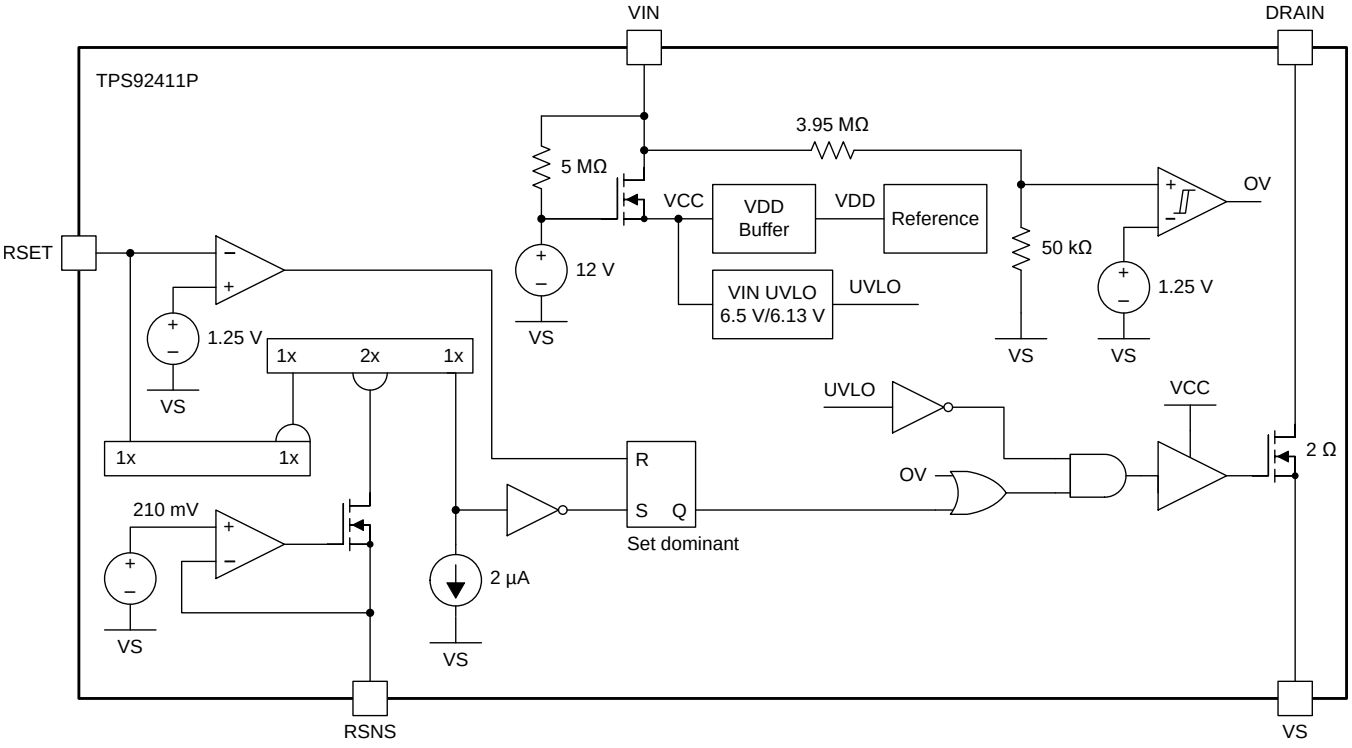
PIN DESCRIPTIONS

PIN			I/O	DESCRIPTION
NAME	NO.			
	DDA(1)	DBV		
DRAIN	8	4	O	Drain of the internal switch.
N/C	2	—	—	Not internally connected.
	6			
	7			
VIN	1	3	I	Positive power supply for the device.
VS	2	2	I/O	Source of the internal switch. This pin is also the device floating ground.
RSET	3	1	I/O	A resistor connected between the RSET pin and the VIN pin sets the rising threshold to open the switch.
RSNS	5	5	I/O	A resistor connected between the RSNS pin to system ground senses the VS voltage relative to system ground.
Exposed Themal Pad				Connect to VS pin directly beneath the device.

(1) 8-pin PSOP (DDA) package is not available and is currently in preview status

FUNCTIONAL BLOCK DIAGRAMS





TYPICAL CHARACTERISTICS

Unless otherwise stated, –40°C ≤ T_A = T_J ≤ 150°C, (V_{VIN} – V_{VS}) = 30 V, all voltages are with respect to VS.

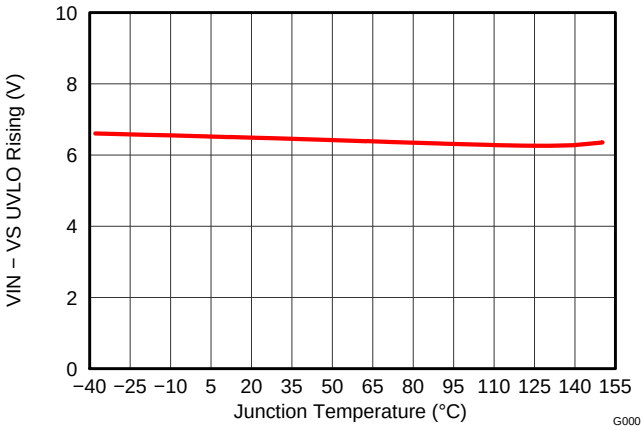


Figure 1. UVLO vs. Temperature

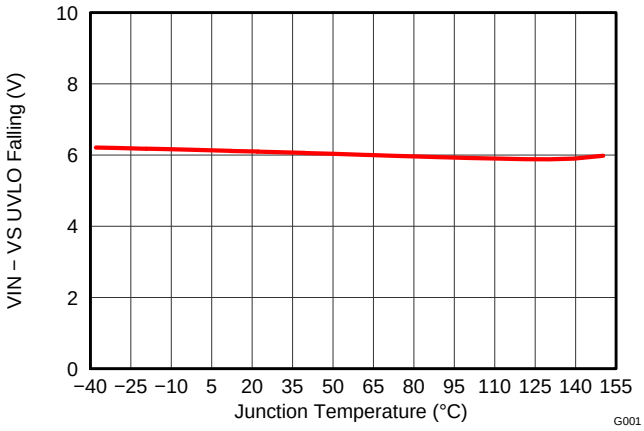


Figure 2. UVLO vs. Temperature

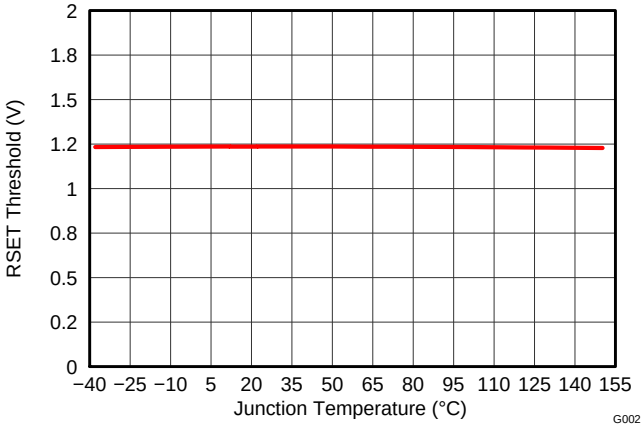


Figure 3. RSET Threshold vs. Temperature

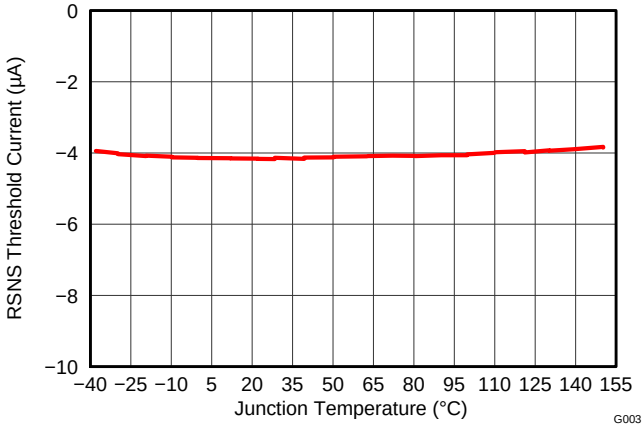


Figure 4. RSNS Threshold Current vs. Temperature

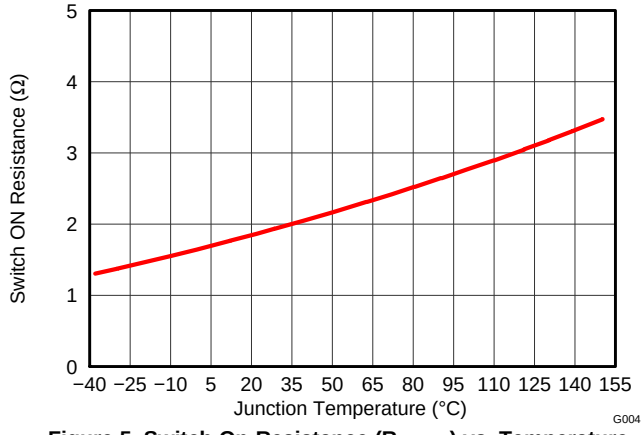


Figure 5. Switch On-Resistance ($R_{DS(on)}$) vs. Temperature

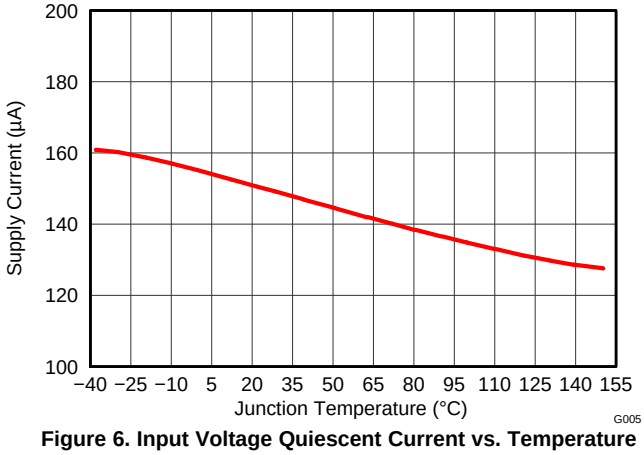


Figure 6. Input Voltage Quiescent Current vs. Temperature

TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated, –40°C ≤ T_A = T_J ≤ 150°C, (V_{VIN} – V_{VS}) = 30 V, all voltages are with respect to VS.

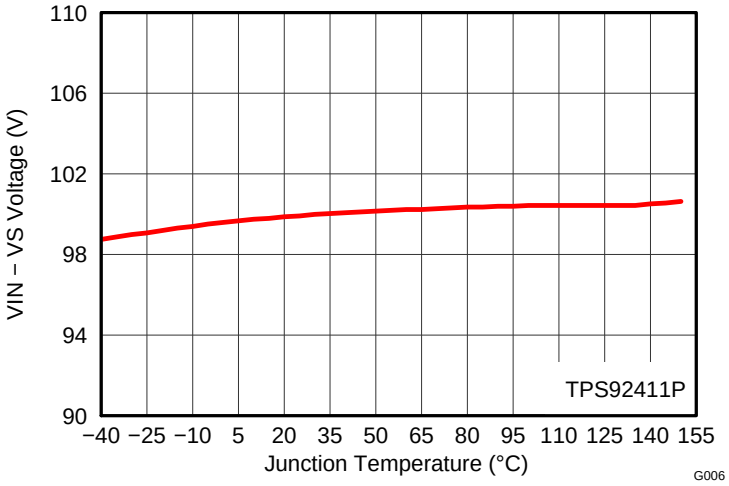


Figure 7. (V_{VIN} – V_{VS}) Overvoltage Threshold vs. Temperature

APPLICATION INFORMATION

APPLICATION

The TPS92411 is an advanced, floating driver specifically designed for use with a linear regulator in low-power offline LED lighting applications. It integrates an on-board 100-V MOSFET switch to shunt LED current as the line transitions. As the line transitions through the cycle, the device monitors critical nodes for zero cross at which time the internal switch is either opened or shorted to steer the current through or away from the LED stack. The device determines the output power by setting the average of the combined LED currents throughout the line cycle using the linear regulator.

SETTING THE SWITCHING THRESHOLDS (RSNS, RSET)

The TPS92411 features two threshold settings to allow for proper LED control. The first setting determines when the internal switch turns off and allows current to charge the capacitor and flow through the LEDs. The second setting determines when the switch turns on to shunt the LEDs and allow the capacitor to supply current. The lower switch turn-on threshold (V_{SNS}) should be set first using a resistor (R_{RSNS}) from the RSNS pin to system ground. For best efficiency set this threshold between 4 V and 6 V. Then the upper switch turn-off threshold (V_{VS}) can be set using a resistor (R_{RSET}) from the RSET pin to the VIN pin. Set this threshold approximately 6 V to 10 V above the LED stack voltage (V_{LED}). The RSET threshold should be greater than the LED stack voltage plus the value of the RSNS threshold to prevent errant switching. These thresholds can be set with resistance calculated using Equation 1 and Equation 2

$$R_{SNS} = \frac{V_{SNS} + 0.21V}{|I_{RSNS}|} \quad (1)$$

$$R_{RSET} = \frac{(V_{LED} - 1.24\,V) \times 2 \times R_{SNS}}{V_{VS} + 0.21V} \quad (2)$$

OVERVOLTAGE PROTECTION (OVP)

Overvoltage protection (OVP) in the TPS92411P version protects the device as well as the LEDs and storage capacitor. The OVP is set at approximately 100 V (V_{VIN} – V_{VS}) and closes the internal switch when the threshold voltage is reached. For this reason LED stack voltages of 94 V or less are recommended. Higher voltages can be used with the TPS92411 version but tolerances must be considered to ensure that the 105 V absolute maximum rating is not exceeded.

INPUT UNDERVOLTAGE LOCKOUT (UVLO)

The TPS92411 includes input UVLO. The UVLO prevents the device from operation until the VIN pin voltage with respect to VS exceeds 6.5 V and ensures the device behaves properly when enabled.

LED CAPACITOR

A capacitor is required across each LED stack to provide current to the LEDs during the switch ON time. Refer to the available calculator software (SLVC516 for 120-V applications or SLVC517 for 230-V applications) for calculating the minimum value required for any particular application. The software calculates the minimum value required for a particular application, but best performance is acheived by using as much capacitance as possible given size and cost constraints. These design tools also calculate a minimum value for any given current ripple percent or flicker index desired for the particular application.

BLOCKING DIODE

A blocking diode is required between the drain of the switch (DRAIN) and the anode of the LED stack. This prevents the LED capacitor from discharging through the switch during the switch ON time instead allowing it to discharge through the LED stack. This diode should be rated for 200 V reverse voltage and capable of forward currents as high as the average linear regulator current setting.

TYPICAL OPERATION (120-VAC APPLICATION)

For the 120-V application shown in Figure 10 the highest efficiency is obtained by using a high-voltage total LED stack to reduce losses in the linear regulator FET. The best current sharing efficiency between stacks can be achieved by using the lowest voltage stack at the bottom and making each stack voltage above 2 times the voltage of the stack below it. In this example 20-V LEDs are used. This effectively gives the lowest stack a total of 20 V, the middle stack a total of 40 V, and the upper stack a total of 80 V. The RSNS resistor is used to set a low voltage point so that when the VS pin voltage falls below this threshold (either from the AC line falling or a higher voltage stack switch above it turning OFF) the TPS92411 switch turns ON and bypasses the LEDs. During the ON-time, the LEDs are supplied current from the capacitor. The RSET voltage is used to set a threshold to detect when the input voltage crosses this threshold it turns OFF the switch and allows the LEDs to conduct current from the line and charge the bypass capacitor.

120-VAC Application Stack Setting Example

- Set V_{RSNS} for all three TPS92411 devices at 4 V
- Set V_{RSET} for the bottom stack at 26 V
- Set V_{RSET} for the middle stack at 46 V
- Set V_{RSET} for the top stack at 86 V

Switching order as the rectified AC line voltage increases is shown in Table 1. Figure 8 illustrates when each switch turns ON or OFF.

Table 1. Switching Order on Rising Edge of Rectified 120-VAC (1)(2)

STACK		
TOP 80-V	**MIDDLE 40-V**	**BOTTOM 20-V**
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

(1) 0 denotes switch ON and LEDs bypassed and supplied by the capacitor.
(2) 1 denotes switch OFF and LEDs conducting from the line, capacitor charging up.

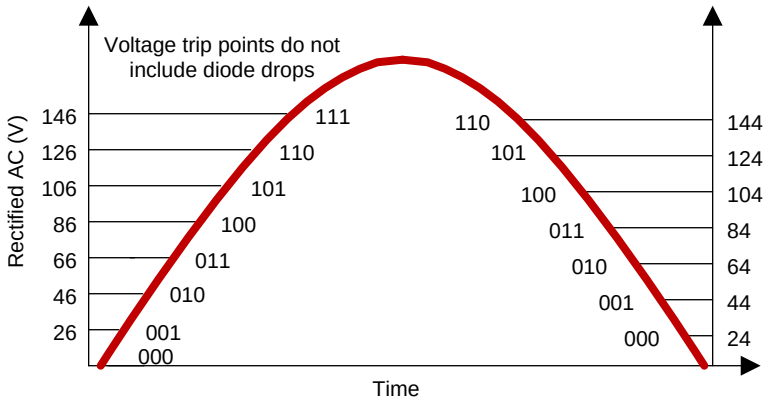


Figure 8. Switching Order on Rectified 120-VAC Waveform

The linear regulator in Figure 10 generates a current sense RMS voltage of approximately 2.3 V. The linear regulator RMS current is equal to the input current drawn from the AC line. For example, for a 11.5-W input power system the input current should be approximately 0.095 A and a 24-Ω resistor should be chosen for RCS. Other input power levels (P_{IN}) can be obtained using Equation 3.

$$R_{CS} = \frac{120\,V_{RMS} \times 2.3 V_{RMS}}{P_{IN}} \quad (3)$$

TYPICAL OPERATION (230-VAC APPLICATION)

In the 230-V application shown in Figure 11, the highest efficiency can be obtained by using a high-voltage total LED stack to reduce losses in the linear regulator FET. The best current sharing between stacks can be achieved by using the lowest voltage stack at the bottom and making each stack voltage above that two times that of the stack below it (as in described in the 120-V application). In this example, very good results can be obtained by setting the lowest stack at 40 V, the middle stack at 80 V, and adding a high-voltage cascode FET with the top stack and using 160 V. Use the RSNS pin to set a low voltage point so that when the VS pin of the device falls below this threshold (either from the AC line falling or a higher voltage stack switch above it turning OFF) the TPS92411 switch turns ON and bypasses the LEDs. During the ON-time, the capacitor supplies current to the LEDs. The RSET voltage threshold for a 230-V application is generally set to approximately 8 V to 12 V above the LED stack voltage connected across the TPS92411. This threshold is higher than in the typical 120-V application to allow more headroom.

230-VAC Application Stack Setting Example

- Set V_{RSNS} for all three TPS92411 devices at 6 V
- Set V_{RSET} for the bottom stack at 49 V
- Set V_{RSET} for the middle stack at 89 V
- Set V_{RSET} for the top stack at 169 V

Switching order as the rectified AC line voltage increases is shown in Table 2. Figure 9 illustrates when each switch turns ON or OFF.

Table 2. Switching Order on Rising Edge of the Rectified 230-VAC Waveform(1)(2)

STACK		
TOP 160-V	MIDDLE 80-V	BOTTOM 40-V
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

(1) 0 denotes switch ON and LEDs bypassed and supplied by the capacitor.
(2) 1 denotes switch OFF and LEDs conducting from the line, capacitor charging up.

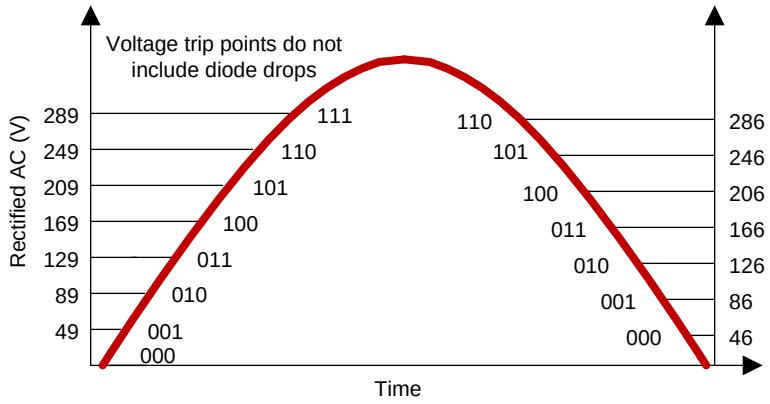


Figure 9. Switching Order on Rising Edge of the Rectified 230-VAC Waveform

The linear regulator in Figure 11 generates a current sense RMS voltage of 2.44 V. The linear regulator RMS current is equal to the input current drawn from the AC line. For example, for a 16-W input power system the input current should be approximately 0.07 A and a 34.8-Ω resistor should be chosen for R_{CS}. Other input power levels (P_{IN}) can be calculated using Equation 4.

$$R_{CS} = \frac{230\,V_{RMS} \times 2.44 V_{RMS}}{P_{IN}} \quad (4)$$

TYPICAL APPLICATIONS CIRCUITS

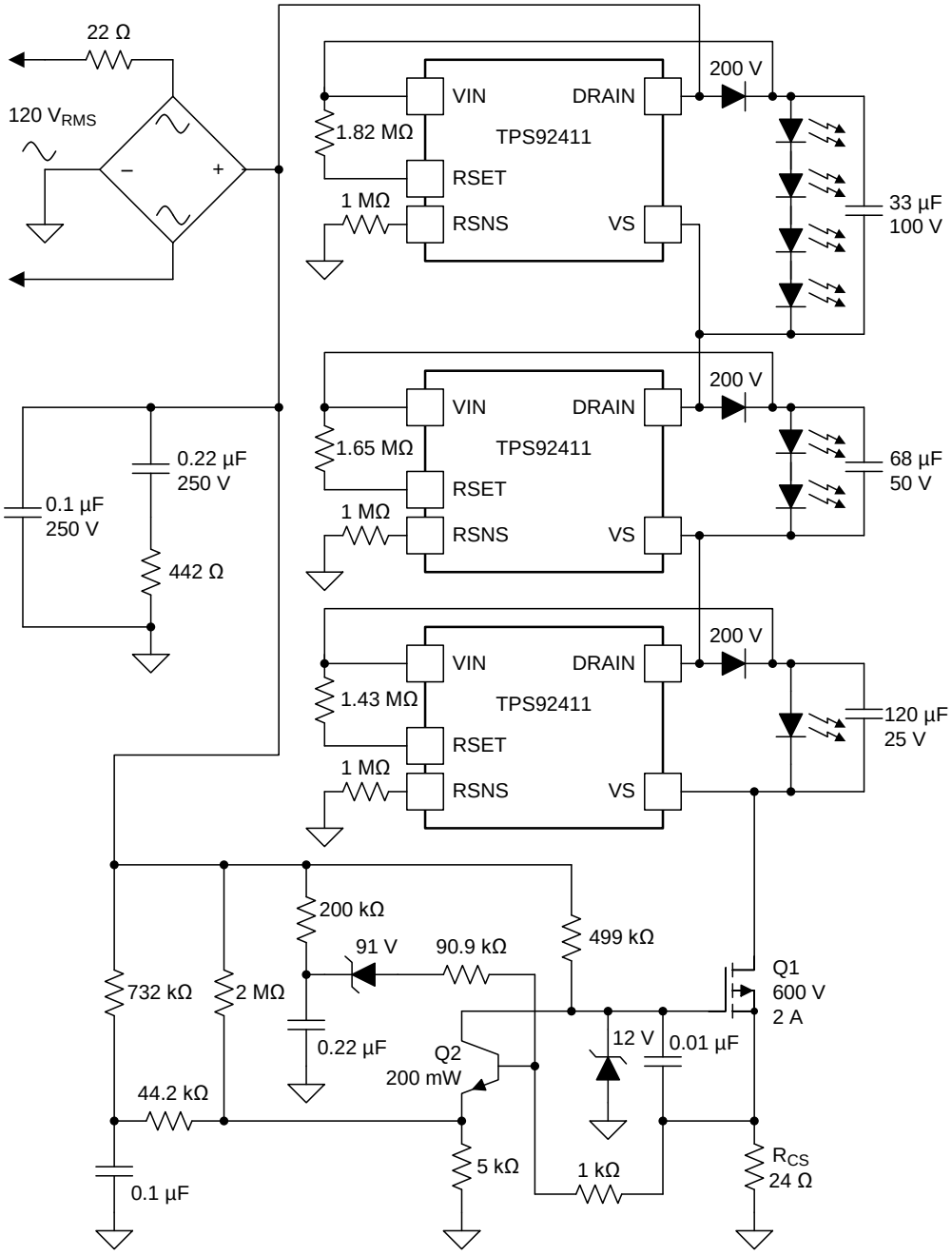


Figure 10. 120-VAC, Phase Dimmable 11.5-W Input with Discrete Linear Regulator

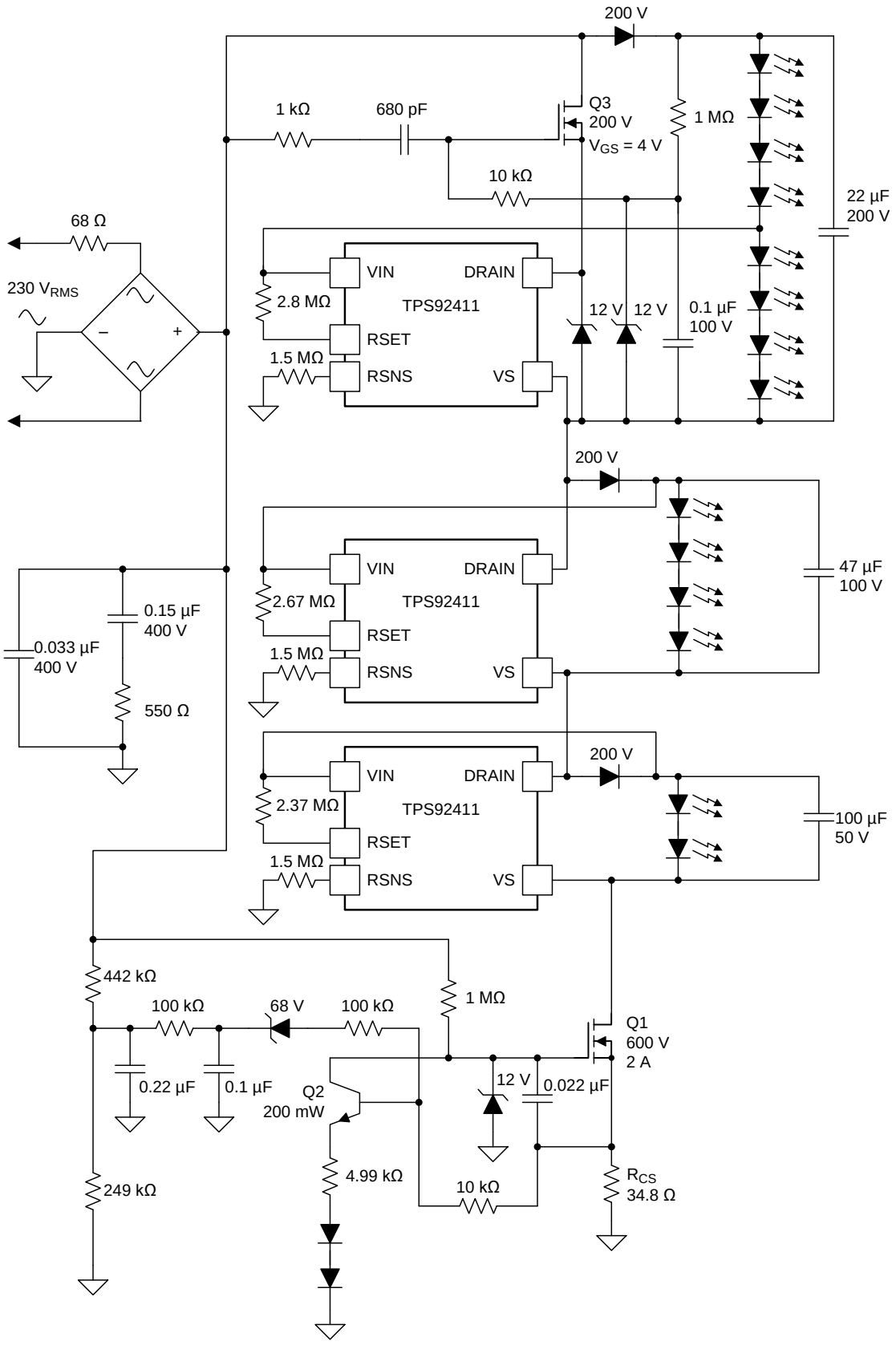


Figure 11. 230-VAC, Phase Dimmable 16-W Input with Discrete Linear Regulator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92411DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	PB9Q	Samples
TPS92411DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	PB9Q	Samples
TPS92411DDA	PREVIEW	SO PowerPAD	DDA	8	75	TBD	Call TI	Call TI	-40 to 150		
TPS92411DDAR	PREVIEW	SO PowerPAD	DDA	8	2500	TBD	Call TI	Call TI	-40 to 150		
TPS92411PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	PB8Q	Samples
TPS92411PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	PB8Q	Samples
TPS92411PDDA	PREVIEW	SO PowerPAD	DDA	8	75	TBD	Call TI	Call TI	-40 to 150		
TPS92411PDDAR	PREVIEW	SO PowerPAD	DDA	8	2500	TBD	Call TI	Call TI	-40 to 150		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

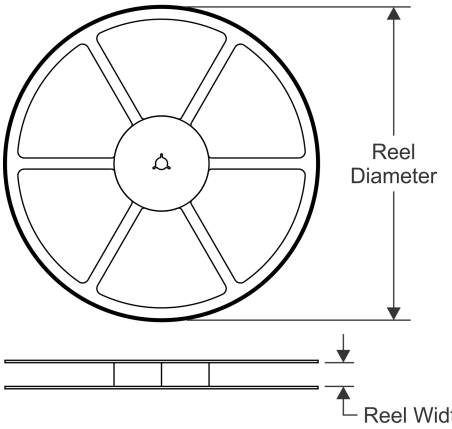
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

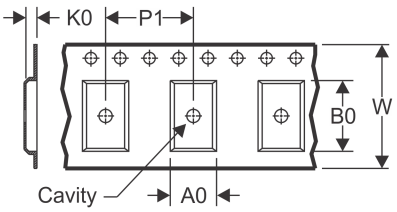
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

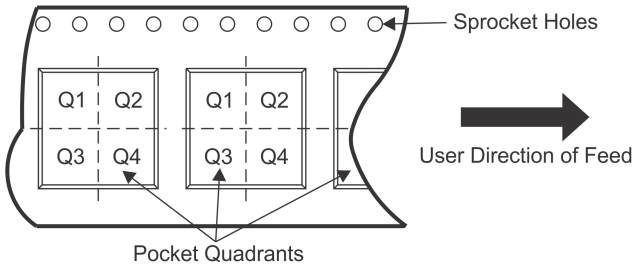


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

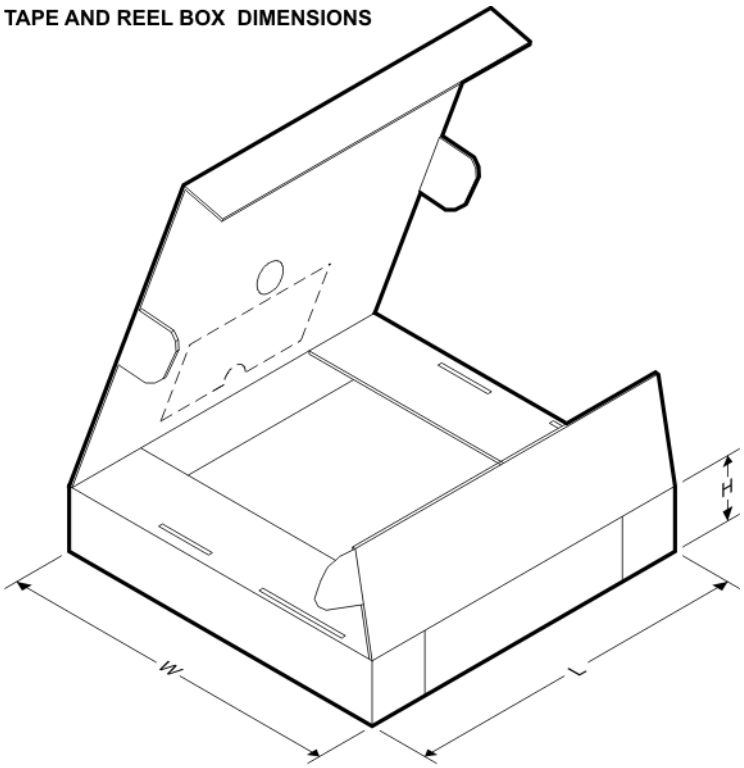
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92411DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS92411DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS92411PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS92411PDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

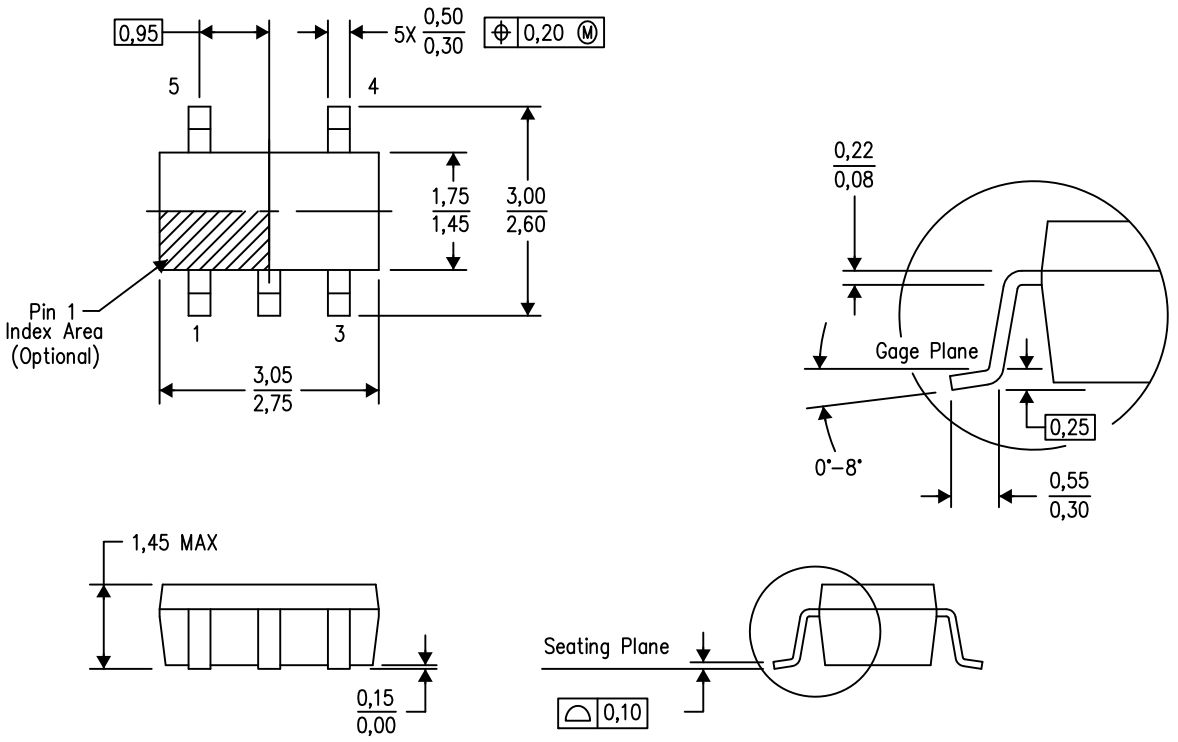
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92411DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS92411DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS92411PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS92411PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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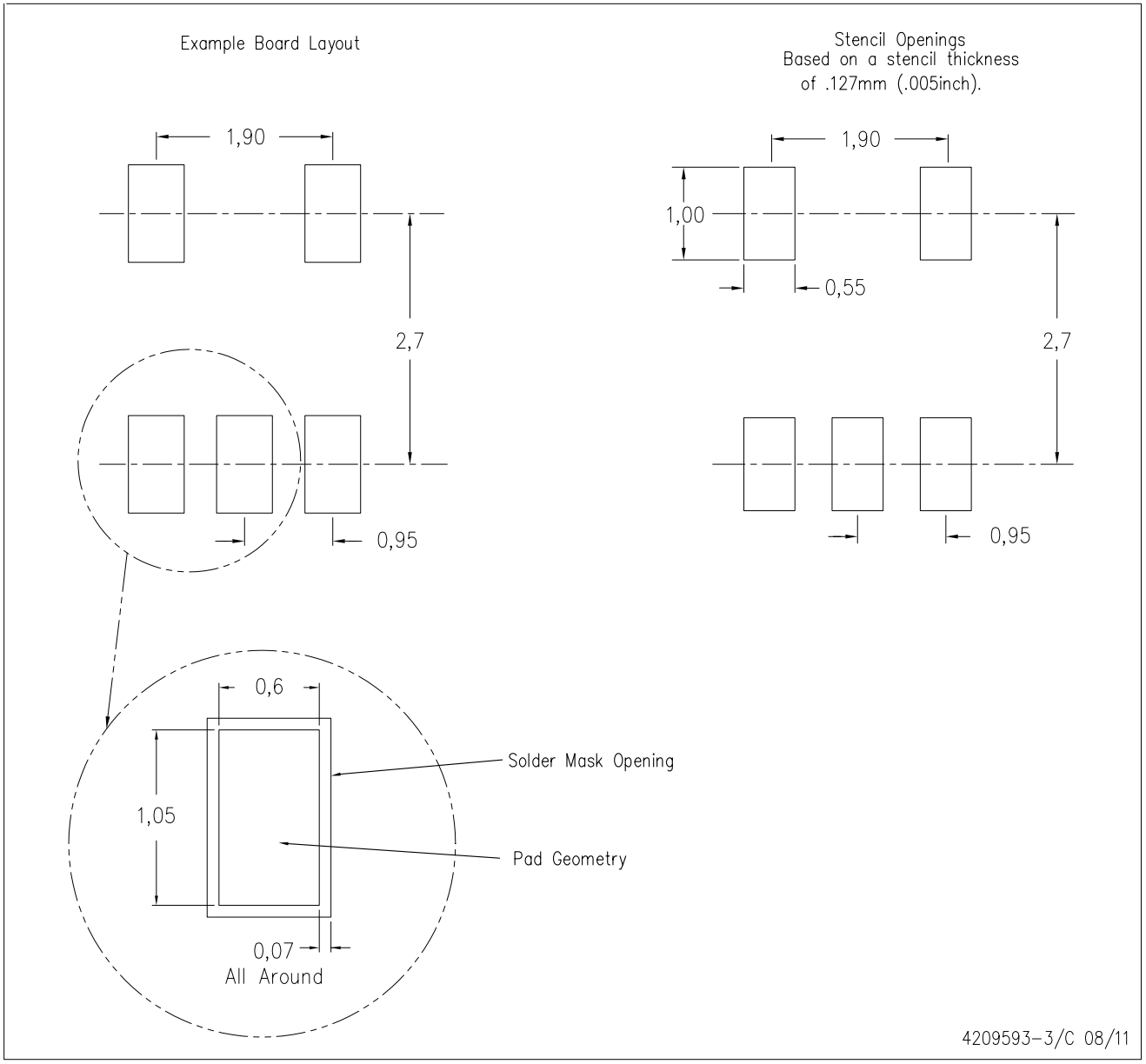
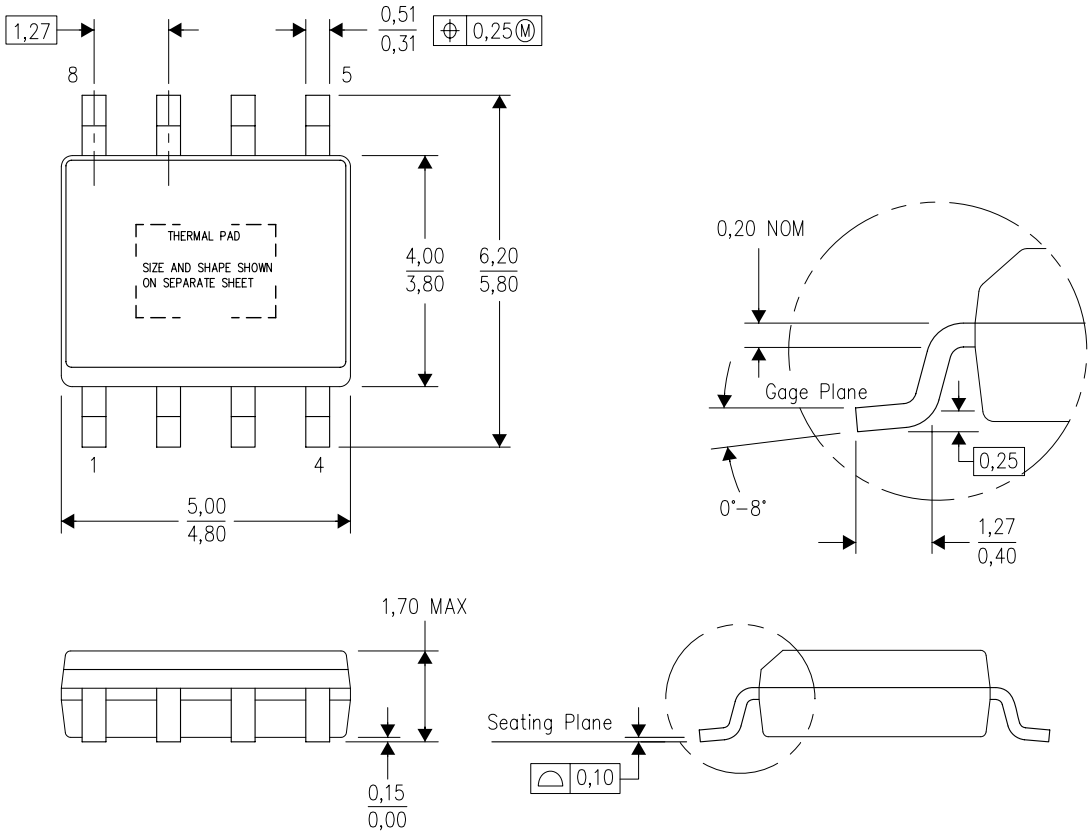
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

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