N-Channel Controller for Dimmable LED Drives with Low-Side Current Sense

Check for Samples: TPS92690

FEATURES

- **TPS92690Q1 is an Automotive Grade Product that is AEC-Q100 Grade 1 Qualified (–40°C to 125°C Operating Junction Temperature)**
- **V_{IN} Range from 4.5V to 75V**
- **Adjustable Current Sense (50mV – 500mV)**
- **Low-side Current Sensing**
- **2-Ω MOSFET Gate Driver**
- **Input Under-Voltage Protection**
- **Output Over-Voltage Protection**
- **Cycle-by-Cycle Current Limit**
- **PWM Dmming Input**
- **Programmable Oscillator Frequency**
- **External Synchronization Capability**
- **Slope Compensation**
- **Programmable Soft-Start**
- **TSSOP-16 Exposed Pad Package**

APPLICATIONS

- **LED Drivers**
- **Constant Current Regulator: Boost, Cuk, Flyback, and SEPIC**

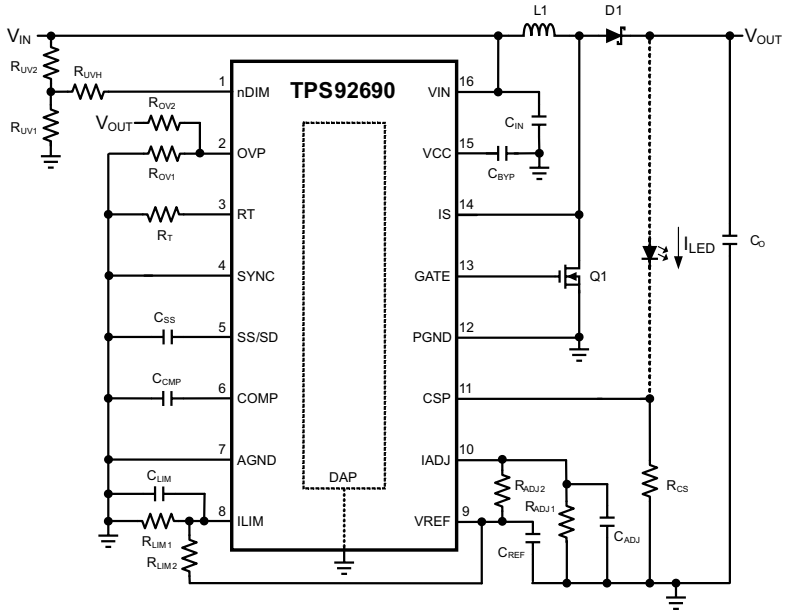
DESCRIPTION

The TPS92690/90Q1 is a high voltage, low-side NFET controller with an adjustable output current sense resistor voltage. Ideal for LED drivers, it contains all of the features needed to implement current regulators based on boost, SEPIC, flyback, and Cuk topologies.

Output current regulation is based on peak current-mode control supervised by a control loop. This methodology eases the design of loop compensation while providing inherent input voltage feed-forward compensation. The TPS92690/90Q1 includes a high-voltage start-up regulator that operates over a wide input range of 4.5V to 75V. The PWM controller is designed for high speed capability including an oscillator frequency range up to 2.0 MHz. The TPS92690/90Q1 includes an error amplifier, precision reference, cycle-by-cycle current limit, and thermal shutdown.

The TPS92690Q1 is AEC-Q100 grade 1 qualified.

TYPICAL APPLICATION DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

GRADE	PACKAGE(2)	PINS	PACKAGE DRAWING	ORDERABLE DEVICE NUMBER	TRANSPORT MEDIA	QUANTITY
Commercial	TSSOP EXP PAD	16	MXA16A	TPS92690PWP	Tube	92
				TPS92690PWPR	Tape and Reel	2500
AEC-Q100 Grade 1 qualified(3)	TSSOP EXP PAD	16	MXA16A	TPS92690Q1PWP	Tube	92
				TPS92690Q1PWPR	Tape and Reel	2500

(1) For the most current package and ordering information; see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Automotive Grade (Q) product incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC-Q100 standard. Automotive grade products are identified with the letter Q.

ABSOLUTE MAXIMUM RATINGS(1)

All voltages are with respect to GND, –40°C < T_J = T_A< 125°C, all currents are positive into and negative out of th specified terminal (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage	VIN	–0.3	76	V
Input voltage range	nDIM, OVP	–0.3	76	V
	IS(2)	–0.3	76	
	CSP, IADJ, SS/SD, ILIM	–0.3	6	
Output voltage range	VCC, GATE(3)	–0.3	14	V
	COMP, RT, VREF	–0.3	6	
Continuous input current	IS		–1	mA
	GATE	–1	1	
	SYNC		1	
Output current	VREF		–1	mA
Junction temperature	T_J(4)		150	°C
Storage temperature	T_{stg}	–65	150	°C
Electrostatic Discharge	(HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Field Induced Charged Device Model (FICDM)		750	V

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) IS can sustain -2V for 100ns without damage.
(3) GATE can sustain –2.5V for 100 ns, VCC +2.5V for 100 ns.
(4) Maximum junction temperature is internally limited.

RECOMMENDED OPERATING CONDITIONS(1)

unless otherwise noted, all voltages are with respect to GND, –40°C < T_J = T_A< 125°C

		MIN	TYP	MAX	UNIT
VIN	Input voltage	4.5	12	75	V
T_J	Operating junction temperature	–40	25	125	°C
$V_{IADJ(MAX)}$	Maximum operating IADJ voltage	0		5	V

(1) Operating Ratings are conditions under which operation of the device is specified and do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS92690 TSSOP (16 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	38.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	23.2	
θ_{JB}	Junction-to-board thermal resistance(4)	16.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.6	
ψ_{JB}	Junction-to-board characterization parameter(6)	16.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	1.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

unless otherwise specified –40°C < T_J = T_A < 125°C, VIN = 14 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR (VCC)						
VCC_{REG}	VCC Regulation	ICC = 0mA	6.35	6.9	7.45	V
ICC_{LIM}	VCC Current limit	VCC = 0V	–20	–30		mA
I_Q	Quiescent current			2	3	mA
I_{SD}	Shutdown current	SS/SD = 0V		45	65	µA
VCC_{UV}	VCC UVLO threshold	VCC rising		4.1	4.50	V
		VCC falling	3.61	4.01		
VCC_{HYS}	VCC UVLO hysteresis			83		mV
REFERENCE VOLTAGE OUTPUT						
VREF	Reference voltage	No Load	2.40	2.45	2.50	V
ERROR AMPLIFIER						
	CSP Input bias current		–0.6	0	0.6	µA
	COMP sink current		17.1	28.5	39.9	µA
	COMP source current	IADJ = 5V	–12.6	–16.8	–21	µA
g_m	Transconductance	IADJ = 1V, 0V < V_{CSP} < 0.8V		33		µA/V
	Transconductance bandwidth	–6dB		1		MHz
	IADJ input impedance			1		MΩ
V_{CSP}	Error Amp reference voltage	Precise value implied in offset		V_{IADJ}/10		V

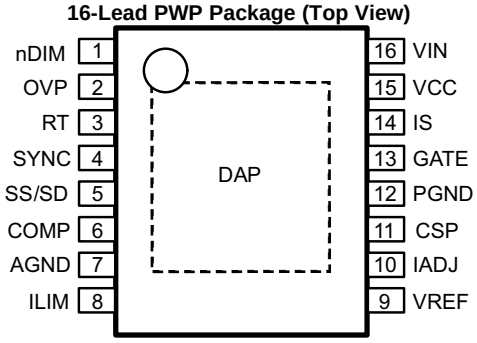
ELECTRICAL CHARACTERISTICS (continued)

unless otherwise specified –40°C < T_J = T_A < 125°C, VIN = 14 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Error Amp input offset voltage	VCC = 4.5V, 1V < V_{COMP} < 1.4V, T_A = 25°C	–1.5	0	1.5	mV
		VCC > 6V, 1V < V_{COMP} < 3V, V_{IADJ} ≤ 1.25V, T_A = 25°C	–1.8	0	1.8	
		VCC > 6V, 1V < V_{COMP} < 3V, V_{IADJ} > 1.25V, T_A = 25°C (% of V_{CSP})	–1.44	0	1.44	%
PWM COMPARATOR and SLOPE COMPENSATION						
D_{MAX}	Maximum duty cycle	Internal oscillator only	90%	94.4%		
	IS to PWM offset voltage	No slope added	950	1100	1250	mV
	IS to PWM offset voltage	D = D_{MAX} (max slope added)		125		mV
I_{OFF}	IS source current	No slope added		–11.9		µA
I_{OFF} + I_{SL}		D = D_{MAX} (max slope added)		–60		µA
CURRENT LIMIT						
	ILIM delay to output			60	100	ns
t_{ON-MIN}	Leading edge blanking time			200	300	ns
	Current limit off-timer			38		µs
	ILIM offset voltage	D = 50%	–19	–5.6	5	mV
LOW POWER SHUTDOWN and SOFTSTART						
V_{SD}	Shutdown threshold voltage	SS/SD falling	30	86		mV
V_{SDH}	Shutdown hysteresis			24		mV
I_{SS}	SS/SD current source	$V_{SS/SD}$ > (V_{SD} + V_{SDH})		–10.8		µA
		$V_{SS/SD}$ < V_{SD}		–1.1		µA
OSCILLATOR and EXTERNAL SYNCHRONIZATION						
f_{SW}	Switching frequency	R_T = 121k	312	350	389	kHz
		R_T = 100k	372	418	464	
		R_T = 84.5k	436	490	544	
	SYNC threshold voltage (Falling edge triggers on-time)	Rising		2.05	2.36	V
		Falling	0.95	1.31		
	SYNC Clamp Voltage	Positive		6.2		V
		Negative		–0.5		
OVER VOLTAGE PROTECTION						
	OVP OVLO threshold	Rising		1.23	1.282	V
		Falling	1.144	1.19		
	OVP hysteresis source current	OVP active (high)	–14	–21.5	-28	µA
PWM DIMMING INPUT and UVLO						
	nDIM/UVLO threshold	Rising		1.23	1.285	V
		Falling	1.14	1.19		
	nDIM hysteresis current		–14	–21.6	-28	µA
GATE DRIVER						
	GATE sourcing resistance	GATE = High		2.4	6.0	Ω
	GATE sinking resistance	GATE = Low		1.0	5.0	Ω
	Peak GATE current	Source		–0.47		A
		Sink		1.1		A
THERMAL SHUTDOWN						
	Thermal shutdown temperature			175		°C
	Thermal shutdown hysteresis			25		°C

DEVICE INFORMATION

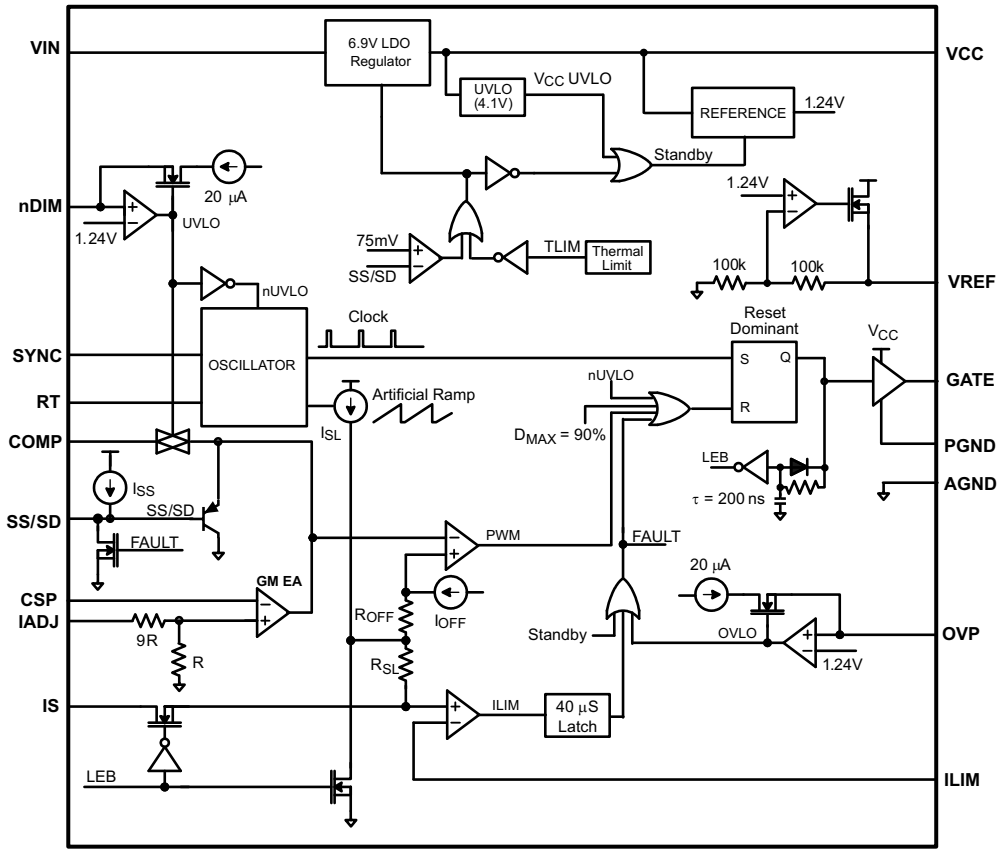
16-Lead PWP Package (Top View)



PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	nDIM	I	Connect resistor divider from VIN to set UVLO threshold and hysteresis. Connect through diode or MOSFET to PWM dim concurrently.
2	OVP	I	Connect resistor divider from output voltage to set OVP threshold and hysteresis.
3	RT	O	Connect resistor to AGND to set base switching frequency.
4	SYNC	I	Connect external PWM signal to set switching frequency. Must be higher than base frequency set at RT pin. Can also connect series resistor and capacitor to drain of main MOSFET and capacitor to AGND to implement zero-crossing detection for quasi-resonant topologies. In either case, a falling edge on SYNC triggers a new on-time at GATE. If tied to ground, internal oscillator is used.
5	SS/SD	I	Connect capacitor to AGND to set soft-start delay. Pull pin below 75mV for low power shutdown.
6	COMP	0	Connect ceramic capacitor to GND to set loop compensation.
7	AGND	-	Connect to PGND through DAP exposed thermal pad for proper ground return path.
8	ILIM	I	Connect resistor divider from VREF to set current limit threshold voltage at IS pin.
9	VREF	O	Connect to IADJ directly or through resistor divider. Bypass with 100nF ceramic capacitor to AGND.
10	IADJ	I	Connect resistor divider from VREF to set error amp reference voltage.
11	CSP	I	Connect to positive terminal of sense resistor in series with LED stack.
12	PGND	-	Connect to AGND through DAP exposed thermal pad for proper ground return path.
13	GATE	-	Connect to main N-channel MOSFET gate of switching converter.
14	IS	I	Connect to drain of main N-channel MOSFET or to source of MOSFET if sense resistor is used for improved accuracy.
15	VCC	O	Bypass with 2.2 µF ceramic capacitor to provide bias supply for controller.
16	VIN	I	Connect to input supply of converter. Bypass with 100nF ceramic capacitor to AGND as close to the device as possible.
-	DAP	-	Exposed thermal pad on the bottom of the package. Connect directly to PGND and AGND beneath the device.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Unless otherwise noted, –40°C ≤ T_A = T_J ≤ +125°C, VIN = 14 V, C_{BYP} = 2.2 µF, C_{COMP} = 0.1 µF

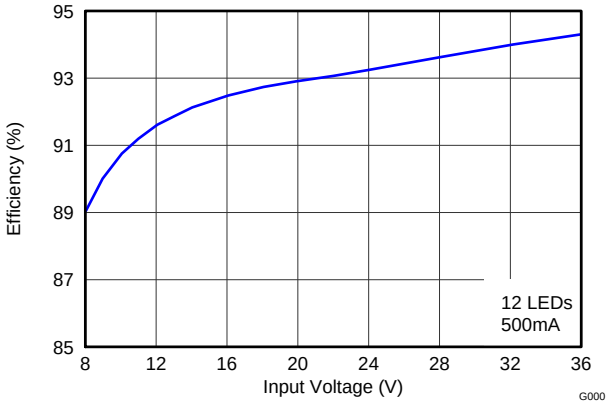


Figure 1. Boost Efficiency vs Input Voltage

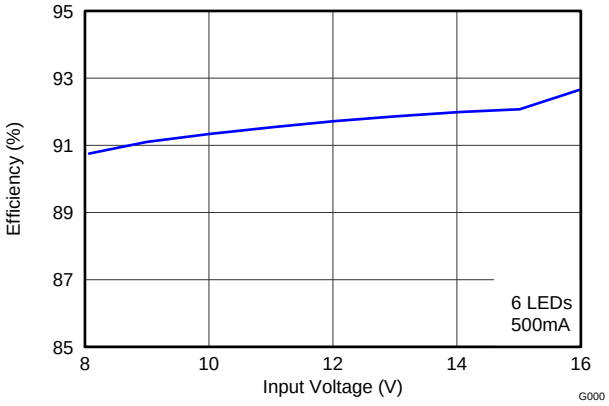


Figure 2. Boost Efficiency vs Input Voltage

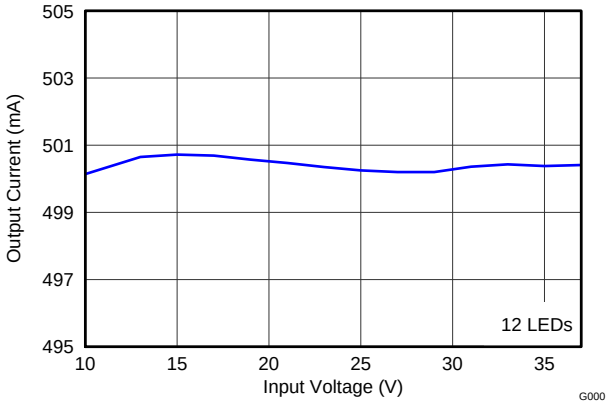


Figure 3. Boost Line Regulation

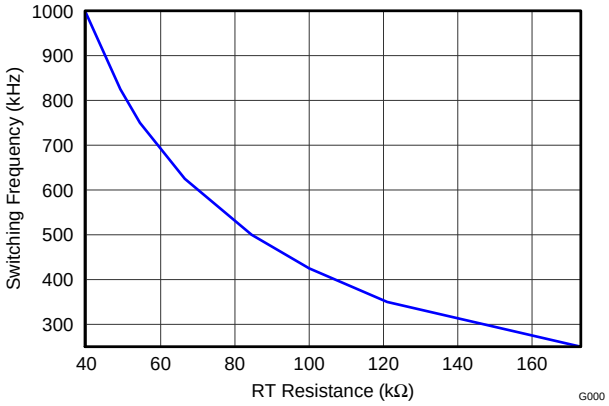


Figure 4. Switching Frequency vs RT Resistance

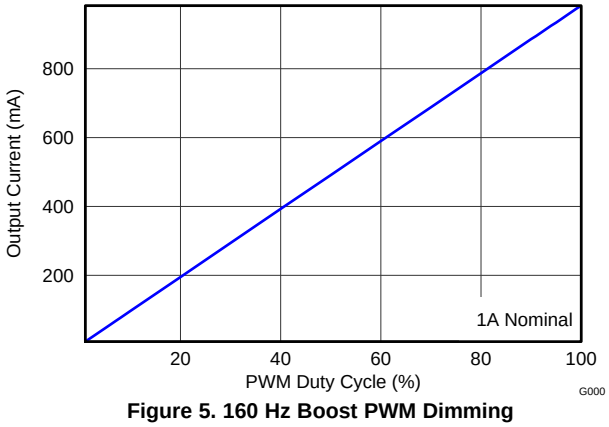


Figure 5. 160 Hz Boost PWM Dimming

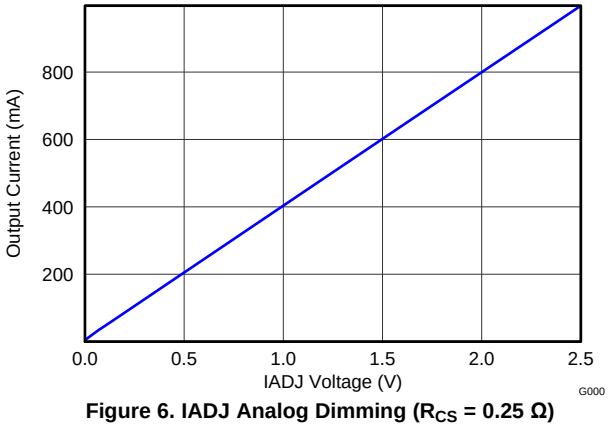


Figure 6. IADJ Analog Dimming (R_{CS} = 0.25 Ω)

TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, –40°C ≤ T_A = T_J ≤ +125°C, VIN = 14 V, C_{BYP} = 2.2 µF, C_{COMP} = 0.1 µF

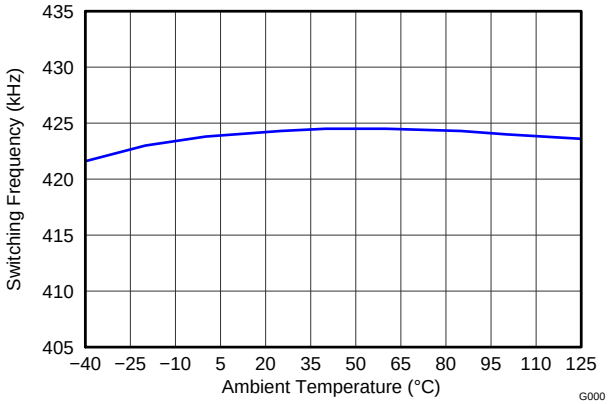


Figure 7. Switching Frequency vs Ambient Temperature (R_T = 100 kΩ)

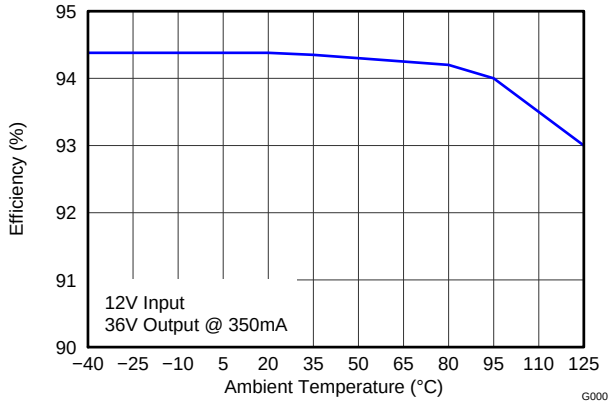


Figure 8. Efficiency vs Ambient Temperature

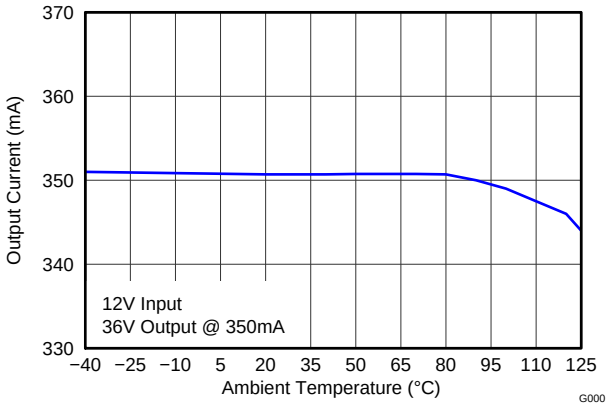


Figure 9. Output Current vs Ambient Temperature

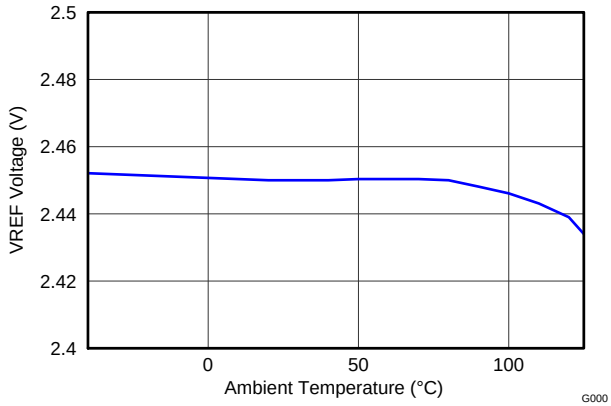


Figure 10. VREF Voltage vs Ambient Temperature

APPLICATION INFORMATION

The TPS92690 is an N-channel MosFET (NFET) controller for boost, SEPIC, Cuk, and flyback current regulators which are ideal for driving LED loads. The controller has wide input voltage range allowing for regulation of a variety of LED loads. The low-side current sense, with low adjustable threshold voltage, provides an excellent method for regulating output current while maintaining high system efficiency.

The TPS92690 uses peak current mode control providing good noise immunity and an inherent cycle-by-cycle current limit. The adjustable current sense threshold provides a way to analog dim the LED current, which can also be used to implement thermal foldback. The dual function nDIM pin provides a PWM dimming input that controls the main GATE output for PWM dimming the LED current also.

When designing, the maximum attainable LED current is not internally limited because the TPS92690 is a controller. Instead it is a function of the system operating point, component choices, and switching frequency allowing the TPS92690 to easily provide constant currents up to 5A. This simple controller contains all the features necessary to implement a high efficiency versatile LED driver.

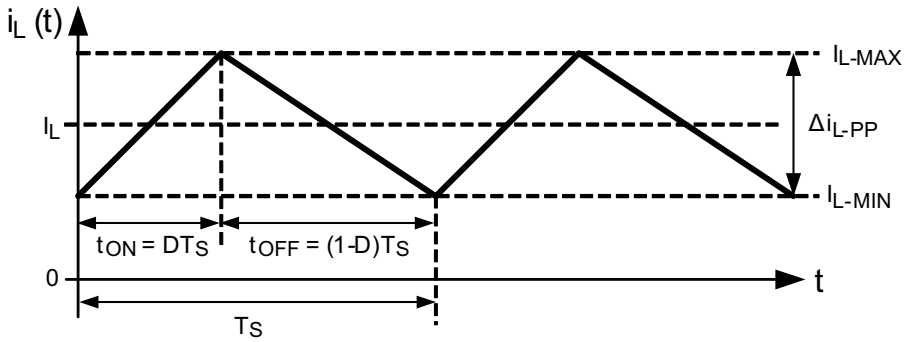


Figure 11. Basic CCM Inductor Current Waveform

CURRENT REGULATORS

Current regulators can be designed to accomplish different functions: boost, buck-boost, and flyback. The TPS92690 is designed to drive a ground referenced NFET and sense a ground referenced LED load. This control architecture is perfect for driving boost, SEPIC, flyback, or Cuk topologies. It does not work with a floating buck or buck-boost topology since the LED current sense amplifier is ground referenced.

Looking at the boost design in the *Typical Boost Application*, the basic operation of a current regulator can be analyzed. During the time that the NFET (Q1) is turned on (t_{ON}), the input voltage source stores energy in the inductor (L1) while the output capacitor (C_O) provides energy to the LED load. When Q1 is turned off (t_{OFF}), the re-circulating diode (D1) becomes forward biased and L1 provides energy to both C_O and the LED load. Figure 11 shows the inductor current ($i_L(t)$) waveform for a regulator operating in CCM.

The average output LED current (I_{LED}) is proportional to the average inductor current (I_L), therefore if I_L is tightly controlled, I_{LED} is well regulated. As the system changes input voltage or output voltage, the ideal duty cycle (D) is varied to regulate I_L and ultimately I_{LED}. For any current regulator, D is a function of the conversion ratio:

Boost

$$D = \frac{V_O - V_{IN}}{V_O} \quad (1)$$

Buck-Boost (SEPIC/Cuk)

$$D = \frac{V_O}{V_O + V_{IN}} \quad (2)$$

Flyback

$$D = \frac{nV_O}{nV_O + V_{IN}} \quad (3)$$

where n is the primary to secondary turns ratio of the coupled inductor, n:1.

PEAK CURRENT MODE CONTROL

Peak current mode control is used by the TPS92690 to regulate the average LED current through an array of HBLEDs. This method of control uses a series resistor in the LED path to sense LED current and can use either a series resistor in the MosFET path or the MosFET R_{DS-ON} for both cycle-by-cycle current limit and input voltage feed forward. The controller has a fixed switching frequency set by an internal programmable oscillator therefore slope compensation is added to mitigate current mode instability. A detailed explanation of this control method is presented in the following sections.

SWITCHING FREQUENCY AND SYNCHRONIZATION

The switching frequency of the TPS92690 is programmed using an external resistor (RT) connected from the RT pin to GND. This switching frequency is defined as:

$$f_{SW} = \frac{1}{2.29 \times 10^{-11} \times R_T + 80 \times 10^{-9}} \quad (4)$$

See Typical Characteristics for a graph of switching frequency versus resistance on RT. For maximum operational range and best efficiency a switching frequency of 1MHz or lower is recommended. Switching frequencies as high as 2MHz are possible for reduced solution size but some factors need to be considered. Higher frequencies require increased gate drive current and result in higher AC losses, both of which result in decreased efficiency. It is also possible that the minimum on time (leading edge blanking time) limits the minimum operational duty cycle and reduces the input voltage range for a given output voltage.

Alternatively, an external PWM signal can be applied to the SYNC pin to synchronize the part to an external clock. If the PWM signal frequency applied is higher than the base frequency set by the RT resistor, the internal oscillator is bypassed and the switching frequency is equal to the synchronized frequency. The PWM signal should have an amplitude between 2.5V and 5V. The TPS92690 triggers a switch-on time on the falling edge of the PWM signal and operates correctly regardless of the duty cycle of the applied signal.

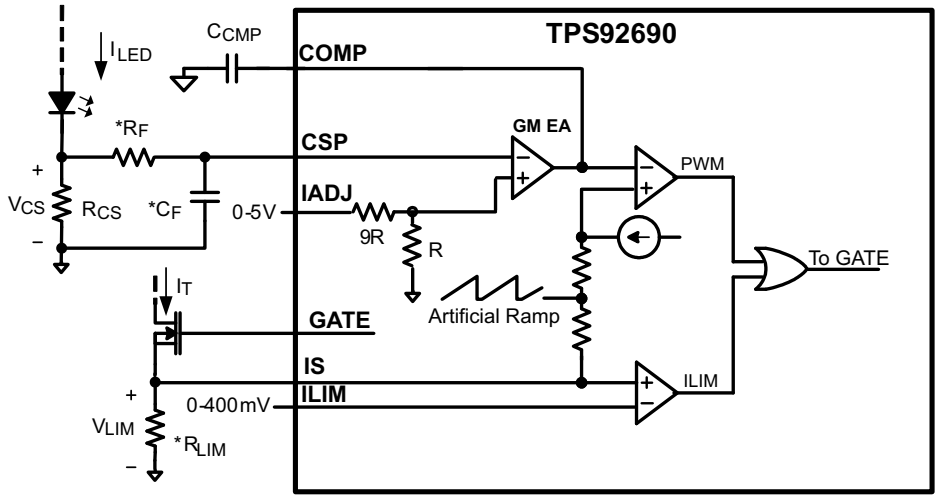


Figure 12. Current Sensed and Control Circuitry (* optional)

CURRENT SENSE/CURRENT LIMIT

The TPS92690 implements peak current mode control using the circuit shown in Figure 12. The peak detection is accomplished with a comparator that monitors the main MosFET current, comparing it with the COMP pin. When the IS voltage (plus the DC level shift and the ramp discussed later) exceeds the COMP voltage, the MosFET is turned off. The MosFET is turned back on when the oscillator starts a new on-time and the cycle repeats.

The IS pin incorporates a cycle-by-cycle over-current protection function. Current limit is accomplished by a redundant internal current sense comparator. If the voltage at the current sense comparator input (IS) exceeds the voltage at the ILIM pin, the MosFET is turned off and COMP is pulled to ground and discharged. The MosFET turns back on after either the 43µs current limit timeout has passed or after COMP is charged back up, whichever is longer. The IS input pin has an internal N-channel MosFET which pulls it down at the conclusion of every cycle. The discharge device remains on an additional 216 ns (typical) after the beginning of a new cycle to blank the leading edge spike on the current sense signal. This blanking time also results in a minimum switch-on time of 216 ns which determines a minimum duty cycle dependent upon switching frequency.

IS sensing can be done in one of two ways. The most accurate current sensing is accomplished by using a resistor, R_{LIM}. This adds a component that dissipates additional power but the result is higher accuracy and no limitation on the maximum MosFET drain voltage. For applications that have a maximum MosFET drain voltage below 75V MosFET R_{DS-ON} sensing can be used by connecting the IS pin directly to the drain of the MosFET and eliminating R_{LIM}. This results in higher efficiency but the accuracy depends on the accuracy of the MosFET R_{DS-ON}. Care must be taken to use the maximum expected R_{DS-ON} when setting the current limit threshold at ILIM.

AVERAGE LED CURRENT

The COMP pin voltage is dynamically adjusted, via the internal error amplifier, to maintain the desired regulation. Average LED current regulation is set using a sense resistor in series with the LEDs. The voltage across the sense resistor (V_{CS}) is regulated to the IADJ voltage divided by 10.

IADJ can be set to any value up to 2.45V by connecting it to VREF through a resistor divider for static output current settings. IADJ can also be used to change the regulation point if connected to a controlled voltage source up to 5V or potentiometer to provide analog dimming. It is also possible to configure IADJ to be used for thermal foldback functions.

$$I_{LED} = \frac{V_{CS}}{R_{CS}} \tag{5}$$

$$V_{CS} = \frac{V_{IADJ}}{10} \tag{6}$$

The TPS92690 maintains high accuracy at any level of V_{CS} but note that the accuracy still is better with higher levels as offsets and other errors become a smaller percentage of the overall V_{CS} voltage. However, power losses are also higher with higher V_{CS} voltages. A good tradeoff for accuracy and efficiency is to set the maximum V_{CS} voltage to between 100mV and 250mV.

In some applications, such as a standard boost or flyback, the output capacitor can be connected from the output directly to ground. In these cases the CS pin can be directly connected to R_{CS}. In other applications an additional filter may be desired on CS (R_F and C_F). These would include topologies where the current through R_{CS} is not continuous such as in the Cuk configuration. Another example would be a boost regulator where PWM dimming is required and the output capacitor is connected directly across the LEDs. In these cases it is recommended to add a 47Ω resistor for R_F and a 47nF capacitor for C_F to achieve the best accuracy and line regulation.

PRECISION REFERENCE (VREF)

The TPS92690 includes a precision 2.45V reference. This can be used in conjunction with a resistor divider to set voltage levels for the ILIM pin and the IADJ pin to set the maximum current limit and LED current. It can also be used with high impedance external circuitry requiring a reference. To set the current limit (I_{CL}) using VREF you can use the following equations:

$$I_{CL} = \frac{V_{LIM}}{R_{LIM}} \tag{7}$$

$$V_{LIM} = V_{ILIM} = VREF \times \frac{R_{LIM1}}{R_{LIM1} + R_{LIM2}} \tag{8}$$

When R_{DS-ON} sensing is being used substitute R_{LIM} in the above equation with R_{DS-ON}. A small amount of capacitance (C_{LIM}) can be placed from ILIM to ground for filtering if desired. If so, a value between 47pF and 100nF should be used but this value should not exceed the value of C_{CMP} to avoid false triggering of the current limit. To set the IADJ voltage level using VREF use the following equation:

$$V_{IADJ} = VREF \times \frac{R_{ADJ1}}{R_{ADJ1} + R_{ADJ2}} \quad (9)$$

If desired, place a small capacitor (C_{ADJ}) from IADJ to ground for additional filtering. A value between 47pF and 100nF should be sufficient.

LOW-LEVEL ANALOG DIMMING

The IADJ pin of the TPS92690 can be driven as low as 0V. At some level however minimum on time is encountered. This level depends on the switching frequency used. When the voltage on IADJ is lowered beyond this point the TPS92690 begins to skip pulses to maintain average output current regulation. Depending on external components and regulator bandwidth this may or may not result in visible flicker. If flicker is present below this level higher inductor and/or output capacitors may help and a lower COMP capacitor value may help. In many cases this level occurs at very low LED current and it is more desirable to simply limit the low level on the IADJ pin as shown in Figure 13:

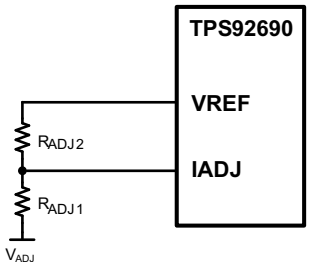


Figure 13. Limiting Minimum IADJ Voltage

The resulting I_{ADJ} voltage can be found using the following equation:

$$V_{IADJ} = (VREF - V_{ADJ}) \times \frac{R_{ADJ1}}{R_{ADJ1} + R_{ADJ2}} \quad (10)$$

SOFT-START/SHUTDOWN

The TPS92690 can be placed into a low power shutdown by grounding the SS/SD pin (any voltage below 100mV). During low power shutdown, the device limits the quiescent current to approximately 40µA, typical.

The SS/SD pin also has a 10uA current source (or 1uA when below the 100mV shutdown threshold), which charges a capacitor from SS/SD to GND to soft-start the converter. The SS/SD pin is attached through a PNP transistor to COMP therefore it controls the speed at which COMP rises at startup. When VCC_{UV} is below the falling threshold, SS/SD is pulled down to reset the capacitor voltage to zero. Then when VCC_{UV} rising threshold is exceeded, the pin is released and charges via the 10µA current source.

VCC REGULATOR AND START-UP

The TPS92690 includes a high voltage, low dropout bias regulator. When power is applied, or SS/SD is released, the regulator is enabled and sources current into an external capacitor (C_{BYP}) connected to the VCC pin. The recommended bypass capacitance for the VCC regulator is 2.2 µF to 3.3 µF. This capacitor should be rated for 10V or greater and an X7R dielectric ceramic is recommended. The output of the VCC regulator is monitored by an internal UVLO circuit that protects the device from attempting to operate with insufficient supply voltage and the supply is also internally current limited. VCC may also be driven externally to increase the GATE voltage and reduce the $R_{DS\text{-}ON}$ of the external switching MosFET. The maximum voltage on this pin is 14V and should not exceed the VIN voltage. The bypass capacitor voltage rating may need to be increased accordingly.

The start-up time of the TPS92690 to full output current depends on the value of C_{BYP}, C_{SS} (soft-start capacitor), C_{CMP}, and C_O (output capacitor) as shown in Figure 14:

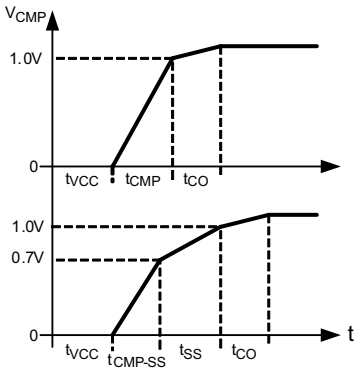


Figure 14. Start-up Waveforms

First, C_{BYP} is charged to be above the VCC UVLO threshold of 4.1V. The C_{BYP} charging time (t_{VCC}) can be estimated as:

$$t_{VCC} = \frac{4.1V \times C_{BYP}}{30mA} \quad (11)$$

Assuming there is no C_{SS} (top trace), or if C_{SS} is less than 40% of C_{CMP}, C_{CMP} is then charged to 1V over the charging time (t_{CMP}) which can be estimated as:

$$t_{CMP} = \frac{1V \times C_{CMP}}{V_{CS} \times 35\mu S} \quad (12)$$

Once C_{CMP} = 1V, the part starts switching to charge C_O until the LED current is in regulation. The C_O charging time (t_{CO}) can be roughly estimated as:

$$t_{CO} = \frac{C_O \times V_O}{I_{LED}} \quad (13)$$

If C_{SS} is greater than 40% of C_{CMP} (bottom trace), the compensation capacitor only charges to 0.7V over a smaller C_{CMP} charging time (t_{CMP-SS}) which can be estimated as:

$$t_{CMP-SS} = \frac{0.7V \times C_{CMP}}{V_{CS} \times 35\mu S} \quad (14)$$

Then COMP clamps to SS, forcing COMP to rise (the last 300mV before switching begins) according to the C_{SS} charging time (t_{SS}) which can be estimated as:

$$t_{SS} = \frac{0.3V \times C_{SS}}{11\mu A} \quad (15)$$

The system start-up time t_{SU} (for C_{SS} < 0.4 C_{CMP}) or t_{SU-SS} (for C_{SS} > 0.4 C_{CMP} is defined as:

$$t_{SU} = t_{VCC} + t_{CMP} + t_{CO} \quad (16)$$

$$t_{SU-SS} = t_{VCC} + t_{CMP-SS} + t_{SS} + t_{CO} \quad (17)$$

As a general rule of thumb, standard smooth startup operation can be achieved with C_{SS} = C_{CMP}. If SD/SS is being driven by an external source the equations above may need to be modified depending on the current sourcing capability of the external source.

OVER-VOLTAGE PROTECTION (OVP)

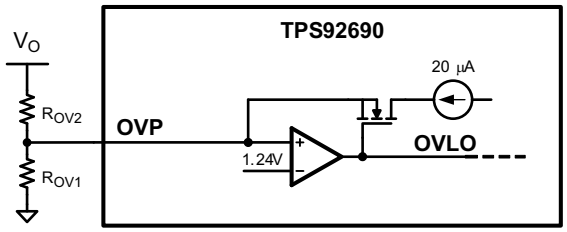


Figure 15. Over-voltage Protection Circuitry

The TPS92690 includes a dedicated OVP pin which can be used for either input or output over-voltage protection. This pin features a precision 1.24V threshold with 20 µA (typical) of hysteresis current as shown in Figure 15. When the OVP threshold is exceeded, the GATE pin is immediately pulled low and a 20 µA current source provides hysteresis to the lower threshold of the OVP hysteretic band.

The over-voltage turn-off threshold ($V_{TURN-OFF}$) and the hysteresis (V_{HYSO}) are defined by:

$$V_{TURN-OFF} = 1.24V \times \frac{R_{OV1} \times R_{OV2}}{R_{OV1}} \quad (18)$$

$$V_{HYSO} = 20\mu A \times R_{OV2} \quad (19)$$

INPUT UNDER-VOLTAGE LOCKOUT (UVLO)

The nDIM pin is a dual function input that features an accurate 1.24V threshold with programmable hysteresis as shown in Figure 16. This pin functions as both the PWM dimming input for the LEDs and as a VIN UVLO. When the pin voltage rises and exceeds the 1.24V threshold, 20 µA (typical) of current is driven out of the nDIM pin into the resistor divider providing programmable hysteresis.

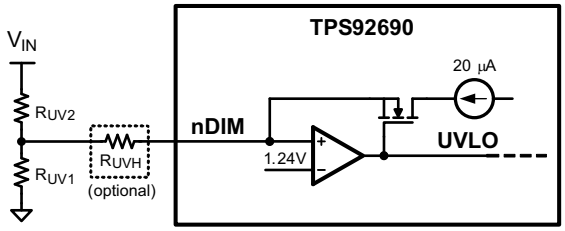


Figure 16. UVLO Circuit

When using the nDIM pin for UVLO and PWM dimming concurrently, the UVLO circuit can have an extra resistor to set the hysteresis. This allows the standard resistor divider to have smaller values minimizing PWM delays due to a pull-down MosFET at the nDIM pin (see *PWM DIMMING* section). In general, at least 3V of hysteresis is preferable when PWM dimming if operating near the UVLO threshold. The turn-on threshold ($V_{TURN-ON}$) is defined as follows:

$$V_{TURN-ON} = 1.24V \times \frac{R_{UV1} \times R_{UV2}}{R_{UV1}} \quad (20)$$

The hysteresis (V_{HYS}) is defined as follows:

UVLO Only

$$V_{HYS} = 20\mu A \times R_{UV2} \quad (21)$$

PWM Dimming and UVLO

$$V_{HYS} = 20\mu A \times \left(R_{UV2} + \frac{R_{UVH} \times (R_{UV1} + R_{UV2})}{R_{UV1}} \right) \quad (22)$$

PWM DIMMING

The active low nDIM pin can be driven with a PWM signal which controls the main NFET. The brightness of the LEDs can be varied by modulating the duty cycle of this signal. LED brightness is approximately proportional to the PWM signal duty cycle (i.e. 30% nDIM high duty cycle ~30% LED brightness). This function can be ignored if PWM dimming is not required by using nDIM solely as a VIN UVLO input as described in the *INPUT UNDER-VOLTAGE LOCKOUT* section or by tying it directly to VCC or VIN when UVLO is not required.

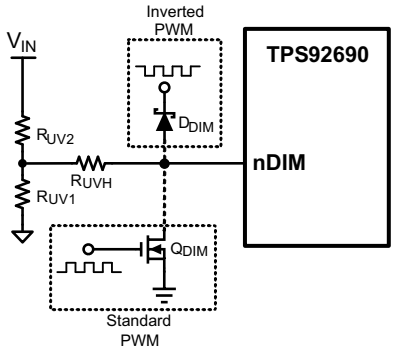


Figure 17. PWM Dimming Circuit

When using a MosFET (QDIM), connect the drain to the nDIM pin and the source to GND. Apply an external logic-level PWM signal to the gate of Q_{DIM}. Brightness is proportional to the negative duty cycle of the PWM signal. When using a Schottky diode (D_{DIM}), connect the anode to the nDIM pin. Apply an external logic-level PWM signal to the cathode of the diode and brightness is proportional to the positive duty cycle of the PWM signal.

CONTROL LOOP COMPENSATION

Compensating the TPS92690 is relatively simple for most applications. To prevent subharmonic oscillations due to current mode control a minimum inductor value should be chosen. This minimum value can be approximated with the following equation:

$$L_{min} = \frac{V_O \times 425 \times 10^3}{2 \times f_{SW}} (\mu H) \quad (23)$$

Compensating the control loop simply requires a capacitor from the COMP pin to ground. Most LED driver applications do not require high bandwidth response since there are no significant output transients and generally limited, low bandwidth input transients. The high output impedance (R_O) of the error amplifier (typically 200MΩ) enables a low bandwidth system where standard poles and zeros, including the right half plane zero in many cases, can be neglected. In this case the bandwidth of the system generally becomes the bandwidth of the error amplifier. A C_{CMP} value of 1nF to 100nF is recommended and results in the following dominant pole and crossover frequency:

$$f_{P1} = \frac{1}{2\pi \times R_O \times C_{CMP}} \quad (24)$$

$$f_C = \frac{g_m}{2\pi \times C_{CMP}} \quad (25)$$

A 1nF capacitor results in a bandwith of approximately 5.2kHz while a 100nF capacitor results in a bandwidth of approximately 52Hz. Larger values are recommended for most applications unless higher bandwidth is required. Larger values are also recommended for applications requiring PWM dimming as it allows the COMP pin to hold its level more accurately during the LED current off time. In applications where the duty cycle (D) exceeds 0.5 ($V_{IN} < V_O/2$ for a boost regulator) the location of the right half plane zero should be calculated to ensure stability using the following equation:

$$f_{RHPZ} = \frac{r_D \times D'^2}{2\pi \times D \times L1} \quad (26)$$

Where D and D' are calculated using the minimum input voltage. The crossover frequency f_C should be a decade below f_{RHPZ} for maximum stability. C_{CMP} should be adjusted accordingly if required.

THERMAL SHUTDOWN

The TPS92690 includes thermal shutdown protection. If the die temperature reaches approximately 175°C the device shuts down (GATE pin low). If the die temperature is allowed to cool until it reaches approximately 150°C the device resumes normal operation.

DESIGN CONSIDERATIONS

This section describes the application level considerations when designing with the TPS92690.

INDUCTOR

The inductor (L1) is the main energy storage device in a switching regulator. Depending on the topology, energy is stored in the inductor and transfered to the load in different ways (as an example, boost operation is detailed in the CURRENT REGULATORS section). The size of the inductor, the voltage across it, and the length of the switching subinterval (t_{ON} or t_{OFF}) determines the inductor current ripple ($\Delta i_{L\text{-}PP}$). In the design process, L1 is chosen to provide a desired $\Delta i_{L\text{-}PP}$. For a Cuk regulator the second inductor (L2) has a direct connection to the load, which is good for a current regulator. This requires little to no output capacitance therefore $\Delta i_{L\text{-}PP}$ is basically equal to the LED ripple current $\Delta i_{LED\text{-}PP}$ since the inductor ripple in L2 is equal to that in L1. However, for boost and other buck-boost regulators, there is always an output capacitor which reduces $\Delta i_{LED\text{-}PP}$, therefore the inductor ripple can be larger than in the Cuk regulator case where output capacitance is minimal or completely absent.

In general, $\Delta i_{LED\text{-}PP}$ is recommended by manufacturers to be less than 40% of the average LED current (I_{LED}). Therefore, for the CUK regulator with no output capacitance, $\Delta i_{LED\text{-}PP}$ should also be less than 40% of I_{LED}. For the boost and other buck-boost topologies, $\Delta i_{L\text{-}PP}$ can be much higher depending on the output capacitance value. However, $\Delta i_{L\text{-}PP}$ is suggested to be less than 100% of the average inductor current (Δi_L) to limit the RMS inductor current. $\Delta i_{L\text{-}PP}$ is defined as:

$$\Delta i_{L-PP} = \frac{V_{IN} \times D}{L \times f_{SW}} \tag{27}$$

Be sure to observe the minimum inductor value from the *CONTROL LOOP COMPENSATION* section. L1 is also suggested to have an RMS current rating at least 25% higher than the calculated minimum allowable RMS inductor current ($I_{L\text{-}RMS}$).

LED DYNAMIC RESISTANCE

When the load is a string of LEDs, the output load resistance is the LED string dynamic resistance plus R_{CS}. LEDs are PN junction diodes, and their dynamic resistance shifts as their forward current changes. Dividing the forward voltage of a single LED (V_{LED}) by the forward current (I_{LED}) can lead to an incorrect calculation of the dynamic resistance of a single LED (r_{LED}). The result can be 5 to 10 times higher than the true r_{LED} value.

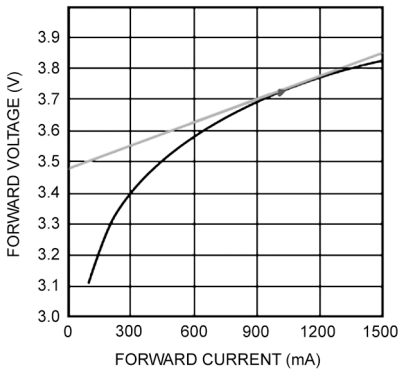


Figure 18. Dynamic Resistance

Obtaining r_{LED} is accomplished by refering to the manufacturer's LED I-V characteristic. It can be calculated as the slope at the nominal operating point as shown in Figure 18. For any application with more than 2 series LEDs, R_{CS} can be neglected allowing r_D to be approximated as the number of LEDs multiplied by r_{LED}.

OUTPUT CAPACITOR

For boost, SEPIC, and flyback regulators, the output capacitor (C_O) provides energy to the load when the recirculating diode (D1) is reverse biased during the first switching subinterval. An output capacitor in a Cuk topology simply reduces the LED current ripple (Δi_{LED-PP}) below the inductor current ripple (Δi_{L-PP}). In all cases, C_O is sized to provide a desired Δi_{LED-PP}. As mentioned in the INDUCTOR section, Δi_{LED-PP} is recommended by manufacturers to be less than 40% of the average LED current (I_{LED}).

C_O should be carefully chosen to account for derating due to temperature and operating voltage. It must also have the necessary RMS current rating. Ceramic capacitors are the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dieletric rating is suggested.

INPUT CAPACITOR

The input capacitor (C_{IN}) only needs to provide the ripple current due to the direct connection to the inductor. C_{IN} is selected given the maximum input voltage ripple (ΔV_{IN-PP}) which can be tolerated. ΔV_{IN-PP} is suggested to be less than 10% of the input voltage (V_{IN}). An input capacitance at least 100% greater than the calculated C_{IN} value is recommended to account for derating due to temperature and operating voltage. When PWM dimming, even more capacitance can be helpful to minimize the large current draw from the input voltage source during the rising transition of the LED current waveform.

The chosen input capacitors must also have the necessary RMS current rating. Ceramic capacitors are again the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dieletric rating is suggested.

For most applications, it is recommended to bypass the VIN pin with an 0.1µF ceramic capacitor placed as close as possible to the pin. In situations where the bulk input capacitance may be far from the TPS92690 device, a 10Ω series resistor can be placed between the bulk input capacitance and the bypass capacitor, creating a 150kHz filter to eliminate undesired high frequency noise.

MOSFET SELECTION

The TPS92690 requires an external NFET (Q1) as the main power MosFET for the switching regulator. Q1 is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node. In practice, all switching regulators have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. The current rating is recommended to be at least 10% higher than the average transistor current. The power rating is then verified by calculating the power loss given the average transistor current and the NFET on-resistance (R_{DS-ON}).

In general, the NFET should be chosen to minimize total gate charge (Q_g) when f_{SW} is high and minimize R_{DS-ON} otherwise. This minimizes the dominant power losses in the system. Frequently, higher current NFETs in larger packages are chosen for better thermal performance.

RE-CIRCULATING DIODE

A re-circulating diode (D1) is required to carry the inductor current during t_{OFF}. The most efficient choice for D1 is a Schottky diode due to low forward voltage drop and near-zero reverse recovery time. Similar to Q1, D1 is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current. The power rating is verified by calculating the power loss through the diode. This is accomplished by checking the typical diode forward voltage from the I-V curve on the product datasheet and multiplying by the average diode current. In general, higher current diodes have a lower forward voltage and come in better performing packages minimizing both power losses and temperature rise.

CIRCUIT LAYOUT

The performance of any switching regulator depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines maximimizes noise rejection and minimizes the generation of EMI within the circuit.

Discontinuous currents are the most likely to generate EMI, therefore care should be taken when routing these paths. In the TPS92690 boost regulator, the discontinuous current flows through the output capacitor (C_O), D1, Q1, and R_{LIM} (if used). These loops should be kept as small as possible and the connections between all the components should be short and thick to minimize parasitic inductance. In particular, the switch node (where L1, D1 and Q1 connect) should be just large enough to connect the components. To minimize excessive heating, large copper pours can be placed adjacent to the short current path of the switch node.

The RT, COMP, CSP, IS, IADJ, ILIM, and SYNC pins are all high-impedance inputs which couple external noise easily, therefore the loops containing these nodes should be minimized whenever possible.

In some applications the LED or LED array can be far away (several inches or more) from the TPS92690, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the regulator, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.

TYPICAL APPLICATION CIRCUITS

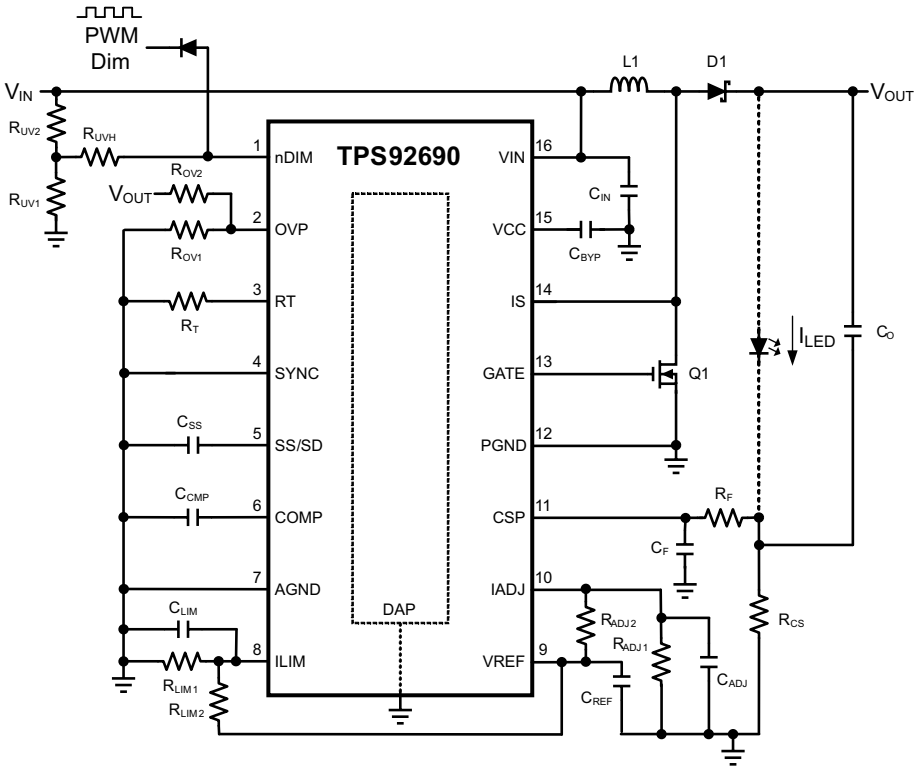


Figure 19. Boost Topology with PWM Dimming

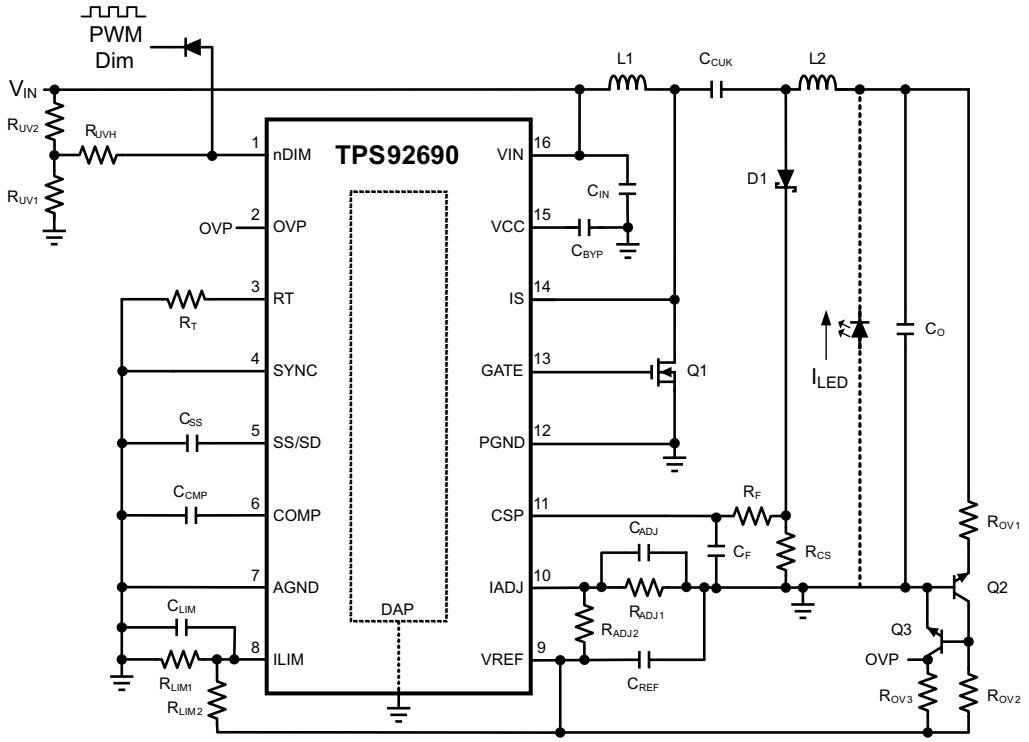


Figure 20. Cuk Topology (buck-boost)

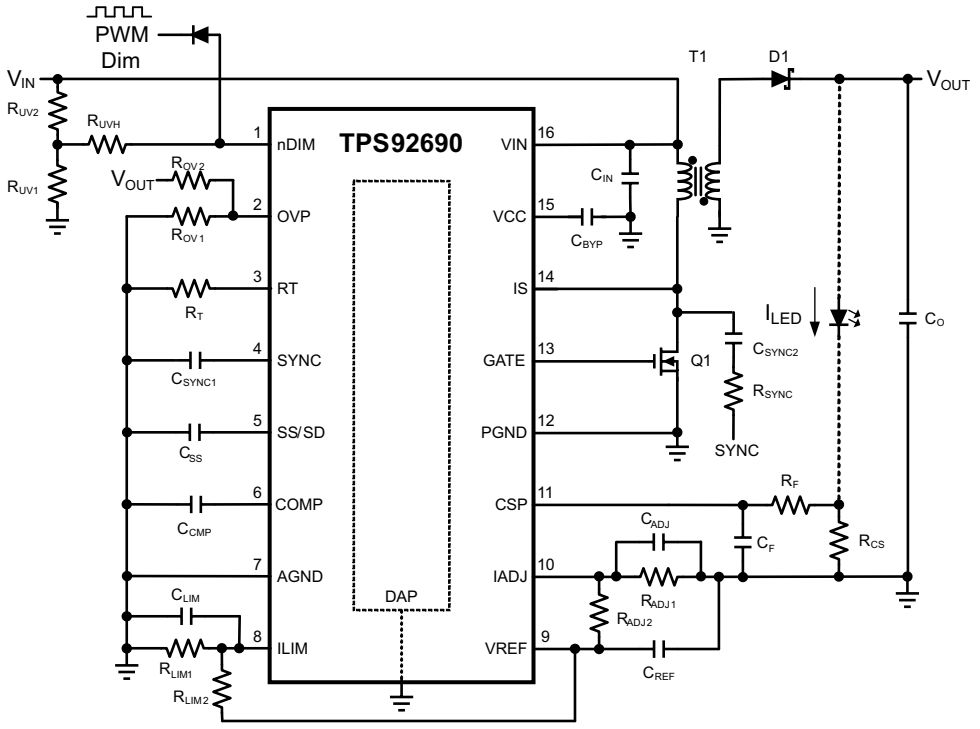


Figure 21. Quasi-Resonant Flyback Topology

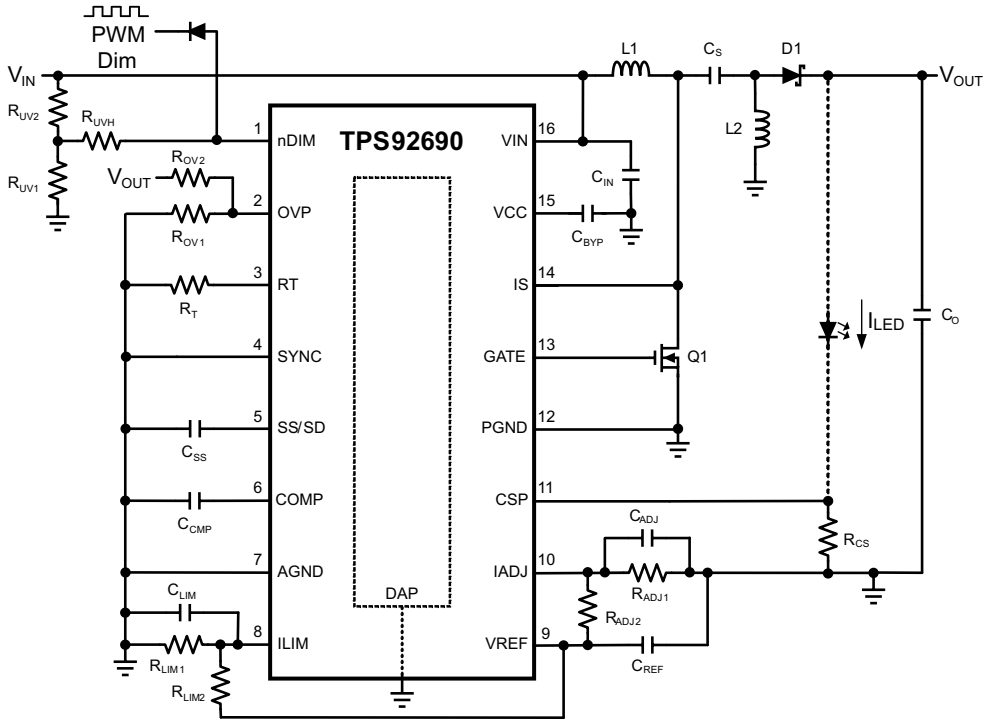


Figure 22. SEPIC Topology (buck-boost)

PHYSICAL DIMENSIONS

in millimeters unless otherwise noted

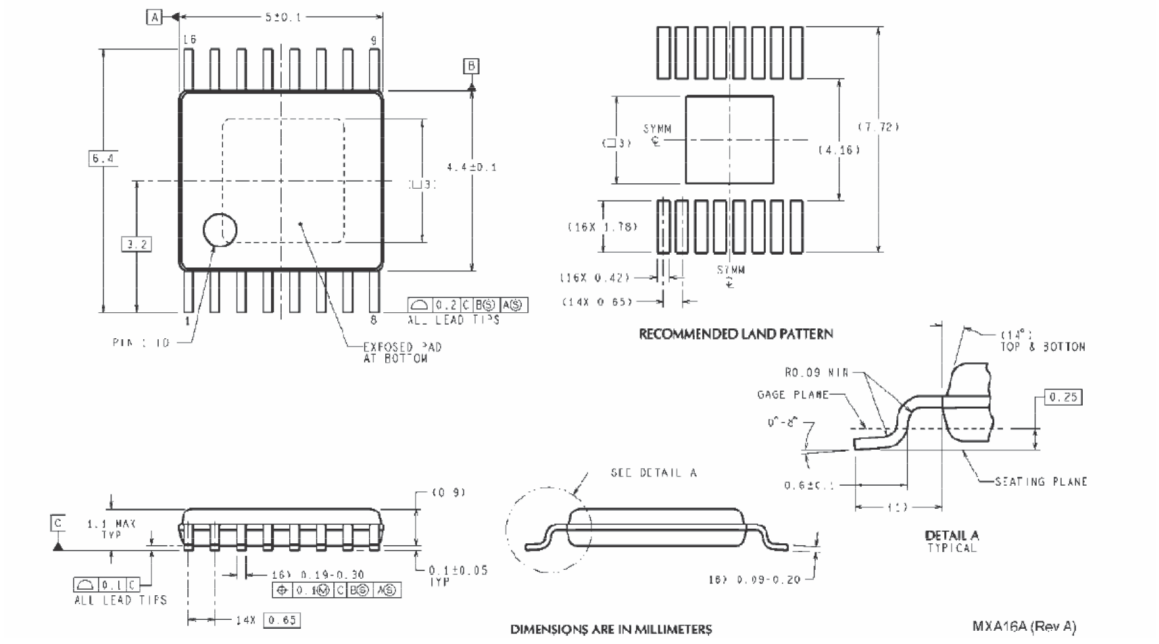


Figure 23. 16-lead TSSOP Exposed Pad Package

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92690PWP/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TP92690 PWP	Samples
TPS92690PWPR/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TP92690 PWP	Samples
TPS92690Q1PWP/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TP92690 Q1PWP	Samples
TPS92690Q1PWPR/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TP92690 Q1PWP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS92690, TPS92690-Q1 :

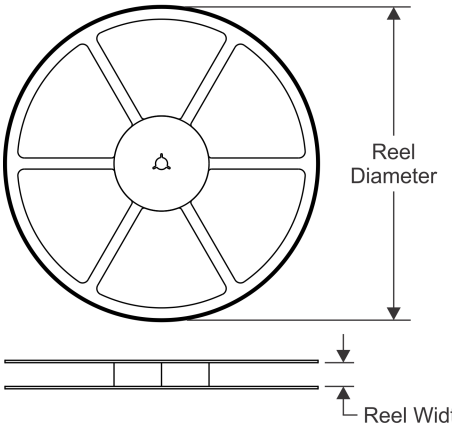
- Catalog: TPS92690
- Automotive: TPS92690-Q1

NOTE: Qualified Version Definitions:

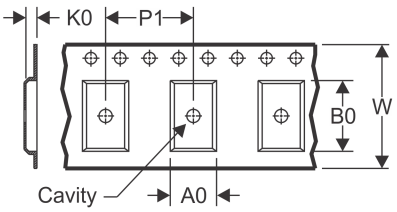
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

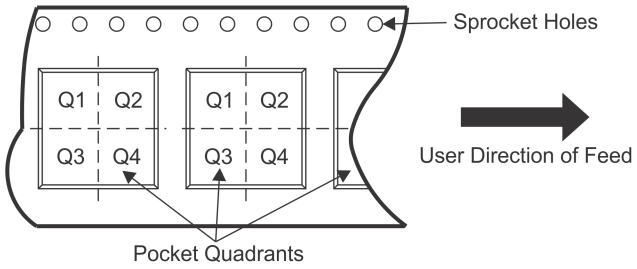


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

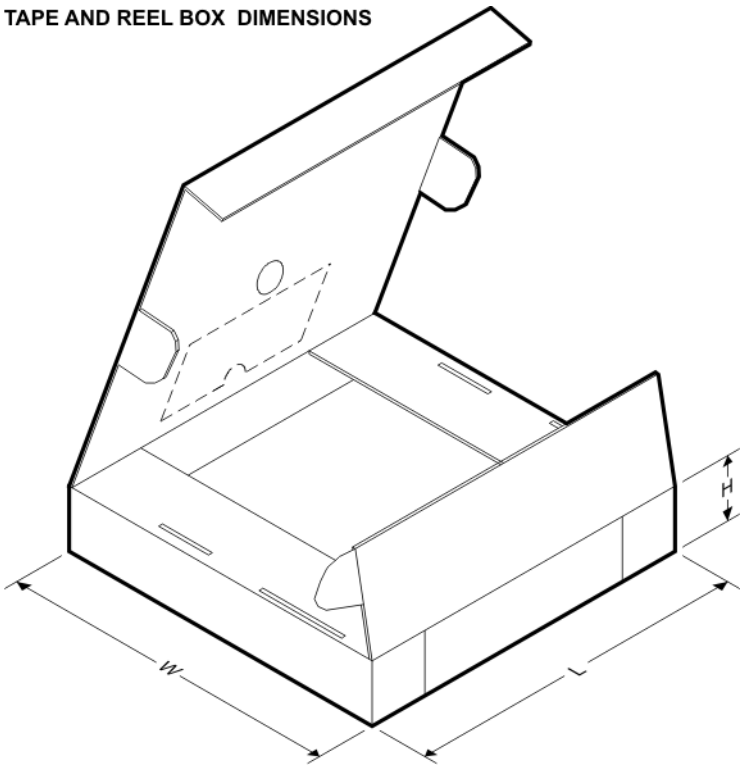
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92690PWPR/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
TPS92690Q1PWPR/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

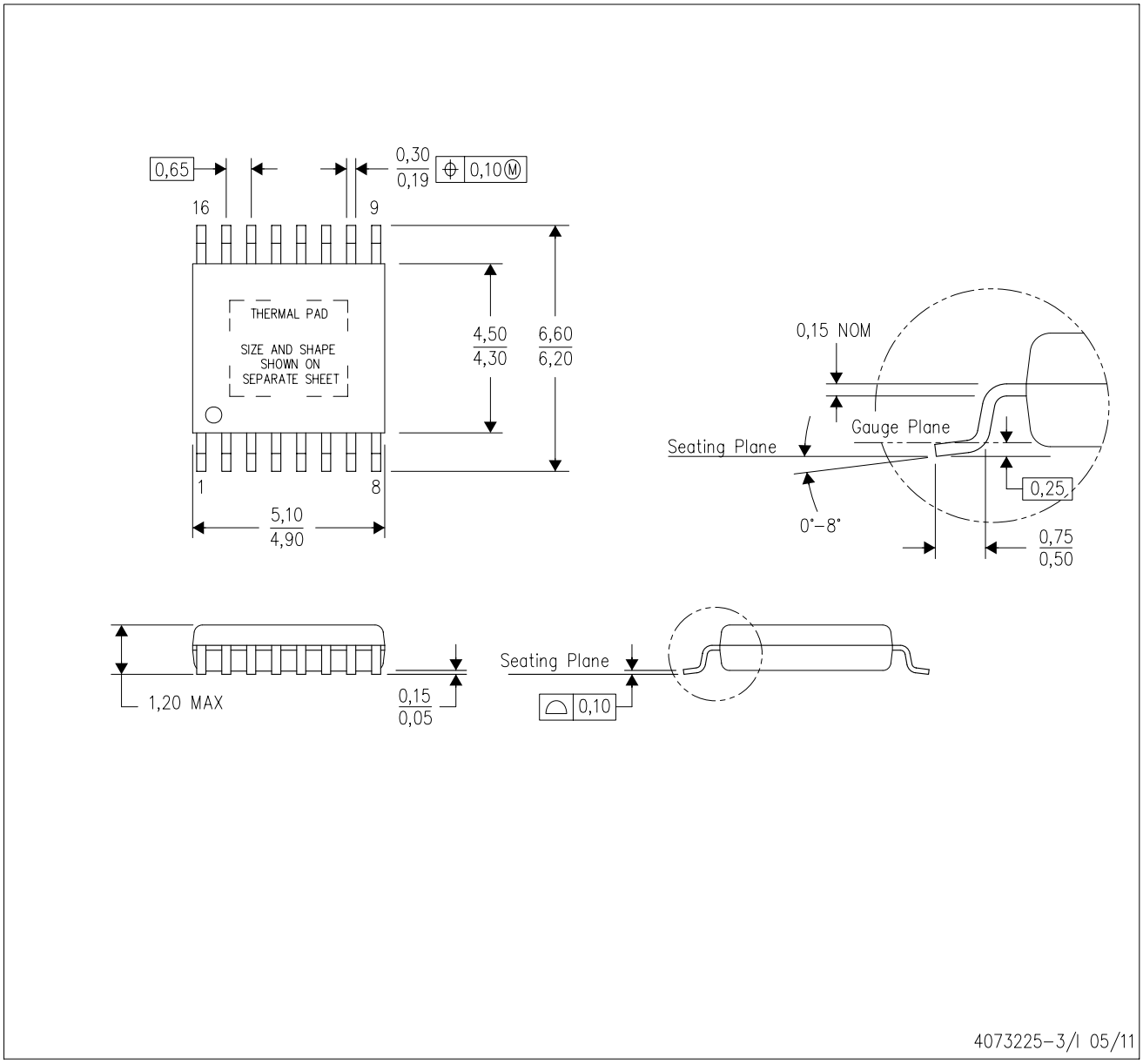
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

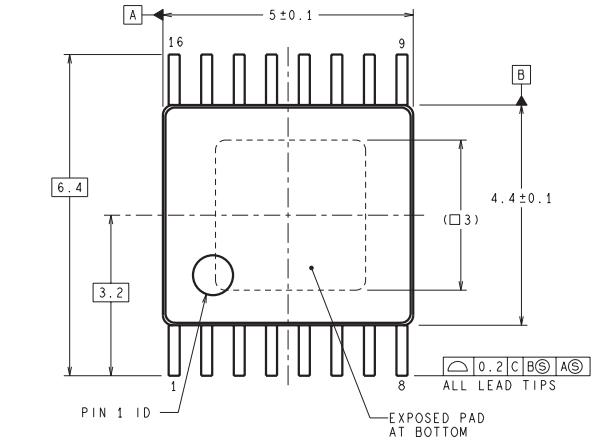
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92690PWPR/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
TPS92690Q1PWPR/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0

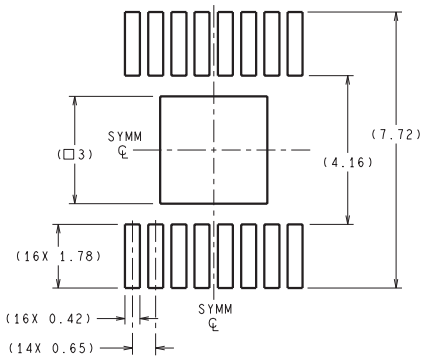
PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



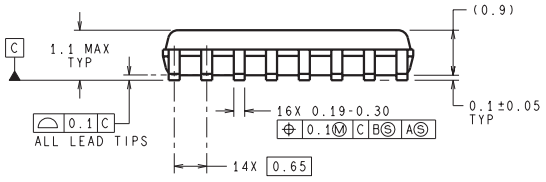
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

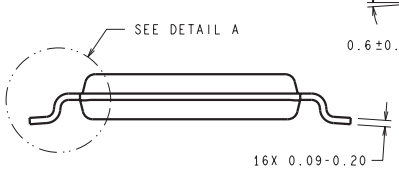
PWP0016A

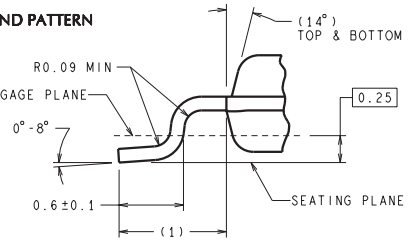




RECOMMENDED LAND PATTERN







DETAIL A
TYPICAL

DIMENSIONS ARE IN MILLIMETERS

MXA16A (Rev A)

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