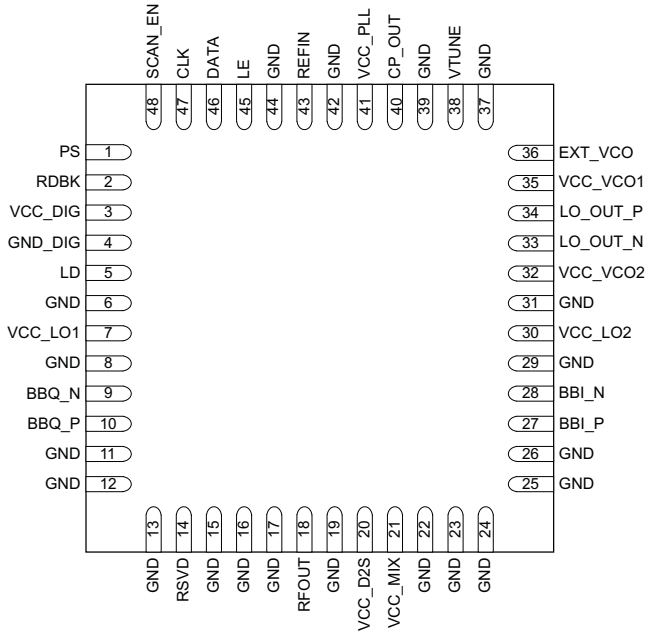
Integrated IQ Modulator PLL/VCO

FEATURES

- Fully Integrated PLL/VCO and IQ Modulator
- LO Frequency from 300MHz to 4.8GHz
- 76-dBc Single-Carrier WCDMA ACPR at –8dBm Channel Power
- OIP3 of 26 dBm
- P1dB of 11.5 dBm
- Integer/Fractional PLL
- Phase Noise –132 dBc/Hz (at 1MHz, f_{VCO} of 2.3 GHz)
- Low Noise Floor: –160 dBm/Hz
- Input Reference Frequency Range: Up to 160MHz
- VCO Frequency Divided by 1-2-4-8 Output



APPLICATIONS

- Wireless Infrastructure
  - CDMA: IS95, UMTS, CDMA2000, TD-SCDMA
  - TDMA: GSM, IS-136, EDGE/UWC-136
  - LTE
- Wireless Local Loop
- Point-to-Point Wireless Access
- Wireless MAN Wideband Transceivers

DESCRIPTION

TRF372017 is a high performance direct up-conversion device, integrating a high linearity, low noise IQ modulator and an integer-fractional PLL/VCO. The VCO uses integrated frequency dividers to achieve a wide, continuous tuning range of 300MHz–4800MHz. The LO is available as an output with independent frequency dividers. The device also accepts input from an external LO or VCO. The modulator baseband inputs can be biased either internally or externally. Internal DC offset adjustment enables carrier cancellation. The device is controlled through a 3 wire serial programming interface (SPI). A control pin invokes power-save mode to reduce power consumption while keeping the VCO locked for fast startup.

FREQUENCY RANGE OPERATION

VCO Frequency		Div by 2		Div by 4		Div by 8	
Fmin	Fmax	Fmin	Fmax	Fmin	Fmax	Fmin	Fmax
2400	4800	1200	2400	600	1200	300	600

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE DEVICE OPTIONS

PRODUCT	PACKAGE LEAD	PACKAGE DESIGNATOR	SPECIFIED OPERATING TEMPERATURE	PACKAGE MARKING	MEDIA, QUANTITY
TRF372017IRGZT	QFN-48	RGZ	–40°C to 85°C	TRF372017	Tape and Reel, 250
TRF372017IRGZR	QFN-48	RGZ	–40°C to 85°C	TRF372017	Tape and Reel, 2500

FUNCTIONAL BLOCK DIAGRAM

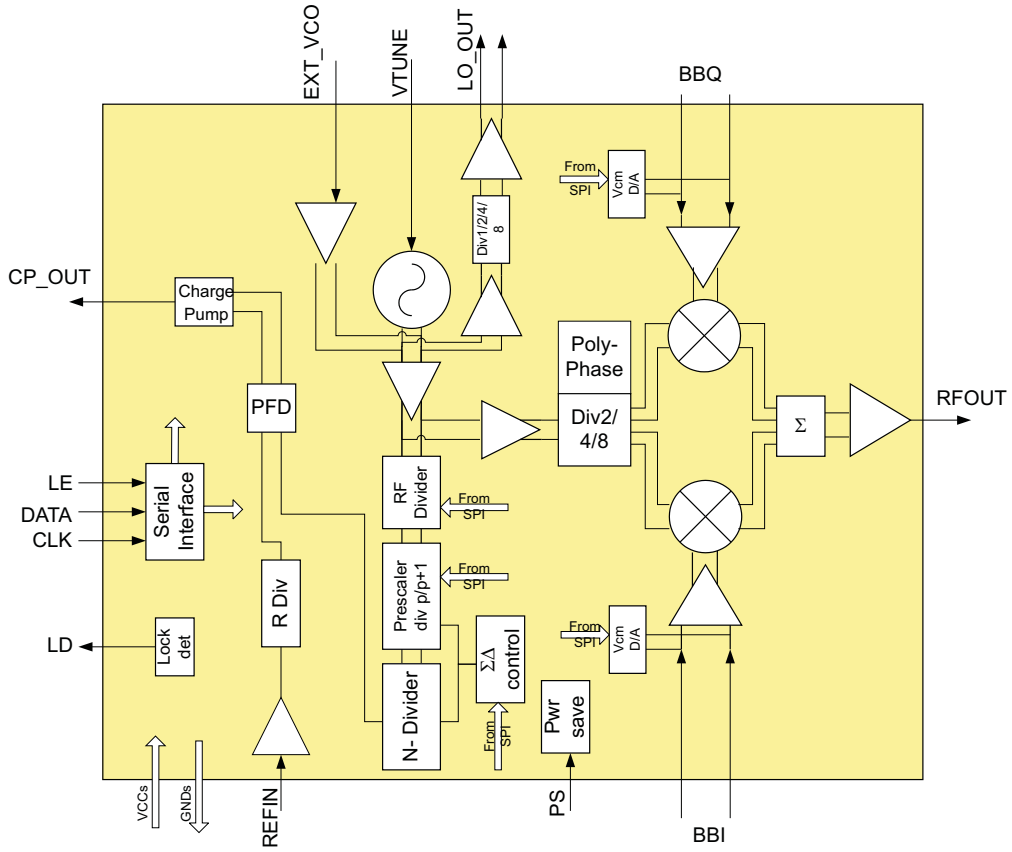

Figure 1. TRF372017 Block Diagram

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PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NAME	NO		
PS	1	I	Power saving mode enable (Low = normal mode; High = power saving mode)
RDBK	2	O	SPI internal registers readback output
VCC_DIG	3		3.3V digital power supply
GND_DIG	4		Digital ground
LD	5	O	PLL lock detect output
GND	6		Ground
VCC_LO1	7		3.3V Tx path local oscillator chain power supply
GND	8		Ground
BBQ_N	9	I	Base-band in-quadrature input: negative terminal
BBQ_P	10	I	Base-band in-quadrature input: positive terminal
GND	11		Ground
GND	12		Ground
GND	13		Ground
RSVD	14		Reserved. Normally open.
GND	15		Ground
GND	16		Ground
GND	17		Ground
RFOUT	18	O	RF output
GND	19		Ground
VCC_D2S	20		5V modulator output buffer power supply
VCC_MIX	21		5V modulator power supply
GND	22		Ground
GND	23		Ground
GND	24		Ground
GND	25		Ground
GND	26		Ground
BBI_P	27	I	Base-band in-phase input: positive terminal
BBI_N	28	I	Base-band in-phase input: negative terminal
GND	29		Ground
VCC_LO2	30		3.3V output local oscillator chain power supply
GND	31		Ground
VCC_VCO2	32		3.3 – 5.0V VCO power supply
LO_OUT_N	33	O	Local oscillator output: negative terminal
LO_OUT_P	34	O	Local oscillator output: positive terminal
VCC_VCO1	35		3.3V VCO power supply
EXT_VCO	36	I	External local oscillator input
GND	37		Ground
VTUNE	38	I	VCO control voltage input
GND	39		Ground
CP_OUT	40	O	Charge pump output
VCC_PLL	41		3.3V PLL power supply
GND	42		Ground
REFIN	43	I	Reference clock input
GND	44		Ground
LE	45	I	SPI latch enable. Digital input
DATA	46	I	SPI data input. Digital input

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PIN FUNCTIONS (continued)

PIN		TYPE	DESCRIPTION
NAME	NO		
CLK	47	I	SPI clock input. Digital input
SCAN_EN	48	I	Internal testing mode. Connect to ground in normal operation

THERMAL INFORMATION

THERMAL METRIC(1)		TRF372017 RGZ 48 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	30	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	10	
θ_{JB}	Junction-to-board thermal resistance	8	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

	VALUE	UNIT
Supply voltage range(3)	–0.3 to 5.5	V
Digital I/O voltage range	–0.3 to V_{CC} + 0.5	V
Operating virtual junction temperature range, T_J	–40 to 150	°C
Operating ambient temperature range, T_A	–40 to 85	°C
Storage temperature range, T_{stg}	–40 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) ESD rating not valid for RF sensitive pins.
(3) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC5V}	5V Power supply voltage	4.5	5.0	5.5	V
V_{CC3V}	3.3V Power supply voltage	3.0	3.3	3.6	V
VCC_VCO2	3.3–5V Power supply voltage	3.0	3.3	5.5	V
T_A	Operating ambient temperature range	–40		85	°C
T_J	Operating virtual junction temperature range	–40		125	°C

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ELECTRICAL CHARACTERISTICS

V_{CC5V} = 5.0V, V_{CC3V} = 3.3V, VCC_VCO2 = 3.3V, T_A = 25°C, internal LO, internal VCM (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PARAMETERS						
I_{CC}	Total supply current, LO on(1)	3.3V power supply, LO on		200	250	mA
		5V power supply, LO on		117	148	mA
	Supply current, LO on(1)	VCC_DIG, LO on		3	5	mA
		VCC_LO1 and VCC_LO2		121	130	mA
		VCC_D2S		43	60	mA
		VCC_MIX		74	90	mA
		VCC_VCO1		20	28	mA
		VCC_VCO2		17	20	
		LO_OUT_N and LO_OUT_P		17	28	mA
		VCC_PLL		24	40	mA
	Total supply current, LO off(1)	3.3V power supply, LO off		165	204	mA
		5V power supply, LO off		117	149	mA
	Total supply current, PS on(1)	3.3V power supply, PS on		65	94	mA
		5V power supply, PS on		51	73	mA
BASEBAND INPUTS						
V_{cm}	I and Q Input DC common voltage(2)	Externally generated		1.7		V
		Set internally	1.6	1.7	1.85	V
BW	1dB Input frequency bandwidth			1000		MHz
Z_I	Input Impedance	Resistance		5		kΩ
		Parallel Capacitance		3		pF
BASEBAND INPUT DC OFFSET CONTROL D/A(3)						
	Number of bits	Programmed via SPI		8		
	Programmable DC offset setting	|BBI_P - BBI_N| or |BBQ_P - BBQ_N|, 100-Ω differential load			0.02	V
DIGITAL INTERFACE						
V_{IH}	High-level input voltage		2	3.3		V
V_{IL}	Low-level input voltage		0		0.8	V
V_{OH}	High-level output voltage	Referenced to VCC_DIG	0.8xVcc			V
V_{OL}	Low-level output voltage	Referenced to VCC_DIG			0.2xVcc	V
REFERENCE OSCILLATOR PARAMETERS						
F_{ref}	Reference Frequency				160	MHz
	Reference input sensitivity		0.2		3.3	Vp-p
	Reference input impedance	Parallel capacitance		5		pF
		Parallel resistance	3900			Ω
PFD CHARGE PUMP						
	PFD frequency(4)				100	MHz
I_{CP}	Charge pump current	SPI programmable		1.94		mA

(1) Maximum current is worst-case over voltage, temperature, and expected process variations.
(2) The TRF372017 can generate the input common voltage internally or can accept an external common mode voltage. The two modes are selectable via SPI
(3) When the internal input common mode voltage is selected, it is possible to apply some dc offset with the integrated D/A
(4) See Application Information for discussion on selection of PFD frequency.

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TRF372017 ELECTRICAL CHARACTERISTICS

V_{CC5V} = 5.0V, V_{CC3V} = 3.3V, VCC_VCO2 = 3.3V, T_A = 25°C, internal LO, internal VCM (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IQ MODULATOR OUTPUT, F_{LO} = 750 MHz						
G	Voltage gain	Output rms voltage over se input I (or Q) rms voltage	–4	–3.2	–2.4	dB
P1dB	Output compression point			11		dBm
IP3	Output IP3	2 input tones at 4.5 and 5.5MHz		26		dBm
IP2	Output IP2	2 input tones at 4.5 and 5.5MHz		56.5		dBm
	Carrier feedthrough	Unadjusted		–43.5		dBm
	Sideband suppression	Unadjusted		–46		dBc
	Output return loss			10		dB
	Output noise	DC only to BB inputs; 13 MHz offset from LO; Pout = –10 dBm		–162		dBm/Hz
IQ MODULATOR OUTPUT, F_{LO} = 900 MHz						
G	Voltage Gain	Output rms voltage over se input I (or Q) rms voltage	–4	–3.4	–2.4	dB
P1dB	Output Compression Point			11		dBm
IP3	Output IP3	2 input tones at 4.5 and 5.5 MHz		26.5		dBm
IP2	Output IP2	2 input tones at 4.5 and 5.5 MHz		56.5		dBm
	Carrier Feedthrough	Unadjusted		–43		dBm
	Sideband suppression	Unadjusted		–45		dBc
	Output Return Loss			10		dB
	Output Noise	DC only to BB inputs; 13 MHz offset from LO; Pout = –10 dBm		–160		dBm/Hz
IQ MODULATOR OUTPUT, F_{LO} = 2150 MHz						
G	Voltage Gain	Output rms voltage over se input I (or Q) rms voltage	–4.2	–3.1	–2	dB
P1dB	Output Compression Point			11.5		dBm
IP3	Output IP3	2 input tones at 4.5 and 5.5 MHz		25		dBm
IP2	Output IP2	2 input tones at 4.5 and 5.5 MHz		56		dBm
	Carrier Feedthrough	Unadjusted		–40		dBm
	Sideband suppression	Unadjusted		–32		dBc
	Output Return Loss			10		dB
	Output Noise	DC only to BB inputs; 13 MHz offset from LO; Pout = –10 dBm		–158		dBm/Hz
ACPR	Adjacent-channel power ratio	1 WCDMA signal; Pout = –8 dBm		–75		dBc
		2 WCDMA signals; Pout = –11 dBm per carrier		–71		dBc
IQ MODULATOR OUTPUT, F_{LO} = 2700 MHz						
G	Voltage gain	Output rms voltage over se input I (or Q) rms voltage	–4.1	–2.7	–1.3	dB
P1dB	Output compression point			12		dBm
IP3	Output IP3	2 input tones at 4.5 and 5.5 MHz		26.5		dBm
IP2	Output IP2	2 input tones at 4.5 and 5.5 MHz		50		dBm
	Carrier feedthrough	Unadjusted		–43		dBm
	Sideband suppression	Unadjusted		–41		dBc
	Output return loss			10		dB
	Output noise	DC only to BB inputs; 13 MHz offset from LO; Pout = –10 dBm		–153		dBm/Hz

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TRF372017 ELECTRICAL CHARACTERISTICS (continued)

V_{CC5V} = 5.0V, V_{CC3V} = 3.3V, VCC_VCO2 = 3.3V, T_A = 25°C, internal LO, internal VCM (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOCAL OSCILLATOR						
F_{VCO}	Frequency Range	VCO range	2400		4800	MHz
		Divide by 2	1200		2400	
		Divide by 4	600		1200	
		Divide by 8	300		600	
	Free running VCO Phase Noise, Fout=2.3GHz	10kHz		–85		dBc/Hz
		1MHz		–132		dBc/Hz
		10MHz		–150		dBc/Hz
		50MHz		–153		dBc/Hz
P_{LO}	LO Output power(1)	100 Ω differential, external load; single-ended	–2.5	3		dBm

(1) With VCO frequency at 4.6 GHz and LO in divide-by-2 mode at 2.3 GHz

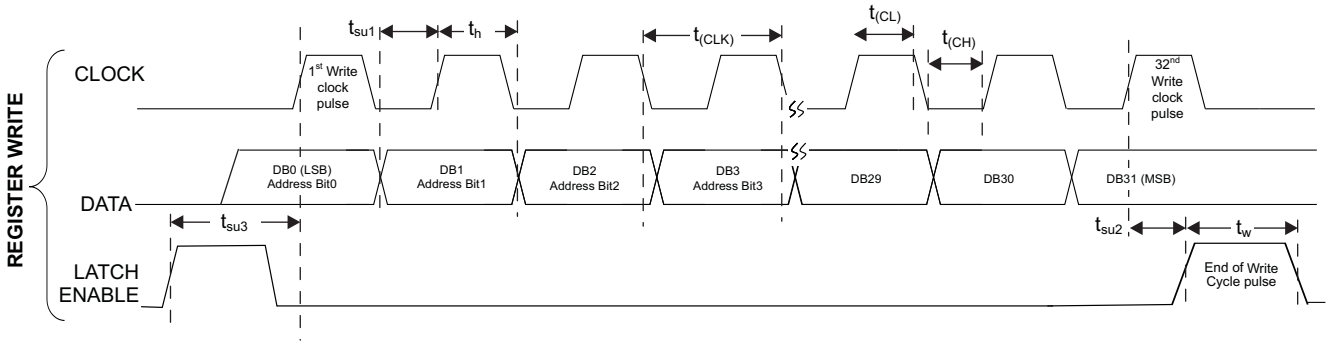

Figure 2. SPI Write Timing Diagram

Table 1. SPI Timing: Writing Phase

PARAMETER		MIN	TYP	MAX	UNITS
t_h	Hold time, data to clock	20			ns
t_{SU1}	Setup time, data to clock	20			ns
$T_{(CH)}$	Clock low duration	20			ns
$T_{(CL)}$	Clock high duration	20			ns
t_{SU2}	Setup time, clock to enable	20			ns
$t_{(CLK)}$	Clock period	50			ns
t_W	Enable time	50			ns
t_{SU3}	Setup time, latch to Data	70			ns

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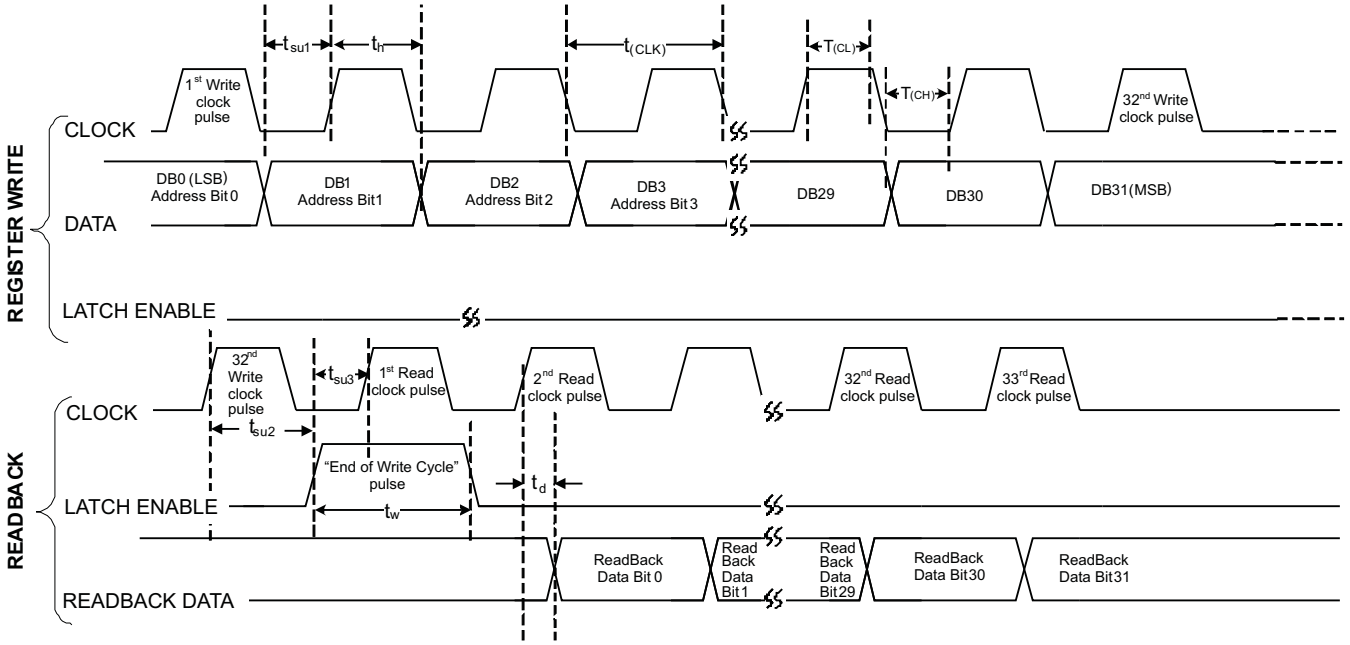

Figure 3. SPI Read-Back Timing Diagram

Table 2. SPI Timing Read-Back Phase

PARAMETER		MIN	TYP	MAX	UNITS	COMMENTS
t_h	Hold time, data to clock	20			ns	
t_{SU1}	Setup time, data to clock	20			ns	
$T_{(CH)}$	Clock low duration	20			ns	
$T_{(CL)}$	Clock High duration	20			ns	
t_{SU2}	Setup time, clock to enable	20			ns	
t_d	Delay time, clock to readback data output	10			ns	
t_W	Enable Time	50			ns	Equals Clock period
$t_{(CLK)}$	Clock period	50			ns	

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TYPICAL CHARACTERISTICS

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

OPEN LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

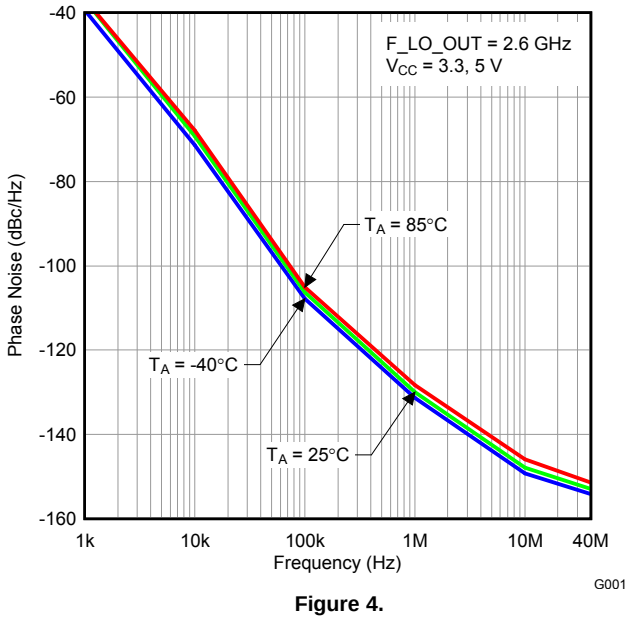

Figure 4.

OPEN LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

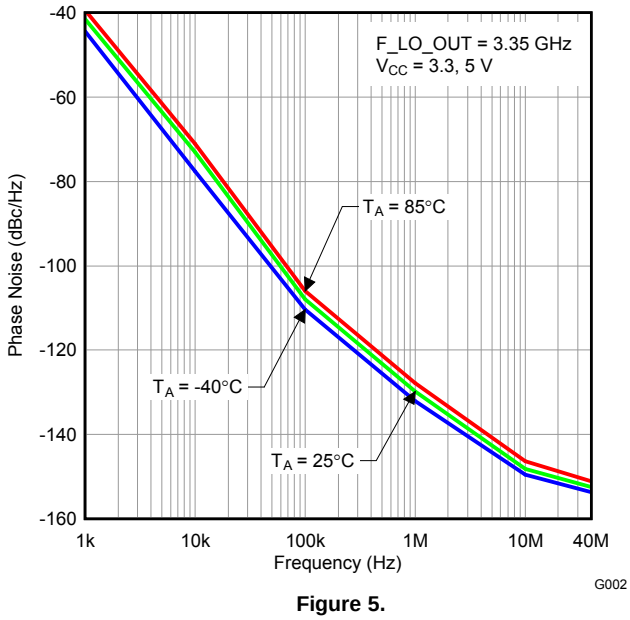

Figure 5.

OPEN LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

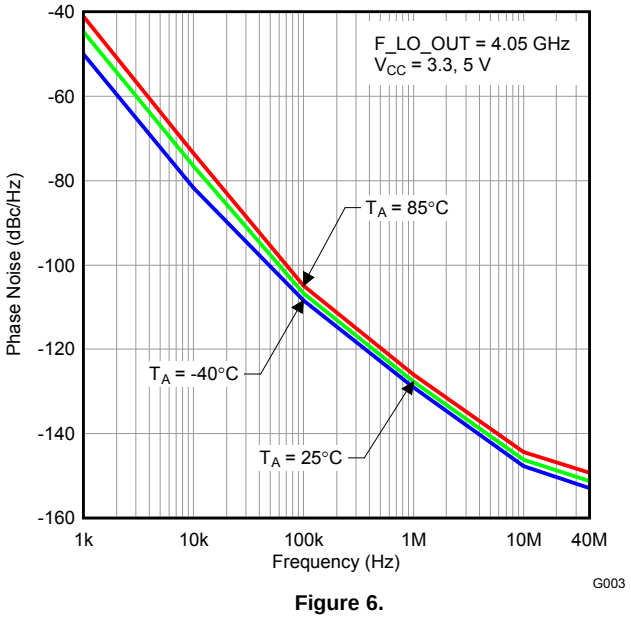

Figure 6.

OPEN LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

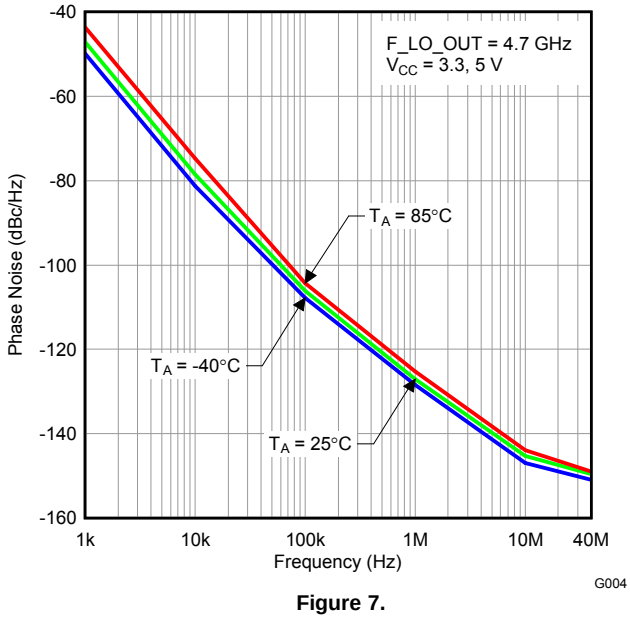

Figure 7.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

OPEN LOOP PHASE NOISE vs FREQUENCY AND SUPPLY VOLTAGE

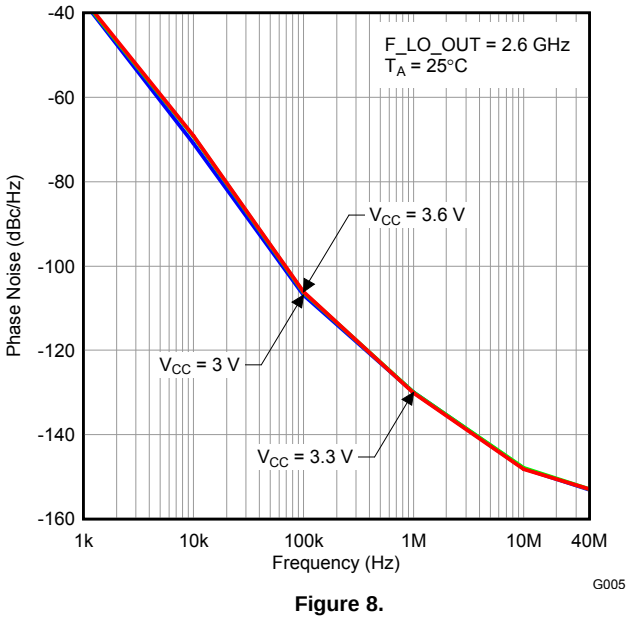

Figure 8.

OPEN LOOP PHASE NOISE vs FREQUENCY AND SUPPLY VOLTAGE

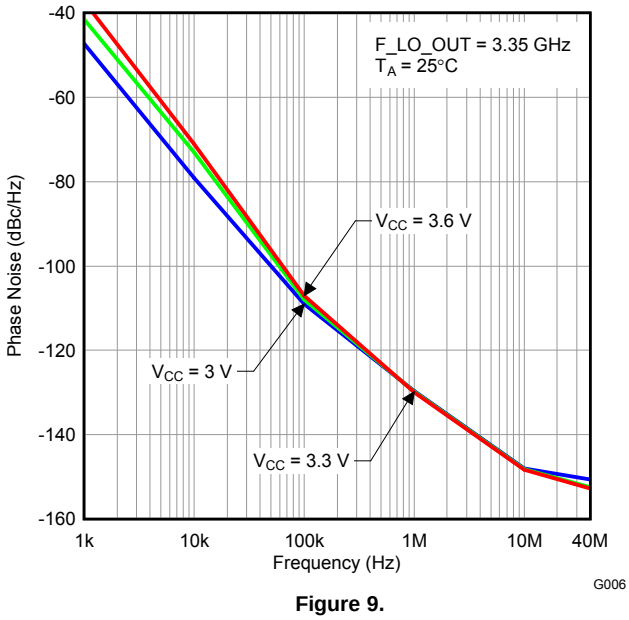

Figure 9.

OPEN LOOP PHASE NOISE vs FREQUENCY AND SUPPLY VOLTAGE

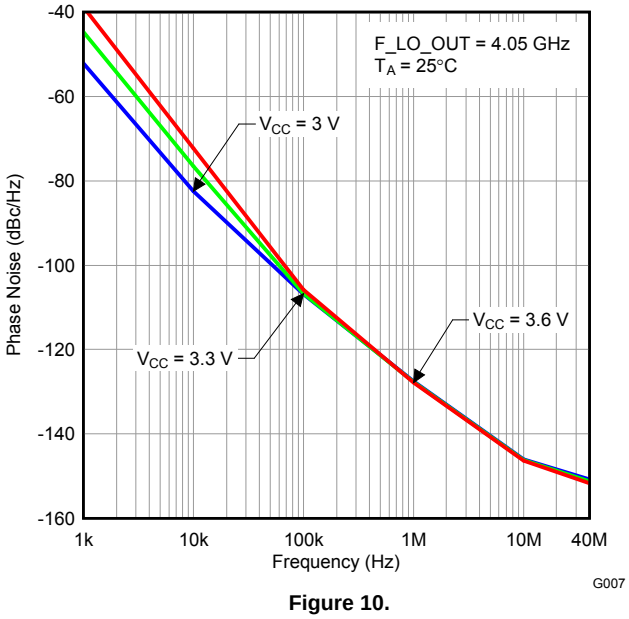

Figure 10.

OPEN LOOP PHASE NOISE vs FREQUENCY AND SUPPLY VOLTAGE

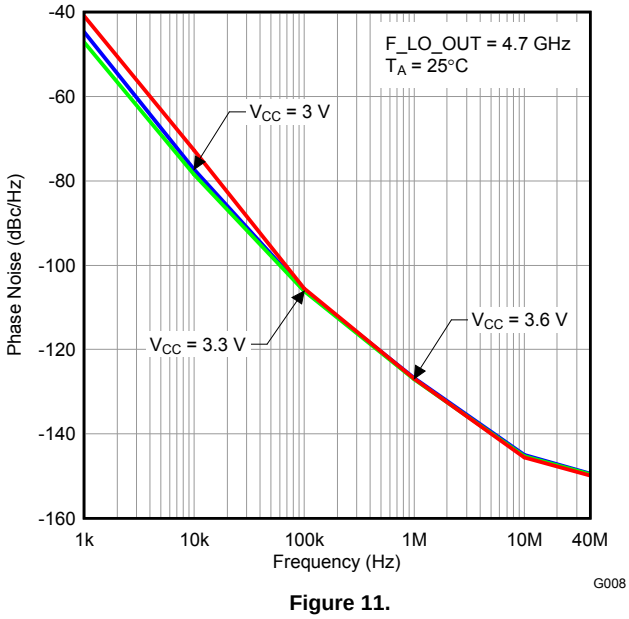

Figure 11.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

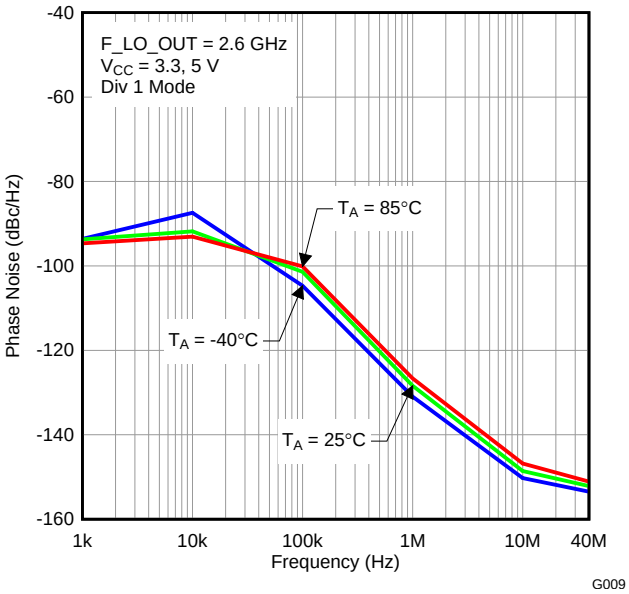

Figure 12.

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

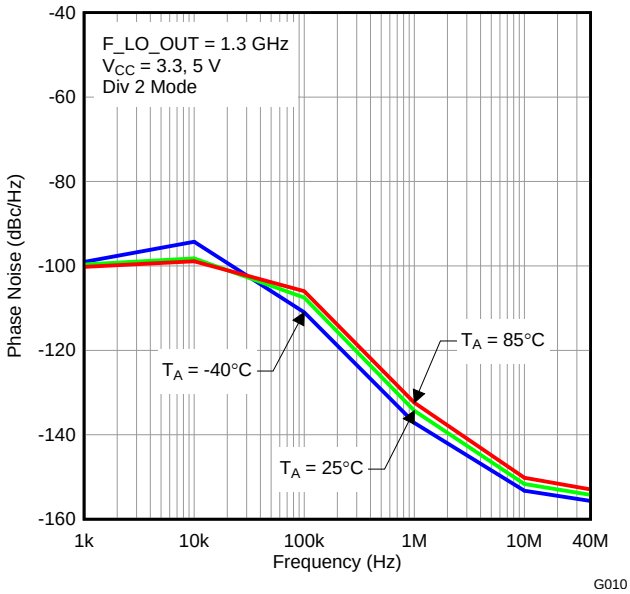

Figure 13.

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

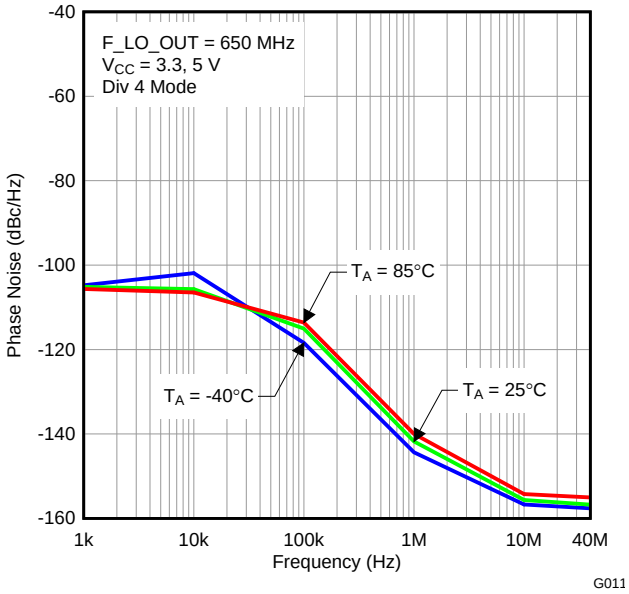

Figure 14.

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

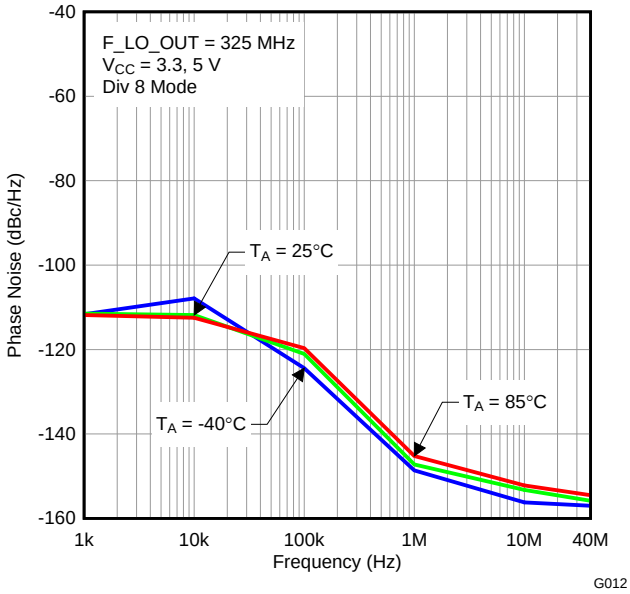

Figure 15.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

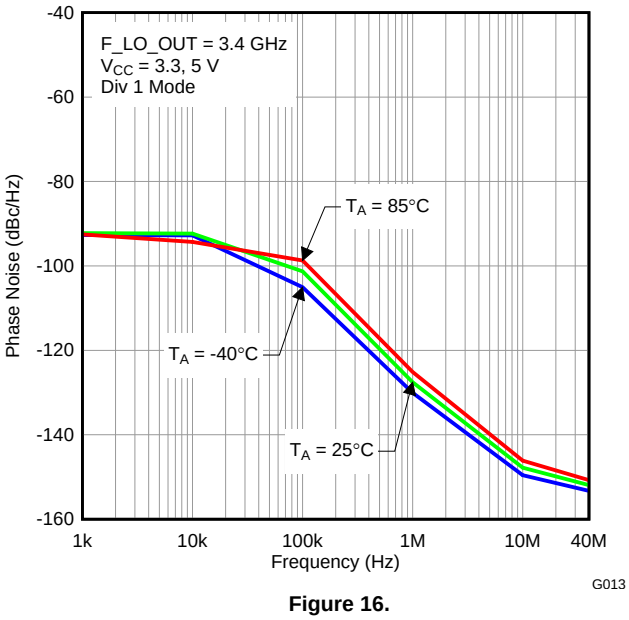

Figure 16.

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

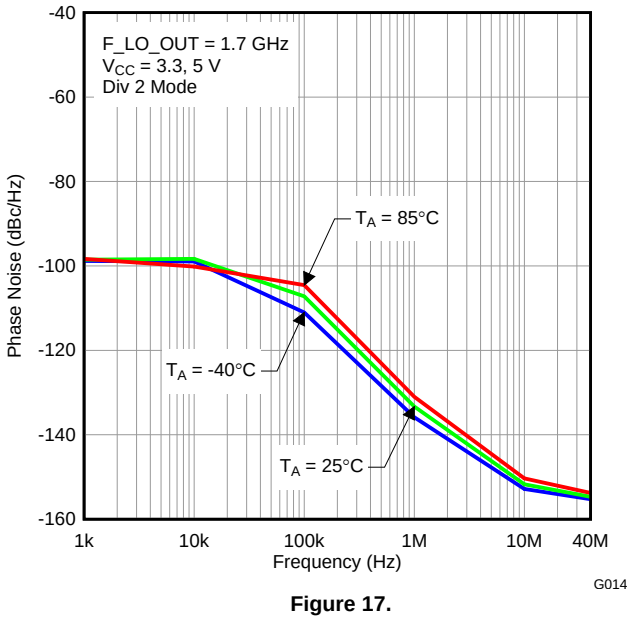

Figure 17.

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

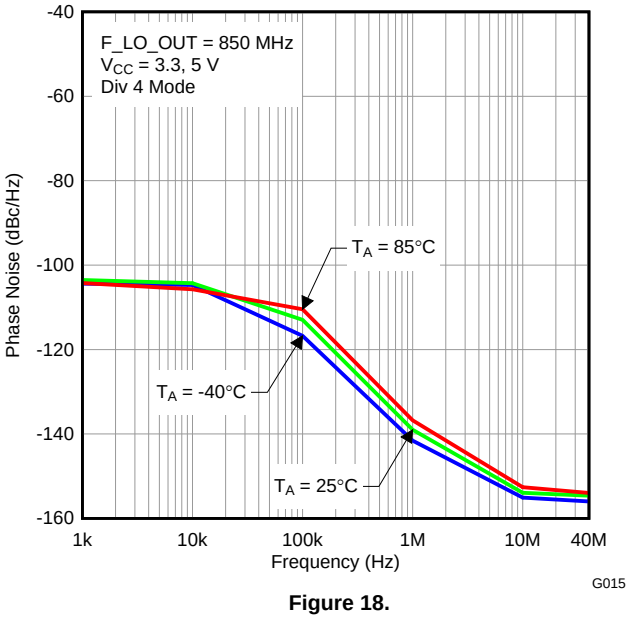

Figure 18.

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

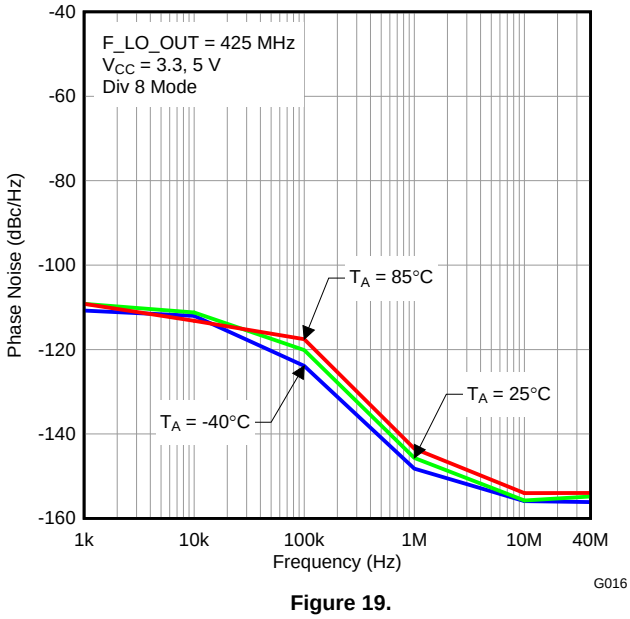

Figure 19.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

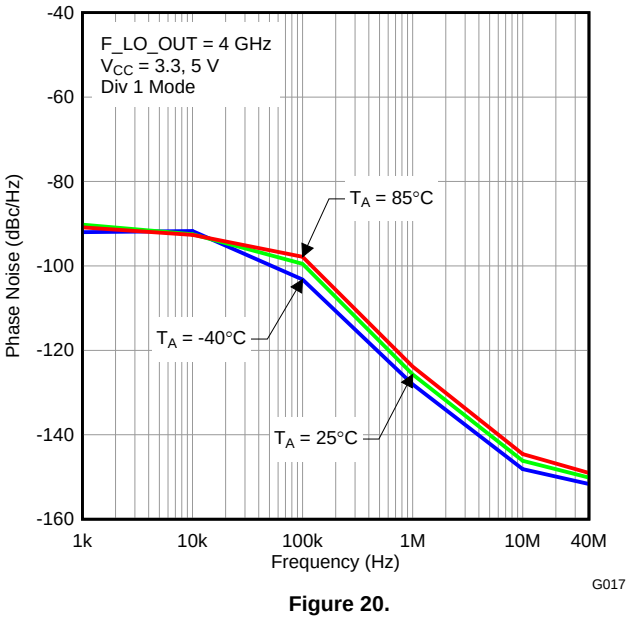

Figure 20.

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

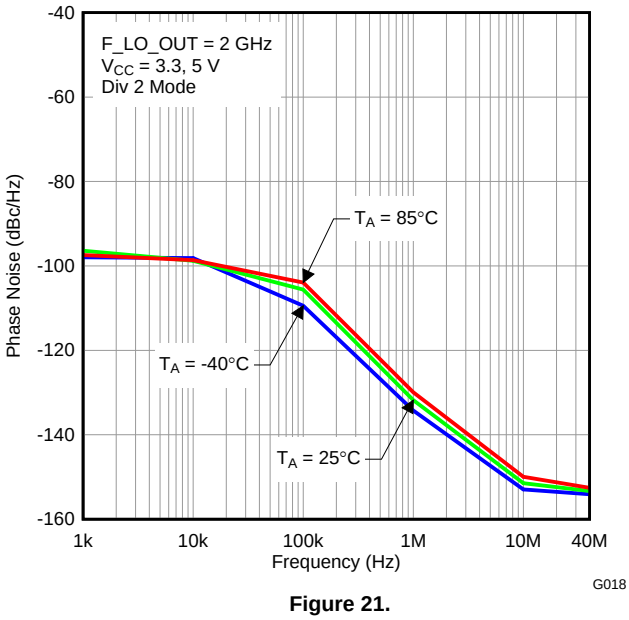

Figure 21.

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

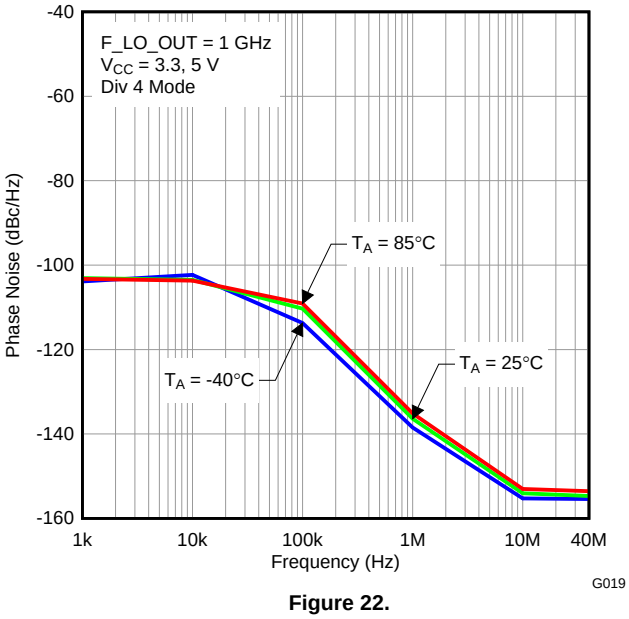

Figure 22.

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

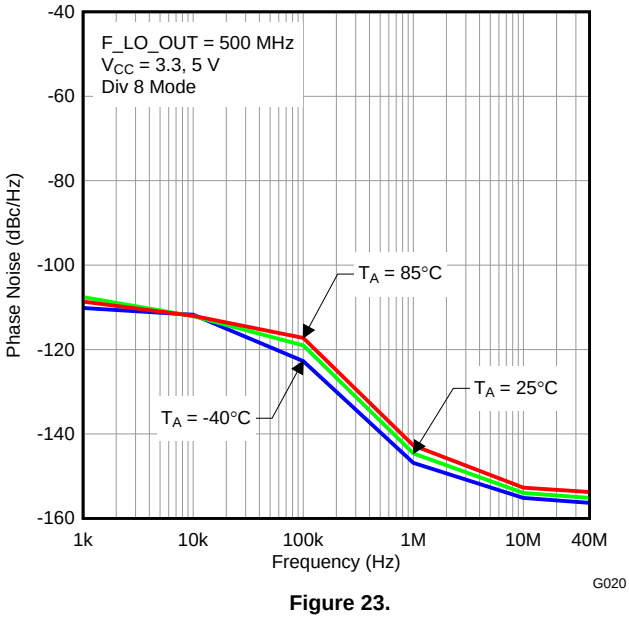

Figure 23.

TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

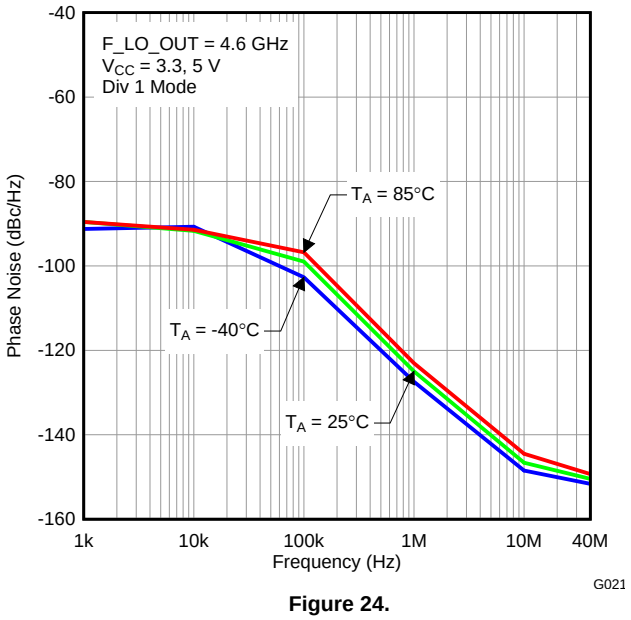

Figure 24.

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

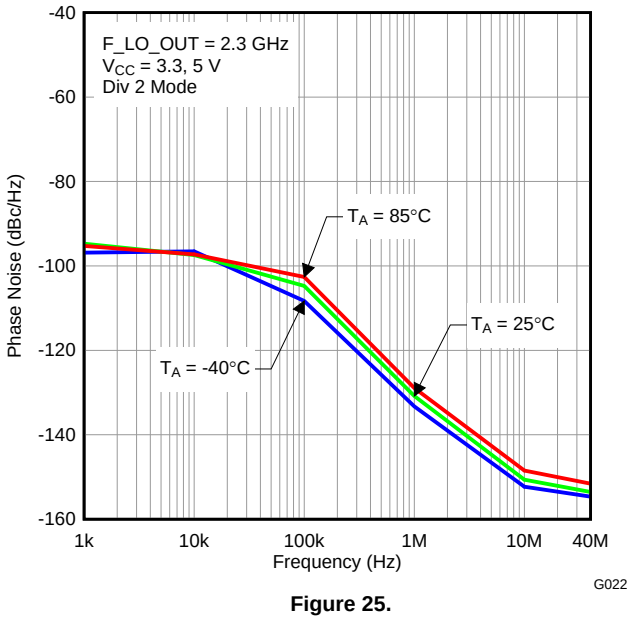

Figure 25.

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

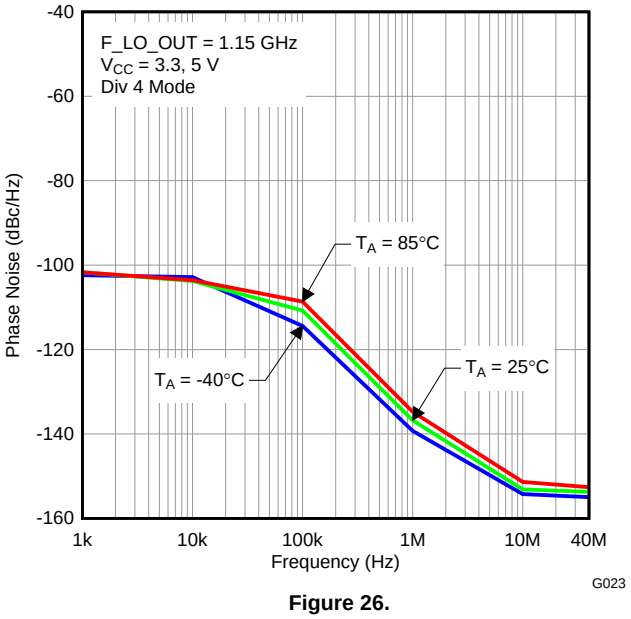

Figure 26.

CLOSED LOOP PHASE NOISE vs FREQUENCY AND TEMPERATURE

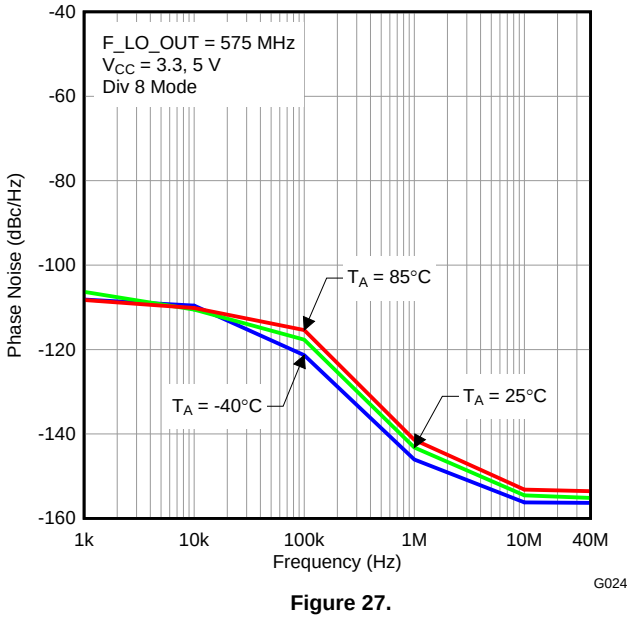

Figure 27.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

NOISE AT 13-MHz OFFSET vs FREQUENCY AND TEMPERATURE WITH INTERNAL VCO

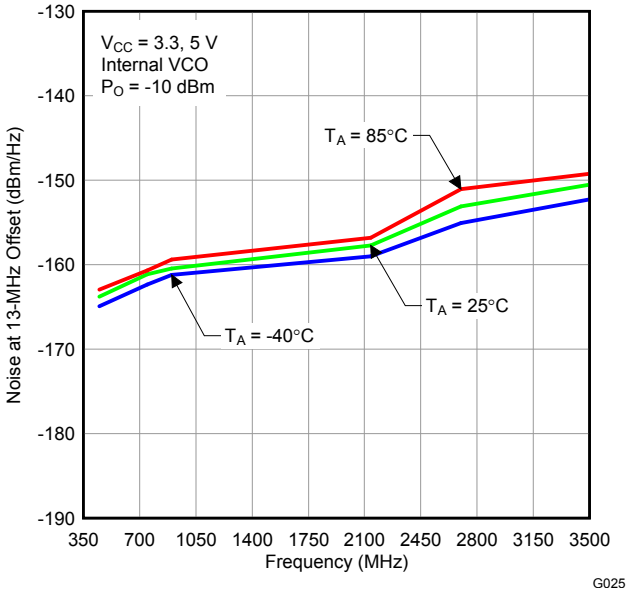

Figure 28.

NOISE AT 13-MHz OFFSET vs FREQUENCY AND SUPPLY VOLTAGE WITH INTERNAL VCO

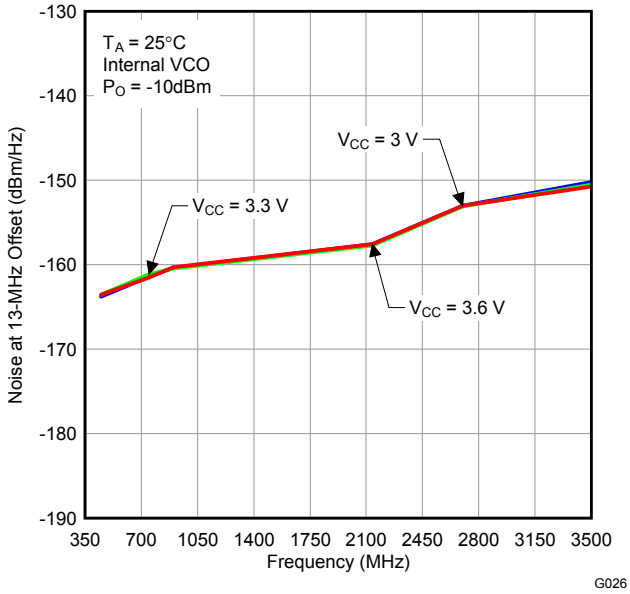

Figure 29.

NOISE AT 13-MHz OFFSET vs FREQUENCY AND TEMPERATURE WITH EXTERNAL VCO

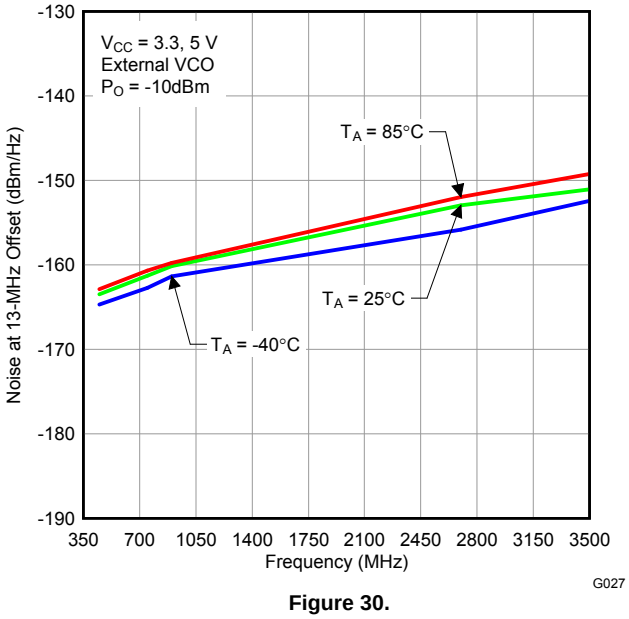

Figure 30.

NOISE AT 13-MHz OFFSET vs FREQUENCY AND SUPPLY VOLTAGE WITH EXTERNAL VCO

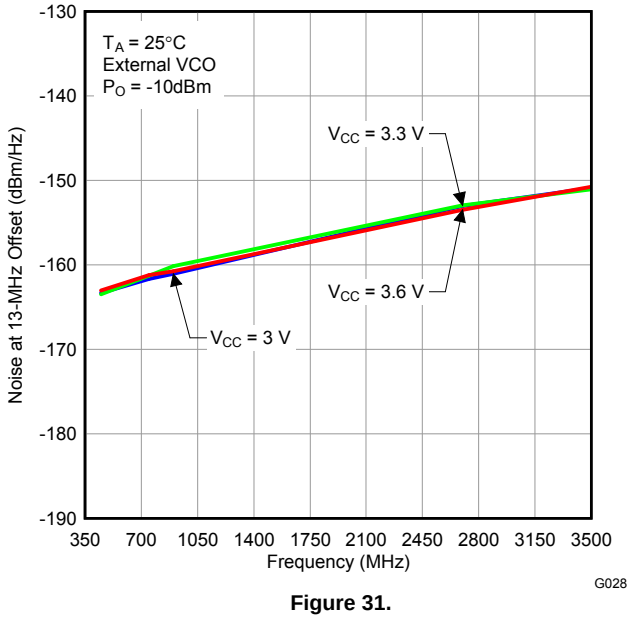

Figure 31.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

NOISE AT 13-MHz OFFSET vs OUTPUT POWER AND FREQUENCY

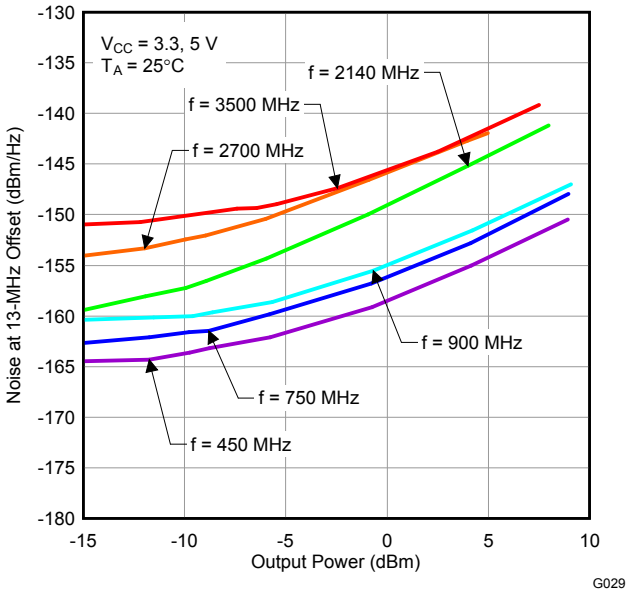

Figure 32.

VOLTAGE GAIN vs FREQUENCY AND TEMPERATURE

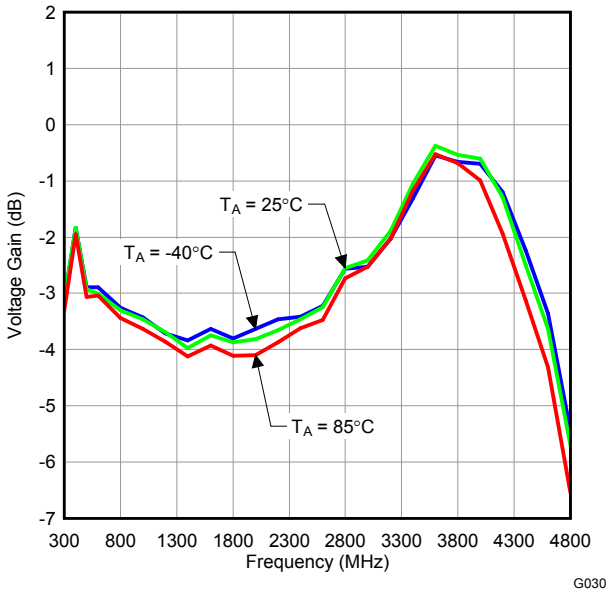

Figure 33.

VOLTAGE GAIN vs FREQUENCY AND TEMPERATURE at 750 MHz

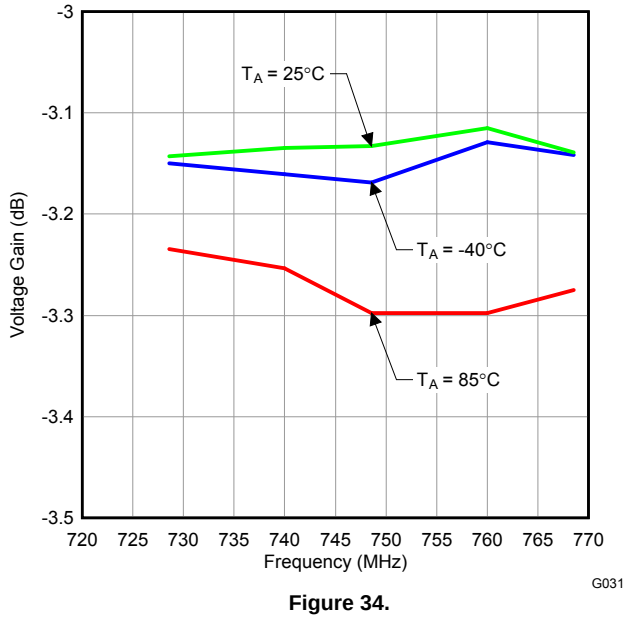

Figure 34.

VOLTAGE GAIN vs FREQUENCY AND TEMPERATURE at 900 MHz

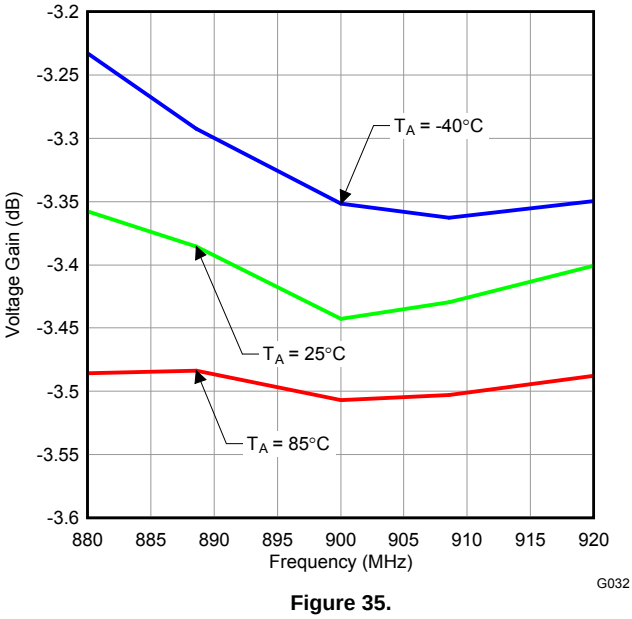

Figure 35.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

VOLTAGE GAIN vs FREQUENCY AND TEMPERATURE at 1500 MHz

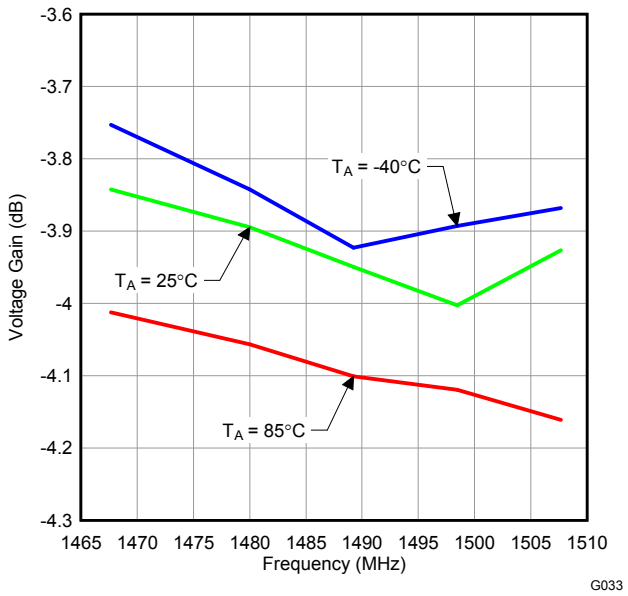

Figure 36.

VOLTAGE GAIN vs FREQUENCY AND TEMPERATURE at 2150 MHz

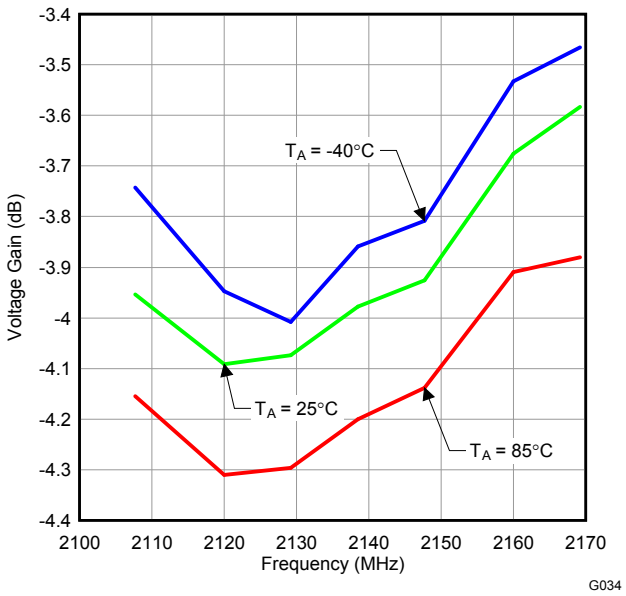

Figure 37.

VOLTAGE GAIN vs FREQUENCY AND TEMPERATURE at 2650 MHz

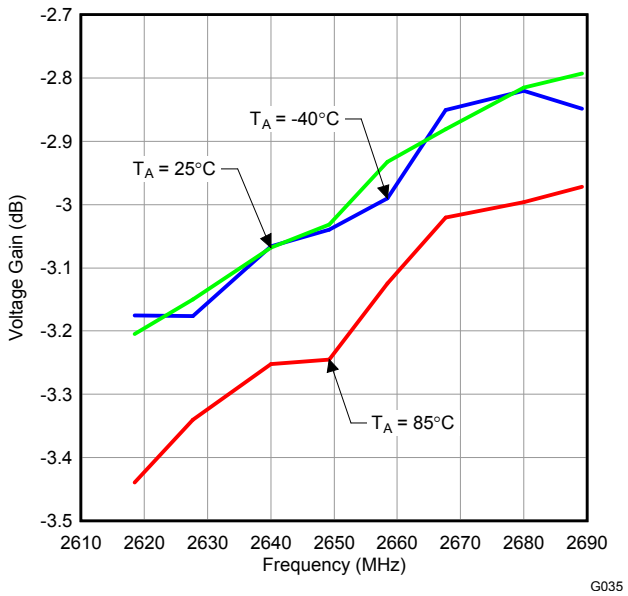

Figure 38.

VOLTAGE GAIN vs COMMON-MODE VOLTAGE AND FREQUENCY

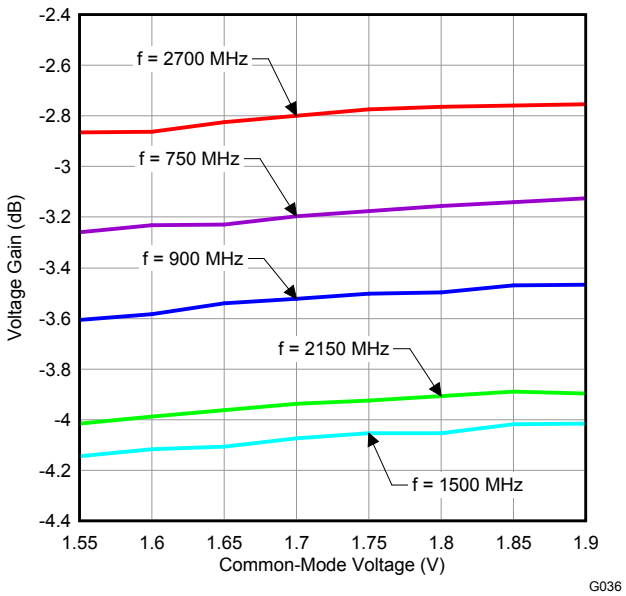

Figure 39.

TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

VOLTAGE GAIN vs BASEBAND VOLTAGE AMPLITUDE AND FREQUENCY

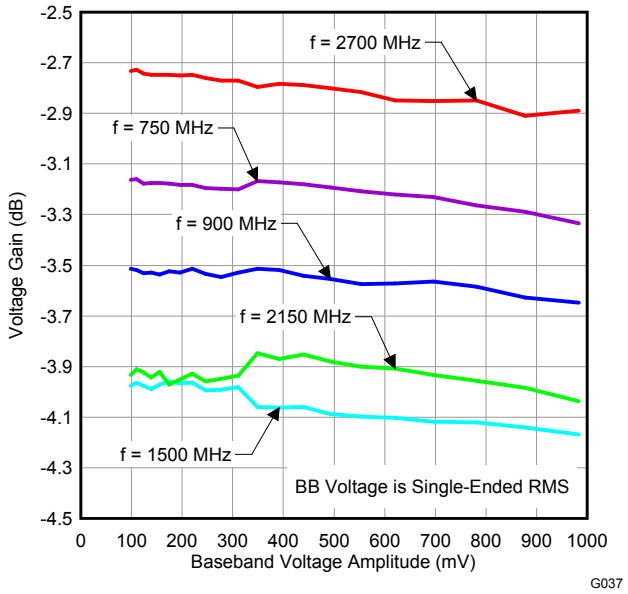

Figure 40.

VOLTAGE GAIN vs FREQUENCY AND SUPPLY VOLTAGE

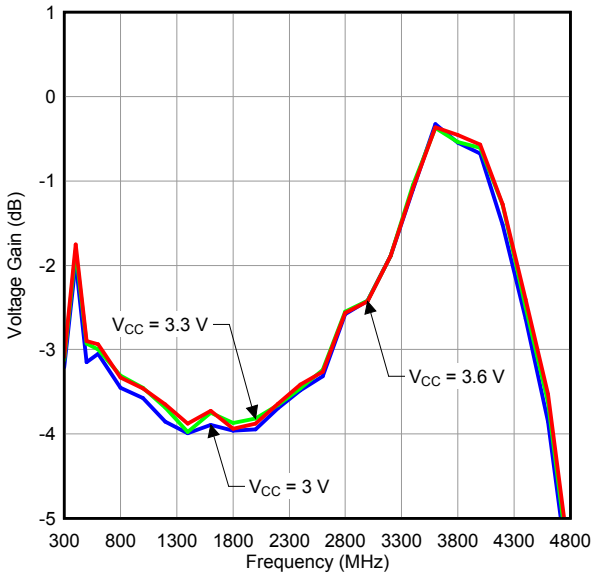

Figure 41.

P1dB vs FREQUENCY AND TEMPERATURE

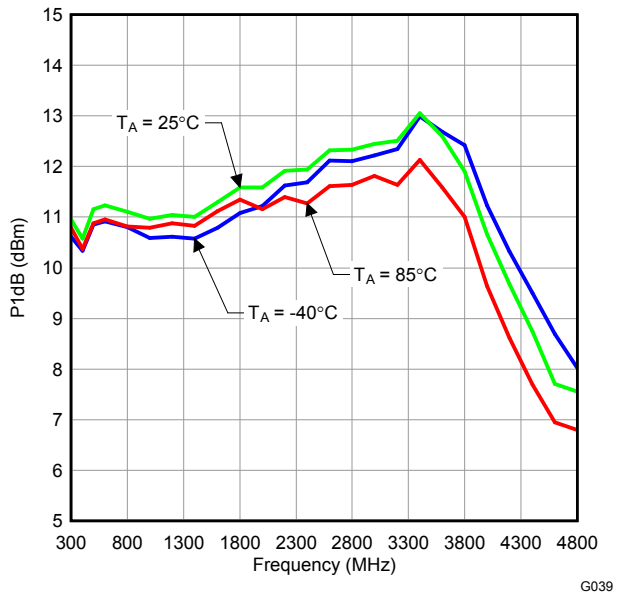

Figure 42.

P1dB vs FREQUENCY AND TEMPERATURE at 750 MHz

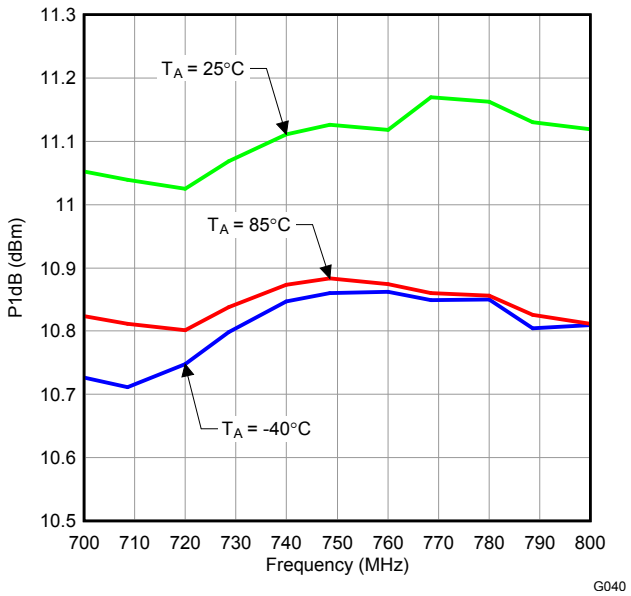

Figure 43.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

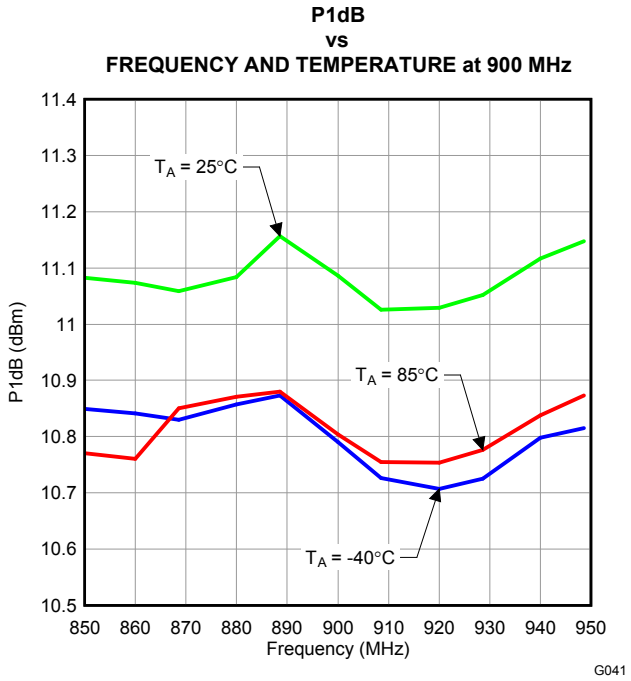

Figure 44.

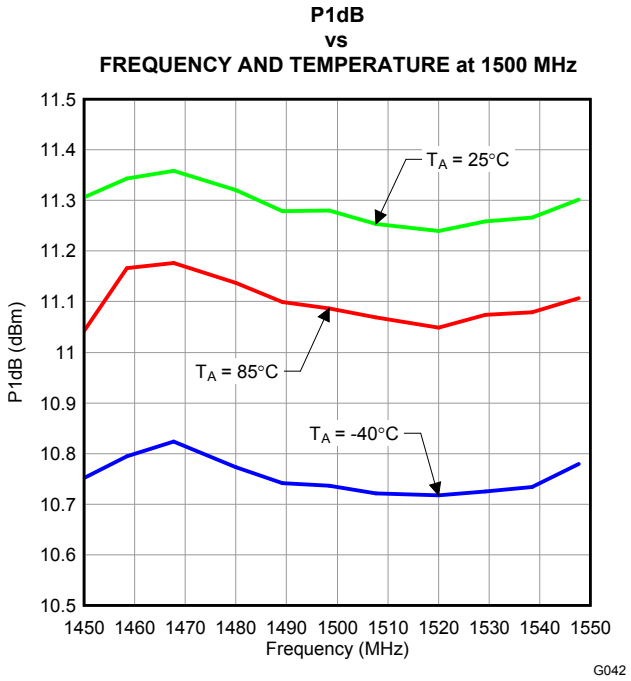

Figure 45.

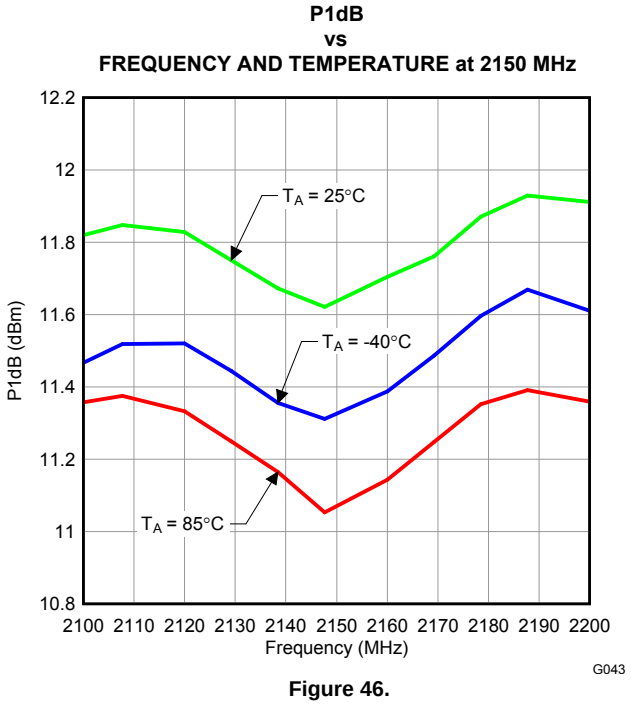

Figure 46.

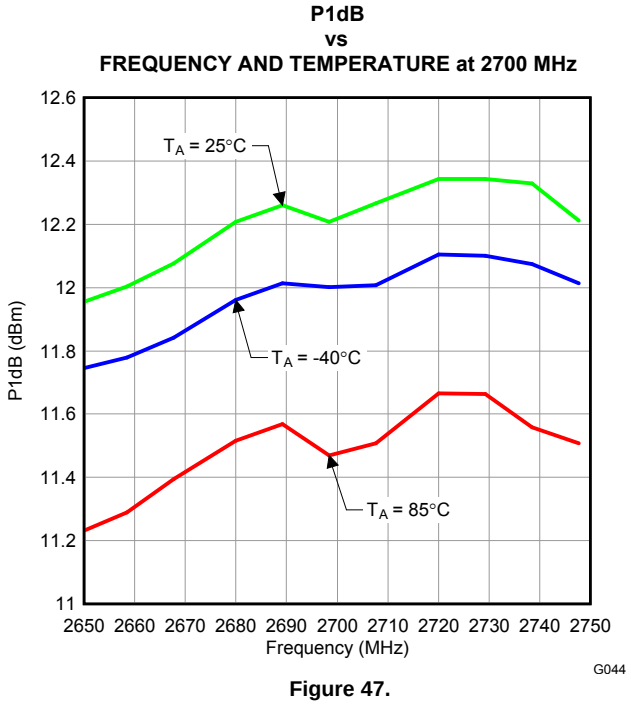

Figure 47.

TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

P1dB vs COMMON-MODE VOLTAGE AND FREQUENCY

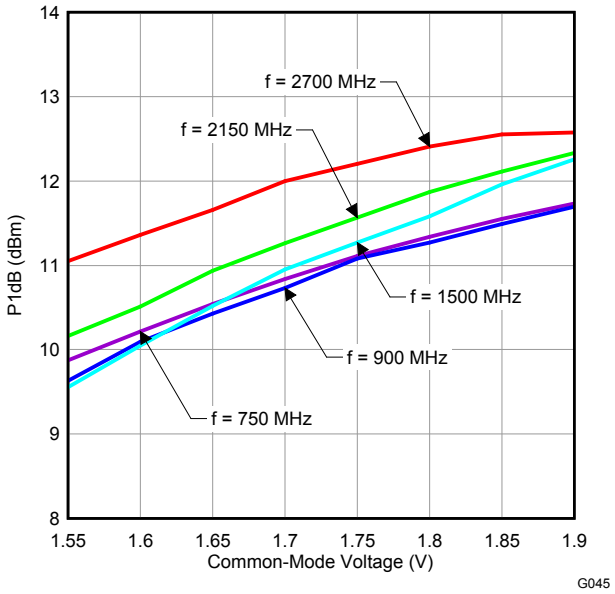

Figure 48.

P1dB vs FREQUENCY AND SUPPLY VOLTAGE

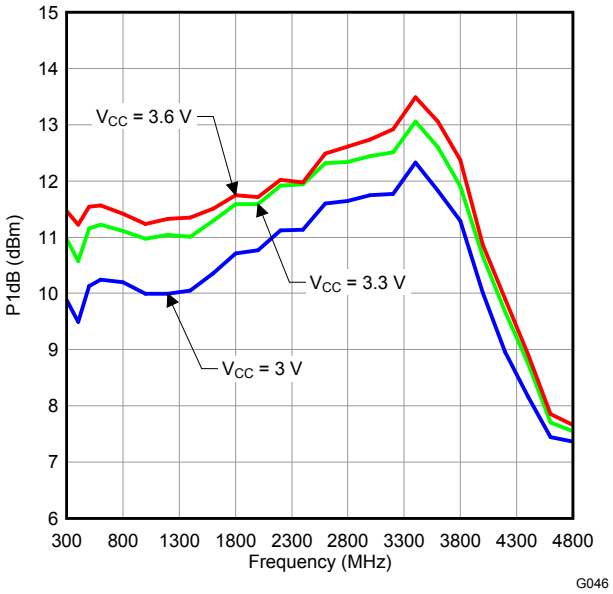

Figure 49.

OIP3 vs FREQUENCY AND TEMPERATURE

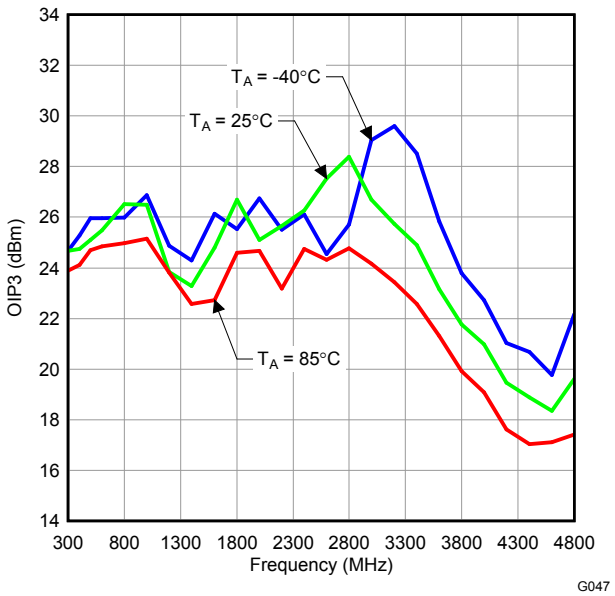

Figure 50.

OIP3 vs TEMPERATURE AND FREQUENCY at 900 MHz

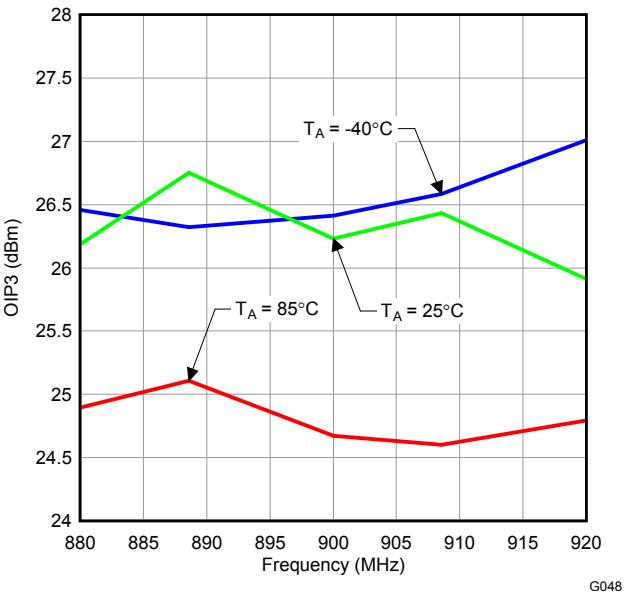

Figure 51.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

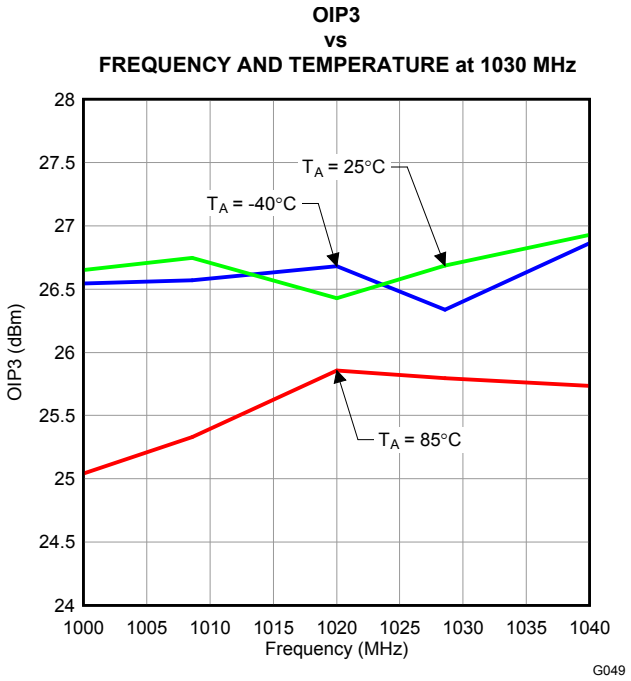

Figure 52.

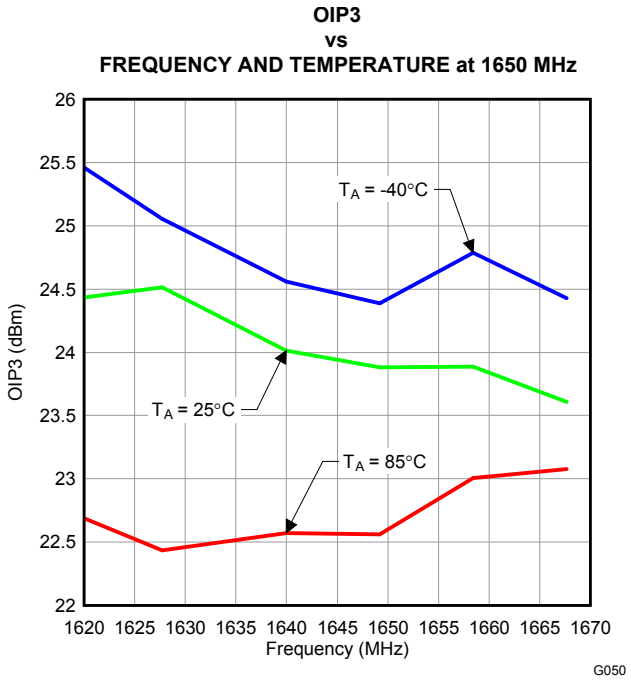

Figure 53.

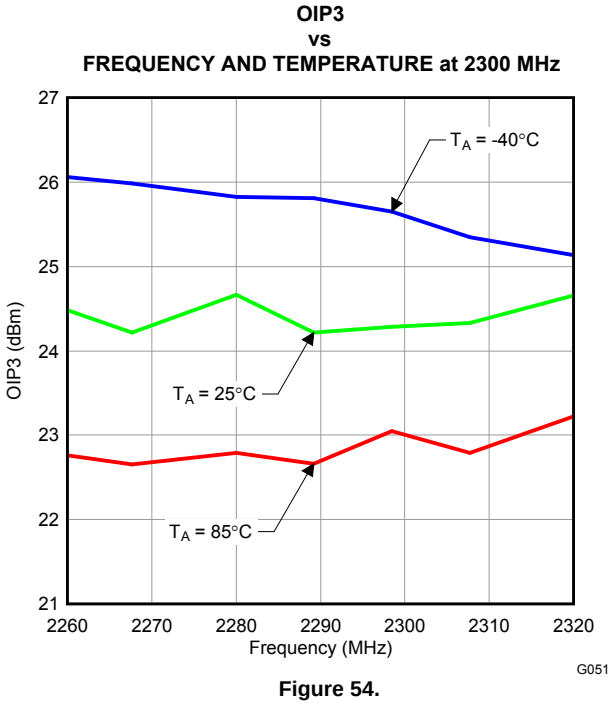

Figure 54.

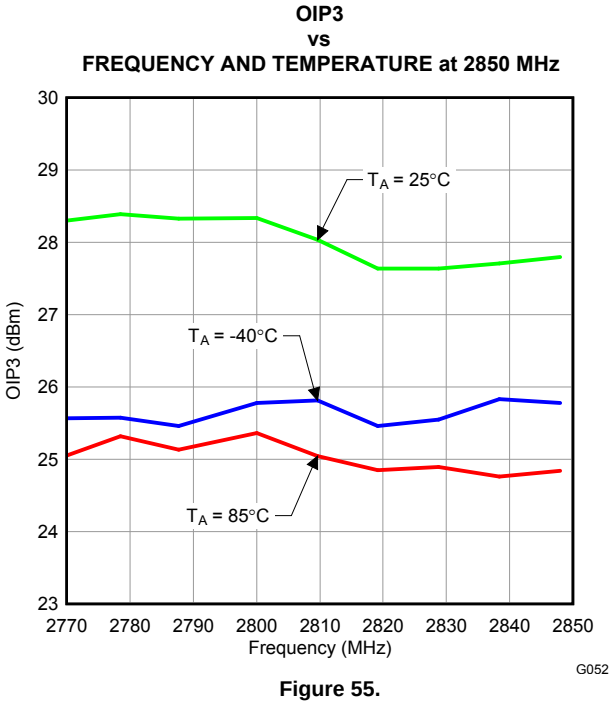

Figure 55.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

OIP3 vs COMMON-MODE VOLTAGE AND FREQUENCY

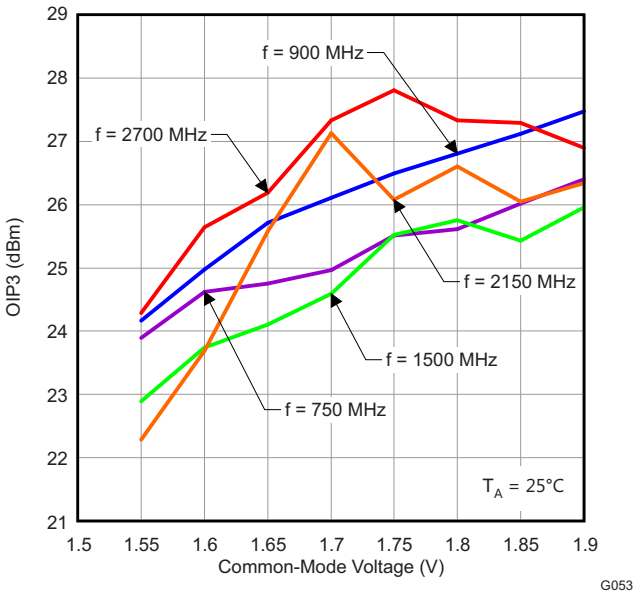

Figure 56.

OIP3 vs BASEBAND VOLTAGE AMPLITUDE AND FREQUENCY

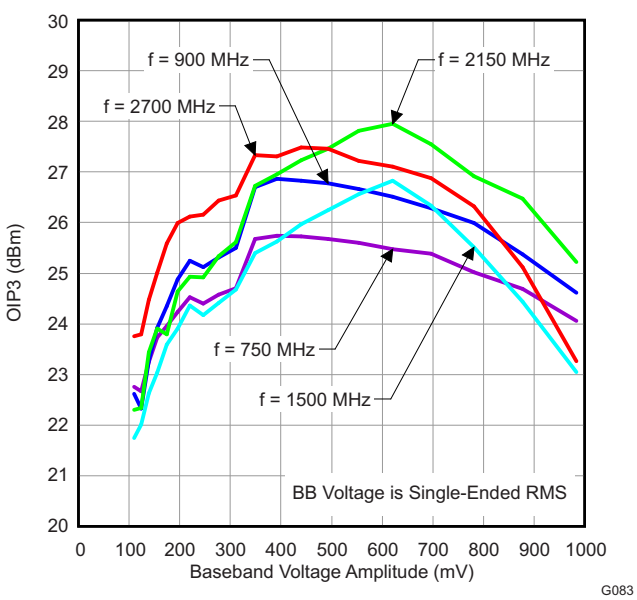

Figure 57.

OIP2 vs FREQUENCY AND TEMPERATURE

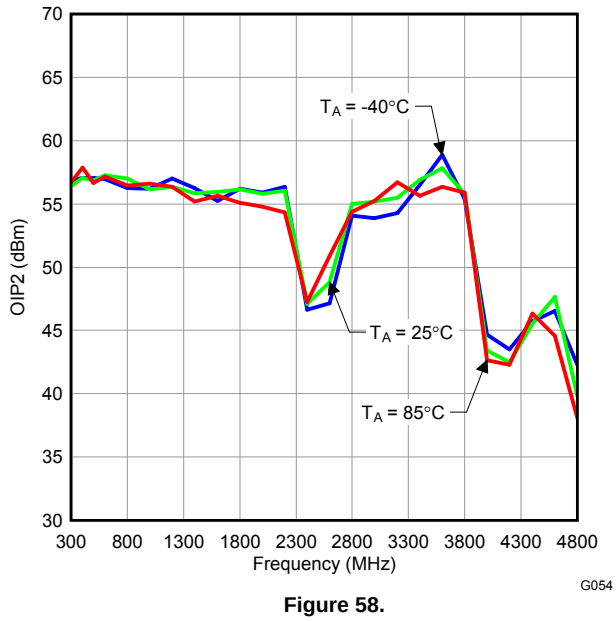

Figure 58.

OIP2 vs FREQUENCY AND TEMPERATURE at 750 MHz

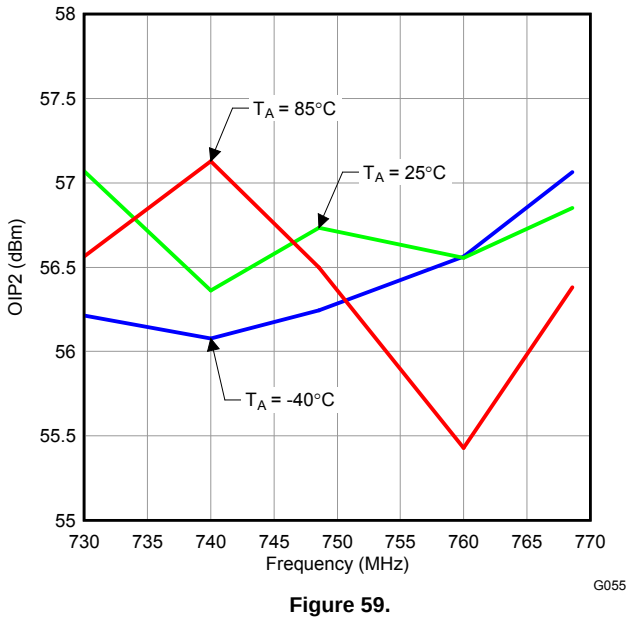

Figure 59.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

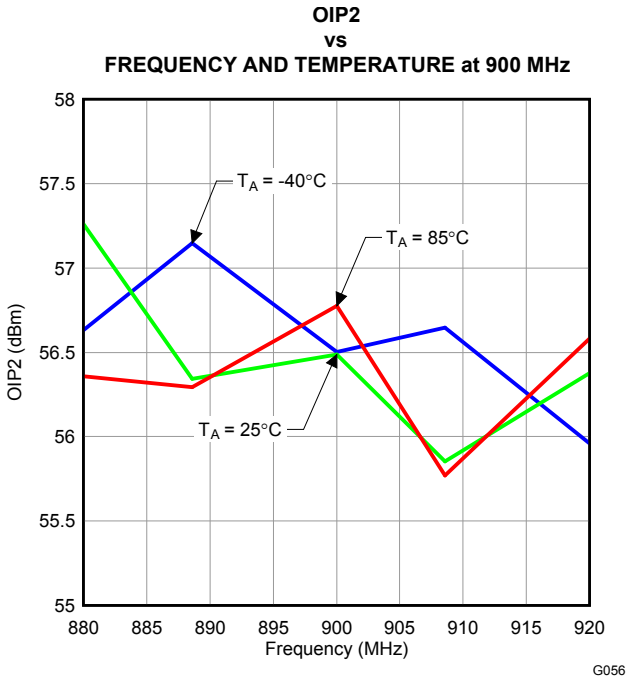

Figure 60.

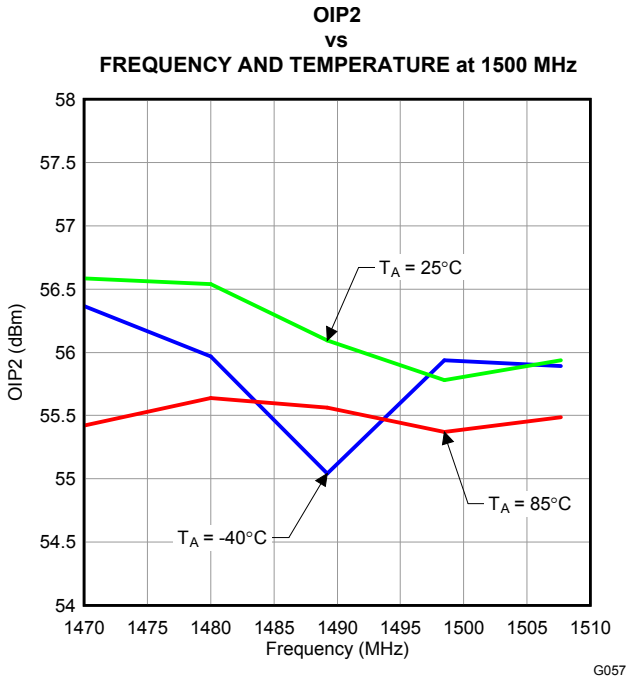

Figure 61.

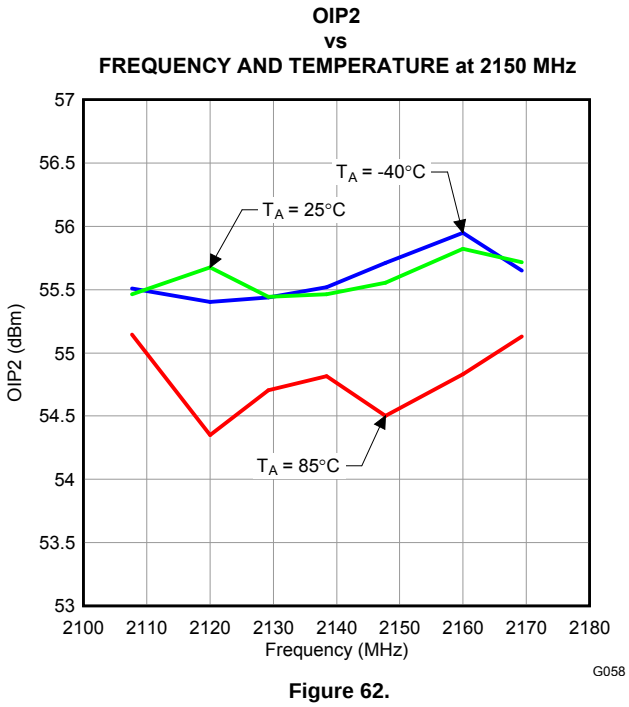

Figure 62.

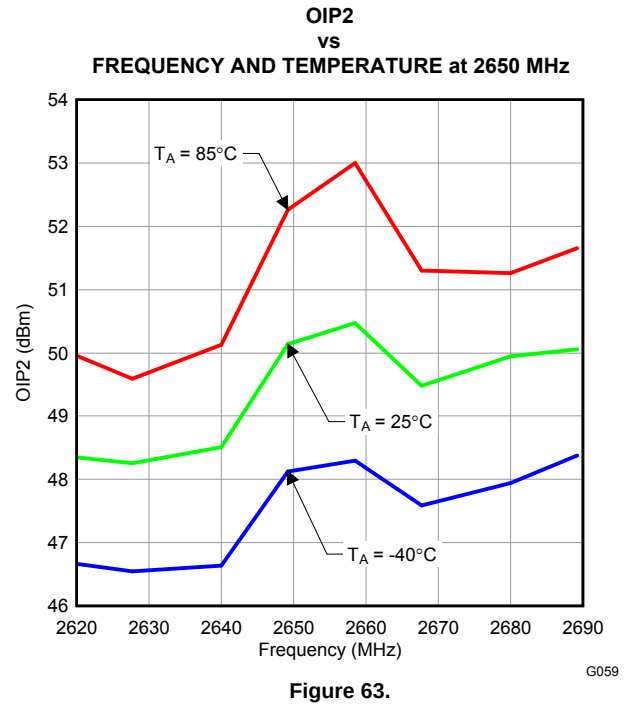

Figure 63.

TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

UNADJUSTED SIDEBAND SUPPRESSION vs FREQUENCY AND TEMPERATURE

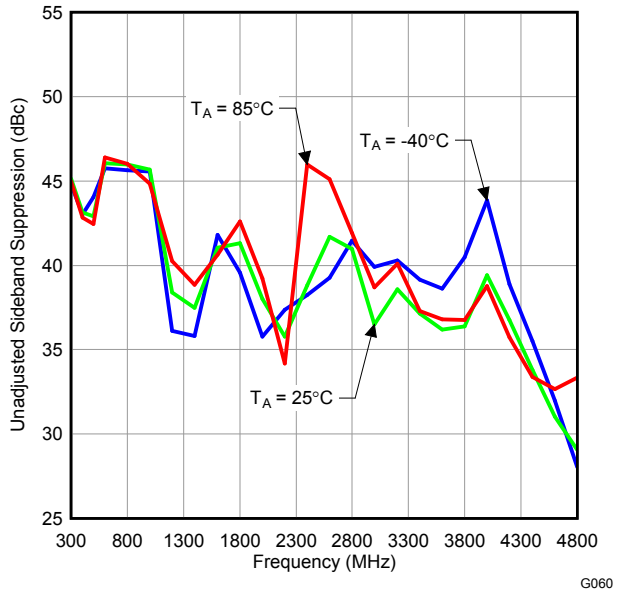

Figure 64.

UNADJUSTED SIDEBAND SUPPRESSION vs FRQUENCY AND TEMPERATURE at 900 MHz

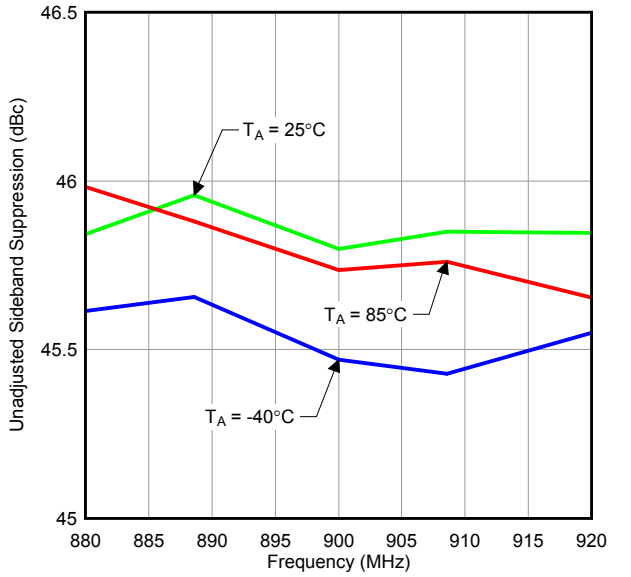

Figure 65.

UNADJUSTED SIDEBAND SUPPRESSION vs FREQUENCY AND TEMPERATURE at 1030 MHz

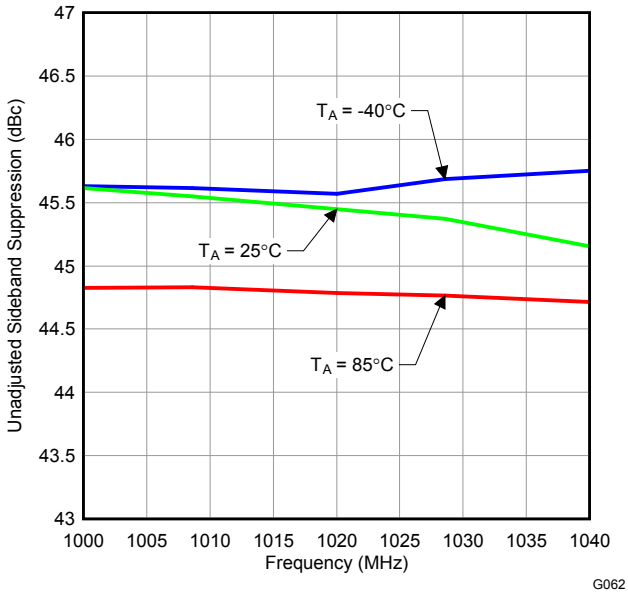

Figure 66.

UNADJUSTED SIDEBAND SUPPRESSION vs FREQUENCY AND TEMPERATURE at 1650 MHz

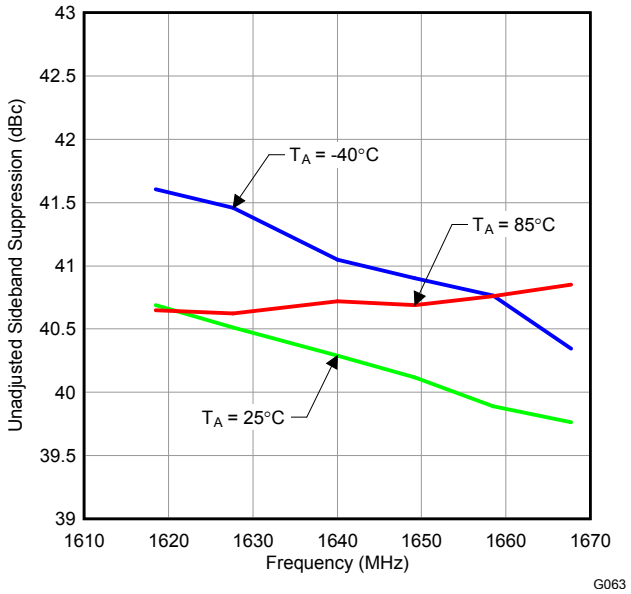

Figure 67.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

UNADJUSTED SIDEBAND SUPPRESSION vs FREQUENCY AND TEMPERATURE at 2300 MHz

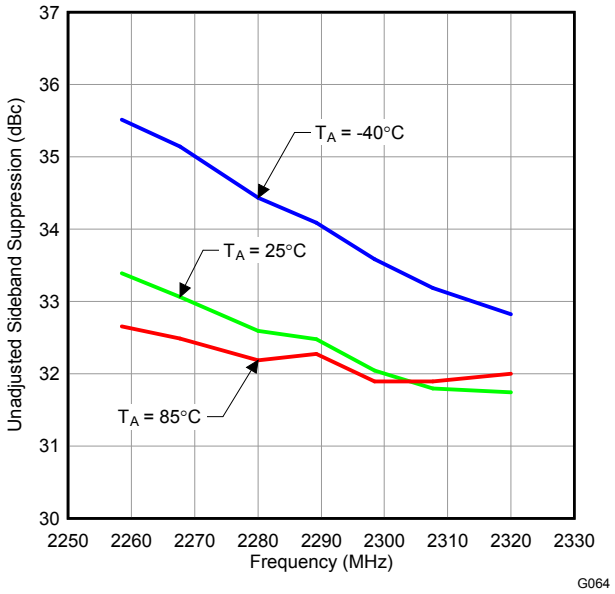

Figure 68.

UNADJUSTED SIDEBAND SUPPRESSION vs FREQUENCY AND TEMPERATURE at 2850 MHz

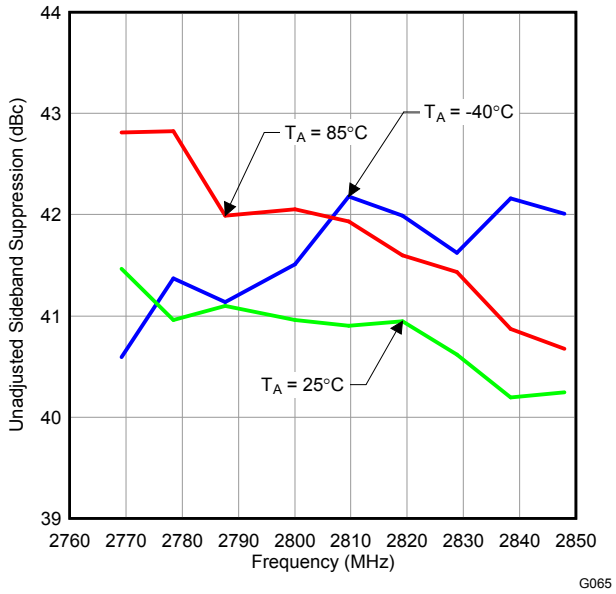

Figure 69.

UNADJUSTED SIDEBAND SUPPRESSION vs COMMON-MODE VOLTAGE AND FREQUENCY

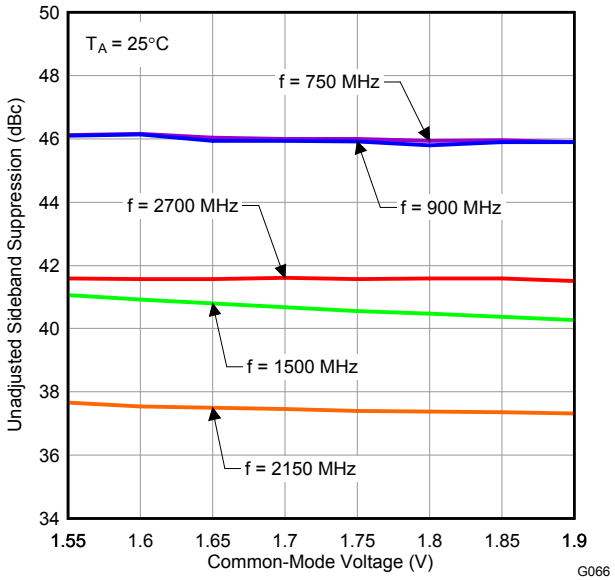

Figure 70.

UNADJUSTED CARRIER SUPPRESSION vs FRQUENCY AND TEMPERATURE

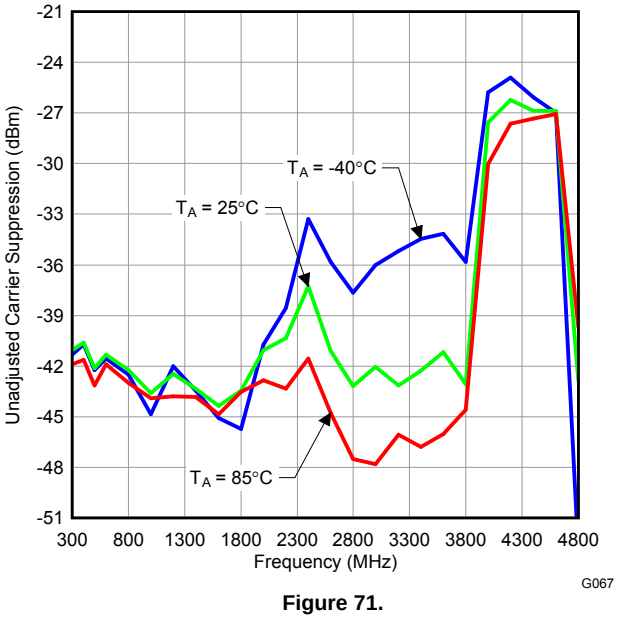

Figure 71.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

UNADJUSTED CARRIER SUPPRESSION vs FREQUENCY AND TEMPERATURE at 900 MHz

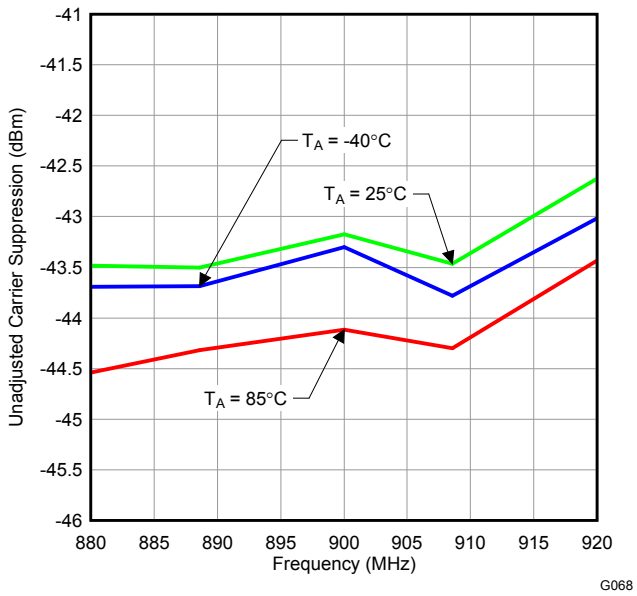

Figure 72.

UNADJUSTED CARRIER SUPPRESSION vs FRQUENCY AND TEMPERATURE at 1030 MHz

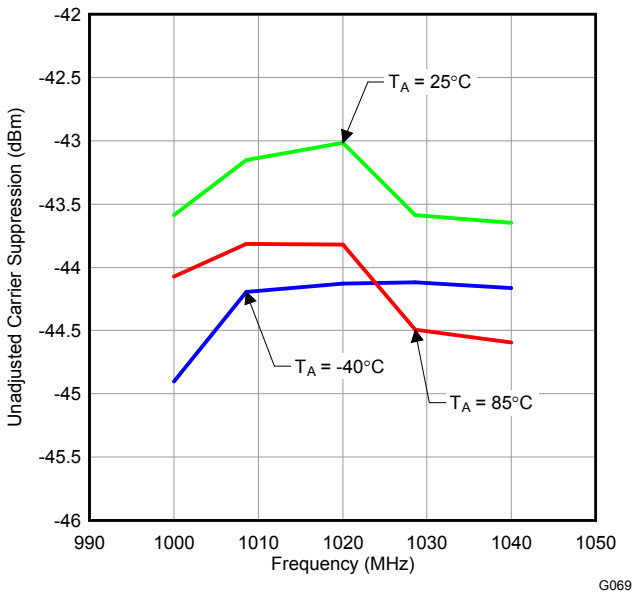

Figure 73.

UNADJUSTED CARRIER SUPPRESSION vs FREQUENCY AND TEMPERATURE at 1650 MHz

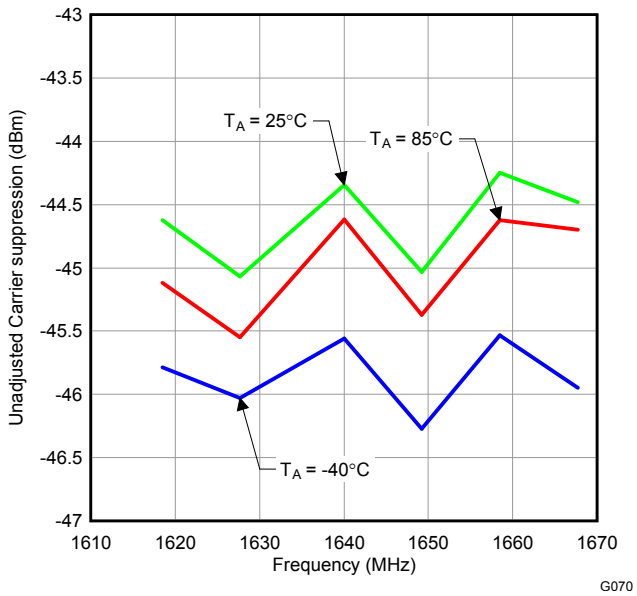

Figure 74.

UNADJUSTED CARRIER SUPPRESSION vs FREQUENCY AND TEMPERATURE at 2300 MHz

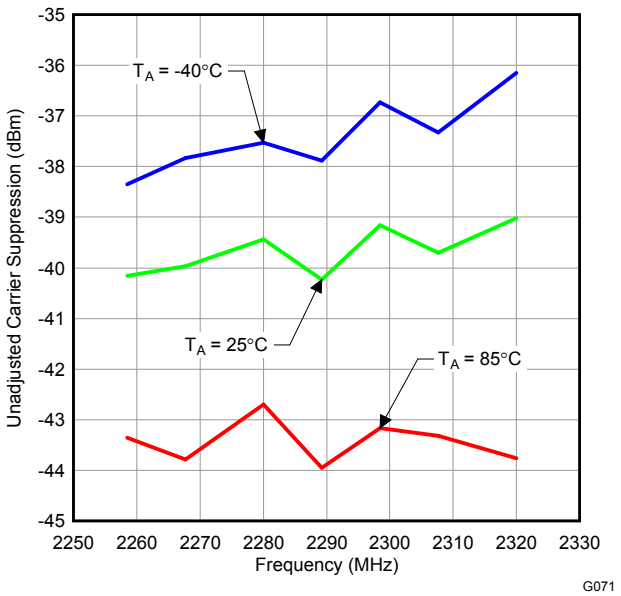

Figure 75.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

UNADJUSTED CARRIER SUPPRESSION vs FREQUENCY AND TEMPERATURE at 2850 MHz

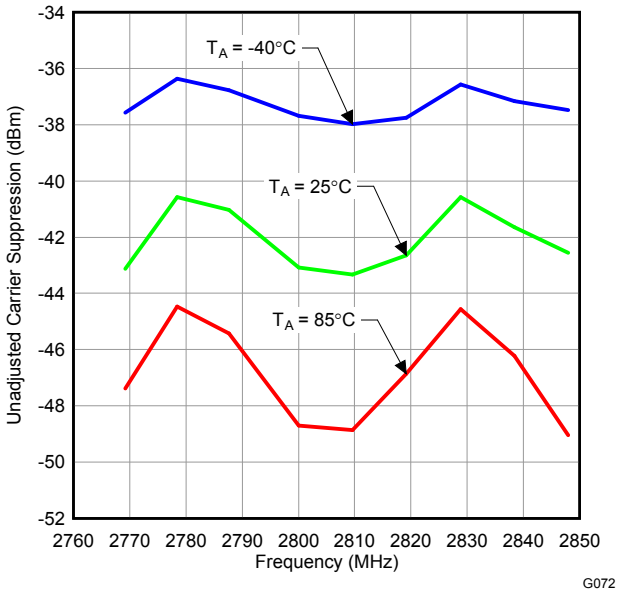

Figure 76.

UNADJUSTED CARRIER SUPPRESSION vs COMMON- MODE VOLTAGE AND FREQUENCY

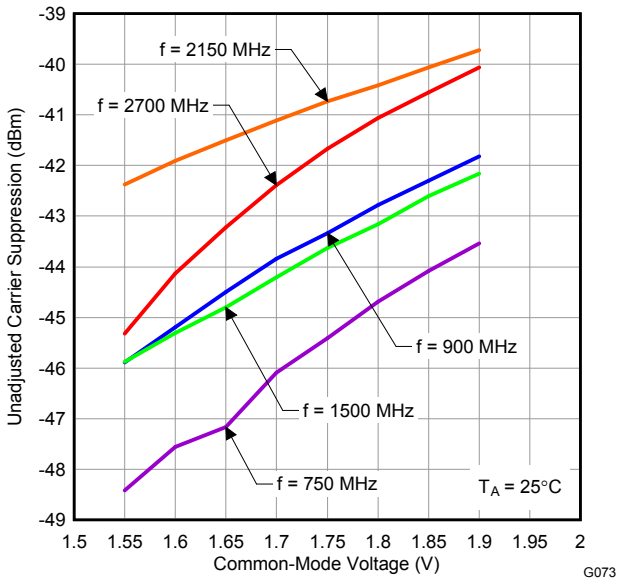

Figure 77.

COMMON-MODE VOLTAGE vs VREF_SEL SETTING AND TEMPERATURE

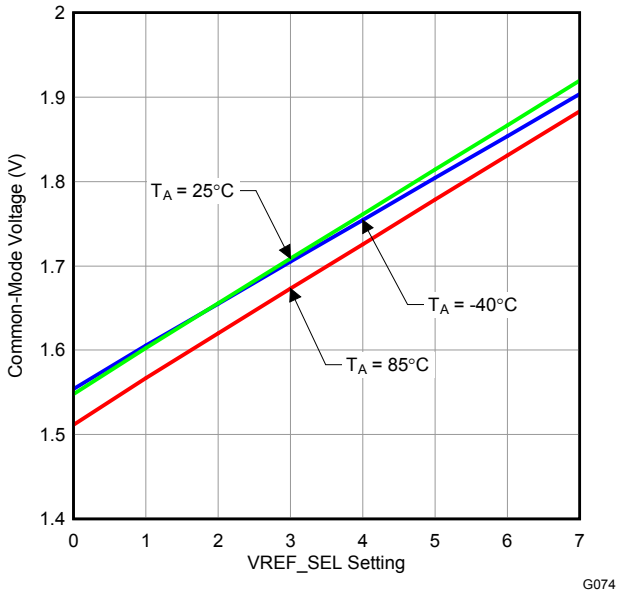

Figure 78.

BASEBAND VOLTAGE OFFSET vs IOFF SETTING AND TEMPERATURE

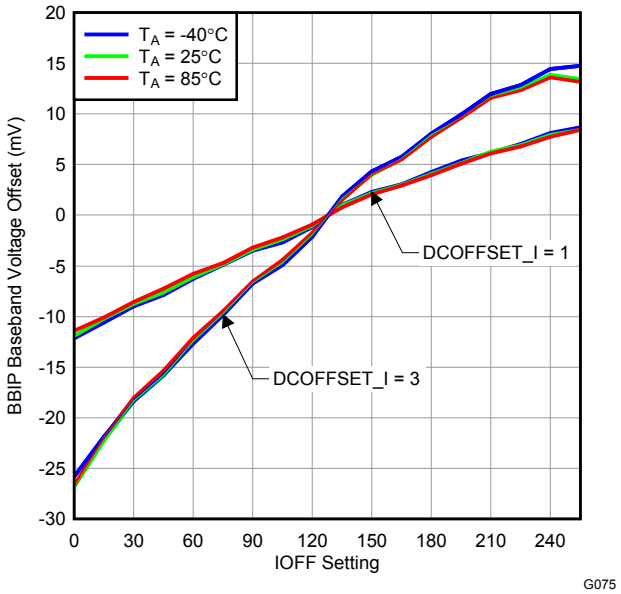

Figure 79.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

GAIN at 2300 MHz DISTRIBUTION

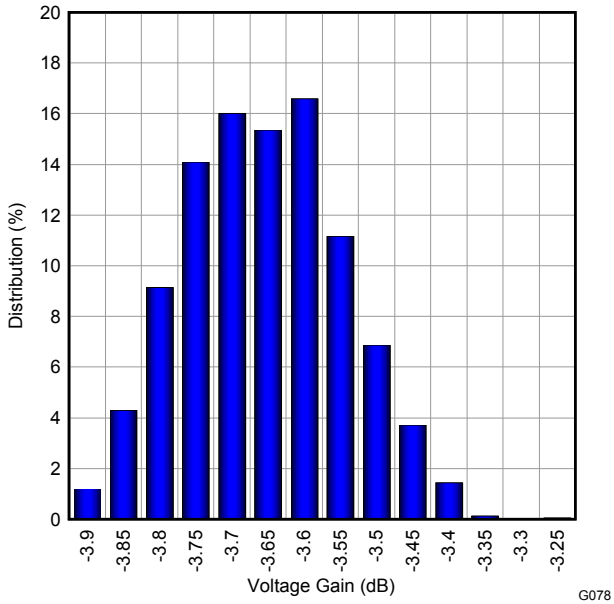

Figure 80.

P1dB at 2300 MHz DISTRIBUTION

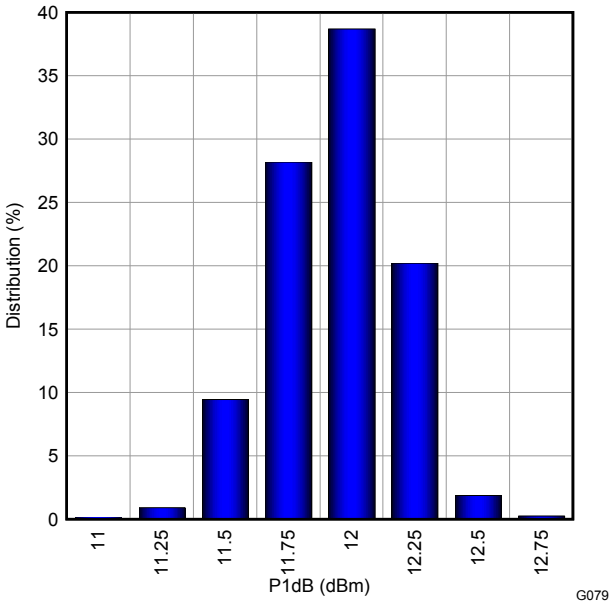

Figure 81.

OIP3 at 2300 MHz DISTRIBUTION

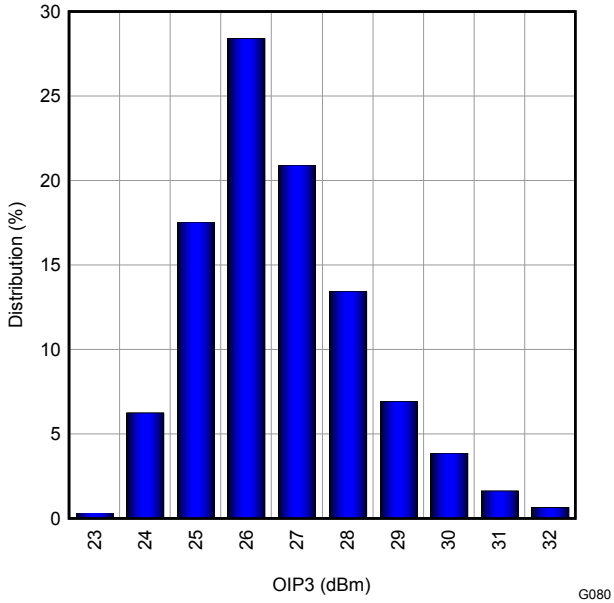

Figure 82.

UNADJUSTED CARRIER SUPPRESSION at 2300 MHz DISTRIBUTION

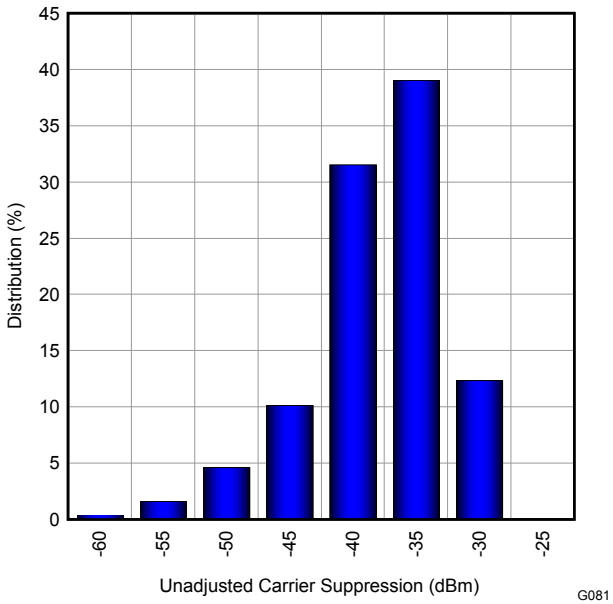

Figure 83.

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TYPICAL CHARACTERISTICS (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, TA = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

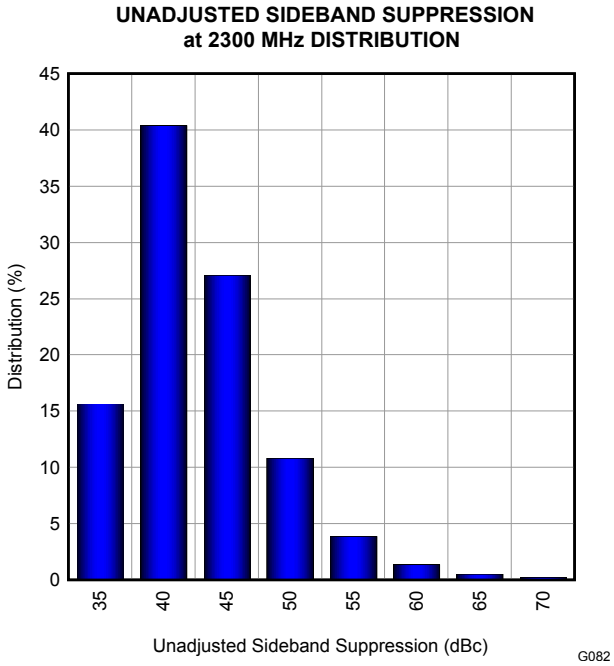

Figure 84.

SERIAL INTERFACE PROGRAMMING REGISTERS DEFINITION

The TRF372017 features a 3-wire serial programming interface (SPI) that controls an internal 32-bit shift register. There are a total of 3 signals that need to be applied: the clock (CLK, pin 47), the serial data (DATA, pin 46) and the latch enable (LE, pin 45). The TRF372017 has an additional pin (RDBK, pin 2) for read-back functionality. This pin is a digital pin and can be used to read-back values of different internal registers.

The DATA (DB0-DB31) is loaded LSB first and is read on the rising edge of the CLOCK. The LE is asynchronous to the CLOCK and at its rising edge the data in the shift register gets loaded onto the selected internal register. The 5 LSB of the Data field are the address bits to select the available internal registers.

PLL SPI REGISTERS

Register 1

Register address					Reference Clock Divider									
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

….		RSV	REF INV	VCO NEG	Charge Pump Current					CP DOUBLE	VCO Cal CLK div/Mult				RSV
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

Register 1	Name	Reset Value	Description
Bit0	ADDR_0	1	Register address bits
Bit1	ADDR_1	0	
Bit2	ADDR_2	0	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	RDIV_0	1	13-bit Reference Divider value (minimum value Rmin= 1, B[17..5] = [00 0000 0000 001]; maximum value Rmax=8191, B[17..5] = [11 1111 1111 111];
Bit6	RDIV_1	0	
Bit7	RDIV_2	0	
Bit8	RDIV_3	0	
Bit9	RDIV_4	0	
Bit10	RDIV_5	0	
Bit11	RDIV_6	0	
Bit12	RDIV_7	0	
Bit13	RDIV_8	0	
Bit14	RDIV_9	0	
Bit15	RDIV_10	0	
Bit16	RDIV_11	0	
Bit17	RDIV_12	0	
Bit18	RSV	0	
Bit19	REF_INV	0	Invert Reference Clock polarity; 1 = use falling edge
Bit20	NEG_VCO	1	VCO polarity control; 1= negative slope (negative K_V)
Bit21	ICP_0	0	Program Charge Pump dc current, ICP 1.94mA, B[25..21] = [00 000] 0.47mA, B[25..21] = [11 111] 0.97mA, default value, , B[25..21] = [01 010]
Bit22	ICP_1	1	
Bit23	ICP_2	0	
Bit24	ICP_3	1	
Bit25	ICP_4	0	
Bit26	ICPDOUBLE	0	1 = set ICP to double the current
Bit27	CAL_CLK_SEL_0	0	Multiplication or division factor to create VCO calibration clock from PFD frequency
Bit28	CAL_CLK _SEL_1	0	
Bit29	CAL_CLK _SEL_2	0	
Bit30	CAL_CLK _SEL_3	1	
Bit31	RSV	0	

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CAL_CLK_SEL[3..0]: Set the frequency divider value used to derive the VCO calibration clock from the phase detector frequency

CAL_CLK_SEL	Scaling Factor
1111	1/128
1110	1/64
1101	1/32
1100	1/16
1011	1/8
1010	1/4
1001	½
1000	1
0110	2
0101	4
0100	8
0011	16
0010	32
0001	64
0000	128

ICP[4..0]: Set the charge pump current

ICP[4..0]	Current (mA)
00 000	1.94
00 001	1.76
00 010	1.62
00 011	1.49
00 100	1.38
00 101	1.29
00 110	1.21
00 111	1.14
01 000	1.08
01 001	1.02
01 010	0.97
01 011	0.92
01 100	0.88
01 101	0.84
01 110	0.81
01 111	0.78
10 000	0.75
10 001	0.72
10 010	0.69
10 011	0.67
10 100	0.65
10 101	0.63
10 110	0.61
10 111	0.59
11 000	0.57
11 001	0.55
11 010	0.54
11 011	0.52

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ICP[4..0]	Current (mA)
11 100	0.51
11 101	0.5
11 110	0.48
11 111	0.47

Register 2

Register address					N-divider value										
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

...					PLL divider setting		Prescaler Select	RSV	RSV	VCO select		FCO sel mode	Cal accuracy		CAL
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

Register 2	Name	Reset Value	Description
Bit0	ADDR_0	0	Register address bits
Bit1	ADDR_1	1	
Bit2	ADDR_2	0	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	NINT_0	0	PLL N-divider division setting
Bit6	NINT_1	0	
Bit7	NINT_2	0	
Bit8	NINT_3	0	
Bit9	NINT_4	0	
Bit10	NINT_5	0	
Bit11	NINT_6	0	
Bit12	NINT_7	1	
Bit13	NINT_8	0	
Bit14	NINT_9	0	
Bit15	NINT_10	0	
Bit16	NINT_11	0	
Bit17	NINT_12	0	
Bit18	NINT_13	0	
Bit19	NINT_14	0	
Bit20	NINT_15	0	
Bit21	PLL_DIV_SEL0	1	Select division ratio of divider in front of prescaler
Bit22	PLL_DIV_SEL1	0	
Bit23	PRSC_SEL	1	Set prescaler modulus (0 → 4/5; 1 → 8/9)
Bit24	RSV	0	
Bit25	RSV	0	
Bit26	VCO_SEL_0	0	Selects between the four integrated VCO's 00 = lowest frequency VCO; 11 = highest frequency VCO
Bit27	VCO_SEL_1	1	
Bit28	VCOSEL_MODE	0	Single VCO auto-calibration mode (1 = active)
Bit29	CAL_ACC_0	0	Error count during the cap array calibration Recommended programming [00]
Bit30	CAL_ACC_1	0	
Bit31	EN_CAL	0	Execute a VCO frequency auto-calibration. Set to 1 to initiate a calibration. Resets automatically.

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PLL_DIV<1,0>: Select division ratio of divider in front of prescaler

PLL DIV	Frequency Divider
00	1
01	2
10	4

VCOSEL_MODE<0>: when it is 1, the cap array calibration is run on the VCO selected through bits VCO_SEL<2,1>

Register 3

Register address					Fractional N-divider value…										
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15
...														RSV	RSV
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

Register 3	Name	Reset Value	Description
Bit0	ADDR_0	1	Register address bits
Bit1	ADDR_1	1	
Bit2	ADDR_2	0	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	NFRAC<0>	0	Fractional PLL N divider value 0 to 0.99999.
Bit6	NFRAC<1>	0	
Bit7	NFRAC<2>	0	
Bit8	NFRAC<3>	0	
Bit9	NFRAC<4>	0	
Bit10	NFRAC<5>	0	
Bit11	NFRAC<6>	0	
Bit12	NFRAC<7>	0	
Bit13	NFRAC<8>	0	
Bit14	NFRAC<9>	0	
Bit15	NFRAC<10>	0	
Bit16	NFRAC<11>	0	
Bit17	NFRAC<12>	0	
Bit18	NFRAC<13>	0	
Bit19	NFRAC<14>	0	
Bit20	NFRAC<15>	0	
Bit21	NFRAC<16>	0	
Bit22	NFRAC<17>	0	
Bit23	NFRAC<18>	0	
Bit24	NFRAC<19>	0	
Bit25	NFRAC<20>	0	
Bit26	NFRAC<21>	0	
Bit27	NFRAC<22>	0	
Bit28	NFRAC<23>	0	
Bit29	NFRAC<24>	0	
Bit30	RSV	0	
Bit31	RSV	0	

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Register 4

Register address					PD PLL	Power Down PLL blocks									PD VCM
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

PD DC off	EXT VCO	PLL Test Control							ΣΔ Mode order			ΣΔ Mode controls			EN Fract mode
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

Register 4	Name	Reset Value	Description
Bit0	ADDR_0	0	Register address bits
Bit1	ADDR_1	0	
Bit2	ADDR_2	1	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	PWD_PLL	0	Power down all PLL blocks (1 = off)
Bit6	PWD_CP	0	When 1, charge pump is off
Bit7	PWD_VCO	0	When 1, VCO is off
Bit8	PWD_VCOMUX	0	Power down the 4 VCO mux block (1 = Off)
Bit9	PWD_DIV124	0	Power down programmable RF divider in PLL feedback path (1 = off)
Bit10	PWD_PRESC	0	Power down programmable prescaler (1 = off)
Bit11	RSV	0	
Bit12	PWD_OUT_BUFF	1	Power down LO output buffer (1 = off).
Bit13	PWD_LO_DIV	1	Power down frequency divider in LO output chain 1 (1 = off)
Bit14	PWD_TX_DIV	1	Power down frequency divider in modulator chain (1 = off)
Bit15	PWD_BB_VCM	1	Power down baseband input DC common block (1 = off)
Bit16	PWD_DC_OFF	1	Power down baseband input DC offset control block (1 = off)
Bit17	EN_EXTVCO	0	Enable external LO/VCO input buffer (1 = enabled)
Bit18	EN_ISOURCE	0	Enable offset current at Charge Pump output (to be used in fractional mode only, 1 = on).
Bit19	LD_ANA_PREC_0	0	Control precision of analog lock detector (1 1 = low; 0 0 = high). See LOCK DETECT section of Application Information for usage details.
Bit20	LD_ANA_PREC_1	0	
Bit21	CP_TRISTATE_0	0	Set the charge pump output in Tristate mode. Normal, B[22..21] = [00] Down, B[22..21] = [01] Up, B[22..21] = [10] Tristate, B[22..21] = [11]
Bit22	CP_TRISTATE_1	0	
Bit23	SPEEDUP	0	Speed up PLL and Tx blocks by bypassing bias stabilizer capacitors.
Bit24	LD_DIG_PREC	0	Lock detector precision (increases sampling time if set to 1)
Bit25	EN_DITH	1	Enable ΔΣ modulator dither (1=on)
Bit26	MOD_ORD_0	0	ΔΣ modulator order (1 through 4). Not used in integer mode. 1st order, B[27..26] = [00] 2nd order, B[27..26] = [01] 3rd order, B[27..26] = [10] 4th order, B[27..26] = [11]
Bit27	MOD_ORD_1	1	
Bit28	DITH_SEL	0	Select dither mode for ΔΣ modulator (0 = const; 1 = pseudo-random)
Bit29	DEL_SD_CLK_0	0	ΔΣ modulator clock delay. Not used in integer mode. Min delay = 00 Max delay = 11
Bit30	DEL_SD_CLK_1	1	
Bit31	EN_FRAC	0	Enable fractional mode (1 = fractional enabled)

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Register 5

Register address					VCO_R Trim			PLL_R_Trim		VCO Current				VCOBUF BIAS	
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

VCOMUX BIAS		OUTBUF BIAS		RSV		BIAS SEL	VCO CAL REF			VCOMUX AMPL		VCO Bias Voltage		RSV	EN_LD ISRC
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

Register 5	Name	Reset Value	Description
Bit0	ADDR_0	1	Register address bits
Bit1	ADDR_1	0	
Bit2	ADDR_2	1	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	VCOBIAS_RTRIM_0	0	VCO bias resistor trimming. Recommended programming [100].
Bit6	VCOBIAS_RTRIM_1	0	
Bit7	VCOBIAS_RTRIM_2	1	
Bit8	PLLBIAS_RTRIM_0	0	PLL bias resistor trimming. Recommended programming [10].
Bit9	PLLBIAS_RTRIM_1	1	
Bit10	VCO_BIAS_0	0	VCO bias reference current. 300 µA, B[13..10] = [00 00] 600 µA, B[13..10] = [11 11] Bias current varies directly with reference current Recommended programming 400 µA, B[13..10] = [0101] with VCC_VCO2 = 3.3 V 600 µA, B[13..10] = [1111] with VCC_VCO2 = 5.0 V
Bit11	VCO_BIAS_1	0	
Bit12	VCO_BIAS_2	0	
Bit13	VCO_BIAS_3	1	
Bit14	VCOBUF_BIAS_0	0	VCO buffer bias reference current. 300 µA, B[15..14] = [00] 600 µA, B[15..14] = [11] Bias current varies directly with reference current Recommended programming [10]
Bit15	VCOBUF_BIAS_1	1	
Bit16	VCOMUX_BIAS_0	0	VCO's muxing buffer bias reference current. 300 µA, B[17..16] = [00] 600 µA, B[17..16] = [11] Bias current varies directly with reference current Recommended programming [11]
Bit17	VCOMUX_BIAS_1	1	
Bit18	BUFOUT_BIAS_0	0	PLL output buffer bias reference current. 300 µA, B[19..18] = [00] 600 µA, B[19..18] = [11] Bias current varies directly with reference current
Bit19	BUFOUT_BIAS_1	1	
Bit20	RSV	0	
Bit21	RSV	1	
Bit22	VCO_CAL_IB	0	Select bias current type for VCO calibration circuitry 0 = PTAT; 1 = constant over temperature Recommended programming [0]
Bit23	VCO_CAL_REF_0	0	VCO calibration reference voltage trimming. 0.9 V, B[25..23] = [000] 1.4 V, B[25..23] = [111] Recommended programming [010]
Bit24	VCO_CAL_REF_1	0	
Bit25	VCO_CAL_REF_2	1	
Bit26	VCO_AMPL_CTRL_0	0	Adjust the signal amplitude at the VCO mux input Recommended programming [11]
Bit27	VCO_AMPL_CTRL_1	1	
Bit28	VCO_VB_CTRL_0	0	VCO core bias voltage control 1.2 V, B[29..28] = [00] 1.35 V, B[29..28] = [01] 1.5 V, B[29..28] = [10] 1.65 V, B[29..28] = [11] Recommended programming [00]
Bit29	VCO_VB_CTRL _1	1	
Bit30	RSV	0	

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Register 5	Name	Reset Value	Description
Bit31	EN_LD_ISOURCE	1	Enable monitoring of LD to turn on Isource when in frac-n mode (EN_FRAC=1). 0 = ISource set by EN_ISOURCE. 1 = ISource set by LD. Recommended programming [0]

Register 6

Register address					BB DC OFFSET										
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

BB DC OFFSET					VREF SEL			TXDIV SEL		LODIV SEL		TXDIV BIAS		LODIV BIAS	
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

Register 6	Name	Reset Value	Description
Bit0	ADDR_0	0	Register address bits
Bit1	ADDR_1	1	
Bit2	ADDR_2	1	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	IOFF_0	0	Adjust Iref current used for defining I DC offset. Full range, 2 × Iref, B[12..5] = [1 1111 111] Mid scale, Iref B[12..5] = [1 0000 000]
Bit6	IOFF_1	0	
Bit7	IOFF_2	0	
Bit8	IOFF_3	0	
Bit9	IOFF_4	0	
Bit10	IOFF_5	0	
Bit11	IOFF_6	0	
Bit12	IOFF_7	1	
Bit13	QOFF_0	0	Adjust Iref current used for defining Q DC offset. Full range, 2 × Iref, B[20..13] = [1 1111 111] Mid scale, Iref B[20..13] = [1 0000 000]
Bit14	QOFF_1	0	
Bit15	QOFF_2	0	
Bit16	QOFF_3	0	
Bit17	QOFF_4	0	
Bit18	QOFF_5	0	
Bit19	QOFF_6	0	
Bit20	QOFF_7	1	
Bit21	VREF_SEL_0	0	Adjust Vref in baseband common mode generation circuit. 0.65 V, B[23..21] = [000] 1 V, B[23..21] = [111] Modulator common mode is Vref + Vbe. Recommended programming [100]
Bit22	VREF_SEL_1	0	
Bit23	VREF_SEL_2	1	
Bit24	TX_DIV_SEL_0	0	Adjust Tx path divider. Div1, [B25..24] = [00] Div2, [B25..24] = [01] Div4, [B25..24] = [10] Div8, [B25..24] = [11]
Bit25	TX_DIV_SEL_1	0	
Bit26	LO_DIV_SEL_0	0	Adjust LO path divider Div1, [B28..27] = [00] Div2, [B28..27] = [01] Div4, [B28..27] = [10] Div8, [B28..27] = [11]
Bit27	LO_DIV_SEL_1	0	
Bit28	TX_DIV_BIAS_0	0	TX divider bias reference current 25 µA, [B29..28] = [00] 37.5 µA, [B29..28] = [01] 50 µA, [B29..28] = [10] 62.5 µA, [B29..28] = [11] Bias current varies directly with reference current
Bit29	TX_DIV_BIAS_1	1	

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Register 6	Name	Reset Value	Description
Bit30	LO_DIV_BIAS_0	0	LO divider bias reference current 25 µA, [B29..28] = [00] 37.5 µA, [B29..28] = [01] 50 µA, [B29..28] = [10] 62.5 µA, [B29..28] = [11] Bias current varies directly with reference current
Bit31	LO_DIV_BIAS_1	1	

Register 7

Register address					VCO CAP ARRAY CONTROL								RSV	VCO test mode	CAL bypass
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

MUX CONTROL			ISRC SINK	OFFSET CURRENT ADJUST			LP PD TimeConst		VCM Bias	MIX LO VCM			DC OFF REF		VCO BIAS SEL
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

Register 7	Name	Reset Value	Description
Bit0	ADDR_0	1	Register address bits
Bit1	ADDR_1	1	
Bit2	ADDR_2	1	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	RSV	0	
Bit6	RSV	0	
Bit7	VCO_TRIM_0	0	VCO capacitor array control bits, used in manual cal mode
Bit8	VCO_TRIM_1	0	
Bit9	VCO_TRIM_2	0	
Bit10	VCO_TRIM_3	0	
Bit11	VCO_TRIM_4	0	
Bit12	VCO_TRIM_5	1	
Bit13	RSV	0	
Bit14	VCO_TEST_MODE	0	Counter mode: measure max/min frequency of each VCO
Bit15	CAL_BYPASS	0	Bypass of VCO auto-calibration. When ‘1’ VCO_TRIM and VCO_SEL bits are used to select the VCO and the cap array setting
Bit16	MUX_CTRL_0	1	Select signal for test output (pin 5, LD). [000] = Ground [001] = Lock detector [010] = NDIV counter output [011] = Ground [100] = RDIV counter output [101] = Ground [110] = A_counter output [111] = Logic high;
Bit17	MUX_CTRL_1	0	
Bit18	MUX_CTRL_2	0	
Bit19	ISOURCE_SINK	0	Charge pump offset current polarity.
Bit20	ISOURCE_TRIM_0	0	Adjust isource bias current in frac-n mode.
Bit21	ISOURCE_TRIM_1	0	
Bit22	ISOURCE_TRIM_2	1	
Bit23	PD_TC_0	0	Time constant control for PWD_OUT_BUFF [00] = Minimum time constant [11] = Maximum time constant
Bit24	PD_TC_1	0	
Bit25	IB_VCM_SEL	0	Select constant/ptat current for Common mode bias generation block 0 = PTAT 1 = const
Bit26	RSV	0	

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Register 7	Name	Reset Value	Description
Bit27	RSV	0	
Bit28	RSV	1	
Bit29	DCOFFSET_I_0	0	Adjust BB input DC offset Iref 50 µA, B[27..26] = [00] 100 µA, B[27..26] = [01] 150 µA, B[27..26] = [10] 200 µA, B[27..26] = [11]
Bit30	DCOFFSET_I_1	1	
Bit31	VCO_BIAS_SEL	0	Select VCO_BIAS trim settings stored in EEPROM 0 = Use EEPROM settings if parity check is 1; otherwise, use SPI settings 1 = Use SPI settings Recommended programming [1]

READBACK MODE

Register 0 functions as a Readback register. TRF372017 implements the capability to read-back the content of any serial programming interface register by initializing register 0.

Each read-back is composed by two phases: writing followed by the actual reading of the internal data. This is shown in the timing diagram in Figure 3. During the writing phase a command is sent to TRF372017 register 0 to set it in read-back mode and to specify which register is to be read. In the proper reading phase, at each rising clock edge, the internal data is transferred into the RDBK pin and can be read at the following falling edge (LSB first). The first clock after the LE goes high (end of writing cycle) is idle and the following 32 clocks pulses will transfer the internal register content to the RDBK pin.

Readback From the Internal Registers Banks

TRF372017 integrates 8 registers: Register 0 (000) to Register 7 (111). Registers 1 through 7 are used to set-up and control the TRF372017 functionalities, while register 0 is used for the readback function.

The latter register needs to be programmed with a specific command that sets TRF372017 in read-back mode and specifies the register to be read:

- set B[31] to 1 to put TRF372017 in read-back mode.
- set B[30,28] equal to the address of the register to be read (000 to 111).
- Set B27 to control the VCO frequency counter in VCO test mode.

Register 0 Write

		Name	Reset Value	Description
Address Bits	B0	ADDR<0>	0	Register 0 to be programmed to set TRF372017 in readback mode.
	B1	ADDR<1>	0	
	B2	ADDR<2>	0	
	B3	ADDR<3>	1	
	B4	ADDR<4>	0	
Data Field	B5	N/C	0	
	B6	N/C	0	
	B7	N/C	0	
	B8	N/C	0	
	B9	N/C	0	
	B10	N/C	0	
	B11	N/C	0	
	B12	N/C	0	
	B13	N/C	0	
	B14	N/C	0	
	B15	N/C	0	
	B16	N/C	0	
	B17	N/C	0	

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		Name	Reset Value	Description
	B18	N/C	0	
	B19	N/C	0	
	B20	N/C	0	
	B21	N/C	0	
	B22	N/C	0	
	B23	N/C	0	
	B24	N/C	0	
	B25	N/C	0	
	B26	N/C	0	
	B27	COUNT_MODE_MUX_SEL	0	Select Readback for VCO maximum frequency or minimum frequency. 0 = Max 1 = Min
	B28	RB_REG<0>	X	3 LSB's of the address for the register that is being read Reg 0, B[30..28] = [000] Reg 7, B[30..28] = [111]
	B29	RB_REG<1>	X	
	B30	RB_REG<2>	X	
	B31	RB_ENABLE	1	1 ≥ Put the device in Readback Mode

The contents of any register specified in RB_REG can be read back during the read cycle, including register 0.

Register address					CHIP_ID	NU						R_SAT_ERR
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12

COUNT0-7/VCO_TRM								COUNT8-10/VCO_SEL			COUNT11-17						
Bit13	Bit14	Bit15	Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30

COUNT_MODE-MUX-SEL
Bit31

Register 0	Name	Reset Value	Description
Bit0	ADDR_0	0	Register address bits
Bit1	ADDR_1	0	
Bit2	ADDR_2	0	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	CHIP_ID_0	1	
Bit6	CHIP_ID_1	1	
Bit7	NU	x	
Bit8	NU	x	
Bit9	NU	x	
Bit10	NU	x	
Bit11	NU	x	
Bit12	R_SAT_ERR	x	Error flag for calibration speed
Bit13	count_0/NU	x	B[30..13] = VCO frequency counter high when COUNT_MODE_MUX_SEL = 0 and VCO_TEST_MODE = 1
Bit14	count_1/NU	x	
Bit15	count_2/VCO_TRIM_0	x	
Bit16	count_3/VCO_TRIM_1	x	
Bit17	count_4/VCO_TRIM_2	x	
Bit18	count_5/VCO_TRIM_3	x	
Bit19	count_6/VCO_TRIM_4	x	
Bit20	count_7/VCO_TRIM_5	x	

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Register 0	Name	Reset Value	Description
Bit21	count_8/NU	x	B[30..13] = VCO frequency counter low when COUNT_MODE_MUX_SEL = 1 and VCO_TEST_MODE = 1 B[20..15] = Autocal results for VCO_TRIM, B[23..22] = Autocal results for VCO_SEL when VCO_TEST_MODE = 0
Bit22	count_9/VCO_sel_0	x	
Bit23	count_10/VCO_sel_1	x	
Bit24	count<11>	x	
Bit25	count<12>	x	
Bit26	count<13>	x	
Bit27	count<14>	x	
Bit28	count<15>	x	
Bit29	count<16>	x	
Bit30	count<17>	x	
Bit31	COUNT_MODE_MUX_SEL	x	0 = Minimum frequency 1 = Maximum frequency

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APPLICATION INFORMATION

INTEGER AND FRACTIONAL MODE SELECTION

The PLL is designed to operate in either Integer mode or Fractional mode. If the desired local oscillator (LO) frequency is an integer multiple of the phase frequency detector (PFD) frequency, f_{PFD}, then Integer mode can be selected. The normalized in-band phase noise floor in Integer mode is lower than in Fractional mode. In Integer mode, the feedback divider is an exact integer, and the fraction is zero. While operating in Integer mode, the register bits corresponding to the fractional control are *don't care*.

In Fractional mode, the feedback divider fractional portion is non-zero on average. With 25-bit fractional resolution, RF stepsize $f_{PFD}/2^{25}$ is less than 1 Hz with a f_{PFD} up to 33 MHz. The appropriate fractional control bits in the serial register must be programmed.

DESCRIPTION OF PLL STRUCTURE

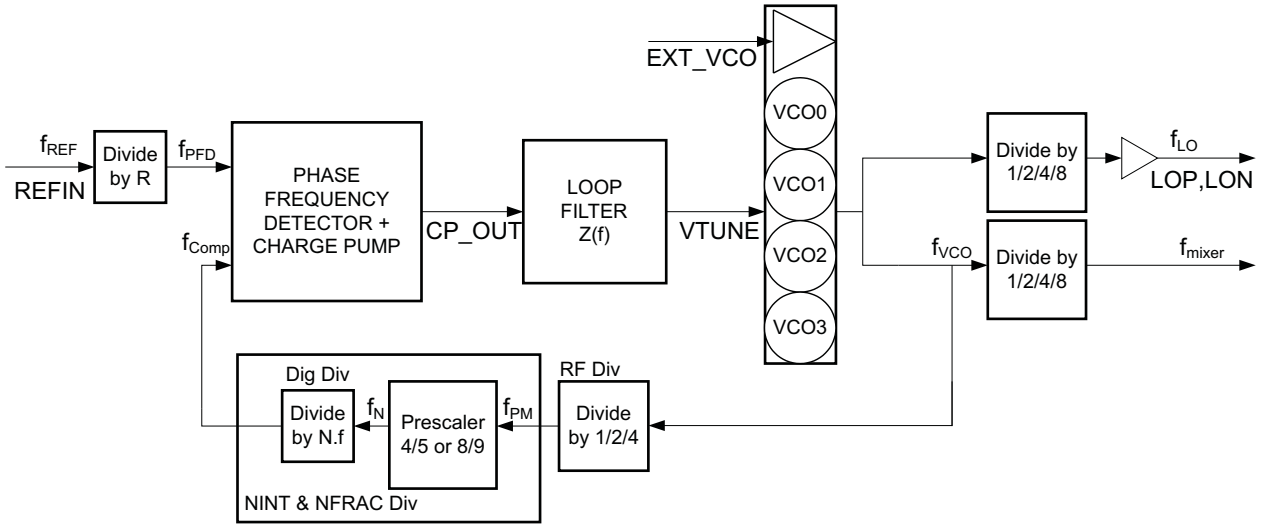

Figure 85. Block Diagram of the PLL Loop

The output frequency is given by Equation 1:

$$f_{VCO} = \frac{f_{REF}}{RDIV} (PLL\_DIV\_SEL)\left[NINT + \frac{NFRAC}{2^{25}}\right] \quad (1)$$

The rate at which phase comparison occurs is f_{REF}/RDIV. In Integer mode, the fractional setting is ignored and Equation 2 is applied.

$$\frac{f_{VCO}}{f_{PFD}} = NINT \times PLL\_DIV\_SEL \quad (2)$$

The feedback divider block consists of a programmable RF divider, a prescaler divider, and an NF divider. The prescaler can be programmed as either a 4/5 or an 8/9 prescaler. The NF divider includes an *A* counter and an *M* counter.

Selecting PLL Divider Values

Operation of the PLL requires the LO_DIV_SEL, RDIV, PLL_DIV_SEL, NINT, and NFRAC bits to be calculated. The LO or mixer frequency is related to f_{VCO} according to divide-by-1/-2/-4/-8 blocks and the operating range of f_{VCO}.

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a. **LO_DIV_SEL**

$$LO\_DIV\_SEL = \begin{cases} 1 & 2400\ MHz \le f_{RF} \le 4800\ MHz \\ 2 & 1200\ MHz \le f_{RF} \le 2400\ MHz \\ 3 & 600\ MHz \le f_{RF} \le 1200\ MHz \\ 4 & 300\ MHz \le f_{RF} \le 600\ MHz \end{cases}$$

Therefore:

$f_{VCO} = LO\_DIV\_SEL \times f_{RF}$

b. **PLL_DIV_SEL**

Given f_{VCO}, select the minimum value for PLL_DIV_SEL so that the programmable RF divider limits the input frequency into the prescaler block, f_{PM}, to a maximum of 3000 MHz.

$$PLL\_DIV\_SEL = \min(1, 2, 4) \text{ such that } f_{PM} \le 3000\ MHz$$

This calculation can be restated as Equation 3.

$$PLL\_DIV\_SEL = Ceiling\left(\frac{LO\_DIV\_SEL \times f_{RF}}{3000\ MHz}\right) \quad (3)$$

Higher values of f_{PFD} correspond to better phase noise performance in Integer mode or Fractional mode. f_{PFD}, along with PLL_DIV_SEL, determines the f_{VCO} stepsize in Integer mode. Therefore, in Integer mode, select the maximum f_{PFD} that allows for the required RF stepsize, as shown by Equation 4.

$$f_{PFD} = \frac{f_{VCO,\ Stepsize}}{PLL\_DIV\_SEL} = \frac{f_{RF,\ Stepsize} \times LO\_DIV\_SEL}{PLL\_DIV\_SEL} \quad (4)$$

In Fractional mode, a small RF stepsize is accomplished through the Fractional mode divider. A large f_{PFD} should be used to minimize the effects of fractional controller noise in the output spectrum. In this case, f_{PFD} may vary according to the reference clock and fractional spur requirements; for example, f_{PFD} = 20 MHz.

c. **RDIV, NINT, NFRAC, PRSC_SEL**

$$RDIV = \frac{f_{REF}}{f_{PFD}}$$

$$NINT = floor\left(\frac{f_{VCO} RDIV}{f_{REF} PLL\_DIV\_SEL}\right)$$

$$NFRAC = floor\left(\left[\left(\frac{f_{VCO} RDIV}{f_{REF} PLL\_DIV\_SEL}\right) - NINT\right] 2^{25}\right)$$

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The P/(P+1) programmable prescaler is set to 8/9 or 4/5 through the PRSC_SEL bit. To allow proper fractional control, set PRSC_SEL according to Equation 5.

$$PRSC\_SEL = \begin{cases} \frac{8}{9} & NINT \geq 75 \text{ in Fractional Mode or } NINT \geq 72 \text{ in Integer mode} \\ \frac{4}{5} & 23 \leq NINT < 75 \text{ in Fractional mode or } 20 \leq NINT < 72 \text{ in Integer mode} \end{cases} \quad (5)$$

The PRSC_SEL limit at NINT < 75 applies to Fractional mode with third-order modulation. In Integer mode, the PRSC_SEL = 8/9 should be used with NINT as low as 72. The divider block accounts for either value of PRSC_SEL without requiring NINT or NFRAC to be adjusted. Then, calculate the maximum frequency to be input to the digital divider at f_N. Use the lower of the possible prescaler divide settings, P = (4,8), as shown by Equation 6.

$$f_{N,Max} = \frac{f_{VCO}}{PLL\_DIV\_SEL \times P} \quad (6)$$

Verify that the frequency into the digital divider, f_N, is less than or equal to 375 MHz. If f_N exceeds 375 MHz, choose a larger value for PLL_DIV_SEL and recalculate f_{PFD}, RDIV, NINT, NFRAC, and PRSC_SEL.

Setup Example for Integer Mode

Suppose the following operating characteristics are desired for Integer mode operation:

- f_{REF} = 40 MHz (reference input frequency)
- Step at RF = 2 MHz (RF channel spacing)
- f_{RF} = 1600 MHz (RF frequency)

The VCO range is 2400 MHz to 4800 MHz. Therefore:

- LO_DIV_SEL = 2
- f_{VCO} = LO_DIV_SEL × 1600 MHz = 3200 MHz

In order to keep the frequency of the prescaler below 3000 MHz:

- PLL_DIV_SEL = 2

The desired stepsize at RF is 2 MHz, so:

- f_{PFD} = 2 MHz
- f_{VCO}, stepsize = PLL_DIV_SEL × f_{PFD} = 4 MHz

Using the reference frequency along with the required f_{PFD} gives:

- RDIV = 20
- NINT = 800

NINT ≥ 75; therefore, select the 8/9 prescaler.

$f_{N,Max}$ = 3200 MHz/(2 × 8) = 200 MHz < 375 MHz

This example shows that Integer mode operation gives sufficient resolution for the required stepsize.

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Setup Example for Fractional Mode

Suppose the following operating characteristics are desired for Fractional mode operation:

- f_{REF} = 40 MHz (reference input frequency)
- Step at RF = 5 MHz (RF channel spacing)
- f_{RF} = 1,600,000,045 Hz (RF frequency)

The VCO range is 2400 MHz to 4800 MHz. Therefore:

- LO_DIV_SEL = 2
- f_{VCO} = LO_DIV_SEL × 1,600,000,045 Hz = 3,200,000,090 Hz

In order to keep the frequency of the prescaler below 3000 MHz:

- PLL_DIV_SEL = 2

Using a typical f_{PFD} of 20 MHz:

- RDIV = 2
- NINT = 80
- NFRAC = 75

NINT ≥ 75; therefore, select the 8/9 prescaler.

$f_{N,Max}$ = 3200 MHz/(2 × 8) = 200 MHz < 375 MHz

The actual frequency at RF is:

- f_{RF} = 1600000044.9419 Hz

For a frequency error of –0.058 Hz.

Fractional Mode Setup

Optimal operation of the PLL in fractional mode requires several additional register settings. Recommended values are listed in Table 3. Optimal performance may require tuning the MOD_ORD, ISOURCE_SINK, and ISOURCE_TRIM values according to the chosen frequency band.

Table 3. Fractional Mode Register Settings

REGISTER BIT	REGISTER ADDRESSING	RECOMMENDED VALUE
EN_ISOURCE	Reg4B18	1
EN_DITH	Reg4B25	1
MOD_ORD	Reg4B[27..26]	B[27..26] = [10]
DITH_SEL	Reg4B28	0
DEL_SD_CLK	Reg4B[30..29]	B[30..29] = [10]
EN_LD_ISOURCE	Reg5B31	0
ISOURCE_SINK	Reg7B19	0
ISOURCE_TRIM	Reg7B[22..20]	B[22..20] = [100]

SELECTING THE VCO AND VCO FREQUENCY CONTROL

To achieve a broad frequency tuning range, the TRF372017 includes four VCOs. Each VCO is connected to a bank of capacitors that determine its valid operating frequency. For any given frequency setting, the appropriate VCO and capacitor array must be selected.

The device contains logic that will automatically select the appropriate VCO and capacitor bank. Set bit EN_CAL to initiate the calibration algorithm. During the calibration process, the device will select a VCO and a capacitor state so that VTune matches the reference voltage set by VCO_CAL_REF_n. Accuracy of the tune is increased through bits CAL_ACC_n. Since a calibration begins immediately when EN_CAL is set, all registers must contain valid value prior to initiating calibration.

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Calibration logic is driven by a CAL_CLK clock derived from the phase frequency detector frequency scaled according to the setting in CAL_CLK_SEL. Faster CAL_CLK frequency enables faster calibration, but the logic is limited to clock frequencies around 1MHz. Table 4 provides suggested CAL_CLK_SEL scaling recommendations for several phase frequency detector frequencies. The flag R_SAT_ERR is evaluated during the calibration process to indicate calibration counter overflow errors, which will occur if CAL_CLK runs too fast. If R_SAT_ERR is set during a calibration, the resulting calibration is not valid and CAL_CLK_SEL must be used to slow the CAL_CLK. CAL_CLK frequencies should not be set below 0.1MHz.

Table 4. Example CAL_CLK_SEL Scaling

PFD FREQUENCY MHz	CAL_CLK_SEL SCALING	CAL_CLK FREQUENCY MHz
20	1/32	0.625
1	1	1
0.1	8	0.8

When VCOSEL_MODE is 0, the device will automatically select both the VCO and capacitor bank within 23 CAL_CLK cycles. When VCOSEL_MODE is 1, the device will use the VCO selected in VCO_SEL_0 and VCO_SEL_1 and automatically select the capacitor array within 17 CAL_CLK cycles. The VCO and capacitor array settings resulting from calibration cannot be read from the VCO_SEL_n and VCO_TRIM_n bits in registers 2 and 7. They can only be read from register 0.

Automatic calibration can be disabled by setting CAL_BYPASS to 1. In this manual cal mode, the VCO is selected through register bits VCO_SEL_n, while the capacitor array is selected through register bits VCO_TRIM_n. Calibration modes are summarized in Table 5. After calibration is complete, the PLL is released from calibration mode to reach an analog lock.

During the calibration process, the TRF372017 will scan through many frequencies. RF and LO outputs should be disabled until calibration is complete. At power up the RF and LO output will be disabled by default.

Once a calibration has been performed at a given frequency setting, the calibration is valid over all operating temperature conditions.

Table 5. VCO Calibration Modes

CAL_BYPASS	VCOSEL_MODE	MAX CYCLES CAL_CLK	VCO	CAPACITOR ARRAY
0	0	46	Automatic	
0	1	34	VCO_SEL_n	automatic
1	*don't care*	*na*	VCO_SEL_n	VCO_TRIM_n

EXTERNAL VCO

An external LO or VCO signal may be applied. EN_EXTVCO powers the input buffer and selects the buffered external signal instead of an internal VCO. Dividers, the pfd, and the charge pump remain enabled and may be used to drive an external VCO. NEG_VCO must correspond to the gain of the external VCO.

VCO TEST MODE

Setting VCO_TEST_MODE forces the currently selected VCO to the edge of its frequency range by disconnecting the charge pump input from the pfd and loop filter and forcing its output high or low. The upper or lower edge of the VCO range is selected through COUNT_MODE_MUX_SEL.

VCO_TEST_MODE also reports the value of a frequency counter in COUNT, which can be read back in register 0. COUNT reports the number of digital N divider cycles in the PLL, directly related to the period of fN, that occur during each CAL_CLK cycle. Counter operation is initiated through the bit EN_CAL.

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Table 6. VCO Test Mode

VCO_TEST_MODE	COUNT_MODE_MUX_SEL	VCO Operation	Register 0 B[30..13]
0	*don't care*	Normal	B[30..24] = *undefined* B[23..22] = VCO_SEL selected during autocal B21 = *undefined* B[20..13] = VCO_TRIM selected during autocal
1	0	Max frequency	B[30..13] = Max frequency counter
1	1	Min frequency	B[30..13] = Min frequency counter

LOOP FILTER

Loop filter design is critical for achieving low closed loop phase noise. Some typical loop filter component values are given in Table 7, referenced to designators in Figure 86. These loop filters are designed using charge pump current of 1.94mA to minimize noise.

Table 7. Typical Loop Filter Components

f_{PFD} (MHz)	C1 (pF)	C2 (pF)	R2 (kΩ)	C3 (pF)	R3 (kΩ)	C4 (pF)	R4 (kΩ)
40	1000	10000	0.47	39	1.4	1.8	3.3
1.6	47	560	10	4.7	5	open	0
6.4	100	1000	5	20	5	open	0
10	270	4700	1.5	4700	1.5	open	0
30.72	2200	20000	0.47	220	0.475	220	0.475

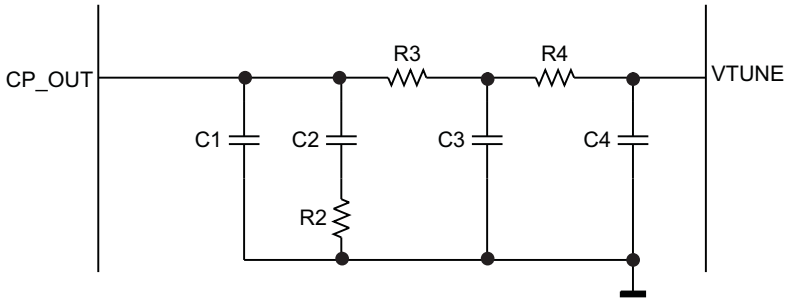

Figure 86. Loop Filter Component Reference Designators

LOCK DETECT

The lock detect signal is generated in the phase frequency detector by comparing the VCO target frequency against the VCO actual frequency. When the phase of the two compared frequencies remains aligned for several clock cycles, an internal signal goes high. The precision of this comparison is controlled through the LD_ANA_PREC bits. This internal signal is then averaged and compared against a reference voltage to generate the LD signal. The number of averages used is controlled through LD_DIG_PREC. Therefore, when the VCO is frequency locked, LD is high. When the VCO frequency is not locked, LD may pulse high or exhibit periodic behavior.

By default, the internal lock detect signal is driven on the LD terminal. Register bits MUX_CTRL_n can be used to control a mux to output other diagnostic signals on the LD output. The LD control signals are shown in Table 8.

Table 8. LD Control Signals

ADJUSTMENT	REGISTER BITS	BIT ADDRESSING
Lock detect precision	LD_ANA_PREC_0	Register 4 Bit 19
Unlock detect precision	LD_ANA_PREC_1	Register 4 Bit 20
LD averaging count	LD_DIG_PREC	Register 4 Bit 24
Diagnostic Output	MUX_CTRL_n	Register 7 Bits 18..16

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Table 9. LD Control Signal Mode Settings

CONDITION	RECOMMENDED SETTINGS
Integer Mode	LD_ANA_PREC_0 = 0 LD_ANA_PREC_1 = 0 LD_DIG_PREC = 1
Fractional Mode	LD_ANA_PREC_0 = 1 LD_ANA_PREC_1 = 1 LD_DIG_PREC = 1

Tx DIVIDER

The Tx divider, illustrated in Figure 87, converts the differential output of the VCO into differential I and Q mixer components. The divide by 1 differential quadrature phases are provided through a polyphase. Divide by 2, 4, and 8 differential quadrature phases are provided through flip-flop dividers. Only one of the dividers operates at a time, and the appropriate output is selected by a mux. DIVn bits are controlled through TX_DIV_SELn.

TX_DIV_I determines the bias level for the divider blocks. The SPEEDUP control is used to bypass a stabilization resistor and reach the final bias level faster after a change in the divider selection. SPEEDUP should be disabled during normal operation.

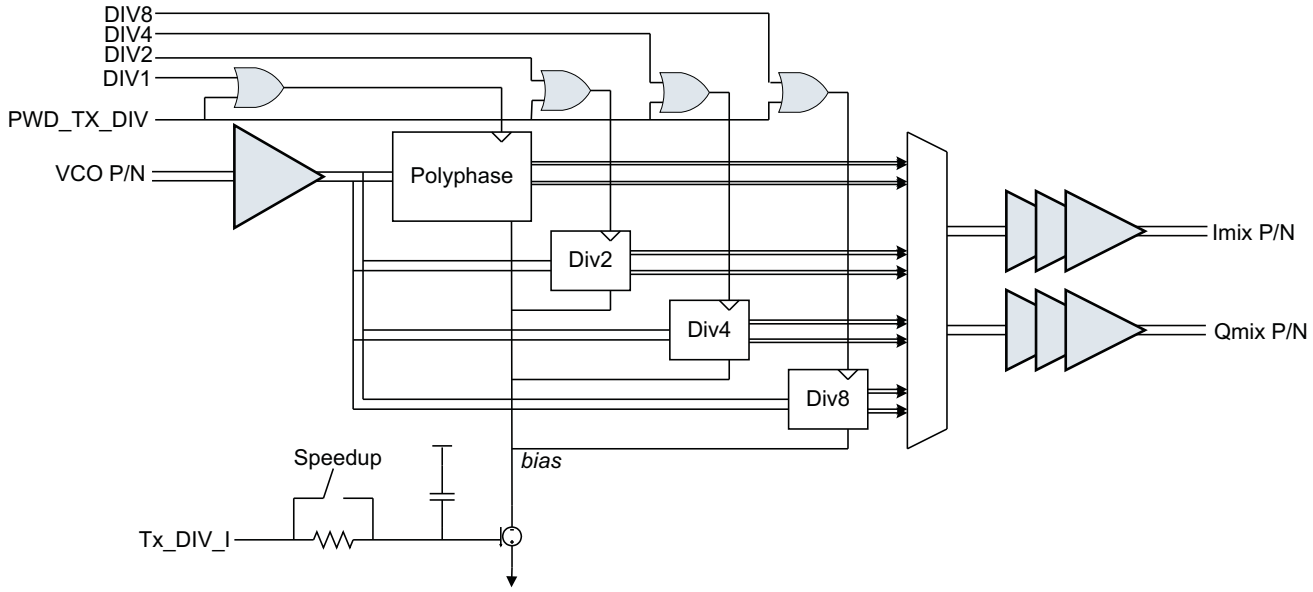

Figure 87. Tx Divider

LO DIVIDER

The LO divider is shown in Figure 88. It frequency divides the VCO output. Only one of the dividers operates at a time, and the appropriate output is selected by a mux. DIVn bits are controlled through LO_DIV_SELn. The output is buffered and provided on output pins LO_OUT_P and LO_OUT_N. The output level is controlled through BUFOUT_BIASn.

LO_DIV_I determines the bias level for the divider blocks. The SPEEDUP control is used to bypass a stabilization resistor and reach the final bias level faster after a change in the divider selection. SPEEDUP should be disabled during normal operation. Although SPEEDUP controls both the Tx and LO divider biases, the Tx and LO divider biases are generated independently.

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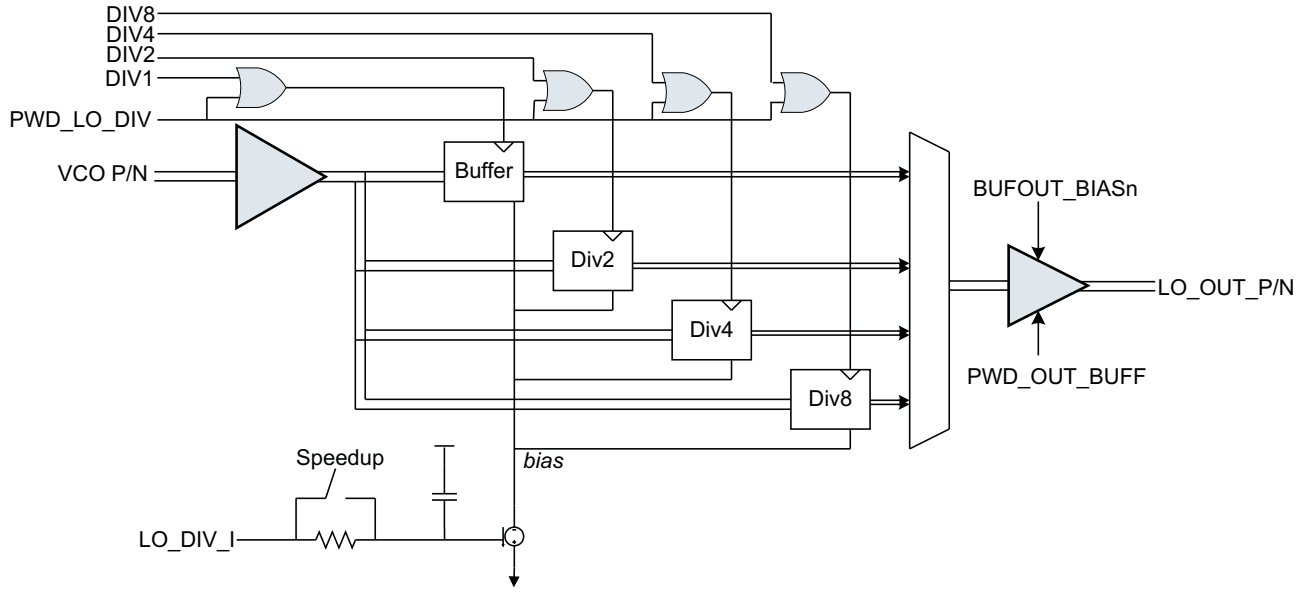

Figure 88. LO Divider

LO OUTPUTS

The LO outputs are open collector outputs. They require a pull-up to VCC. 75Ω pull-up resistors to VCC with local decoupling provides a good broadband match and is shown in an example circuit in Figure 89. An inductor pull-up in parallel with a cap can provide a tuned load for excellent narrowband load matching.

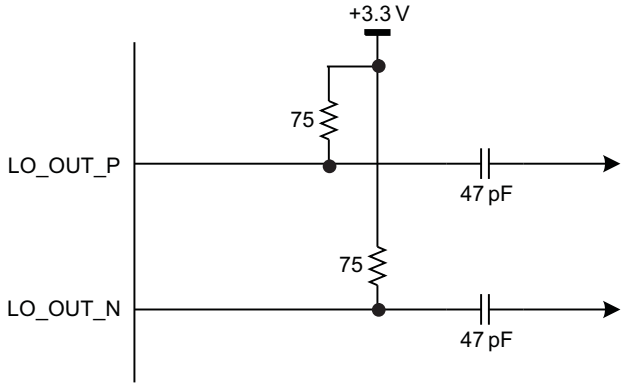

Figure 89. Example LO_OUT Circuit for Broadband Operation

MIXER

A diagram of the mixer is shown in Figure 90. The mixer is followed by a differential to single-ended converter and buffer for output.

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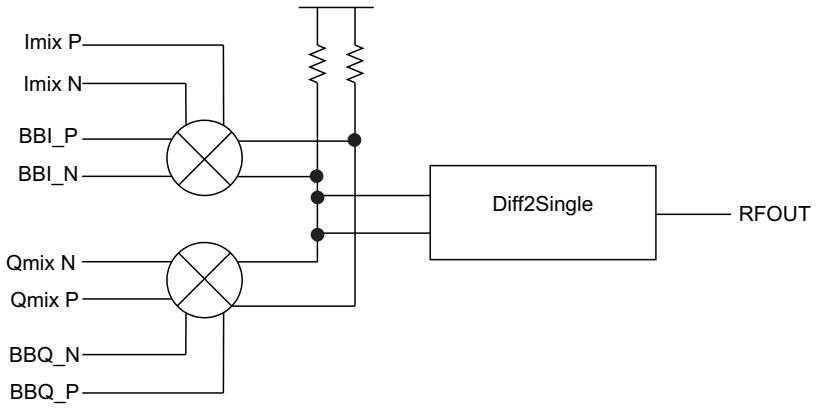

Figure 90. Mixer

DISABLING OUTPUTS

RF frequency outputs are generated at the RFOUT and LO* terminals. Unused RF frequency outputs should be disabled to minimize power consumption and noise generation. Table 10 lists settings used to disable the outputs. Power save mode can also be used to disable outputs.

Table 10. Register Controls for Disabling Outputs

DISABLED OUTPUT	REGISTER BIT	SETTING
RFOUT	PWD_TX_DIV	1
LOP and LON	PWD_OUT_BUFF	1
	PWD_LO_DIV	1

POWERSAVE MODE

Powersave mode can be used to put the device into a low power consumption mode. The PLL block remains active in Powersave mode, reducing the time required for startup. However, the modulator, dividers, output buffers and baseband common mode generation blocks are powered down. The SPI block remains active, and registers are addressable. Use the PS pin to activate powersave mode.

POWER SUPPLY DISTRIBUTION

Power supply distribution for the TRF372017 is shown in Figure 91. Proper isolation and filtering of the supplies is critical for low noise operation of the device. Each supply pin should be supplied with local decoupling capacitance and isolated with a ferrite bead. VCC_VCO2 is tolerant of 5V supply voltages to permit additional supply filtering.

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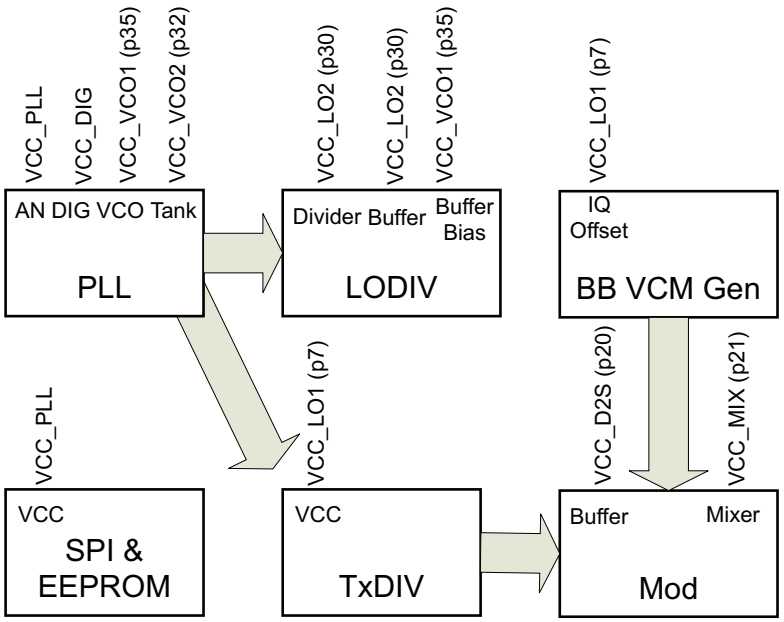

Figure 91. Power Supply Distribution

DAC INTERFACING WITH EXTERNAL BASEBAND BIAS VOLTAGE

Common mode voltage on the baseband inputs can be generated either internally or externally. An external interface should provide 1.7V dc and any necessary filtering. A typical interface to a DAC device is shown in Figure 92.

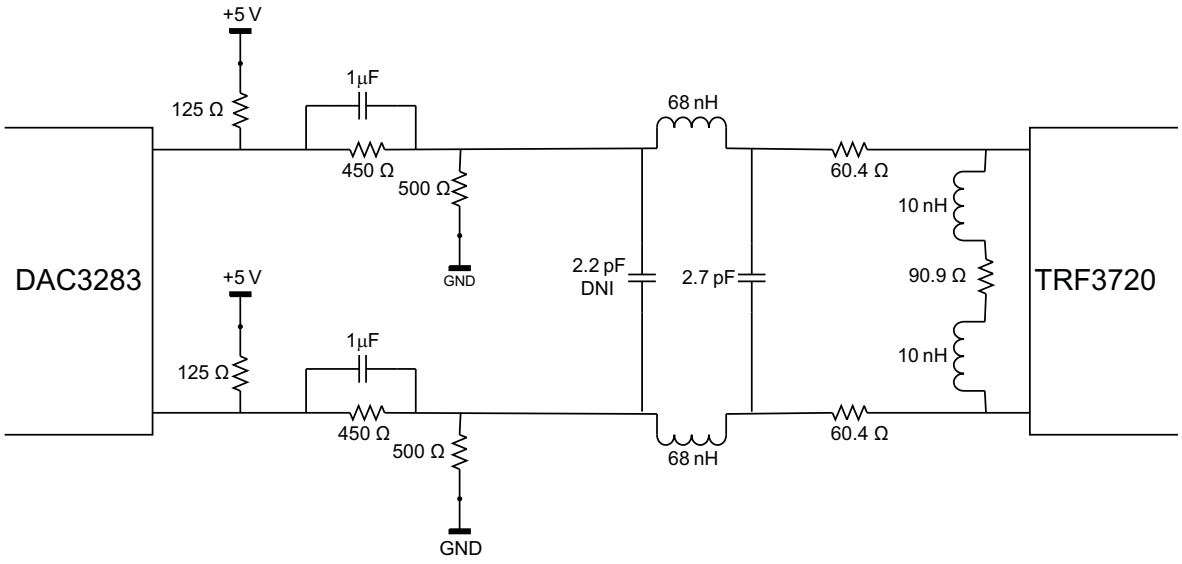

Figure 92. DAC to TRF372017 Interface With External VCM Generation

INTERNAL BASEBAND BIAS VOLTAGE GENERATION

The TRF372017 has the ability to generate DC voltage levels for its baseband inputs internally. Register settings in the device allow the user to adjust common mode voltage of the I and Q signals separately. There are three adjustment factors for the baseband inputs. These are described in Table 1.

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Table 11. Baseband Adjustment Factors

ADJUSTMENT	REGISTER BITS	BIT ADDRESSING
VCM setting	VREF_SEL_n	Register 6 Bits 23..21
VCM Enable	PWD_BB_VCM	Register 4 Bit 15
Bias select	IB_VCM_SEL	Register 7 Bit 25

Each baseband input pair includes the circuitry depicted in Figure 93. The Vref set voltage impacts all four terminals: IP, IN, QP, and QN. The effect of changing the reference voltage is shown in Figure 78. Each node also includes a programmable current DAC that injects current into the positive and negative terminals of each input.

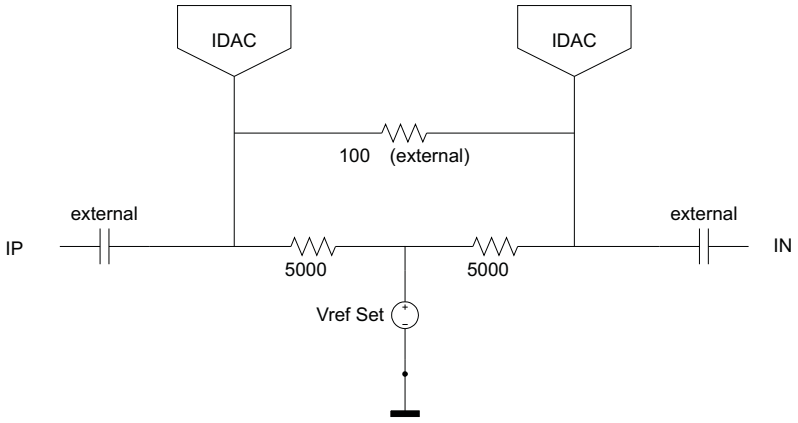

Figure 93. Block Diagram of the Baseband I Input Nodes

A typical DAC to TRF372017 interface using internal VCM generation is shown in Figure 94.

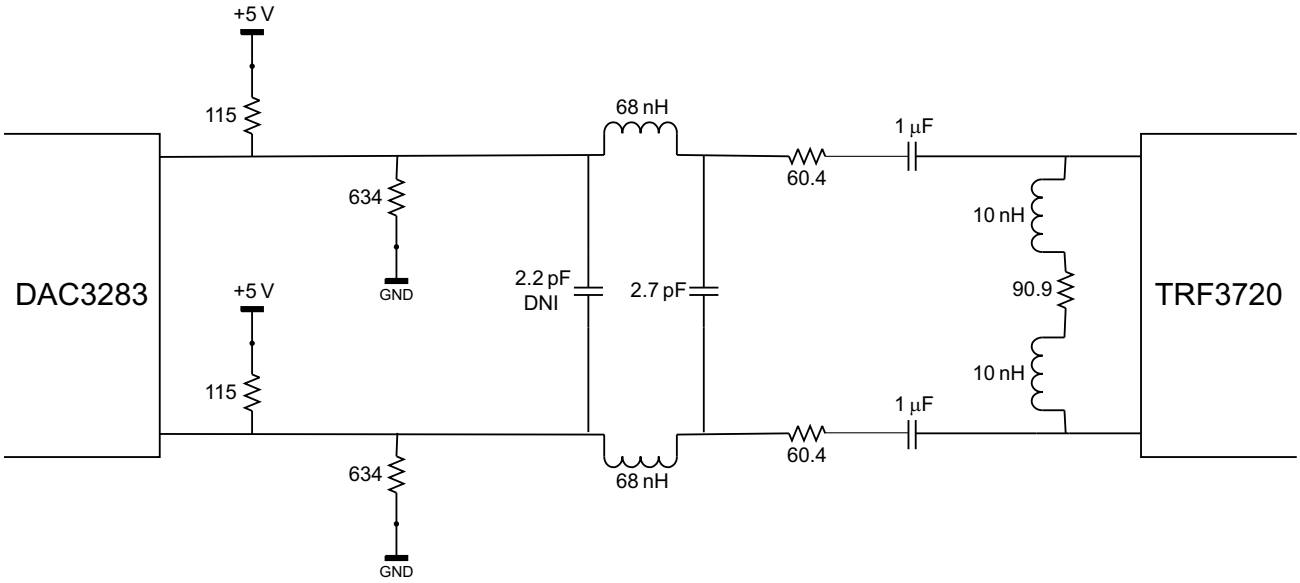

Figure 94. DAC to TRF372017 Interface With Internal VCM Generation

CARRIER FEEDTHROUGH CANCELLATION

The structure of the baseband current DAC is shown in Figure 95. For each input pair, there is a programmable reference current. The reference current for each pair (I and Q) is identical and is programmed through the same register bits, but the reference current source itself is duplicated in the device for both I and Q inputs. This current can be set to change the total current flowing into the P and N nodes, which in turn changes the offset programmability range.

The reference current is then mirrored and multiplied before getting injected into the input node. The total mirrored current will be routed into the two sides of the differential pair and routed according to eight programmable bits. As the 8 bit setting is changed, current is shifted from one side of the pair into the other side for each of the I and Q input pairs. In practical usage, the offset current routing distributes the adjustment for each side of the pair, while the reference current sets the range of adjustment. This effect can be seen in Figure 79, which shows that the gain of the current routing is greater when the reference current setting is higher. However the step size also increases with increase in range. Figure 79 shows the effect on common mode voltage of varying the DAC reference current. Adjustment register bits are shown in Table 12.

Offset adjustment may be provided by an external source, such as a DAC QMC block, for dc-coupled systems.

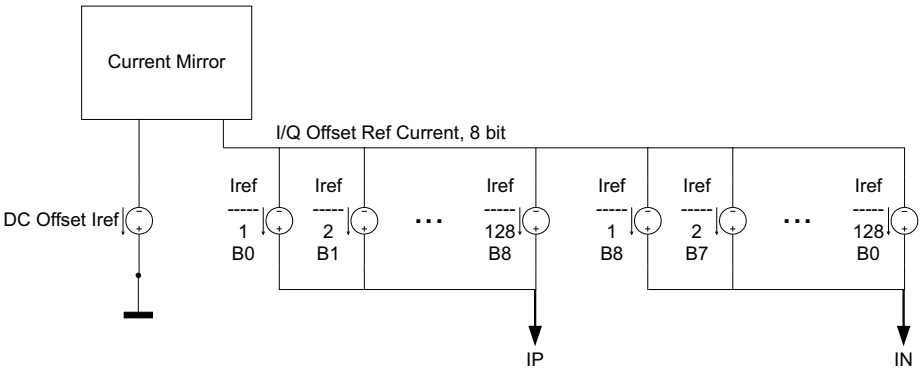

Figure 95. Block Diagram of the Programmable Current DAC

Table 12. Baseband Differential Offset Adjustment Factors

ADJUSTMENT	REGISTER BITS	BIT ADDRESS
I input differential offset programmability	I Offset Ref Curr	IOFF_n Register 6 Bits 12..5
Q input differential offset programmability	Q Offset Ref Curr	QOFF Register 6 Bits 20..13
Offset Programmability Range	DCoffset_I_n	Register 7 Bits 30..29

ESD SENSITIVITY

RF devices may be extremely sensitive to electrostatic discharge (ESD) (see ABSOLUTE MAXIMUM RATINGS table). To prevent damage from electrostatic discharge (ESD), devices should be stored and handled in a way that prevents the build up of electrostatic voltages that exceed the rated level. Rated electrostatic discharge (ESD) levels shall also not be exceeded while the device is installed on a PC board.

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APPLICATION SCHEMATIC

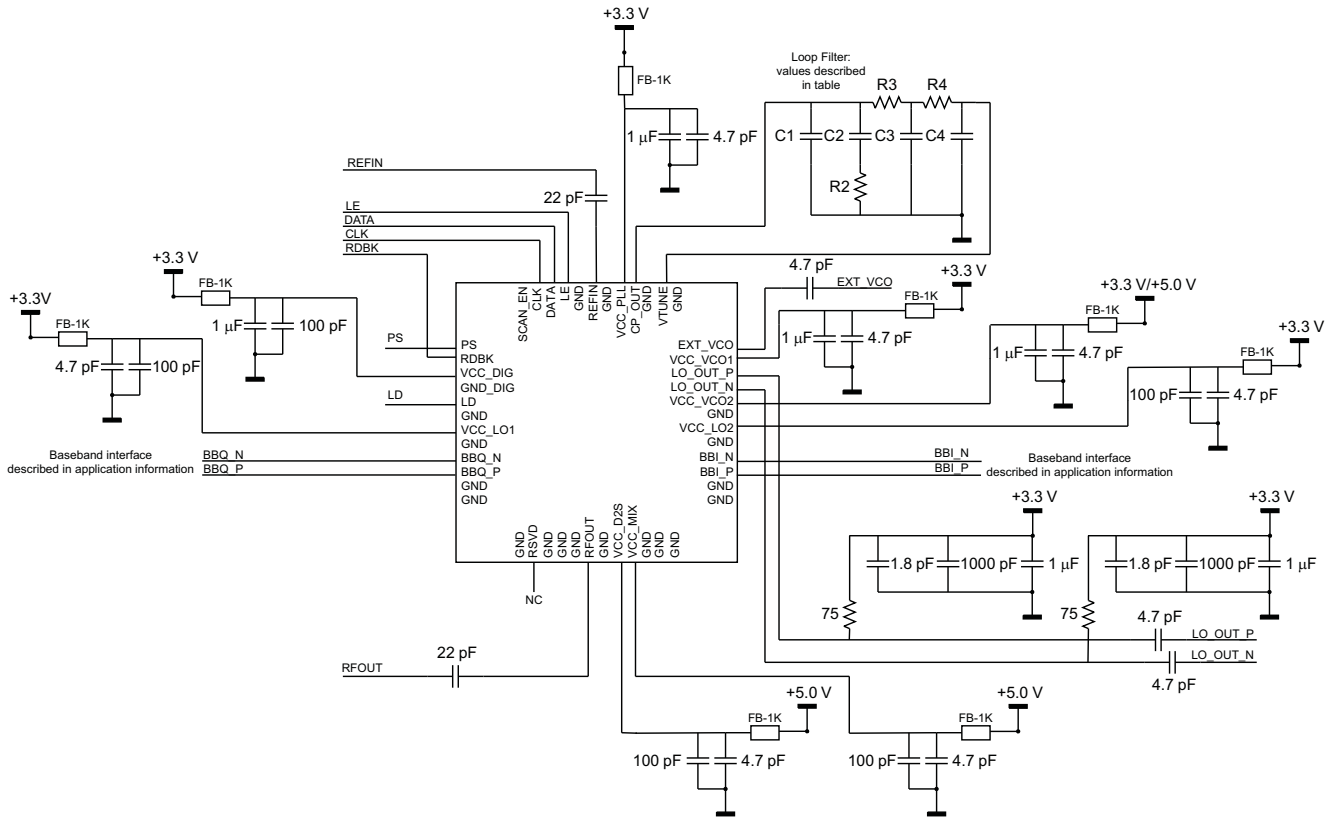

Figure 96. Application Schematic

Table 13. Pin Termination Requirements and Limitations

NAME	PIN NO	DESCRIPTION
RDBK	2	SPI Readback output. Digital output pins can source or sink up to 8mA of current.
LD	5	Lock detector digital output, as configured by MUX_CTRL. Digital output pins can source or sink up to 8mA of current.
BBQ_N	9	Base-band in-quadrature input: negative terminal. Internal 5kΩ to VCM generator. If VCM is internally generated (PWD_BB_VCM = 0), external AC coupling caps and 100Ω differential termination to BBQ_P is required.
BBQ_P	10	Base-band in-quadrature input: positive terminal. Internal 5KΩ to VCM generator. If VCM is internally generated (PWD_BB_VCM = 0), external AC coupling caps and 100Ω differential termination to BBQ_N is required.
RSVD	14	Reserved. Normally open.
RFOUT	18	RF output. Internally matched to 50Ω output. Normally AC coupled.
BBI_P	27	Base-band in-phase input: positive terminal. Internal 5kΩ to VCM generator. If VCM is internally generated (PWD_BB_VCM = 0), external AC coupling caps and 100Ω differential termination to BBI_N is required.
BBI_N	28	Base-band in-phase input: negative terminal. Internal 5kΩ to VCM generator. If VCM is internally generated (PWD_BB_VCM = 0), external AC coupling caps and 100Ω differential termination to BBI_P is required.
LO_OUT_N	33	Local oscillator output: negative terminal. Open collector output. A pull-up is required. Normally AC coupled.
LO_OUT_P	34	Local oscillator output: positive terminal. Open collector output. A pull-up is required. Normally AC coupled.
EXT_VCO	36	External local oscillator input. High impedance. Normally AC coupled.
REFIN	43	Reference clock input. High impedance. Normally AC coupled.
LE	45	SPI latch enable. Digital input. High impedance.
DATA	46	SPI data input. Digital input. High impedance.
CLK	47	SPI clock input. Digital input. High impedance.
SCAN_EN	48	Internal testing mode digital input. Connect to ground in normal operation.

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APPLICATION LAYOUT

Layout of the application board significantly impacts the analog performance of the TRF372017 device. Noise and high-speed signals should be prevented from leaking onto power-supply pins or analog signals. Follow these recommendations:

1. Place supply decoupling capacitors physically close to the device, on the same side of the board. Each supply pin should be isolated with a ferrite bead.
2. Maintain a continuous ground plane in the vicinity of the device and as return paths for all high-speed signal lines. Place reference plane vias or decoupling capacitors near any signal line reference transition.
3. The pad on the bottom of the device must be electrically grounded. Connect GND pins directly to the pad on the surface layer. Connect the GND pins and pad directly to surface ground where possible.
4. Power planes should not overlap each other or high-speed signal lines.
5. Isolate REF_IN routing from loop filter lines, control lines, and other high-speed lines.

See Figure 97 for an example of critical component layout (for the top PCB layer).

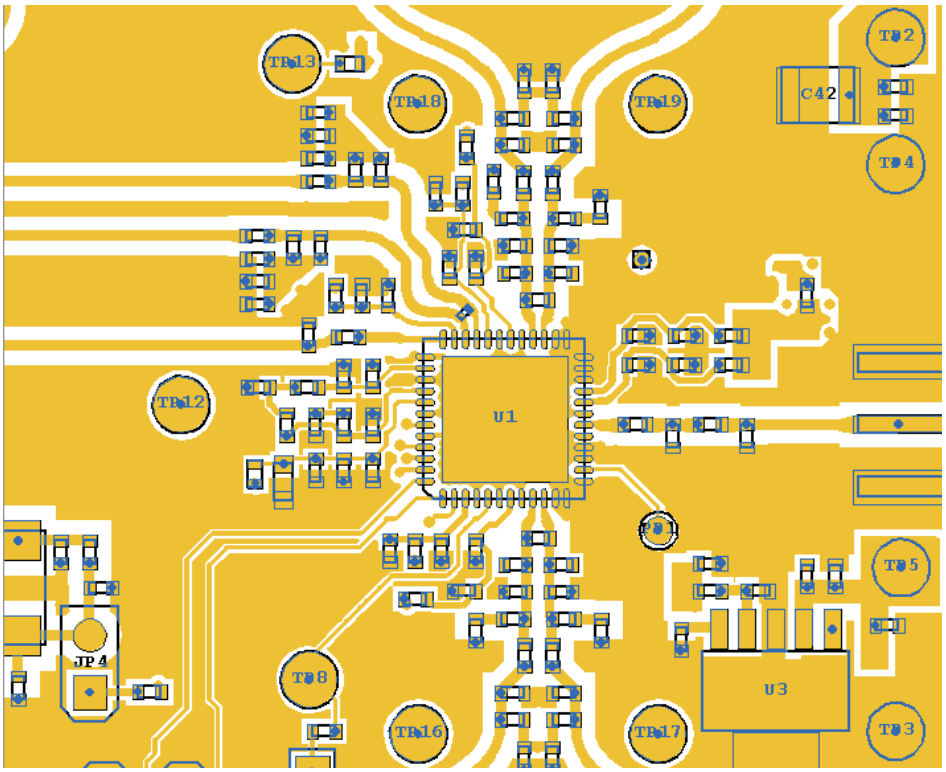

Figure 97. Critical Layout of the TRF372017 EVM Board

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REVISION HISTORY

Note: Page numbers of current version may differ from previous versions.

Changes from Revision A (August 2010) to Revision B — **Page**

- Deleted Comments column from Table 1 7
- Changed graphic entities in Figures 12 through Figure 27 10
- Changed column heading from "Default Value" to "Reset Value" in Register tables 1, 2, 3, 4, 5, 6 and 7 30
- Added "Recommended programming [xx]" to various **Description** statements in Register 2,5,6, and 7. 32
- Changed Register 4, Bit21/Bit22 Description statement from "Off" to "Normal" 34
- Changed Column heading from "Default Value to "Reset Value" in READBACK MODE section, Register 0 38
- Changed Column heading from "Default Value to "Reset Value" in READBACK MODE section, Register 0 39
- Changed Bit5 name from "CHIP_ID" to "CHIP_ID _0" and changed Bit6 name from "NU" to "CHIP_ID_1", Reset Value to 1 39
- Changed Bit5 name from "CHIP_ID" to "CHIP_ID _0" and changed Bit6 name from "NU" to "CHIP_ID_1", Reset Value to 1 40
- Changed the text under INTEGER and FRACTIONAL MODE SELECTION through sub section "Practical Limit on Maximum PFD Frequency" for clarification. 41
- Changed "RDIV = 20" to "RDIV = 2" in the **Setup Example for Fractional Mode** paragraph 44
- Changed EN_LD_ISOURCE Recommended Value from 1 to 0 in Table 3, ... 44
- Changed the graphic entity in Figure 94 for clarification. 51
- Changed the text in the APPLICATION LAYOUT section, and added crossreference to Figure 97 54

Changes from Revision B (March 2012) to Revision C — **Page**

- Added graph titles to Figure 56 and 57 that were missing in Rev B 22

Changes from Revision C (May 2012) to Revision D — **Page**

- Changed text string from "Reg 1, B[30..28] = [000]" to "Reg 0, B[30..28] = [000]" in the Description column associated with RB_REG<0>, RB_REG<1>, and RB_REG<2> 39

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF372017IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TRF372017 IRGZ	Samples
TRF372017IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TRF372017 IRGZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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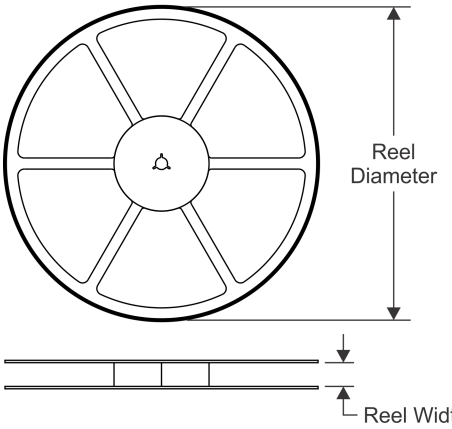
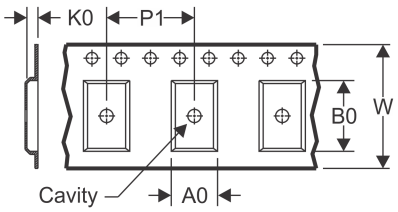
TAPE AND REEL INFORMATION

REEL DIMENSIONS

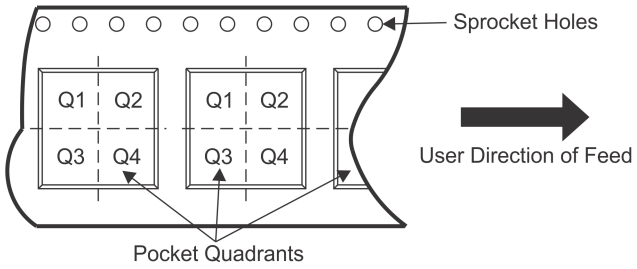


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

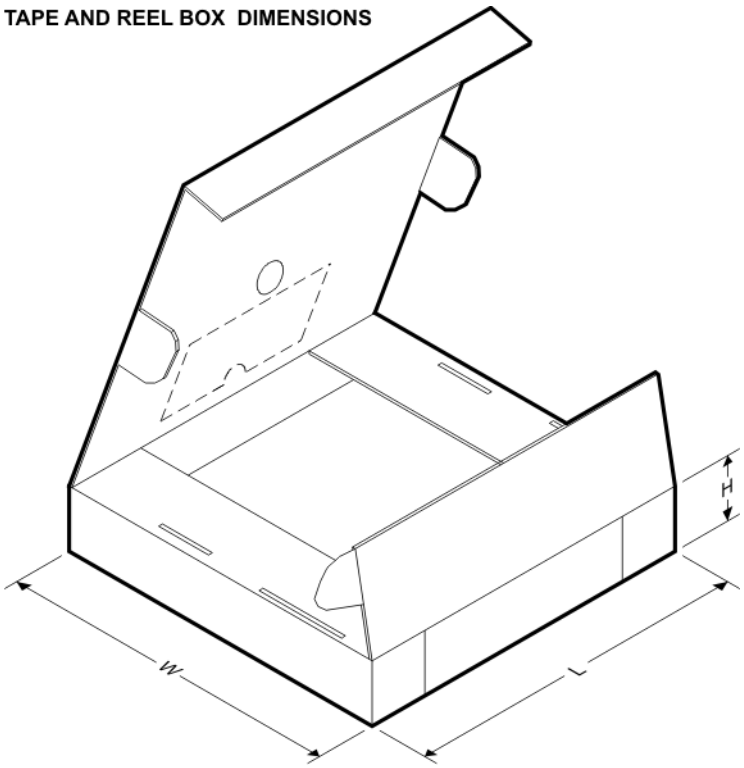
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF372017IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TRF372017IRGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

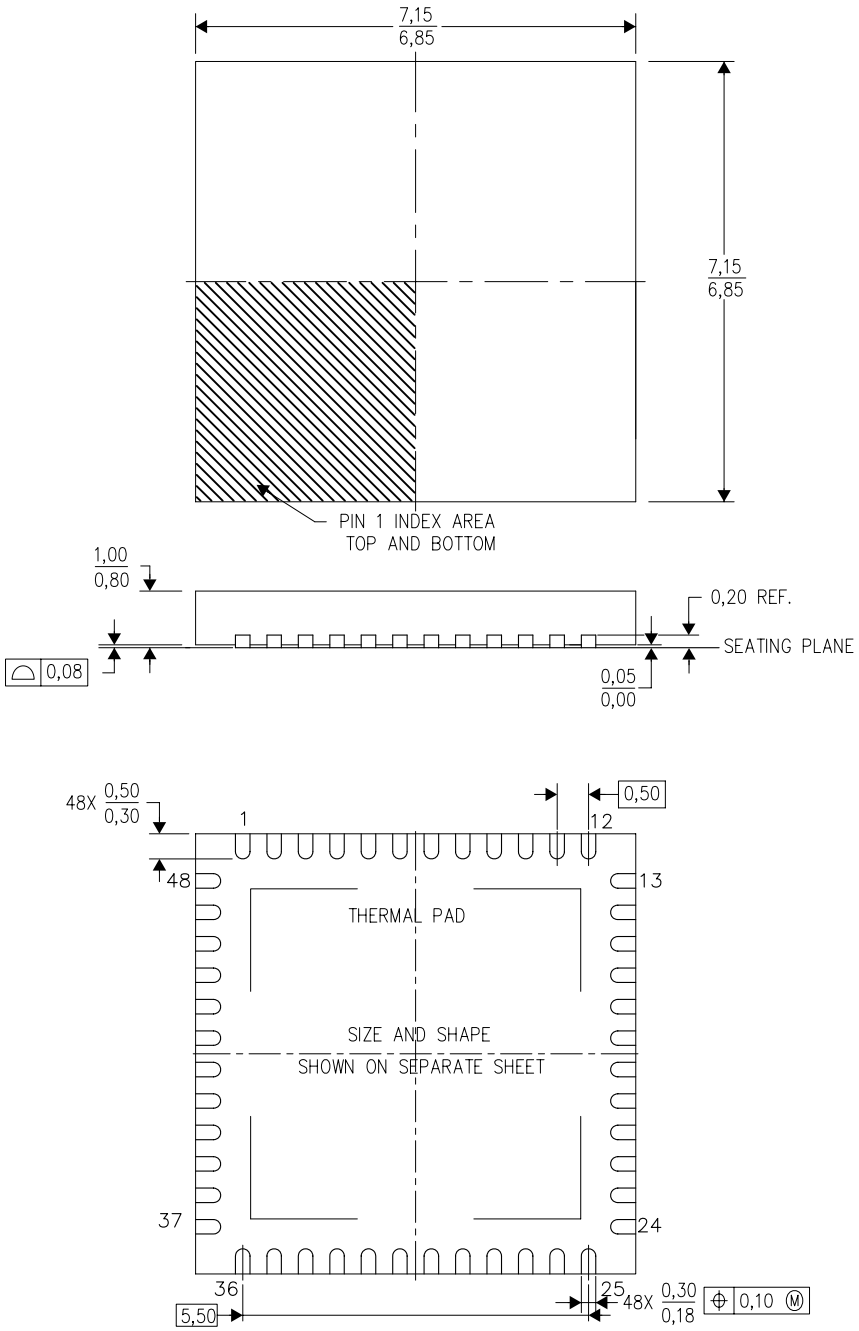
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF372017IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
TRF372017IRGZT	VQFN	RGZ	48	250	336.6	336.6	28.6

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

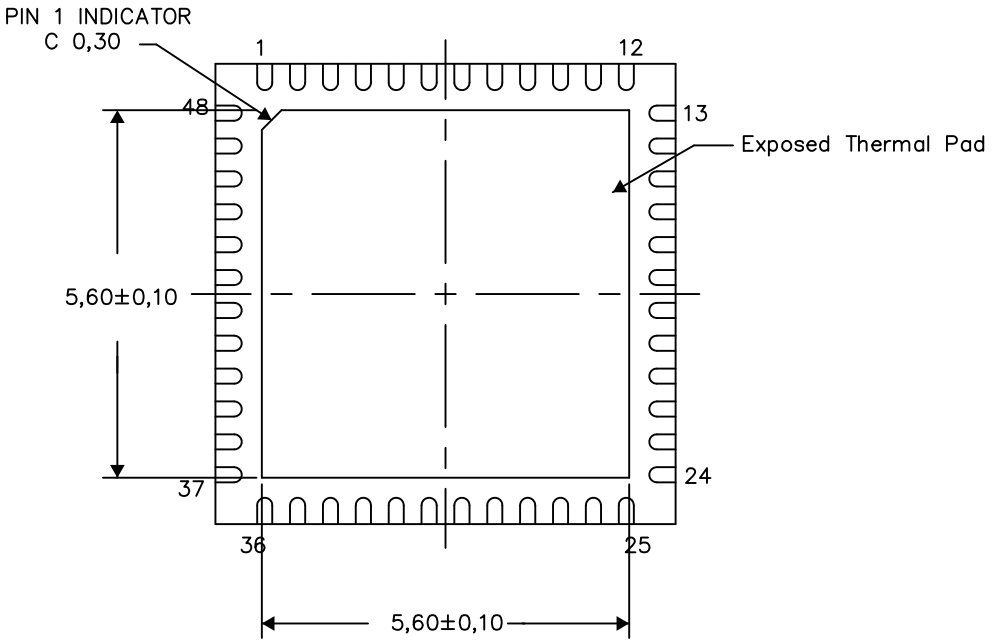
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



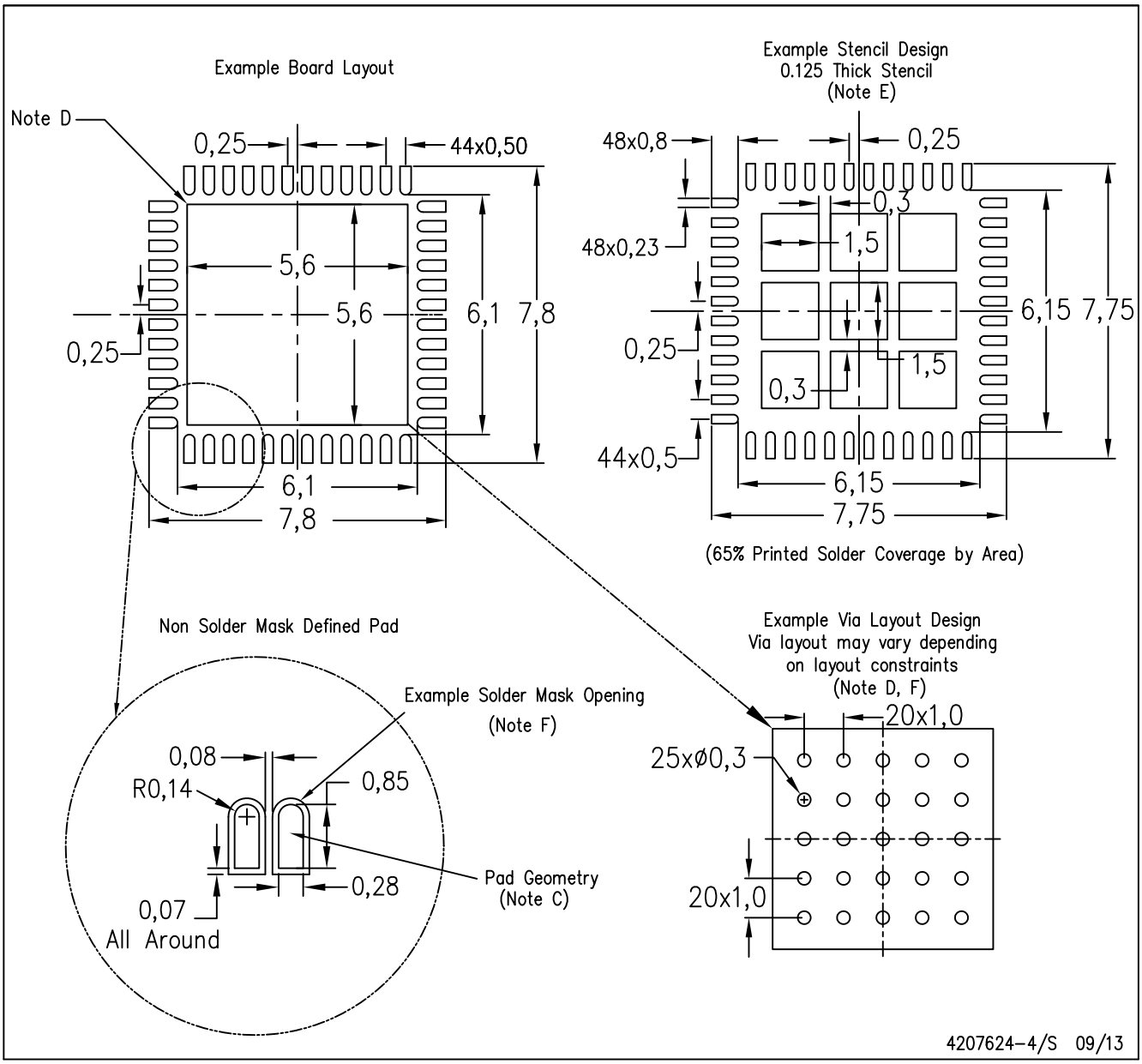
Bottom View

Exposed Thermal Pad Dimensions

4206354–5/W 09/13

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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