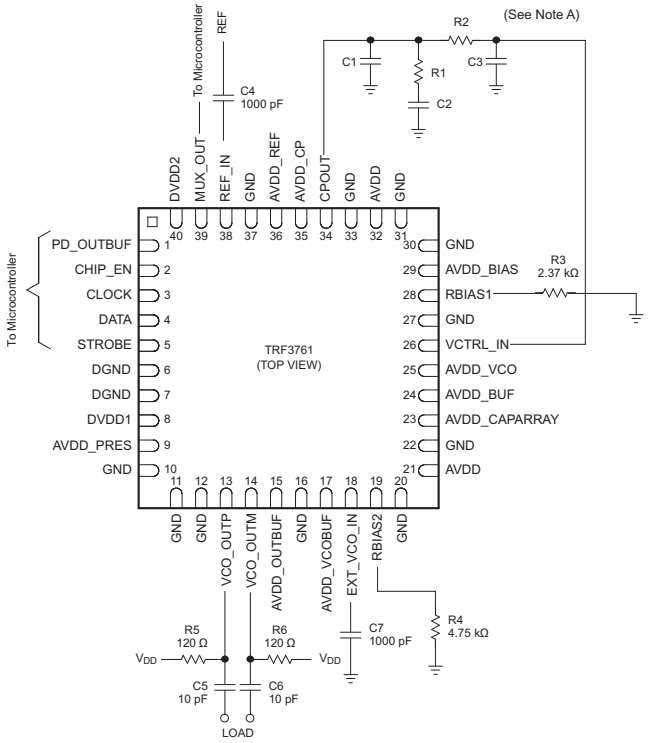
INTEGER-N PLL WITH INTEGRATED VCO

FEATURES

- Fully Integrated VCO
- Low Phase Noise: –137dBc/Hz (at 600kHz, f_{VCO} of 1.9GHz)
- Low Noise Floor: –158dBc/Hz at 10MHz Offset
- Integer-N PLL
- Input Reference Frequency range: 10MHz to 104MHz
- VCO Frequency Divided by 2-4 Output
- Output Buffer Enable Pin
- Programmable Charge Pump Current
- Hardware and Software Power Down
- 3-Wire Serial Interface
- Single Supply: 4.5V to 5.25V Operation

APPLICATIONS

- Wireless Infrastructure
  - WCDMA, CDMA, GSM
  - Wideband Transceivers
  - Wireless Local Loop
  - RFID Transceivers
  - Clock generation
  - IF LO generation



A. See the Application Information section for Loop Filter Design procedures.

AVAILABLE DEVICE OPTIONS

PART NUMBER	Div by 1		Div by 2		Div by 4	
	Fstart	Fstop	Fstart	Fstop	Fstart	Fstop
TRF3761-A	1493	1608	746.5	804	373.25	402
TRF3761-B	1595	1711	797.5	855.5	398.75	427.75
TRF3761-C	1660	1790	830	895	415	447.5
TRF3761-D	1740	1866	870	933	435	466.5
TRF3761-E	1805	1936	902.5	968	451.25	484
TRF3761-F	1850	1984	925	992	462.5	496
TRF3761-G	1920	2059	960	1029.5	480	514.75
TRF3761-H	2028	2175	1014	1087.5	507	543.75
TRF3761-J	2140	2295	1070	1147.5	535	573.75

DESCRIPTION

TRF3761 is a family of high performance, highly integrated frequency synthesizers, optimized for high performance applications. The TRF3761 includes a low-noise, voltage-controlled oscillator (VCO) and an integer-N PLL.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION CONTINUED

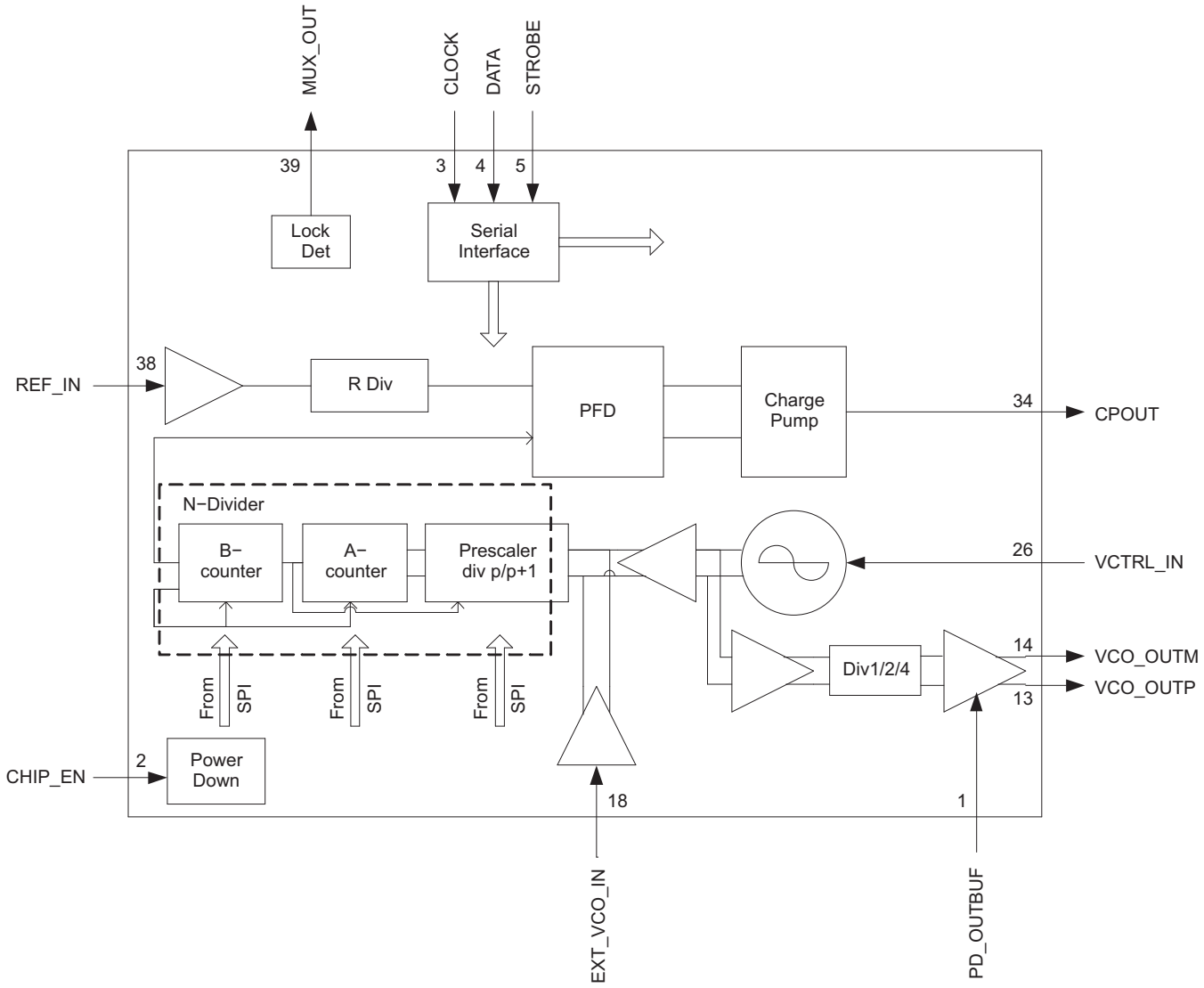
TRF3761 integrates divide-by 1, 2, or 4 options for a more flexible output frequency range. It is controlled through a 3-wire serial-programming-interface (SPI) interface. For power sensitive applications the TRF3761 can be powered down by the SPI interface or externally via chip_en pin 2.

PACKAGE/ORDERING INFORMATION(1)

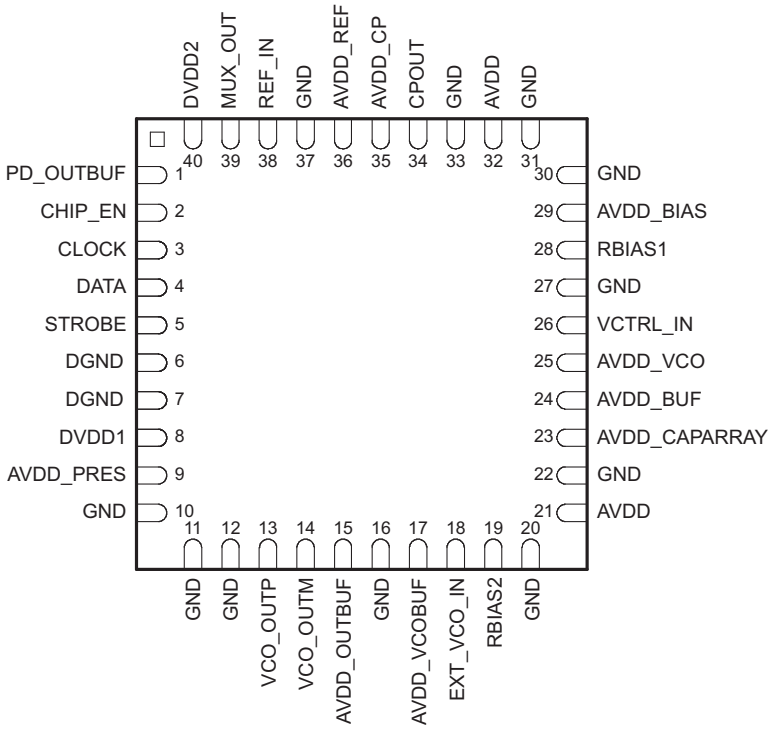
PRODUCT	PACKAGE LEAD	PACKAGE DESIGNATOR(2)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKINGS	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TRF3761-A	QFN-40	RHA	–40°C to 85°C	TRF3761-A	TRF3761-AIRHAR	Tape and Reel, 2500
					TRF3761-AIRHAT	Tape and Reel, 250
TRF3761-B	QFN-40	RHA	–40°C to 85°C	TRF3761-B	TRF3761-BIRHAR	Tape and Reel, 2500
					TRF3761-BIRHAT	Tape and Reel, 250
TRF3761-C	QFN-40	RHA	–40°C to 85°C	TRF3761-C	TRF3761-CIRHAR	Tape and Reel, 2500
					TRF3761-CIRHAT	Tape and Reel, 250
TRF3761-D	QFN-40	RHA	-40°C to 85°C	TRF3761-D	TRF3761-DIRHAR	Tape and Reel, 2500
					TRF3761-DIRHAT	Tape and Reel, 250
TRF3761-E	QFN-40	RHA	–40°C to 85°C	TRF3761-E	TRF3761-EIRHAR	Tape and Reel, 2500
					TRF3761-EIRHAT	Tape and Reel, 250
TRF3761-F	QFN-40	RHA	–40°C to 85°C	TRF3761-F	TRF3761-FIRHAR	Tape and Reel, 2500
					TRF3761-FIRHAT	Tape and Reel, 250
TRF3761-G	QFN-40	RHA	–40°C to 85°C	TRF3761-G	TRF3761-GIRHAR	Tape and Reel, 2500
					TRF3761-GIRHAT	Tape and Reel, 250
TRF3761-H	QFN-40	RHA	–40°C to 85°C	TRF3761-H	TRF3761-HIRHAR	Tape and Reel, 2500
					TRF3761-HIRHAT	Tape and Reel, 250
TRF3761-J	QFN-40	RHA	–40°C to 85°C	TRF3761-J	TRF3761-JIRHAR	Tape and Reel, 2500
					TRF3761-JIRHAT	Tape and Reel, 250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Thermal pad size: 177 × 177 mils.

Functional Block Diagram



RHA PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL (1)		I/O	DESCRIPTION
NAME	NO.		
PD_OUTBUF	1	I	Once configured in register 1, this pin will control the output buffer. Logic level 0 turns on the buffer and logic level 1 turns off the buffer.
CHIP_EN	2	I	This pin requires 4.5 to 5.25v applied for normal operation. Grounding this pin will disable the chip.
CLOCK	3	I	Serial-programming-interface clock
DATA	4	I/O	Serial-programming-interface data, used for programming the frequency and other features.
STROBE	5	I	Serial-programming-interface strobe required to write the data to the chip
DGND	6, 7		Digital ground
DVDD1	8		Digital power supply, requires 4.5 to 5.25 V, Suggested decoupling, 0.1uF and 10pF capacitors in parallel.
AVDD_PRES	9		Power supply for prescaler circuit, requires 4.5 to 5.25 V, Suggested decoupling, 0.1uF and 10pF capacitors in parallel.
VCO_OUTP	13	O	VCO output, can be used single ended matched to 50 ohms or in conjuction with VCO_OUTM (pin 14) with a balun.
VCO_OUTM	14	O	VCO output, can be used single ended matched to 50 ohms or in conjunction with VCO_OUTP (pin 13) with a balun.
AVDD_OUTBUF	15		Power supply for output buffers, requires 4.5 to 5.25 V, Suggested decoupling, 0.1µF and 10pF capacitors in parallel.
AVDD_VCOBUF	17		Power supply for VCO buffers, requires 4.5 to 5.25 V, Suggested decoupling, 0.1µF and 10pF capacitors in parallel.
EXT_VCO_IN	18	I	External VCO input to prescaler, If using an external VCO instead of the internal VCO.

(1) Power Supply=V_{CC}=(DVDD1, AVDD1, AVDD_PRES, AVDD_VCOBUF, AVDD, AVDD_CAPARRAY, AVDD_BUF, AVDD_VCO, AVDD_BIAS, AVDD_CP, AVDD_REF, DVDD2)

TERMINAL FUNCTIONS (continued)

TERMINAL[1]		I/O	DESCRIPTION
NAME	NO.		
RBIAS2	19	I/O	External bias resistor for setting the internal reference current requires a 4.75K ohm resister to ground.
AVDD	21		Analog power supply, requires 4.5 to 5.25 V, Suggested decoupling, 0.1uF and 10µF capacitors in parallel.
AVDD_CAPARRAY	23		Power supply for VCO core and buffer, requires 4.5 to 5.25 V, Suggested decoupling, 0.1µF and 10pF capacitors in parallel.
AVDD_BUF	24		Power supply for VCO core and buffer, requires 4.5 to 5.25 V, Suggested decoupling, 0.1µF and 10pF capacitors in parallel.
AVDD_VCO	25		Power supply for VCO core and buffer, requires 4.5 to 5.25 V, Suggested decoupling, 0.1uF and 10pF capacitors in parallel.
VCTRL_IN	26	I	VCO control voltage, the output of the loop filter is applied to this pin.
RBIAS1	28	I/O	External bias resistor for setting charge pump reference current, requires 2.37K ohm resistor to ground.
AVDD_BIAS	29		Power supply for band gap current bias, requires 4.5 to 5.25 V, Suggested decoupling, 0.1µF and 10pF capacitors in parallel.
GND	10, 11, 12, 16, 20, 22, 27, 30, 31, 33, 37		Analog ground
AVDD	32		Power supply for FUSE cell, requires 4.5 to 5.25V. Suggested decoupling, 0.1µF, 1nF and 1pF capacitors in parallel.
CPOUT	34	O	Charge pump output, connected to the input of loop filter.
AVDD_CP	35		Analog power supply for charge pump, requires 4.5 to 5.25 V, Suggested decoupling, 0.1µF and 10pF capacitors in parallel
AVDD_REF	36		Power supply for REF_IN circuitry, requires 4.5 to 5.25 V, Suggested decoupling, 0.1µF and 10pF capacitors in parallel.
REF_IN	38	I	Reference signal input, reference oscillator input of 10MHz to 104MHz.
MUX_OUT	39	O	Generally used for digital lock detect, can be used to verify locked condition by microcontroller, high = locked, low = unlocked.
DVDD2	40		Power supply for the digital regulator, requires 4.5 to 5.25 V, Suggested decoupling, 0.1µF and 10pF capacitors in parallel.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER[1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Thermal derating, junction-to-ambient	Soldered slug, no airflow		26		°C/W
		Soldered slug, 200-LFM airflow		20.1		°C/W
		Soldered slug, 400-LFM airflow		17.4		°C/W

(1) Determined using JEDEC standard JESD-51 with High K board

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)[1]

		VALUE	UNIT
	Supply voltage range[2]	–0.3 to 5.5	V
	Digital I/O voltage range	–0.3 to V_{CC} +0.3	V
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power supply voltage	4.5	5	5.25	V
	Power supply voltage ripple			940	μV_{pp}
T_A	Operating free air temperature range	–40		85	°C
T_J	Operating virtual junction temperature range	–40		150	°C

ELECTRICAL CHARACTERISTICS

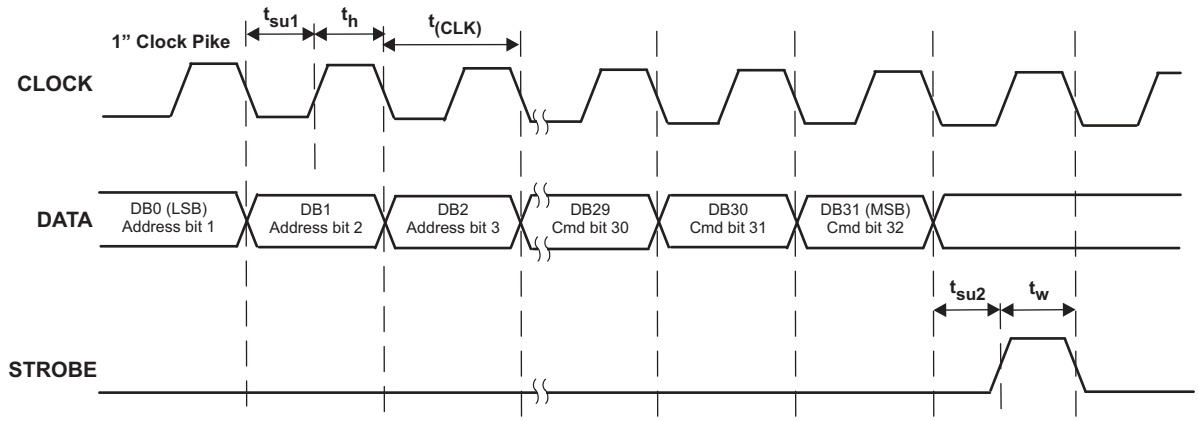
Supply voltage = V_{CC} = 4.5V to 5.25V, T_A = –40 to 85 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC Parameters							
I_{CC}	Total supply current	T_A = 25°C	Divide by 1 output		130		mA
			Divide by 2 output		140		mA
			Divide by 4 output		150		mA
Reference Oscillator Parameters							
f_{ref}	Reference frequency			10		104	MHz
	Reference input sensitivity (REF_IN)			0.2		2.5	V_{PP}
	Reference input impedance (REF_IN)	Parallel capacitance			5	6.52	pF
		Parallel resistance		3913			Ω
PFD Charge Pump							
	PFD frequency					30	MHz
	Charge pump current (I_{CP_OUT})	SPI programmable			5.6		mA
Digital Interface (PD_OUTBUF, CHIP_EN, CLOCK, DATA, STROBE)							
V_{IH}	High-level input voltage			2.5		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.8	V
V_{OH}	High-level output voltage			$0.8V_{CC}$			V
V_{OL}	Low-level output voltage					$0.2V_{CC}$	V
Output Power							
	Single ended				0		dBm
	Differential				3		dBm

TIMING REQUIREMENTS

Supply voltage = V_{CC} = 4.5V to 5.25V, T_A = –40 to 85 °C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CLK)}$	Clock period		50			ns
t_{su1}	Setup time, data		10			ns
t_h	Hold time, data		10			ns
t_w	Pulse width, STROBE		20			ns
t_{su2}	Setup time, STROBE		10			ns



A. The first 4 bits, DB(3-0), of data are Address bits. The 28 remaining bits, DB(31-4), are part of the command. The command is little endian or lower bits first.

Figure 1. Serial Programming Timing Diagram

TRF3761-A ELECTRICAL CHARACTERISTICS

Supply voltage = V_{CC} = 5V, T_A = –40 to 85 °C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 1554MHz, f_O = 1554MHz	100kHz offset		–116.7		dBc/Hz
		600kHz offset		–136		
		1MHz offset		-141.6		
		6MHz offset		–156.1		
		10MHz offset		-158.1		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 1554MHz, f_O = 777 MHz	100kHz offset		-122.8		dBc/Hz
		600kHz offset		–142.7		
		1MHz offset		–147.5		
		6MHz offset		–157		
		10MHz offset		–158.1		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 1554MHz, f_O = 388.5 MHz	100kHz offset		–127.7		dBc/Hz
		600kHz offset		-148.4		
		1MHz offset		-151.8		
		6MHz offset		–156.3		
		10MHz offset		–155.9		
VCO phase noise, Closed loop phase noise direct output(1)(2)(3)	f_{VCO} = 1554MHz, f_O = 1554MHz	1kHz offset		–83.4		dBc/Hz
		600kHz offset		–135		
		1MHz offset		–140.2		
		10MHz offset		–158.2		
RMS phase error Closed loop phase noise direct output(3)	100Hz to 10MHz			0.95°		
VCO phase noise, Closed loop phase noise divide-by-2 output(4)(2)(3)	f_{VCO} = 1554MHz, f_O = 777 MHz	1kHz offset		–90.4		dBc/Hz
		600kHz offset		–141		
		1MHz offset		–146.2		
		10MHz offset		–158.25		
RMS phase error Closed loop phase noise divide-by-2 output(3)	100Hz to 10MHz			0.63°		
VCO phase noise, Closed loop phase noise divide-by-4 output(1)(2)(3)	f_{VCO} = 1554MHz, f_O = 388.5 MHz	1kHz offset		-95.0		dBc/Hz
		600kHz offset		–147		
		1MHz offset		–151		
		10MHz offset		–156		
RMS phase error Closed loop phase noise divide-by-4 output(3)	100Hz to 10MHz			0.39°		
VCO gain, Kv	VCO free running			23		MHz/V
Reference spur(2)				–80		dBc

(1) See Application Circuit Figure 87.
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.
(4) See Application Circuit Figure 87.

TRF3761-B ELECTRICAL CHARACTERISTICS

Supply voltage = V_{CC} = 5V, T_A = –40 to 85 °C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 1651MHz, f_O = 1651MHz	100kHz offset		–119.34		dBc/Hz
		600kHz offset		–139		
		1MHz offset		-142.1		
		6MHz offset		–156.6		
		10MHz offset		-158.6		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 1651MHz, f_O = 825.5 MHz	100kHz offset		-127.8		dBc/Hz
		600kHz offset		–146.5		
		1MHz offset		–149		
		6MHz offset		–156.2		
		10MHz offset		–158.4		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 1651MHz, f_O = 412.75 MHz	100kHz offset		–127.3		dBc/Hz
		600kHz offset		-151.4		
		1MHz offset		-153		
		6MHz offset		–155.5		
		10MHz offset		–155.9		
VCO phase noise, Closed loop phase noise direct output(1)(2)(3)	f_{VCO} = 1651MHz, f_O = 1651MHz	1kHz offset		–83.5		dBc/Hz
		600kHz offset		–138		
		1MHz offset		–141.8		
		10MHz offset		–158.2		
RMS phase error Closed loop phase noise direct output(3)	100Hz to 10MHz			0.85°		
VCO phase noise, Closed loop phase noise divide-by-2 output(1)(2)(3)	f_{VCO} = 1651MHz, f_O = 825.5 MHz	1kHz offset		–90.2		dBc/Hz
		600kHz offset		–146		
		1MHz offset		–147.39		
		10MHz offset		–158.25		
RMS phase error Closed loop phase noise divide-by-2 output(3)	100Hz to 10MHz			0.53°		
VCO phase noise, Closed loop phase noise divide-by-4 output(1)(2)(3)	f_{VCO} = 1651MHz, f_O = 412.75 MHz	1kHz offset		-95.7		dBc/Hz
		600kHz offset		–151		
		1MHz offset		–154		
		10MHz offset		–156		
RMS phase error Closed loop phase noise divide-by-4 output(3)	100Hz to 10MHz			0.33°		
VCO gain, Kv	VCO free running			23		MHz/V
Reference spur(2)				–80		dBc

(1) See Application Circuit Figure 87.
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.

TRF3761-C ELECTRICAL CHARACTERISTICS

Supply voltage = V_{CC} = 5V, T_A = –40 to 85 °C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 1723MHz, f_O = 1700MHz	100kHz offset		–119.5		dBc/Hz
		600kHz offset		–138.8		
		1MHz offset		-143.9		
		6MHz offset		–155.3		
		10MHz offset		–157.5		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 1723MHz, f_O = 861.5 MHz	100kHz offset		–126		dBc/Hz
		600kHz offset		–145.2		
		1MHz offset		–149.5		
		6MHz offset		–157.2		
		10MHz offset		–158		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 1723MHz, f_O = 430.75 MHz	100kHz offset		–133		dBc/Hz
		600kHz offset		-151		
		1MHz offset		-153.8		
		6MHz offset		–156		
		10MHz offset		–156.5		
VCO phase noise, Closed loop phase noise direct output(1)(2)(3)	f_{VCO} = 1723MHz, f_O = 1723MHz,	1kHz offset		–85		dBc/Hz
		600kHz offset		–138.34		
		1MHz offset		–142.68		
		10MHz offset		–157.3		
RMS phase error Closed loop phase noise direct output(3)	100Hz to 10MHz			0.87°		
VCO phase noise, Closed loop phase noise divide-by-2 output(1)(2)(3)	f_{VCO} = 1723MHz, f_O = 861.5 MHz	1kHz offset		–90.1		dBc/Hz
		600kHz offset		–145		
		1MHz offset		–148.6		
		10MHz offset		–158		
RMS phase error Closed loop phase noise divide-by-2 output(3)	100Hz to 10MHz			0.53°		
VCO phase noise, Closed loop phase noise divide-by-4 output(1)(2)(3)	f_{VCO} = 1723MHz, f_O = 430.75 MHz	1kHz offset		–96.2		dBc/Hz
		600kHz offset		–151		
		1MHz offset		–153		
		10MHz offset		–156		
RMS phase error Closed loop phase noise divide-by-4 output(3)	100Hz to 10MHz			0.33°		
VCO gain, Kv	VCO free running			23		MHz/V
Reference spur(2)				–80		dBc

(1) See Application Circuit Figure 87.
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.

TRF3761-D ELECTRICAL CHARACTERISTICS

Supply voltage = V_{CC} = 5V, T_A = –40 to 85 °C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 1817MHz, f_O = 1817MHz	100kHz offset		–118		dBc/Hz
		600kHz offset		–138.5		
		1MHz offset		-144		
		6MHz offset		–156		
		10MHz offset		–158		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 1817MHz, f_O = 908.5MHz	100kHz offset		–124.8		dBc/Hz
		600kHz offset		–145.2		
		1MHz offset		–148		
		6MHz offset		–157.8		
		10MHz offset		–158.2		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 1817MHz, f_O = 454.25MHz	100kHz offset		–132		dBc/Hz
		600kHz offset		-151		
		1MHz offset		-154		
		6MHz offset		–157		
		10MHz offset		–157.5		
VCO phase noise, Closed loop phase noise direct output(1)(2)(1)	f_{VCO} = 1817MHz, f_O = 1817MHz	1kHz offset		–85		dBc/Hz
		600kHz offset		–139		
		1MHz offset		–144		
		10MHz offset		–159		
RMS phase error Closed loop phase noise direct output(3)	100Hz to 10MHz			0.85°		
VCO phase noise, Closed loop phase noise divide-by-2 output(1)(2)(3)	f_{VCO} = 1817MHz, f_O = 908.5MHz	1kHz offset		–91		dBc/Hz
		600kHz offset		–146		
		1MHz offset		–149		
		10MHz offset		–159		
RMS phase error Closed loop phase noise divide-by-2 output(3)	100Hz to 10MHz			0.47°		
VCO phase noise, Closed loop phase noise divide-by-4 output(1)(2)(3)	f_{VCO} = 1817MHz, f_O = 454.25MHz	1kHz offset		–97		dBc/Hz
		600kHz offset		–151		
		1MHz offset		–154		
		10MHz offset		–157		
RMS phase error Closed loop phase noise divide-by-4 output(3)	100Hz to 10MHz			0.34°		
VCO gain, Kv	VCO free running			23		MHz/V
Reference spur(2)				–80		dBc

(1) See Application Circuit Figure 87.
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.

TRF3761-E ELECTRICAL CHARACTERISTICS

Supply voltage = V_{CC} = 5V, T_A = –40 to 85 °C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 1869MHz, f_O = 1869MHz	100kHz offset		–118		dBc/Hz
		600kHz offset		–138		
		1MHz offset		–142		
		6MHz offset		–155		
		10MHz offset		–157.3		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 1869MHz, f_O = 934.5MHz	100kHz offset		–126		dBc/Hz
		600kHz offset		–144		
		1MHz offset		–149		
		6MHz offset		–158		
		10MHz offset		–158.2		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 1869MHz, f_O = 467.25MHz	100kHz offset		–132		dBc/Hz
		600kHz offset		–150		
		1MHz offset		–154		
		6MHz offset		-157		
		10MHz offset		–157.3		
VCO phase noise, Closed loop phase noise direct output(1)(2)(3)	f_{VCO} = 1869MHz, f_O = 1869MHz	1kHz offset		–84.5		dBc/Hz
		600kHz offset		–140		
		1MHz offset		–143.6		
		10MHz offset		–157		
RMS phase error Closed loop phase noise direct output(3)	100Hz to 10MHz			0.9°		
VCO phase noise, Closed loop phase noise divide-by-2 output(1)(2)(3)	f_{VCO} = 1869MHz, f_O = 934.5MHz	1kHz offset		–90.7		dBc/Hz
		600kHz offset		–144		
		1MHz offset		–148.5		
		10MHz offset		–158		
RMS phase error Closed loop phase noise divide-by-2 output(3)	100Hz to 10MHz			0.53°		
VCO phase noise, Closed loop phase noise divide-by-4 output(1)(2)(3)	f_{VCO} = 1869MHz, f_O = 467.25MHz	1kHz offset		–95		dBc/Hz
		600kHz offset		–150		
		1MHz offset		–154		
		10MHz offset		–157		
RMS phase error Closed loop phase noise divide-by-4 output(3)	100Hz to 10MHz			0.35°		
VCO gain, Kv	VCO free running			23		MHz/V
Reference spur(2)				–80		dBc

(1) See Application Circuit Figure 87.
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.

TRF3761-F ELECTRICAL CHARACTERISTICS

Supply voltage = V_{CC} = 5V, T_A = –40 to 85 °C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 1916MHz, f_O = 1916MHz	100kHz offset		-116		dBc/Hz
		600kHz offset		-137		
		1MHz offset		-141		
		6MHz offset		-155		
		10MHz offset		-157		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 1916MHz, f_O = 958MHz	100kHz offset		-113		dBc/Hz
		600kHz offset		-136		
		1MHz offset		-147.5		
		6MHz offset		-155		
		10MHz offset		-157.5		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 1916MHz, f_O = 479MHz	100kHz offset		-128		dBc/Hz
		600kHz offset		-148		
		1MHz offset		-150		
		6MHz offset		-155		
		10MHz offset		-156		
VCO phase noise, Closed loop phase noise direct output(1)(2)(3)	f_{VCO} = 1916MHz, f_O = 1916MHz	1kHz offset		-82.5		dBc/Hz
		600kHz offset		-136.7		
		1MHz offset		-142		
		10MHz offset		-157		
RMS phase error Closed loop phase noise direct output(3)	100Hz to 10MHz			0.947°		
VCO phase noise, Closed loop phase noise divide-by-2 output(1)(2)(3)	f_{VCO} = 1916MHz, f_O = 958MHz	1kHz offset		-88.6		dBc/Hz
		600kHz offset		-142.6		
		1MHz offset		-148.2		
		10MHz offset		-158		
RMS phase error Closed loop phase noise divide-by-2 output(3)	100Hz to 10MHz			0.477°		
VCO phase noise, Closed loop phase noise divide-by-4 output(1)(2)(3)	f_{VCO} = 1916MHz, f_O = 479MHz	1kHz offset		-95		dBc/Hz
		600kHz offset		-148		
		1MHz offset		-152		
		10MHz offset		-156		
RMS phase error Closed loop phase noise divide-by-4 output(3)	100Hz to 10MHz			0.231°		
VCO gain, Kv	VCO free running			23		MHz/V
Reference spur(2)				–80		dBc

(1) See Application Circuit Figure 87.
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.

TRF3761-G ELECTRICAL CHARACTERISTICS

Supply voltage = V_{CC} = 5V, T_A = –40 to 85 °C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 1989MHz, f_O = 1989MHz	100kHz offset		-115		dBc/Hz
		600kHz offset		-136		
		1MHz offset		-141.2		
		6MHz offset		-155.6		
		10MHz offset		-159		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 1989MHz, f_O = 994.5MHz	100kHz offset		-121.3		dBc/Hz
		600kHz offset		-142.4		
		1MHz offset		-141.5		
		6MHz offset		-157.2		
		10MHz offset		-158		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 1989MHz, f_O = 497.25MHz	100kHz offset		-128		dBc/Hz
		600kHz offset		-148		
		1MHz offset		-151		
		6MHz offset		-156.8		
		10MHz offset		-157		
VCO phase noise, Closed loop phase noise direct output(1)(2)(3)	f_{VCO} = 1989MHz, f_O = 1989MHz	1kHz offset		-83		dBc/Hz
		600kHz offset		-136		
		1MHz offset		-141		
		10MHz offset		-159		
RMS phase error Closed loop phase noise direct output(3)	100Hz to 10MHz			1°		
VCO phase noise, Closed loop phase noise divide-by-2 output(1)(2)(3)	f_{VCO} = 1989MHz, f_O = 994.5MHz	1kHz offset		-88.7		dBc/Hz
		600kHz offset		-141.9		
		1MHz offset		-147.5		
		10MHz offset		-158		
RMS phase error Closed loop phase noise divide-by-2 output(3)	100Hz to 10MHz			0.509°		
VCO phase noise, Closed loop phase noise divide-by-4 output(1)(2)(3)	f_{VCO} = 1989MHz, f_O = 497.25MHz	1kHz offset		-95		dBc/Hz
		600kHz offset		-147.9		
		1MHz offset		-151.3		
		10MHz offset		-156		
RMS phase error Closed loop phase noise divide-by-4 output(3)	100Hz to 10MHz			0.252°		
VCO gain, Kv	VCO free running			23		MHz/V
Reference spur(2)				–80		dBc

(1) See Application Circuit Figure 87.
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.

TRF3761-H ELECTRICAL CHARACTERISTICS

Supply voltage = V_{CC} = 5V, T_A = –40 to 85 °C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 2116MHz, f_O = 2116MHz	100kHz offset		–116		dBc/Hz
		600kHz offset		–136		
		1MHz offset		-142		
		6MHz offset		–154.2		
		10MHz offset		–156		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 2116MHz, f_O = 1058	100kHz offset		–123.3		dBc/Hz
		600kHz offset		–143		
		1MHz offset		–147.6		
		6MHz offset		–157		
		10MHz offset		–158.3		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 2116MHz, f_O = 529MHz	100kHz offset		–129.4		dBc/Hz
		600kHz offset		-149.8		
		1MHz offset		-152.7		
		6MHz offset		–157.7		
		10MHz offset		–158		
VCO phase noise, Closed loop phase noise direct output(1)(2)(3)	f_{VCO} = 2116MHz, f_O = 2116MHz	1kHz offset		–84		dBc/Hz
		600kHz offset		–136		
		1MHz offset		–141		
		10MHz offset		–157		
RMS phase error Closed loop phase noise direct output(3)	100Hz to 10MHz			0.99°		
VCO phase noise, Closed loop phase noise divide-by-2 output(1)(2)(3)	f_{VCO} = 2116MHz, f_O = 1058MHz	1kHz offset		-89		dBc/Hz
		600kHz offset		–143		
		1MHz offset		–148		
		10MHz offset		–159		
RMS phase error Closed loop phase noise divide-by-2 output(3)	100Hz to 10MHz			0.54°		
VCO phase noise, Closed loop phase noise divide-by-4 output(1)(2)(3)	f_{VCO} = 2116MHz, f_O = 529MHz	1kHz offset		–95		dBc/Hz
		600kHz offset		–149.5		
		1MHz offset		–153		
		10MHz offset		–158		
RMS phase error Closed loop phase noise divide-by-4 output(3)	100Hz to 10MHz			0.35°		
VCO gain, Kv	VCO free running			23		MHz/V
Reference spur(2)				–80		dBc

(1) See Application Circuit Figure 87.
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.

TRF3761-J ELECTRICAL CHARACTERISTICS

Supply voltage = V_{CC} = 5V, T_A = –40 to 85 °C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 2289MHz, f_O = 2289MHz	100kHz offset		–116.7		dBc/Hz
		600kHz offset		–135.4		
		1MHz offset		-141		
		6MHz offset		–153.8		
		10MHz offset		–156.4		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 2289MHz, f_O = 1144.5	100kHz offset		–123		dBc/Hz
		600kHz offset		–142		
		1MHz offset		–147		
		6MHz offset		–156.2		
		10MHz offset		–157.5		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 2289MHz, f_O = 572.25MHz	100kHz offset		–129		dBc/Hz
		600kHz offset		-149		
		1MHz offset		-153		
		6MHz offset		–157.5		
		10MHz offset		–158		
VCO phase noise, Closed loop phase noise direct output(1)(2)(3)	f_{VCO} = 2289MHz, f_O = 2289MHz	1kHz offset		–83		dBc/Hz
		600kHz offset		–135		
		1MHz offset		–140		
		10MHz offset		–156		
RMS phase error Closed loop phase noise direct output(3)	100Hz to 10MHz			1.1°		
VCO phase noise, Closed loop phase noise divide-by-2 output(1)(2)(3)	f_{VCO} = 2289MHz, f_O = 1144.5MHz	1kHz offset		–89		dBc/Hz
		600kHz offset		-141		
		1MHz offset		–145.7		
		10MHz offset		–158		
RMS phase error Closed loop phase noise divide-by-2 output(3)	100Hz to 10MHz			0.59°		
VCO phase noise, Closed loop phase noise divide-by-4 output(1)(2)(3)	f_{VCO} = 2289MHz, f_O = 572.25MHz	1kHz offset		–95		dBc/Hz
		600kHz offset		–148		
		1MHz offset		–152		
		10MHz offset		–158.1		
RMS phase error Closed loop phase noise divide-by-4 output(3)	100Hz to 10MHz			0.37°		
VCO gain, Kv	VCO free running			23		MHz/V
Reference spur(2)				–80		dBc

(1) See Application Circuit Figure 87.
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.

TRF3761-A TYPICAL CHARACTERISTICS
(See Figure 87)

Closed Loop VCO Phase Noise

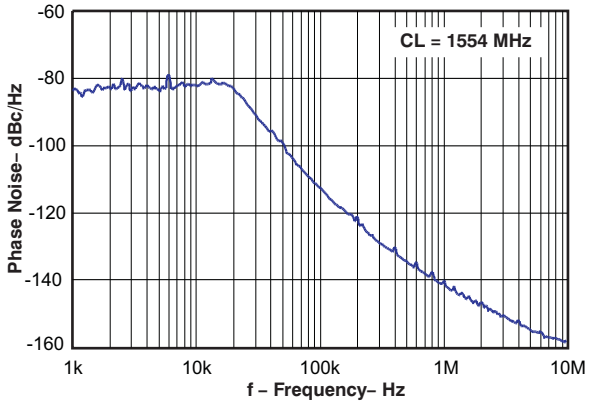


Figure 2.

Open Loop VCO Phase Noise

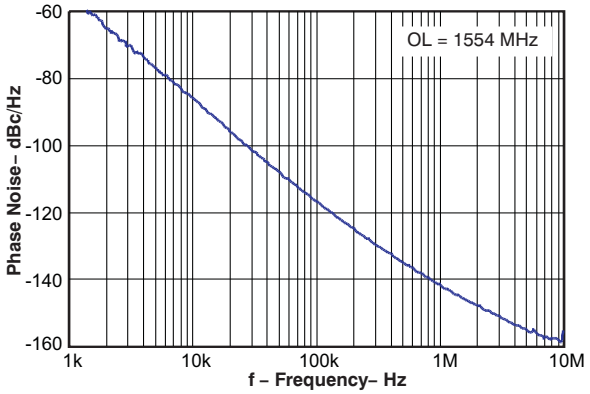


Figure 3.

Closed Loop VCO Phase Noise

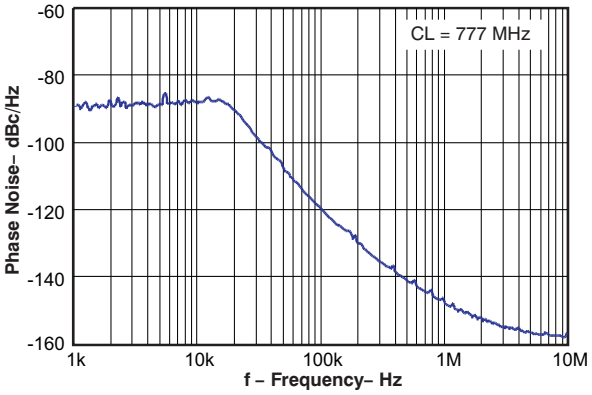


Figure 4.

Open Loop VCO Phase Noise

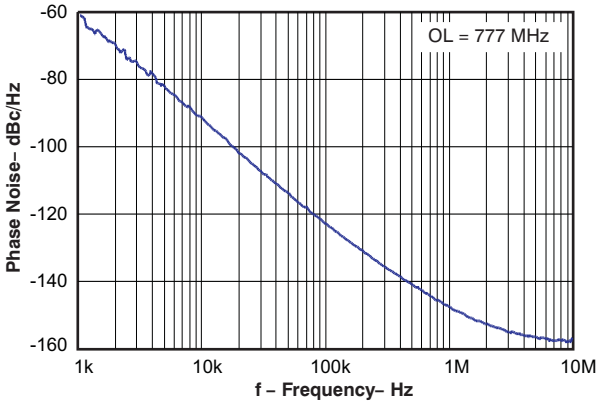


Figure 5.

Closed Loop VCO Phase Noise

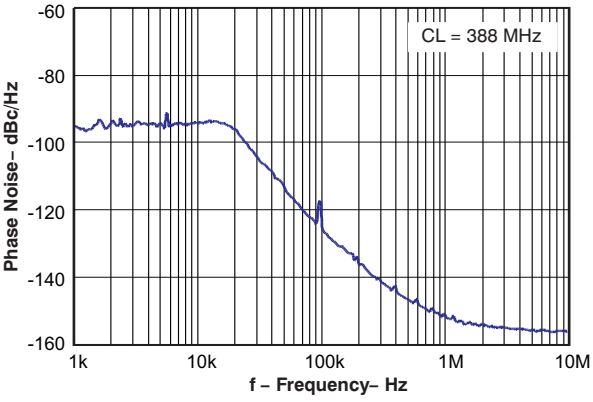


Figure 6.

Open Loop VCO Phase Noise

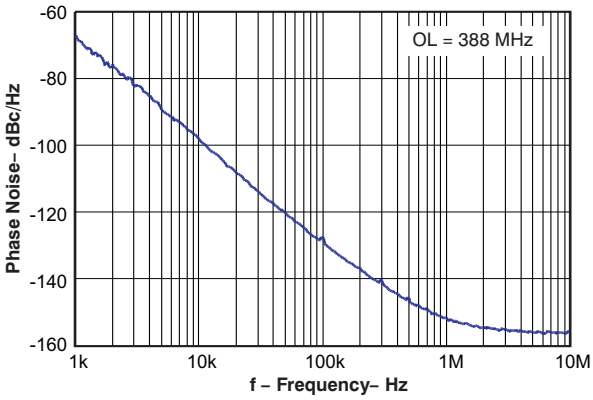


Figure 7.

TRF3761-A TYPICAL CHARACTERISTICS (See Figure 87) (continued)

Direct Output: PFD Frequency Spurs

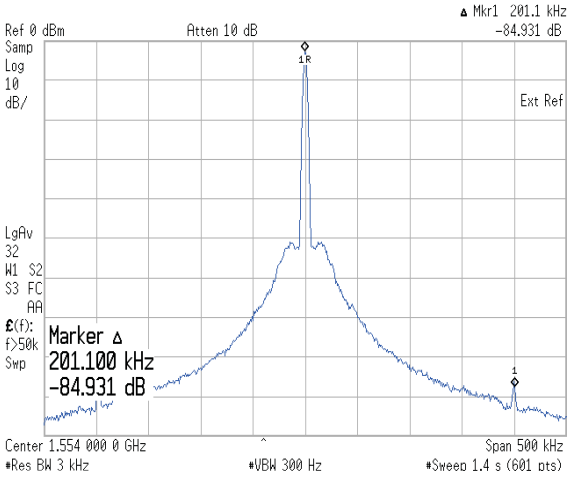


Figure 8.

Direct-By-2 Output: PFD Frequency Spurs

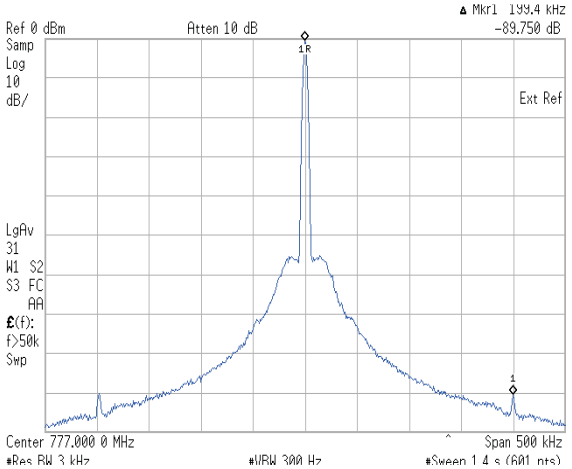


Figure 9.

Divide-By-4 Output: PFD Frequency Spurs

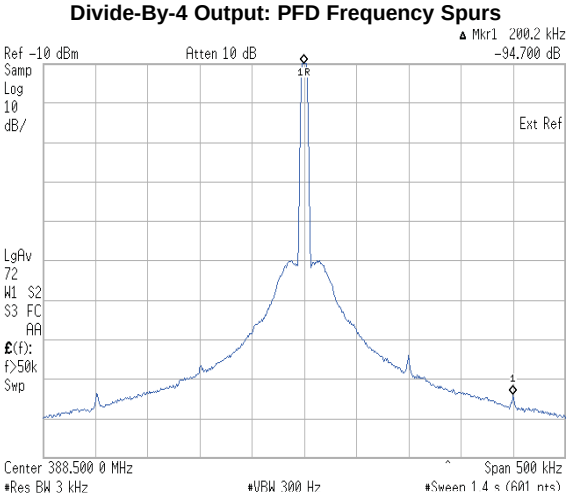


Figure 10.

TRF3761-B TYPICAL CHARACTERISTICS
(See Figure 87)

Closed Loop VCO Phase Noise

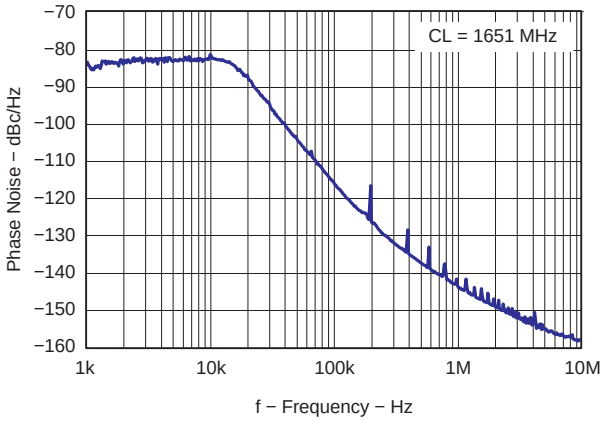


Figure 11.

Open Loop VCO Phase Noise

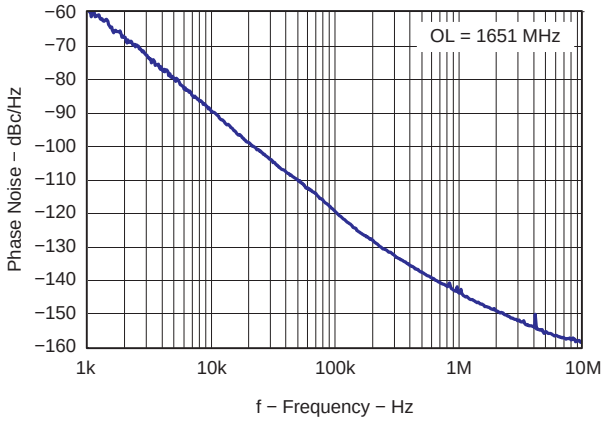


Figure 12.

Closed Loop VCO Phase Noise

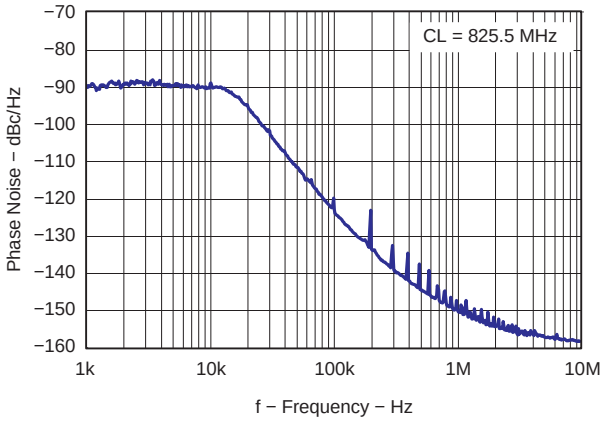


Figure 13.

Open Loop VCO Phase Noise

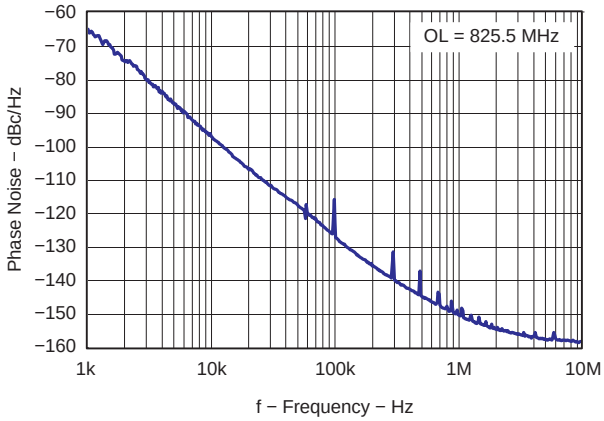


Figure 14.

Closed Loop VCO Phase Noise

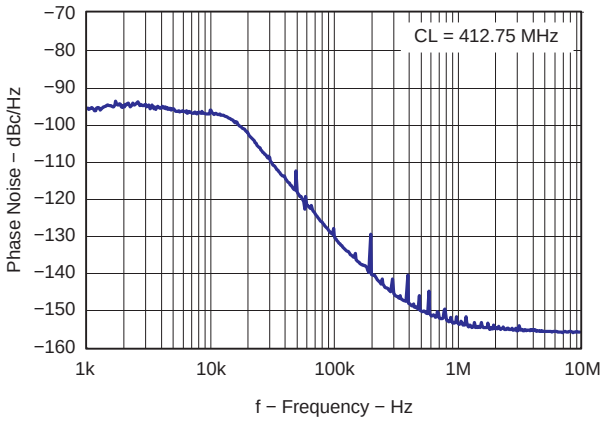


Figure 15.

Open Loop VCO Phase Noise

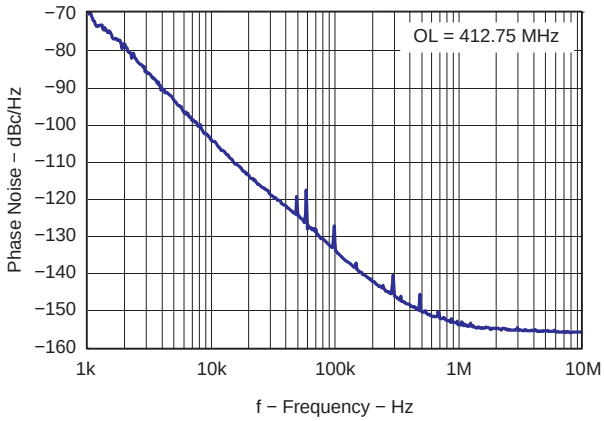


Figure 16.

TRF3761-B TYPICAL CHARACTERISTICS (See Figure 87) (continued)

Direct Output: PFD Frequency Spurs

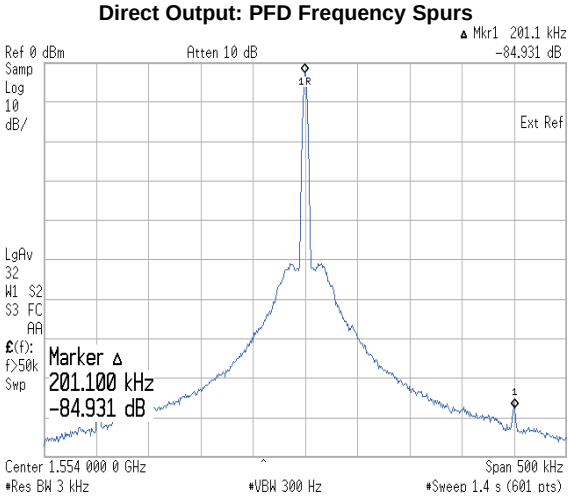


Figure 17.

Divide-By-2 Output: PFD Frequency Spurs

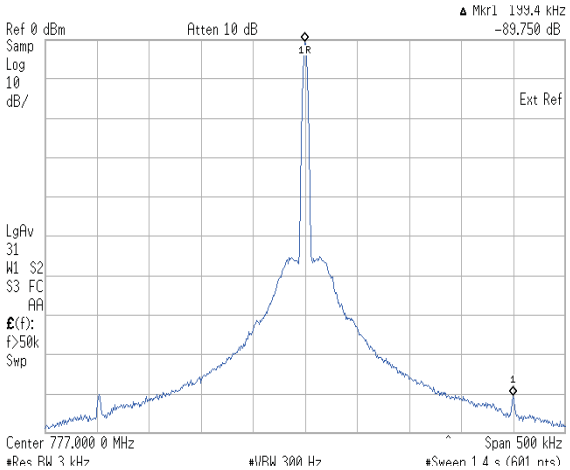


Figure 18.

Divide-By-4 Output: PFD Frequency Spurs

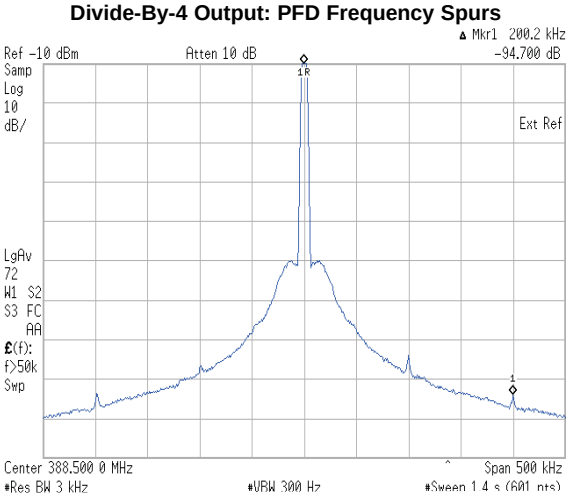


Figure 19.

TRF3761-C TYPICAL CHARACTERISTICS
(See Figure 87)

Closed Loop VCO Phase Noise

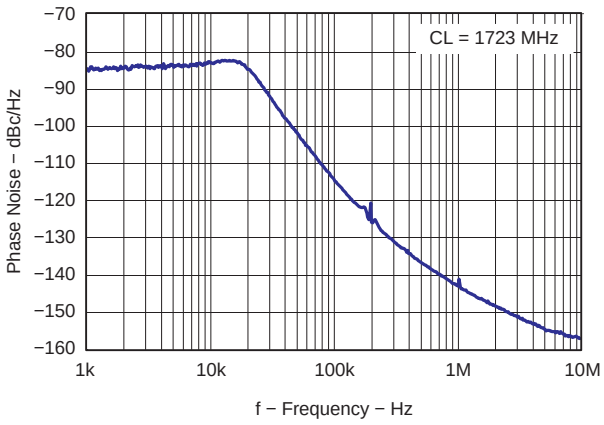


Figure 20.

Open Loop VCO Phase Noise

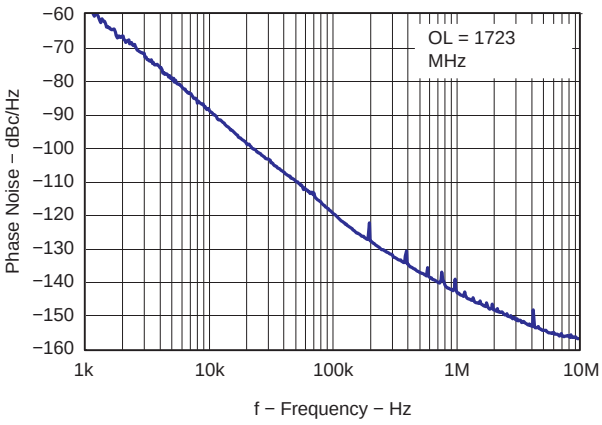


Figure 21.

Closed Loop VCO Phase Noise

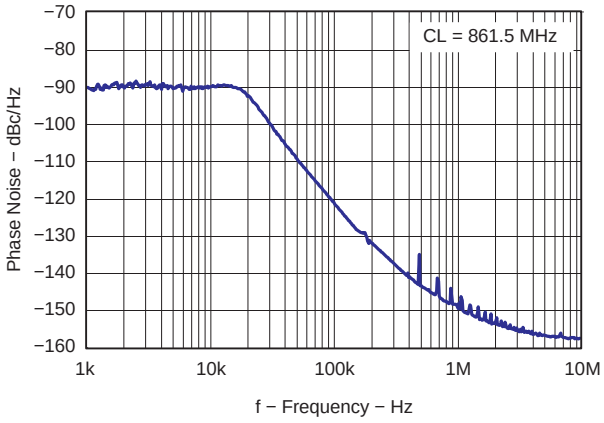


Figure 22.

Open Loop VCO Phase Noise

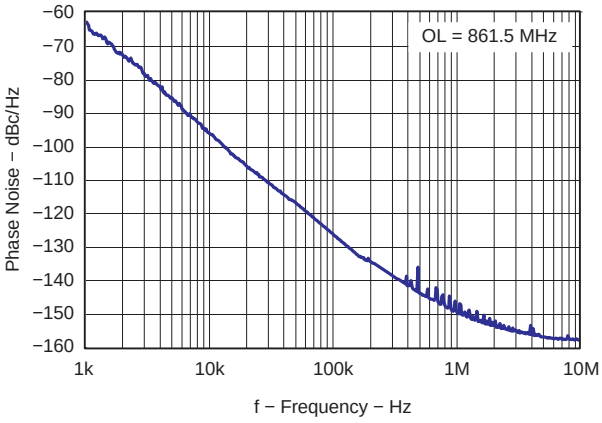


Figure 23.

Closed Loop VCO Phase Noise

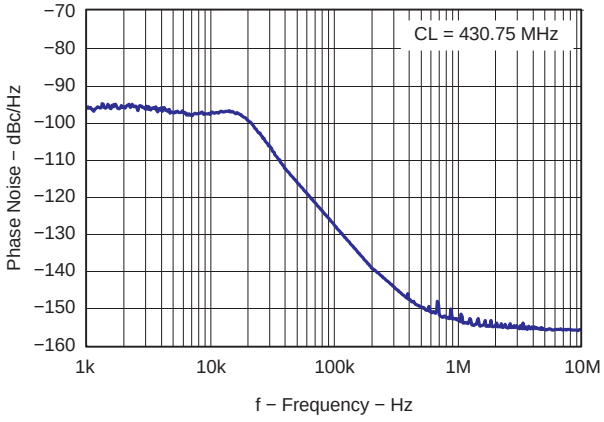


Figure 24.

Open Loop VCO Phase Noise

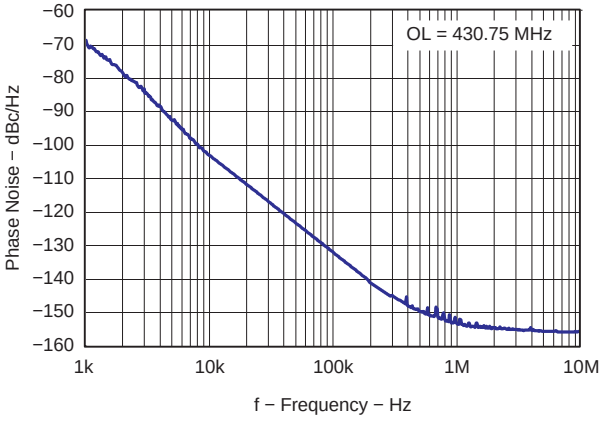


Figure 25.

TRF3761-C TYPICAL CHARACTERISTICS (See Figure 87) (continued)

Direct Output: PFD Frequency Spurs

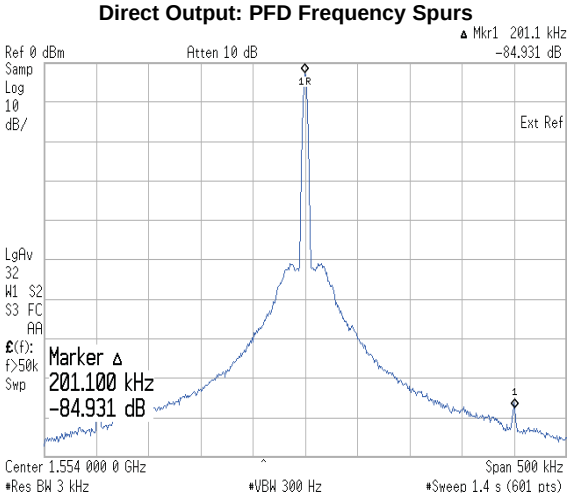


Figure 26.

Divide-By-2 Output: PFD Frequency Spurs

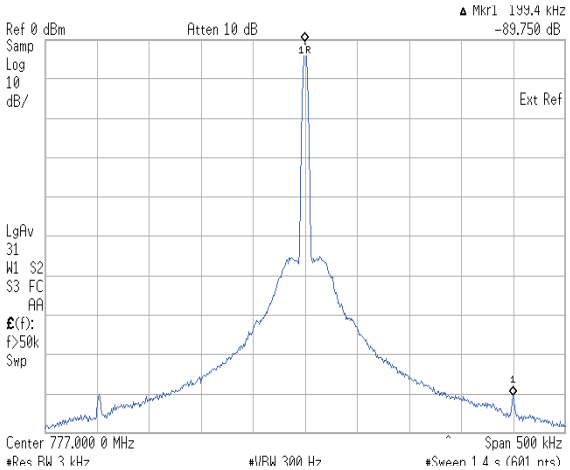


Figure 27.

Divide-By-4 Output: PFD Frequency Spurs

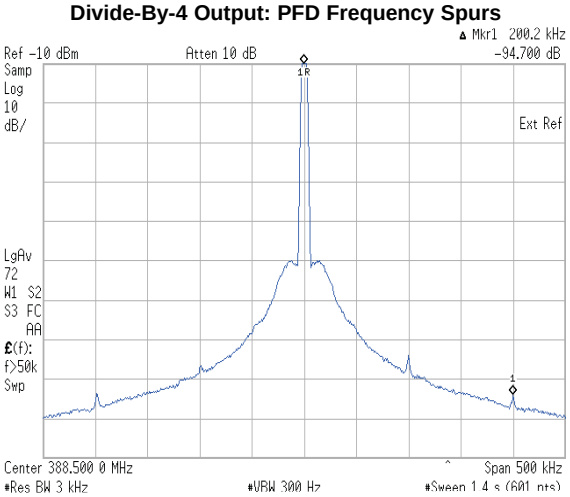


Figure 28.

TRF3761-D TYPICAL CHARACTERISTICS
(See Figure 87)

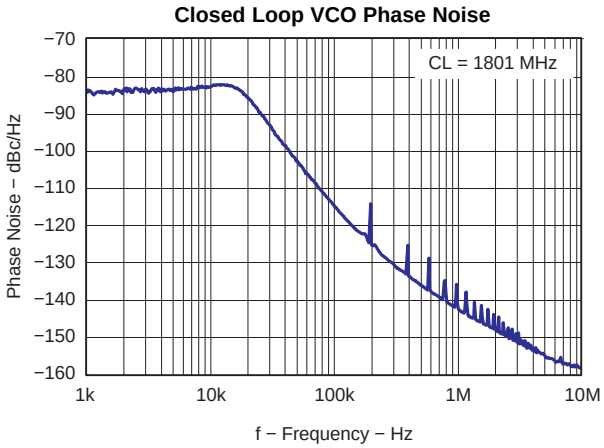


Figure 29.

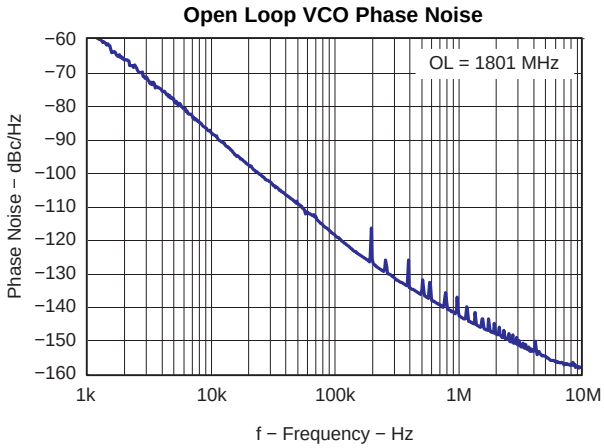


Figure 30.

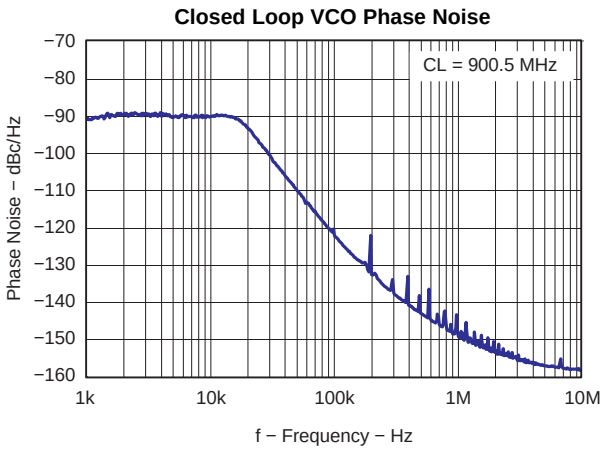


Figure 31.

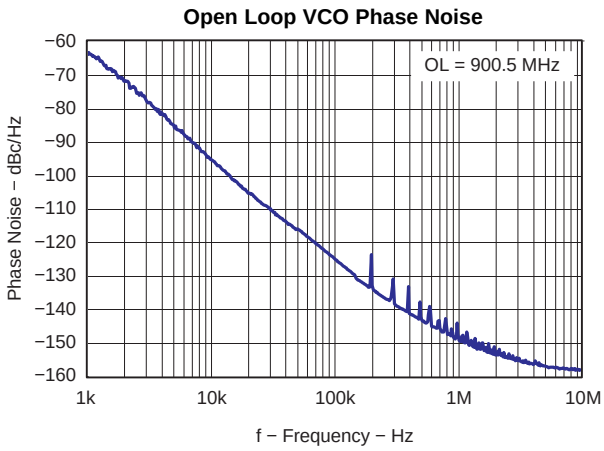


Figure 32.

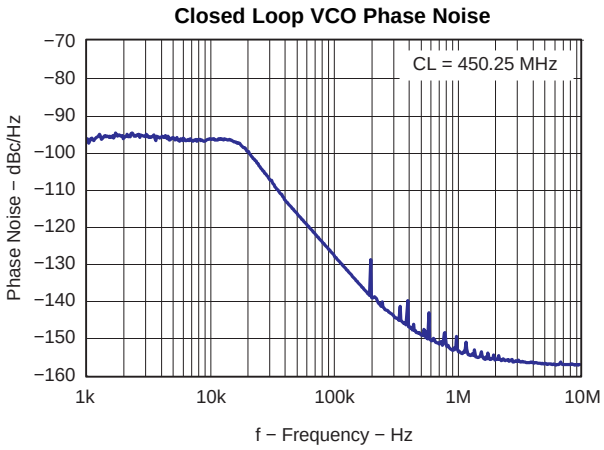


Figure 33.

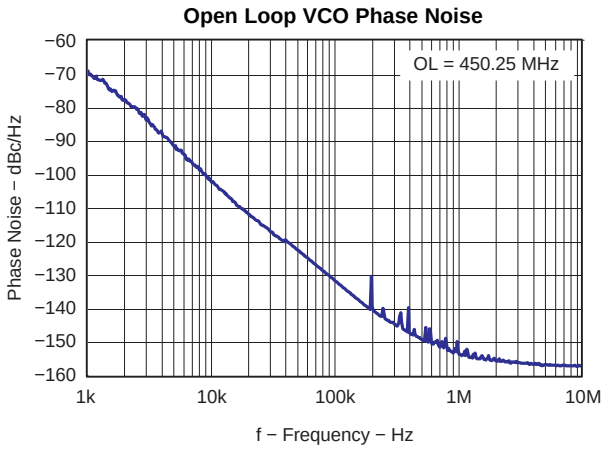


Figure 34.

TRF3761-D TYPICAL CHARACTERISTICS (Continued)

Direct Output: PFD Frequency Spurs

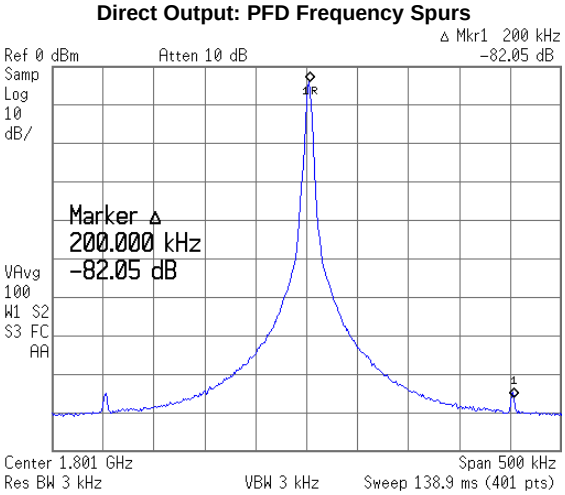


Figure 35.

Divide-By-2 Output: PFD Frequency Spur

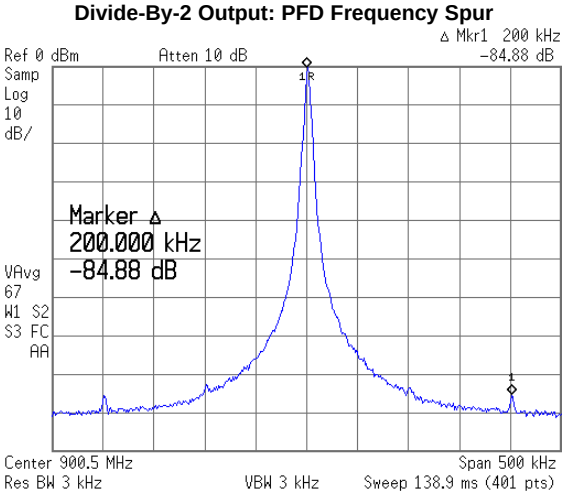


Figure 36.

Divide-By-4 Output: PFD Frequency Spurs

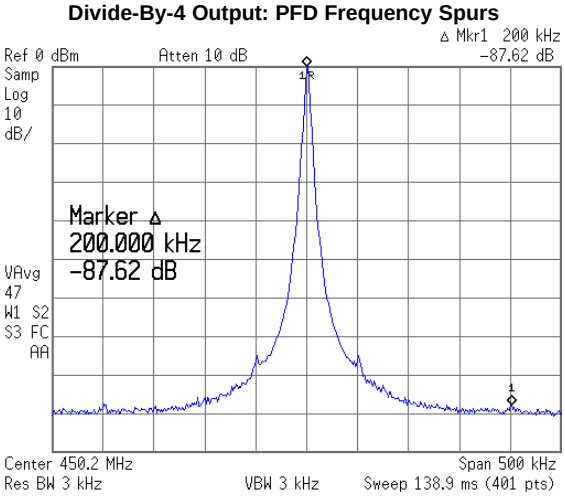


Figure 37.

TRF3761-E TYPICAL CHARACTERISTICS
(See Figure 87)

Closed Loop VCO Phase Noise

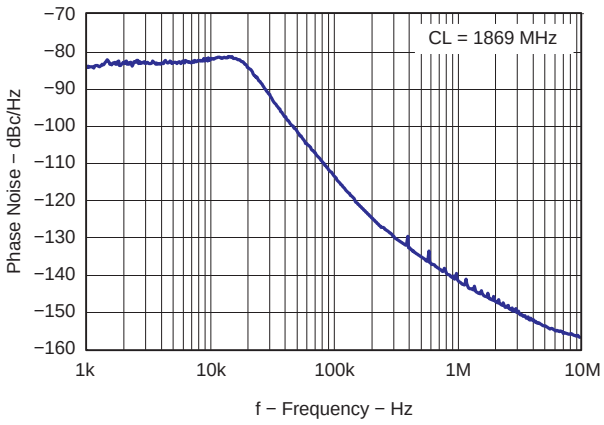


Figure 38.

Open Loop VCO Phase Noise

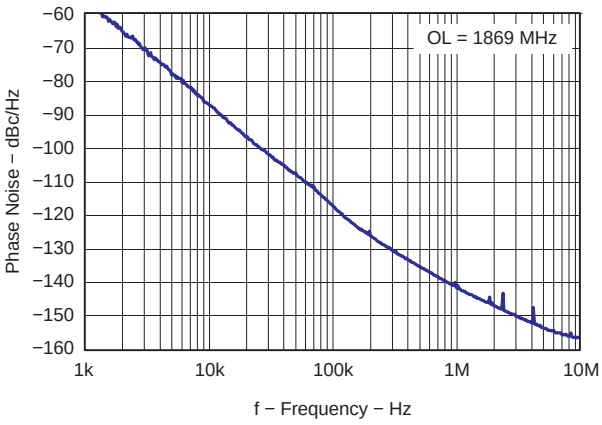


Figure 39.

Closed Loop VCO Phase Noise

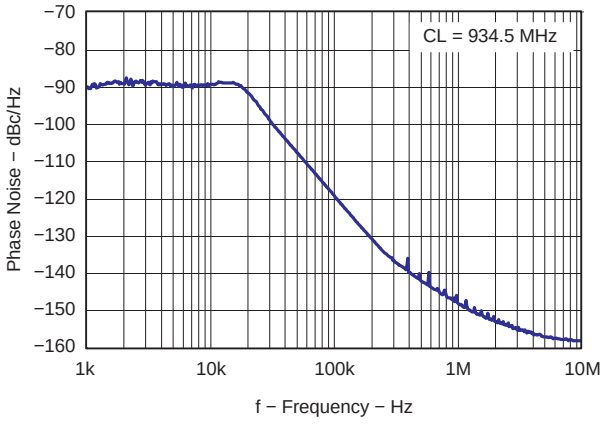


Figure 40.

Open Loop VCO Phase Noise

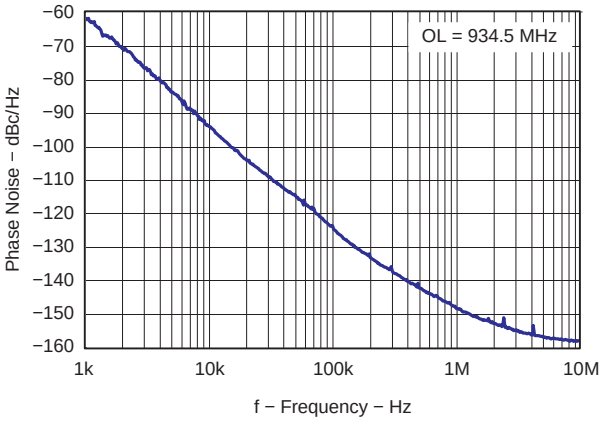


Figure 41.

Closed Loop VCO Phase Noise

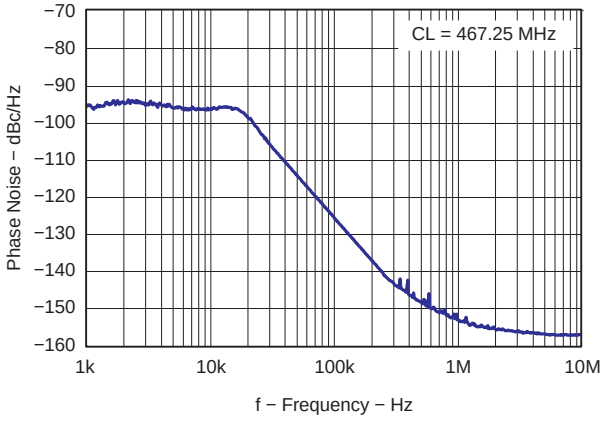


Figure 42.

Open Loop VCO Phase Noise

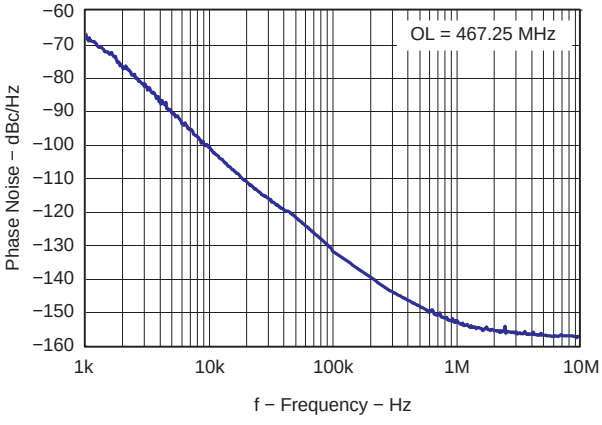


Figure 43.

TRF3761-E TYPICAL CHARACTERISTICS (See Figure 87) (continued)

Direct Output: PFD Frequency Spurs

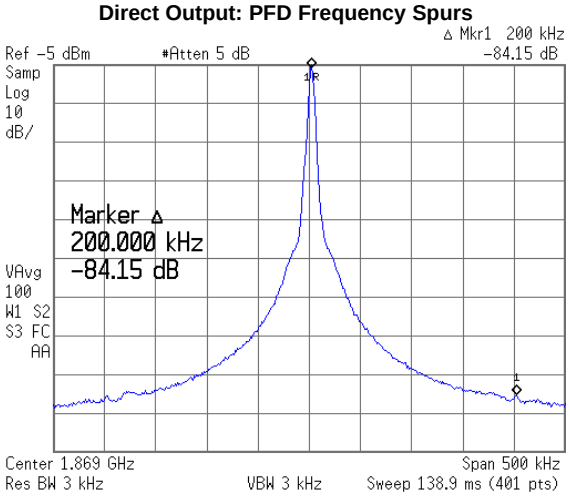


Figure 44.

Divide-By-2 Output: PFD Frequency Spurs

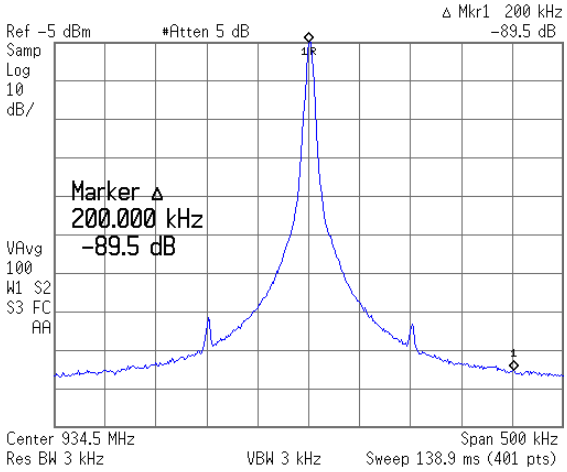


Figure 45.

Divide-By-4 Output: PFD Frequency Spurs

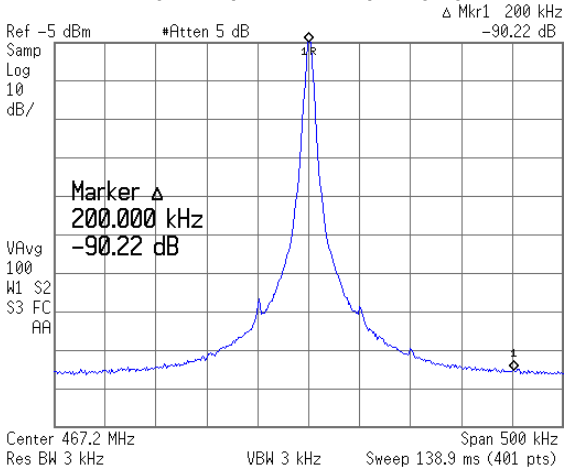


Figure 46.

TRF3761-F TYPICAL CHARACTERISTICS
(See Figure 87)

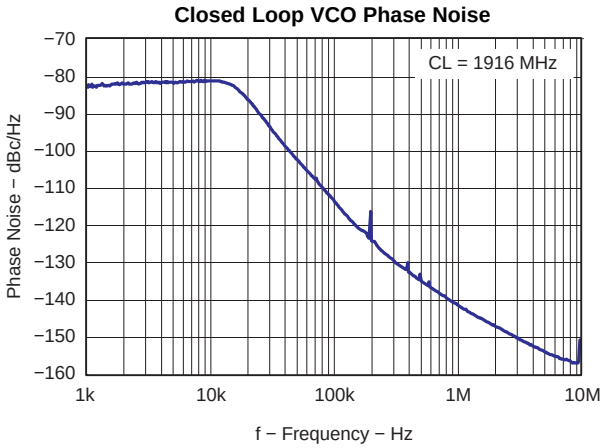


Figure 47.

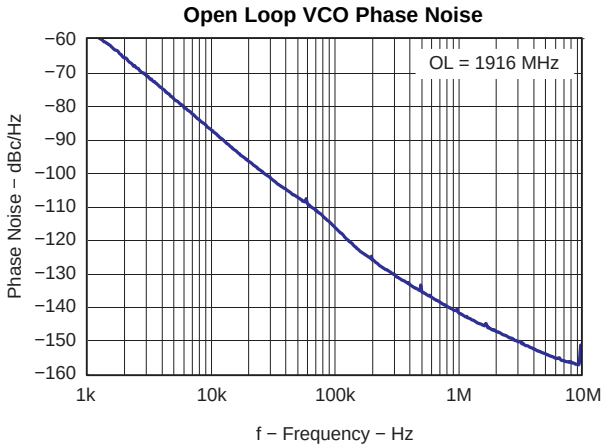


Figure 48.

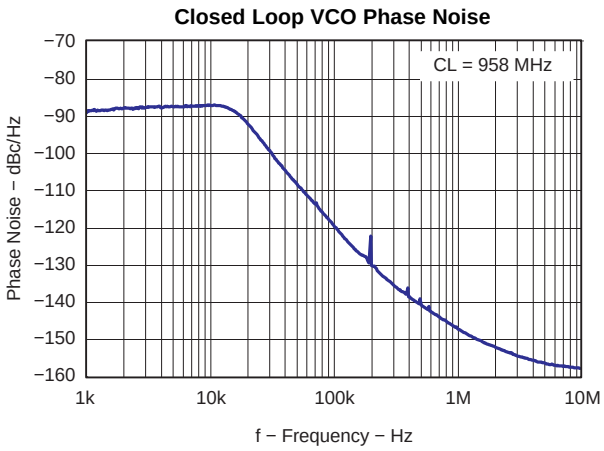


Figure 49.

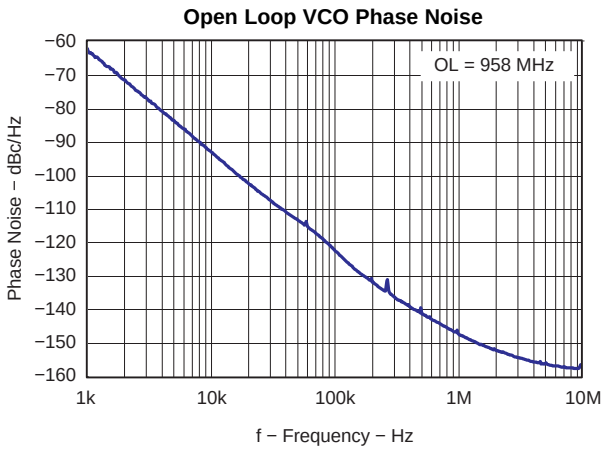


Figure 50.

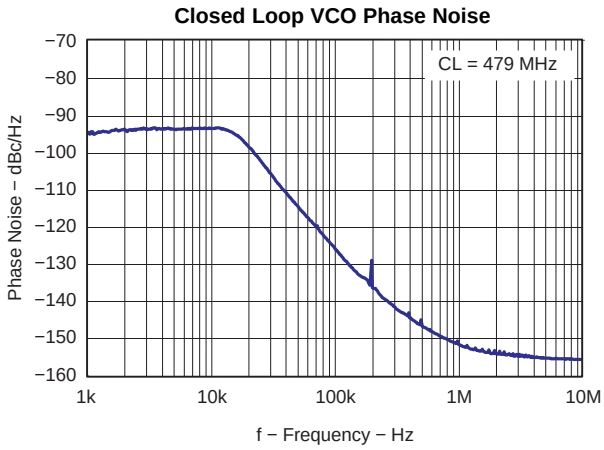


Figure 51.

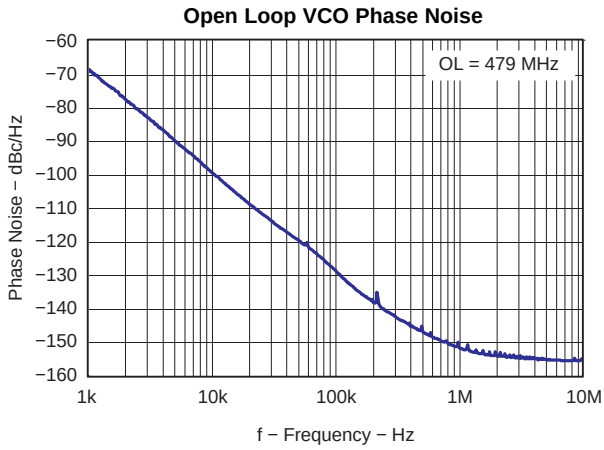


Figure 52.

TRF3761-F TYPICAL CHARACTERISTICS (See Figure 87) (continued)

Direct Output: PFD Frequency Spurs

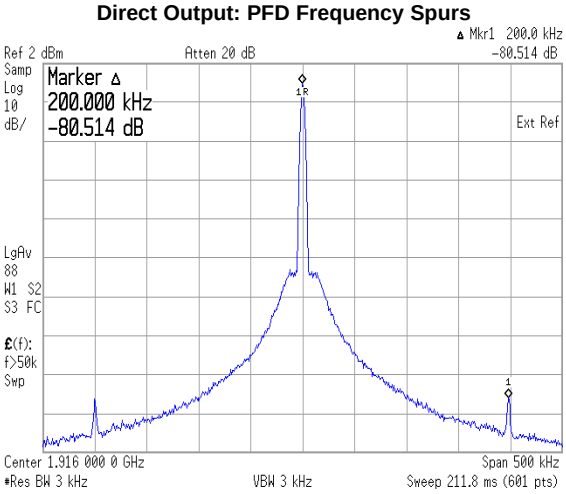


Figure 53.

Divide-By-2 Output: PFD Frequency Spurs

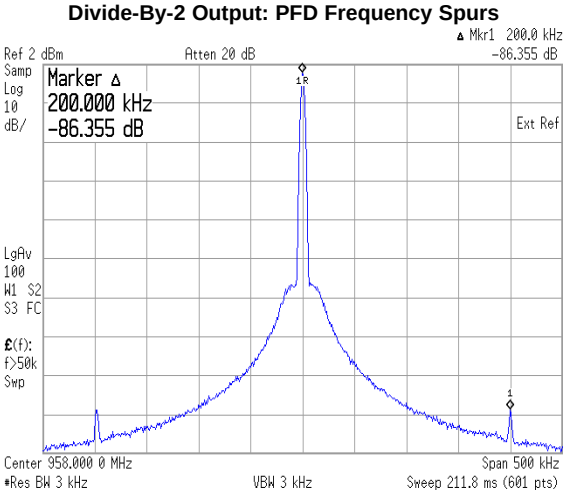


Figure 54.

Divide-By-4 Output: PFD Frequency Spurs

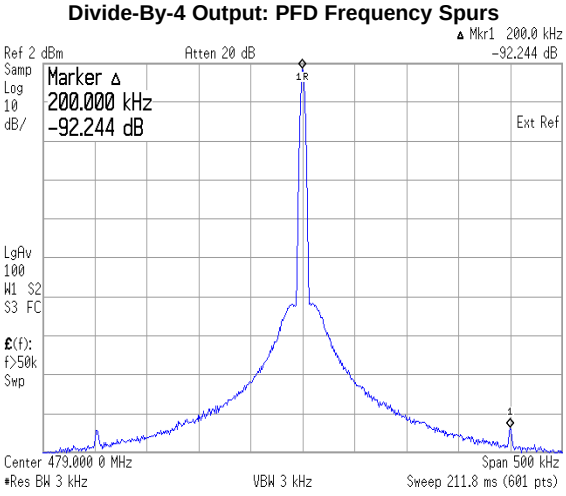


Figure 55.

TRF3761-G TYPICAL CHARACTERISTICS
(See Figure 87)

Closed Loop VCO Phase Noise

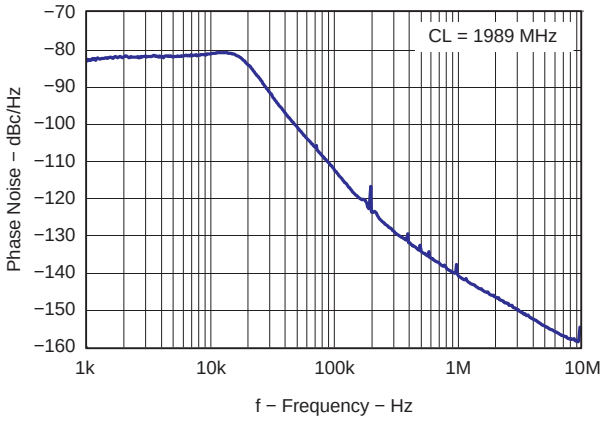


Figure 56.

Open Loop VCO Phase Noise

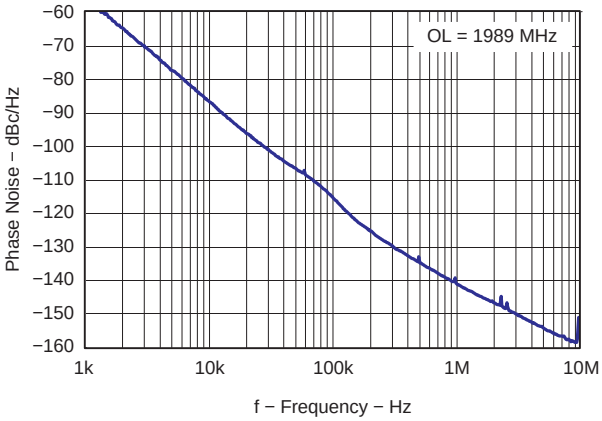


Figure 57.

Closed Loop VCO Phase Noise

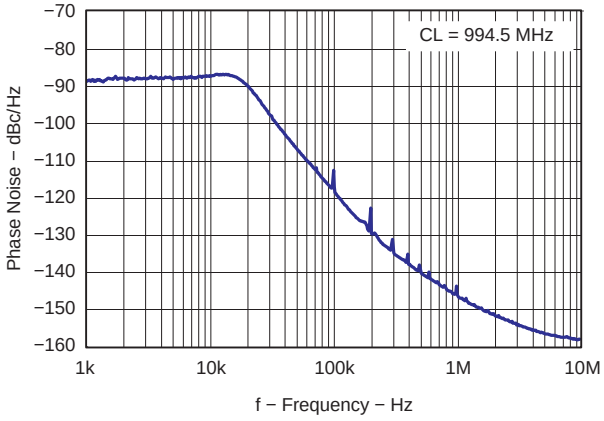


Figure 58.

Open Loop VCO Phase Noise

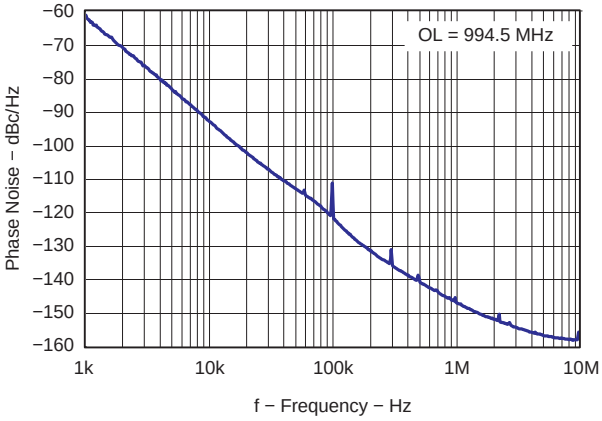


Figure 59.

Closed Loop VCO Phase Noise

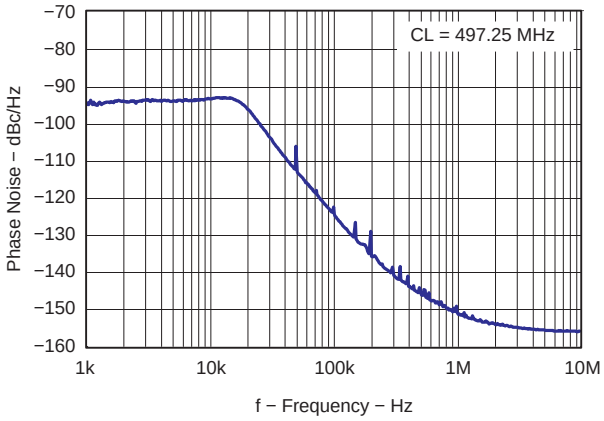


Figure 60.

Open Loop VCO Phase Noise

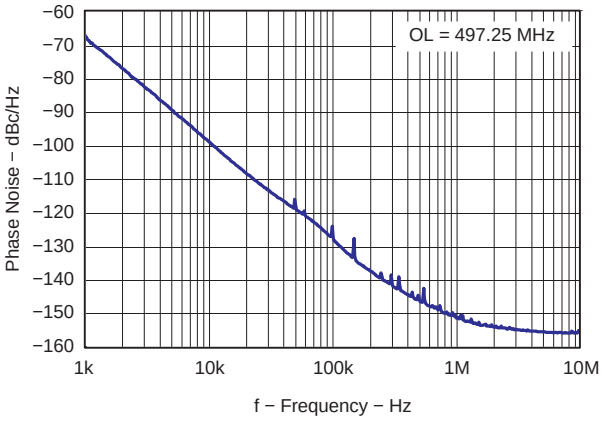


Figure 61.

TRF3761-G TYPICAL CHARACTERISTICS (See Figure 87) (continued)

Direct Output: PFD Frequency Spurs

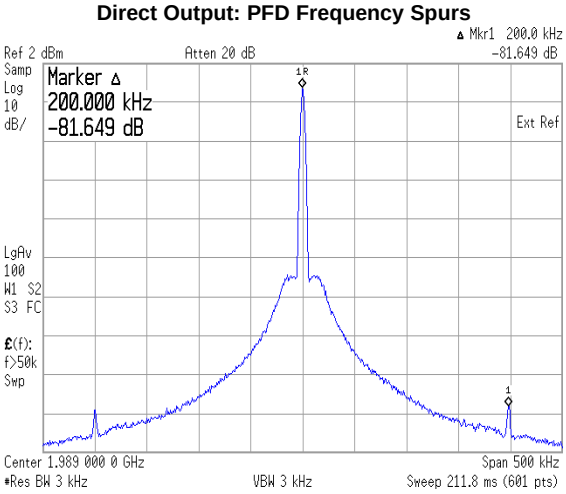


Figure 62.

Divide-By-2 Output: PFD Frequency Spurs

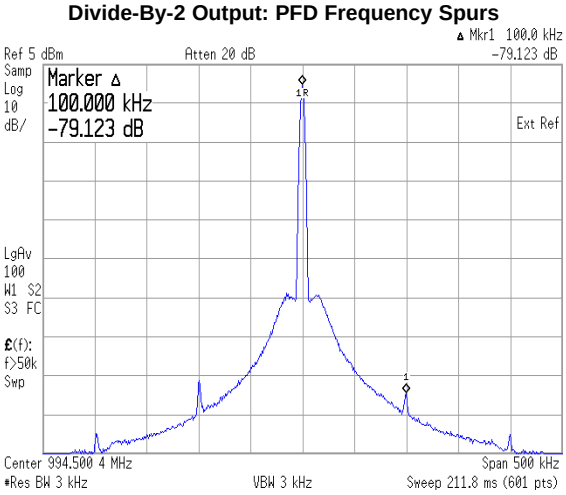


Figure 63.

Divide-By-4 Output: PFD Frequency Spurs

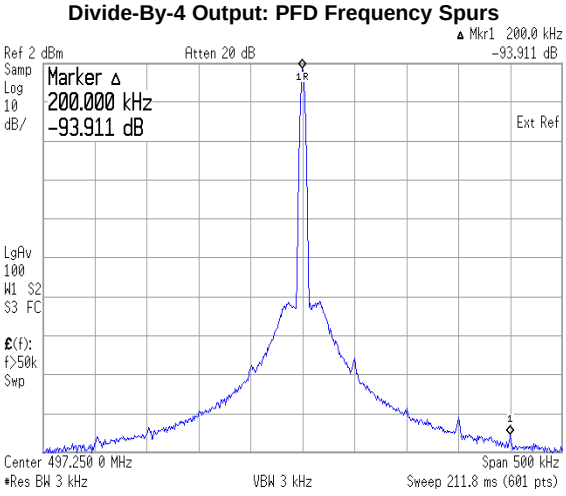


Figure 64.

TRF3761-H TYPICAL CHARACTERISTICS
(See Figure 87)

Closed Loop VCO Phase Noise

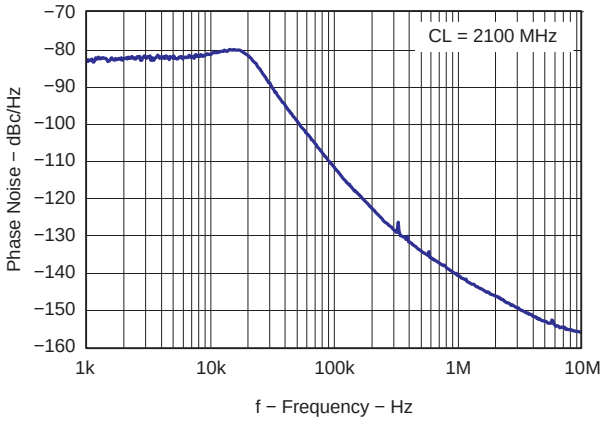


Figure 65.

Open Loop VCO Phase Noise

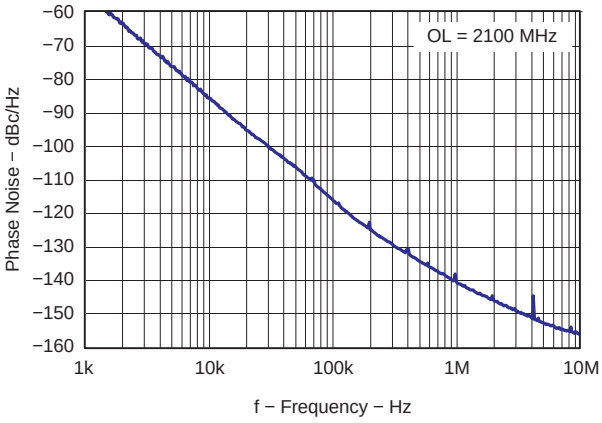


Figure 66.

Closed Loop VCO Phase Noise

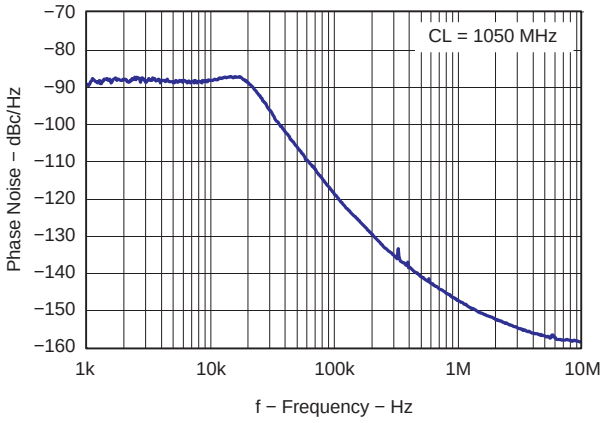


Figure 67.

Open Loop VCO Phase Noise

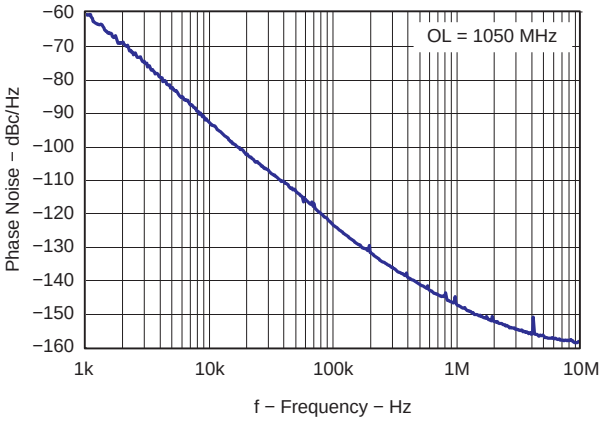


Figure 68.

Closed Loop VCO Phase Noise

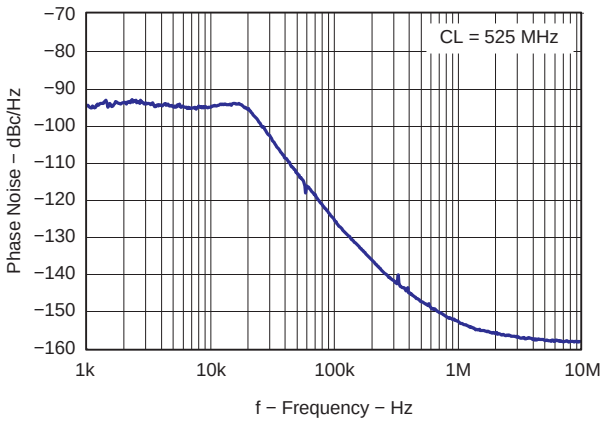


Figure 69.

Open Loop VCO Phase Noise

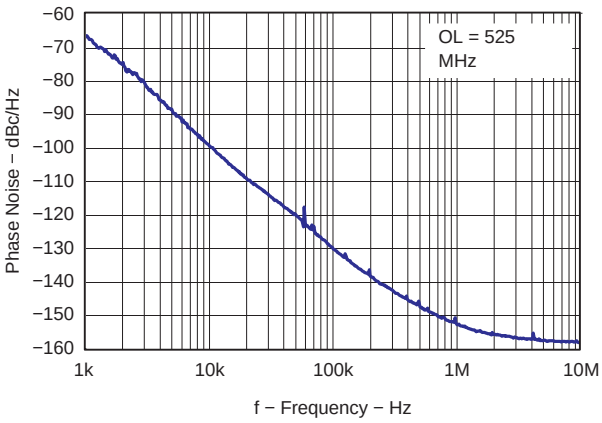


Figure 70.

TRF3761-H TYPICAL CHARACTERISTICS (See Figure 87) (continued)

Direct Output: PFD Frequency Spurs

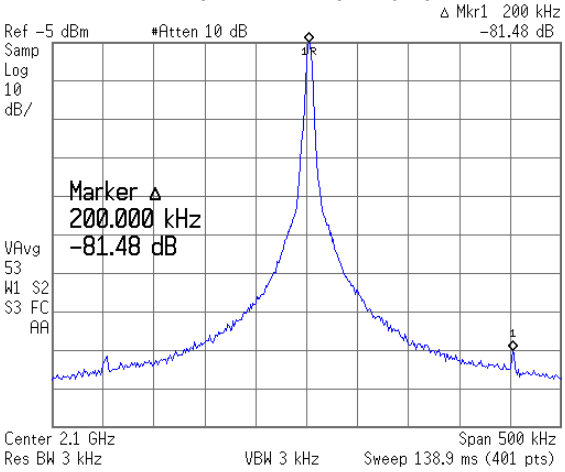


Figure 71.

Divide-By-2 Output: PFD Frequency Spurs

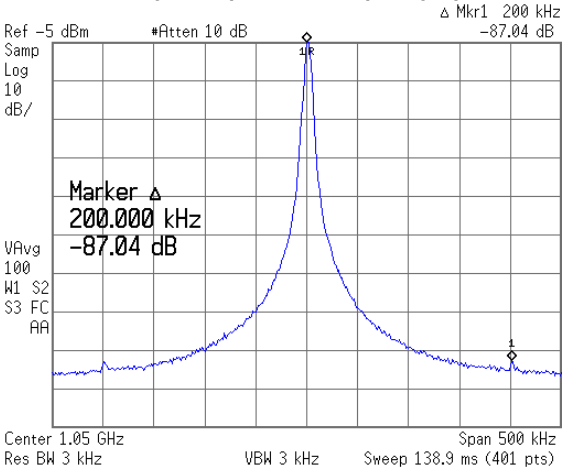


Figure 72. Divide-By-2 Output: PFD Frequency Spurs

Divide-By-4 Output: PFD Frequency Spurs

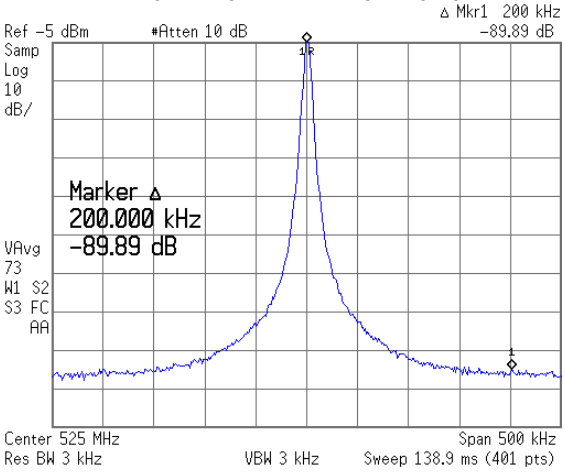


Figure 73.

TRF3761-J TYPICAL CHARACTERISTICS
(See Figure 87)

Closed Loop VCO Phase Noise

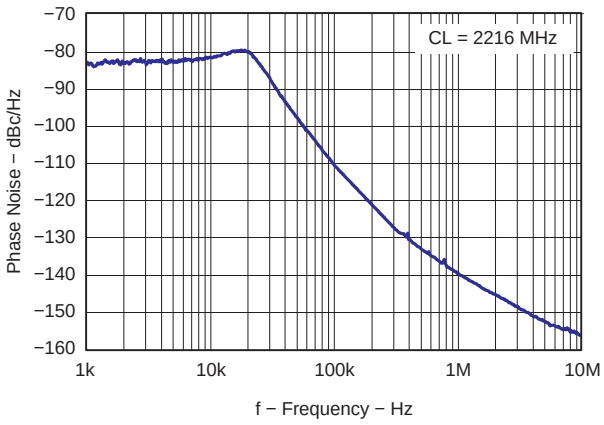


Figure 74.

Open Loop VCO Phase Noise

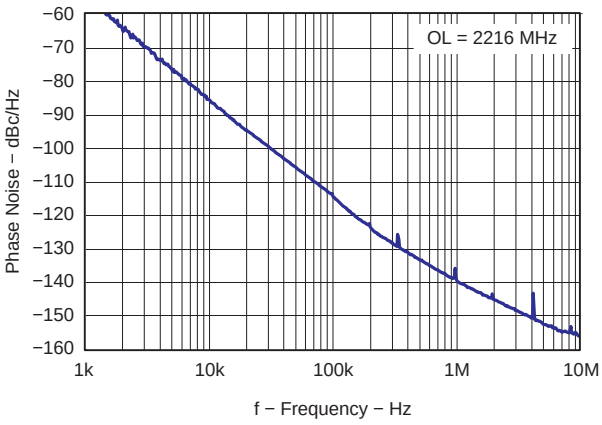


Figure 75.

Closed Loop VCO Phase Noise

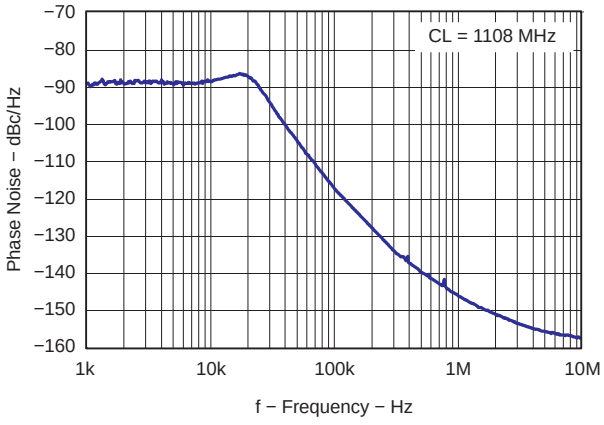


Figure 76.

Open Loop VCO Phase Noise

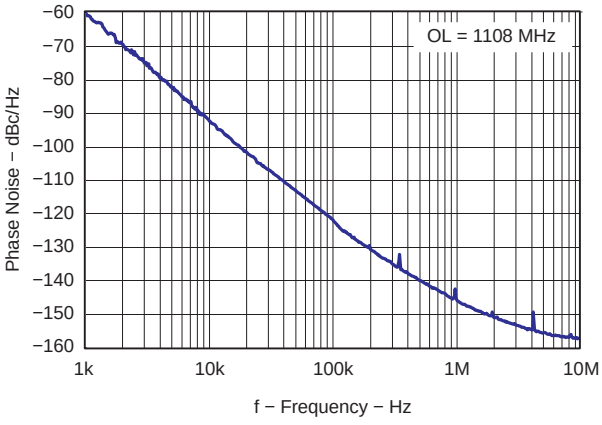


Figure 77.

Closed Loop VCO Phase Noise

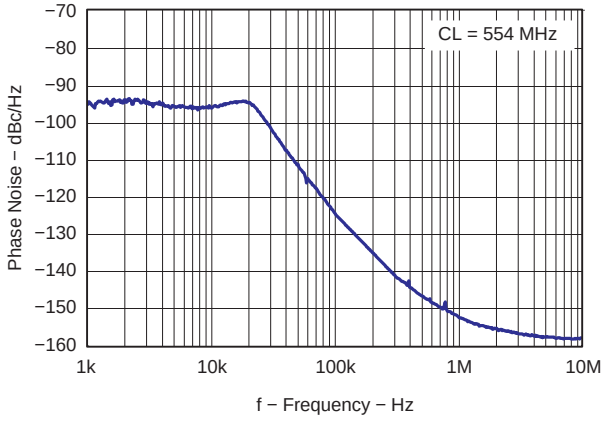


Figure 78.

Open Loop VCO Phase Noise

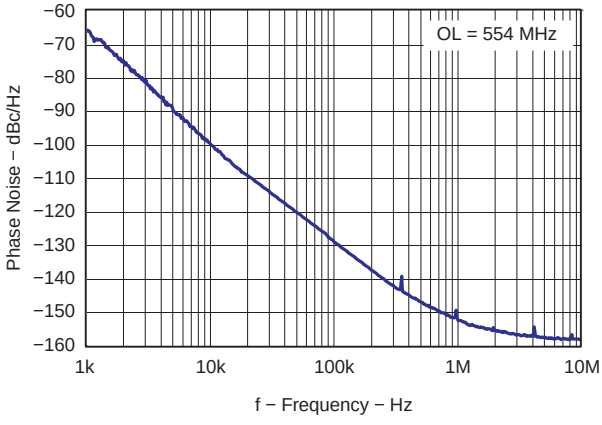


Figure 79.

TRF3761-J TYPICAL CHARACTERISTICS (See Figure 87) (continued)

Direct Output: PFD Frequency Spurs

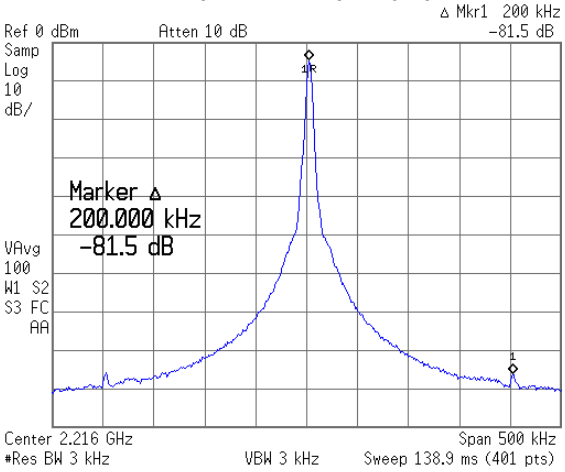


Figure 80.

Divide-By-2 Output: PFD Frequency Spurs

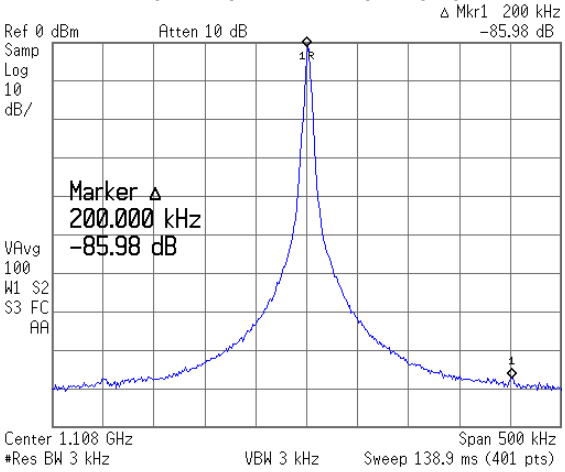


Figure 81.

Divide-By-4 Output: PFD Frequency Spurs

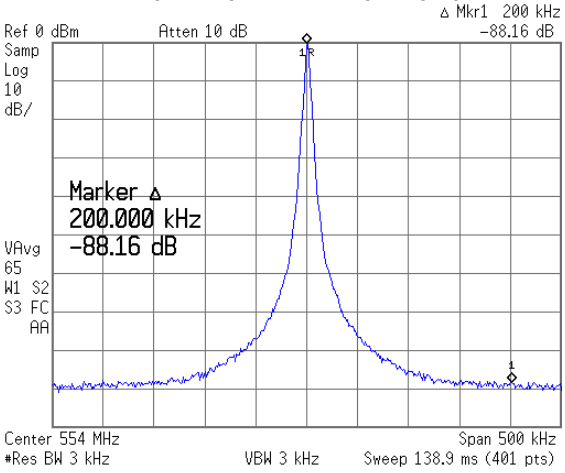
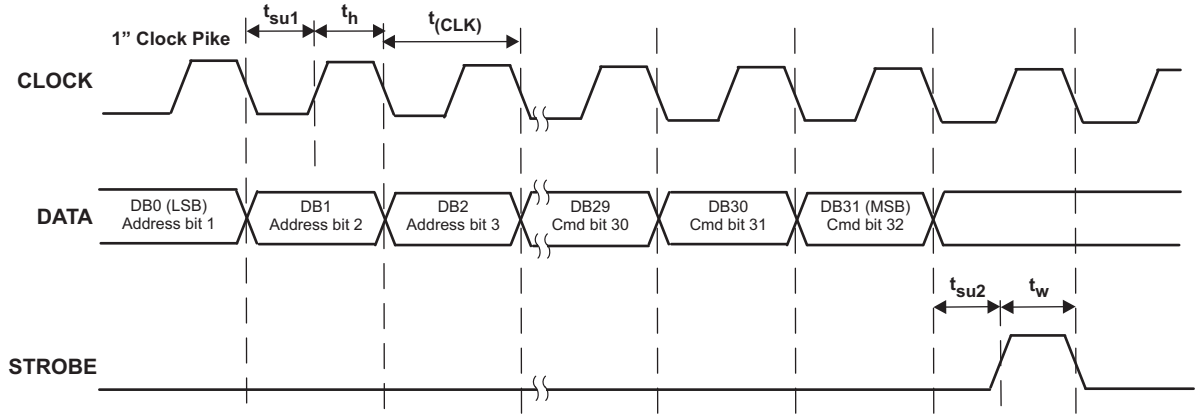


Figure 82.

SERIAL INTERFACE PROGRAMMING REGISTERS DEFINITION

The TRF3761 features a 3-wire serial programming interface that controls an internal, 32-bit shift register. There are a total of 3 signals that need to be applied: the CLOCK (pin 3), the serial DATA (pin 4) and the STROBE (pin 5). The DATA (DB0-DB31) is loaded LSB first and is read on the rising edge of the CLOCK. The STROBE is asynchronous to the CLOCK and at its rising edge the data in the shift register gets loaded onto the selected internal register. The first four bits (DB0-DB3) is the address to select the available internal registers.



A. The first 4 bits, DB(3-0), of data are Address bits. The 28 remaining bits, DB(31-4), are part of the command. The command is little endian or lower bits first.

Figure 83. Serial Programming Timing Diagram

Register Address				REST	Charge Pump Current Select			Output Mode		OUTBUF EN_SEL	PD BUFOUT	Reference Clock Divider (RDiv)			
DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15

Reference Clock Divider (RDiv)										Anti Backlash		PFD_POL	TRIS_CP	CP_TEST	Full Cal Req
DB16	DB17	DB18	DB19	DB20	DB21	DB22	DB23	DB24	DB25	DB26	DB27	DB28	DB29	DB30	DB31

Figure 84. Register 1

Table 1. Register 1: Device Setup

REGISTER 1 MAPPING				
Data Field	**DB31**	FULL_CAL_REQ	This is a read only bit, that indicates if a power-up cal is required	0 power-up cal is not required 1 power-up cal is required
	DB30	CP_TEST	TI internal use only	1 test enabled
	DB29	TRIS_CP	High-impedance state charge pump output	1 CP high-impedance state 0 for normal operation
	DB28	PFD_POL	Selects Polarity of PFD, should match polarity of VCO gain. If using external VCO with Negative gain then set to 0 and vise versa. The internal VCO has positive gain so set to positve(1)	0 negative 1 positive
	DB27	ABPW1	ABPW<1,0>: anti-backlash pulse width	00 1.5ns delay 01 0.9ns delay 10 3.8ns delay 11 2.7ns delay
	DB26	ABPW0		
	DB25	RDIV_13	14-bit reference clock divider	RDIV<13,0>:00...01: divide by 1 RDIV<13,0>:00...10: divide by 2 RDIV<13,0>:00...11: divide by 3
	DB24	RDIV_12		
	DB23	RDIV_11		
	DB22	RDIV_10		
	DB21	RDIV_9		
	DB20	RDIV_8		
	DB19	RDIV_7		
	DB18	RDIV_6		
	DB17	RDIV_5		
	DB16	RDIV_4		
	DB15	RDIV_3		
	DB14	RDIV_2		
	DB13	RDIV_1		
	DB12	RDIV_0		
	DB11	PD_BUFOUT	If DB10 = 0 then it controls power down of output buffer	<DB10:11>: 00 default; output buffer on 01 output buffer off 1x output buffer on/off controlled by OUTBUF_EN pin
	DB10	OUTBUF_EN_SEL	Select Output Buffer enable control:	0 internal 1 through OUTBUF_EN pin
	DB9	OUT_MODE_1	OUTBUFMODE<1,0>: Selection of RF output buffer division ratio	00 divide by 1 01 divide by 2 10 divide by4
	DB8	OUT_MODE_0		
	DB7	ICP2	ICP<2,0>: select charge pump current (1 mA step). From 1.4mA to 11.2mA with Rbias set to 2.37Kohms.	
	DB6	ICP1		
	DB5	ICP0		
	DB4	RESET	Registers reset	1 high 0 low for normal operation
Address Bits	**DB3**		Address Bits <3,0>=0000 for register 1	
	DB2			
	DB1			
	DB0			

OUT_MODE<1,0>: TRF3761 has an optional divide by 2 or 4 output, which is selectable by programming bits <OUT_MODE_1, OUT_MODE_0> of register 1 (see Table 1).

CP_TEST: By setting bit DB30 to 1 it is possible to test the PFD up or down pulses. Internal TI use only.

TRIS_CP: If bit DB29 is set to 1, the charge pump output goes in tri-state. For normal operation, DB29 must be set to 0.

ABPW: Bits <DB27, DB26> are used to program the width of the anti-backlash pulses of the PFD. The user selects one of the following values: 0.9ns, 1.5ns, 2.7ns and 3.8ns. Backlash can occur when Fpfd becomes phase aligned with Fout of the VCO. This will cause a high impedance state on the phase detector and allow the output frequency to drift until the phase difference is enough to cause the phase detector to start sending signals to the charge pump to correct the difference. This slight variation will show up as a sub harmonic of the pfd signal in the passband of the loop filter which would result in a significant spur in the output of the VCO. It is recommended that the anti-backlash pulse be set to the 1.5ns which gives the best spur reduction for the TRF3761.

PFD_POL: Bit DB28 of register 1 sets the polarity of the PFD. A Low (0) selects a negative polarity, and a High (1) selects a positive polarity. By choosing the correct polarity, the TRF3761 will works with an external VCO having both positive and negative gain (Kv). For example if an external VCO has a Kv = –23MHz/V then the PFD polarity would need to be negative, so DB28 would be set to a Low (0). When using the internal VCO with a Kv of 23MHz/V, the PDF_POL should be set to 1.

RDiv: A 14-bit word programs the RDiv for the reference signal, DB25 is the MSB and DB12 is the LSB. RDiv value is determined by dividing the reference frequency by the channel step size. For example if the reference frequency is 10MHz and the channel step size is 200KHz then RDiv would be 50. This sets up the Fpfd for the phase detector, in other words the reference frequency will be divided down by a factor of RDiv which in this example is 50.

ICP: Bits <DB7, DB5> set the charge pump current.

$$I_{CP} = \frac{1.2\ V}{R_{bias1}} \times (N + 1) \times \frac{22.168}{8} \quad (1)$$

which reduces to:

$$I_{CP} = \frac{3.3252 \times (N + 1)}{R_{bias1}} \quad (2)$$

where N = decimal value of [Reg1 DB<7:5>]. The range is set by N and Rbias2. It is recommended that Icp be set to 7mA or <DB7, DB5>=101.

OUTBUF_EN_SEL: Output buffer on/off state is controlled through serial interface or an external pin. If bit DB10 is a 0 (default state) the output buffers state is elected through bit DB11. If DB10 is a 1, the buffers on/off are directly controlled by the OUTBU_EN pin.

RESET: Setting bit DB4 to 1, all registers are reset to default values.

Refer to **Register 1** under the *Application Information* section.

Register Address				Reference Frequency (Integer Part)							Refernece Frequency (Fractional Part)				
DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15

Reference Frequency Continued		VCO Frequency in MHz													START _CAL
DB16	DB17	DB18	DB19	DB20	DB21	DB22	DB23	DB24	DB25	DB26	DB27	DB28	DB29	DB30	DB31

Figure 85. Register 2

Table 2. Register 2: VCO Calibration

REGISTER 2 MAPPING				
Data Field	**DB31**	START_CAL		1 start calibration
	DB30	FOUT12	VCO frequency in MHz start calibration	
	DB29	FOUT11		
	DB28	FOUT10		
	DB27	FOUT9		
	DB26	FOUT8		
	DB25	FOUT7		
	DB24	FOUT6		
	DB23	FOUT5		
	DB22	FOUT4		
	DB21	FOUT3		
	DB20	FOUT2		
	DB19	FOUT1		
	DB18	FOUT0		
	DB17	REF_FRAC6	Reference frequency in MHz (fractional part)	0000000 = 0.00MHz 0000001 = 0.01MHz 0000010 = 0.02MHz . . . . . 1100011 = 0.99MHz
	DB16	REF_FRAC5		
	DB15	REF_FRAC4		
	DB14	REF_FRAC3		
	DB13	REF_FRAC2		
	DB12	REF_FRAC1		
	DB11	REF_FRAC0		
	DB10	REF6	Reference frequency in MHz (integer part)	0001010 =10MHz 0001011 =11MHz . . . . . 1101000 = 104MHz
	DB9	REF5		
	DB8	REF4		
	DB7	REF3		
	DB6	REF2		
	DB5	REF1		
	DB4	REF0		
Address Bits	**DB3**	0	Address Bits <3,0>=0001 for register 2	
	DB2	0		
	DB1	0		
	DB0	1		

Reference Frequency: The 14 bits <DB17, DB4> are used to specify the input reference frequency as multiples of 10kHz. Bits <DB10,DB4> specify the integer part of the reference frequency expressed in MHz. Bits <DB17,DB11> set the fraction part. Those values are then used during the calibration of the internal VCO. For example if using a 20MHz reference oscillator then bits<DB10,DB4> would be 0010100 and bits<DB17,DB11> would be 0000000. If the reference oscillator is 13.1MHz then bits<DB10,DB4> would be 0001101 and bits<DB17,DB11> would be 0001010.

Start Calibration: A 1 in DB31 starts the internal VCO calibration. When the calibration is complete, DB31 bit is internally reset to 0.

FOUT<12,0>: This 13-bit word <DB30,DB18> specifies the VCO output frequency in MHz. If output frequency is not a integer multiple of MHz, this value must be approximated to the closest integer in MHz.

Refer to **Register 2** under the *Application Information* section.

Register Address				Dual-Modulus Prescalar Mode		A-Counter						B-Counter			
DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15

B-Counter									Test MUX				Lock PLL	RSRV	RSRV
DB16	DB17	DB18	DB19	DB20	DB21	DB22	DB23	DB24	DB25	DB26	DB27	DB28	DB29	DB30	DB31

Figure 86. Register 3

Table 3. Register 3: A and B Counters

REGISTER 3 MAPPING				
Data Field	**DB31**	Rsrv	Reserved	
	DB30	Rsrv	Reserved	
	DB29	START_LK	Lock PLL to frequency	1 active
	DB28	TEST_MUX_3	See Table 4 for descriptions and settings.	0001 = LOCK_DETECT enabled
	DB27	TEST_MUX_2		
	DB26	TEST_MUX_1		
	DB25	TEST_MUX_0		
	DB24	B_12	13-bit B counter	
	DB23	B_11		
	DB22	B_10		
	DB21	B_9		
	DB20	B_8		
	DB19	B_7		
	DB18	B_6		
	DB17	B_5		
	DB16	B_4		
	DB15	B_3		
	DB14	B_2		
	DB13	B_1		
	DB12	B_0		
	DB11	A_5	6-bit A counter	
	DB10	A_4		
	DB9	A_3		
	DB8	A_2		
	DB7	A_1		
	DB6	A_0		
	DB5	PRESC_MOD1	Dual-modulus prescaler mode	<B5,B4>:00 for 8/9 <B5,B4>:01 for 16/17 <B5,B4>:10 for 32/33 <B5,B4>:11 for 64/65
	DB4	PRESC_MOD0		
Address Bits	**DB3**	0	Address Bits	<3,0>=0010 for register 3
	DB2	0		
	DB1	1		
	DB0	0		

B<12,0>: This 13-bit word <DB24,DB12> controls the value of the B counter of the N divider. The valid range is from 3 to 8191.

A<5,0>: These 6 bits <DB11,DB6> control the value of the A counter. The valid range is from 0 to 63.

PRESC_MOD<1,0>: These bits <DB5,DB4> define the mode of the dual-modulus prescaler according to Table 3.

START_LK: TRF3761 does not load the serial interface registers values into the dividers registers until bit DB29 of register 3 is set to 1. After TRF3761 is locked to the new frequency, bit DB29 is internally reset to 0.

Refer to **Register 3** under the *Application Information* section.

FUNCTIONAL DESCRIPTION

VCO

The TRF3761 integrates a high-performance, LC tank, voltage-controlled oscillator (VCO). For each of the devices of the TRF3761 family, the inductance and capacitance of the tank are optimized to yield the best phase-noise performance. The VCO output is fed externally and to the prescaler through a series of very low noise buffers, that greatly reduce the effect of load pulling onto the VCO.

Divide by 2, by 4, and Output Buffer

To extend the frequency coverage, the TRF3761 integrates a divide by 2 and by 4 with a low noise floor. The VCO signal is fed externally through a final open-collector differential-output buffer. This buffer is able to provide up to 3dBm (typical) of power into a 200Ω differential resistive load. The open-collector structure gives the flexibility to choose different load configurations to meet different requirements.

N-Divider

Prescaler Stage

This stage divides down the VCO frequency before the A and B counters. This is a dual-modulus prescaler and the user can select any of the following settings: 8/9, 16/17, 32/33, and 64/65. Prescaling is used due to the fact that the internal devices are limited in frequency operations of 200MHz. To determine the proper prescaler value, Fout which is the frequency out of the VCO is divided by the numerator of the prescaler if the answer is less than 200MHz then that is the prescalar to use, see Equation 3. If the value is higher than 200MHz then repeat this procedure with the next prescalar numerator until a value of 200MHz or less is achieved. See the Synthesizing a Selected Frequency in the Section 10 Register 3.

$$\frac{F_{OUT}}{Prescalar_{num}} \leq 200MHz \quad (3)$$

A and B Counter Stage

The TRF3761 includes a 6-bit A counter and a 13-bit B counter that operate on the output of the prescaler. The A counter can take values from 0 to 63, while the B counter can take values from 3 to 8191. Also, the value for the B counter must be greater than or equal to the value for the A counter. The A and B counter with the prescaler stage create the VCO N-divider, see Equation 4 and Equation 5. Refer to Synthesizing a Selected Frequency in the Section 10 Register 3.

$$N = \frac{F_{OUT}}{F_{PFD}} = \left(A_{COUNTER} + Prescalar_{num} \times B_{COUNTER}\right) \quad (4)$$

$$\frac{N}{Prescalar_{num}} = x_{integer} \times y_{decimal}, \Rightarrow$$

$$B_{COUNTER} = x_{integer} \text{ and } A_{COUNTER} = Prescalar_{num} \times y_{decimal} \quad (5)$$

Reference Divider

TRF3761 includes a 14-bit RDiv, also known as RDiv, that allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD) this clock is also known as F_{PFD} which is also the channel step size. Division ratios from 1 to 16,383 are allowed. To determine RDiv use Equation 6.

$$R_{DIV} = \frac{F_{REF\_IN}}{F_{PFD}} \quad (6)$$

The output frequency (Fout) is determined using Equation 7.

$$F_{OUT} = F_{PFD} \times N = \frac{F_{REF\_IN}}{R_{DIV}} \times \left(A_{COUNTER} + Prescalar_{num} \times B_{COUNTER}\right) \quad (7)$$

Phase Frequency Detector (PFD) and Charge Pump Stage

The outputs of the RDiv and the N counter are fed into the PFD stage, where the two signals are compared in frequency and phase. The TRF3761 features an anti-backlash pulse, whose width is controllable by the user through the serial programming interface. The PFD feeds the charge pump, whose output current pulses are fed into an external loop filter, which eventually produces the tuning voltage needed to control the integrated VCO to the desired frequency.

Mux Out

MUX_OUT pin (39) provides a communication port to the microcontroller circuit. See Table 4 in the Application Information section.

Div 1/2/4

Div 1/2/4 is the frequency divider for the TRF3761. This circuit can be programmed thru the serial programming interface (SPI) to divide the output frequency of the VCO by 1, 2 or 4. This feature allows for the same loop filter design to be used for any of the 3 divide by modes, 1, 2 and 4. For example, if the VCO is running at 1499MHz to 1608MHz band then with the same exact circuit, run the output in the divide by 2 mode 749.5MHz to 804MHz band or in the divide by 4 mode 374.75MHz to 402MHz.

Serial interface

The programming interface pins (3, 4, 5) to the chip are the serial programming interface (SPI). The interface requires a Clock, Data, and Strobe signal to operate. See timing diagram Figure 83.

CHIP ENABLE

This feature provides a way to shut down the chip when not needed in order to conserve power. CHIP_EN Pin (2) needs to be High for normal operation.

Buffer Power Down

PD_OUTBUFF pin (1), when enabled in software can provide a -40dB reduction in the output power while the VCO is locked and running. This feature is to help with isolation between RX and TX.

External VCO IN

EXT_VCO_IN pin (18) allows for the use of an external VCO to use the phase lock loop circuit in the TRF3761. This feature enables higher frequencies to be synthesized.

APPLICATION INFORMATION

Initial Calibration and Frequency Setup at Power Up

The integrated high performance VCO requires an internal frequency calibration at power up. To perform such calibration the following procedure is recommended:

- Apply 5V power supply to IC.
- Apply an input reference frequency to pin (38) and ensure the signal is stable.
- Turn on the TRF3761 using the chip enable pin (CHIP_EN, pin 2), by applying 5V.

Register 1

- Setup the device through Register 1 referencing Table 1.
  a. The first 4 bits of the 32-bit code sent to the chip are set DB <3:0> to 0000; which is the address of register 1.
  b. Bit 5, DB4, sets the soft reset for the chip. Soft reset allows for the registers to be reset without powering down the chip. If a soft reset is used then write to register 1 twice: once with DB4 set high and once with DB4 set low. Typically, this bit is only used when the chip has been powered up and registers 1, 2, and 3 have already been written to, so on power-up reset is not required, so DB4 is, by default, set low.
  c. DB <7: 5> sets the charge pump current based on the resistor value on pin 28 of the TRF3761 and the decimal value of Register 1, DB<7:5> used in Equation 1. This equation reduces to Equation 2, where N = decimal value of [Reg1 DB<7:5>].
  d. DB <9: 8> sets the mode of the chip. The mode is how the device will or will not divide down the VCO's frequency. There are 3 choices for the mode setting, divide by 1, 2 or 4 per Table 1. For example, if 393.75MHz is required from the TRF3761 which has a main frequency of 1575MHz then the divide-by-4 mode is chosen by setting DB <9: 8> to 10.
  e. DB <11:10> controls the output buffer. Both of these are set to 00 by default, so the buffer is controlled internally. See Table 1 for more information.
  f. DB <25:12> sets the RDiv value. Once the calculations under the *Synthesizing a Selected Frequency* section have been completed the value is known, based on the external reference oscillator. The value for R is entered into the DB <25:12>. For example, if the reference oscillator is at a frequency (F_{REF_IN}) of 61.44MHz and a channel step size of 120kHz is required, which is also the frequency (F_{PFD}) the phase frequency detector will use to compare against the VCO's output frequency (F_{OUT}), then F_{REF_IN} /F_{PFD} = 512, which is entered as follows: MSB: LSB 0001000000000.
  g. By default, DB <27:26> are set to 00 for a 1.5ns delay on the anti-backlash pulse width. See Table 1 for more information.
  h. DB 28 is set to 1 for positive by default. See Table 1 for more information.
  i. DB 29 is set to 0 for normal operation. See Table 1 for more information.
  j. DB 30 is set to 0 by default. See Table 1 for more information.
  k. DB 31 is set to 0 by default. See Table 1 for more information.

Register 2

- Initiate calibration procedure by programming register 2 as follows: Reference Table 2
  a. The first 4 bits of the 32-bit code sent to the chip are set DB <3:0> to 0001; which is the address of register 2.
  b. Use bits DB<17, 4> of register 2 to specify the input reference frequency in MHz. The value is split into an integer and a fraction part. For example: to insert a f_{REF} of 30.72MHz, set:
     – DB<10, 4> (integer part) equal to 0011110 (30) and
     – DB<17, 11> (fraction part) equal to 1001000 (72).

c. Set DB<30:18> of register 2 to the desired frequency. For example: 2200MHz would be 0100010011000 (2200).

d. Set DB31of register 2 to 1 to start the calibration. The VCO calibration runs for 5ms. During the cal procedure it will not be possible to program register 2 and 3. At the end of the calibration, bit DB31 of register 2 resets to 0.

e. Subsequent frequency programming requires DB31 to be set to 0.

Register 3

- Completion of the frequency set up, on initial calibration, cannot proceed until 5ms has elapsed, due to full calibration, then it will require that the A and B values, the prescalar ratio, be known. See *Synthesizing a Selected Frequency* section below for calculation. Reference Table 3.

a. The first 4 bits of the 32-bit code sent to the chip are set DB <3:0> to 0010; which is the address of register 3.

b. DB<5:4> sets the prescalar ratio, 8/9, 16/17, 32/33, 64/65. For example: if 16/17 are required, set the register bits DB<5:4> to 01.

c. DB<11:6> sets the A value for the N counter. For example: if A is 4, set DB<11:6> as follows: 000100 (4).

d. DB<24:12> sets the B value for the N counter. For example: if B is 1156, set DB<24:12> as follows: 0010010000100 (4).

e. DB<28:25> sets the TEST_MUX. This allows the user to check via the microcontroller the state of the TRF3761 by programming it to one of 6 states. The most common state to use is the Digital lock Detect which places the pin in a logic high state with indicates the VCO is locked.

Table 4. MUX-Out Settings

STATE	DB<28:25>	STATE	DB<28:25>
3-state o/p (High impedance state on Pin 39)	0000	RDiv o/p (Shows R-value on Pin 39)	0100
Digital lock Detect (High when locked on Pin 39)	0001	Analog lock detect (High when locked on Pin 39)	0101
N-Divider o/p (Shows N-value on Pin 39)	0010	Read back (read back register settings)	0110
DVDD (internal TI use)	0011	DGND (internal TI use)	0111

f. DB29 sets the START LOCK, which is set to 0, on the initial frequency setup and then set to 1 on additional frequency changes.

Once all registers are written, the TRF3761 will lock to the desired frequency. In order to change the frequency once the initial calibration is complete, only registers 2 and 3 need to be reprogrammed. No calibration is required.

Re-Calibration After Power Up

Assuming the TRF3761 is powered up and operational, a VCO calibration is also possible without powering down the IC. To perform such calibration the following procedure is recommended:

- Set bit DB4 (RESET) of register 1 to 1. This performs a software reset and clears all registers of VCO calibration data. Once the reset command is issued then DB4 of register 1 will need to be set to 0.
- Repeat the *Initial Calibration and Frequency setup at Power up* section, skipping the power up section and performing the register programming sequence.

Synthesizing a Selected Frequency

The TRF3761 is an integer-N PLL synthesizer, and because of its flexibility (14-bit RDiv, 6-bit A counter, 13-bit B counter, and dual modulus prescaler), is ideal for synthesizing virtually any desired frequency. If synthesizing a 900MHz local oscillator, with spacing capability (minimum frequency increment) of 200kHz, as in a typical GSM application, the choice of the external reference oscillator is beyond the scope of this section. However, if a 10MHz reference is selected, the settings are calculated to yield the desired output frequency and channel spacing. There is more than one solution to a specific set of conditions, so below is one way of achieving the desired result. First, select the appropriate RDiv counter value. Since a channel spacing of 200kHz is desired, the F_{PFD} is set to 200kHz. Calculate the RDiv value through:

$RDiv = F_{REFIN}/F_{PFD} = 10MHz/ 200kHz = 50.$

Assume a prescaler value of 8/9 is selected. This is a valid choice, since the prescaler output is well within the 200MHz limit (900MHz / 8 = 112.5MHz). Select the appropriate A and B counter values.

$RFOUT = F_{PFD} \times N = (F_{REFIN} / RDiv) \times (A \text{ counter} + \text{Prescalar numerator} \times B \text{ counter}).$

Therefore, the following equation must be solved:

$900MHz = 200kHz \times (A + 8 \times B).$

There are many solutions to this single equation with two unknowns; there are some basic constraints on the solution, since $3 \le B \le 8191$, and also $B \ge A$. So, if A = 4, solving the equation yields B = 562. One complete solution would be to choose:

RDiv = 50, A counter = 4, Bcounter = 562 and Prescalar = 8/9

resulting in the desired N counter value = 4500. This is how the A counter, B counter and prescalar make up the N counter.

When this procedure is complete the values for the N counter , R, and the prescalar ratio should be known. Registers 2 and 3 need to be set up for operation of the chip. See Table 2 and Table 3 for this procedure. Register 2 bits <DB30:DB18> 12:0 set the output frequency of the device along with register 3. See the *N-Divider* section under the *Functional Description*.

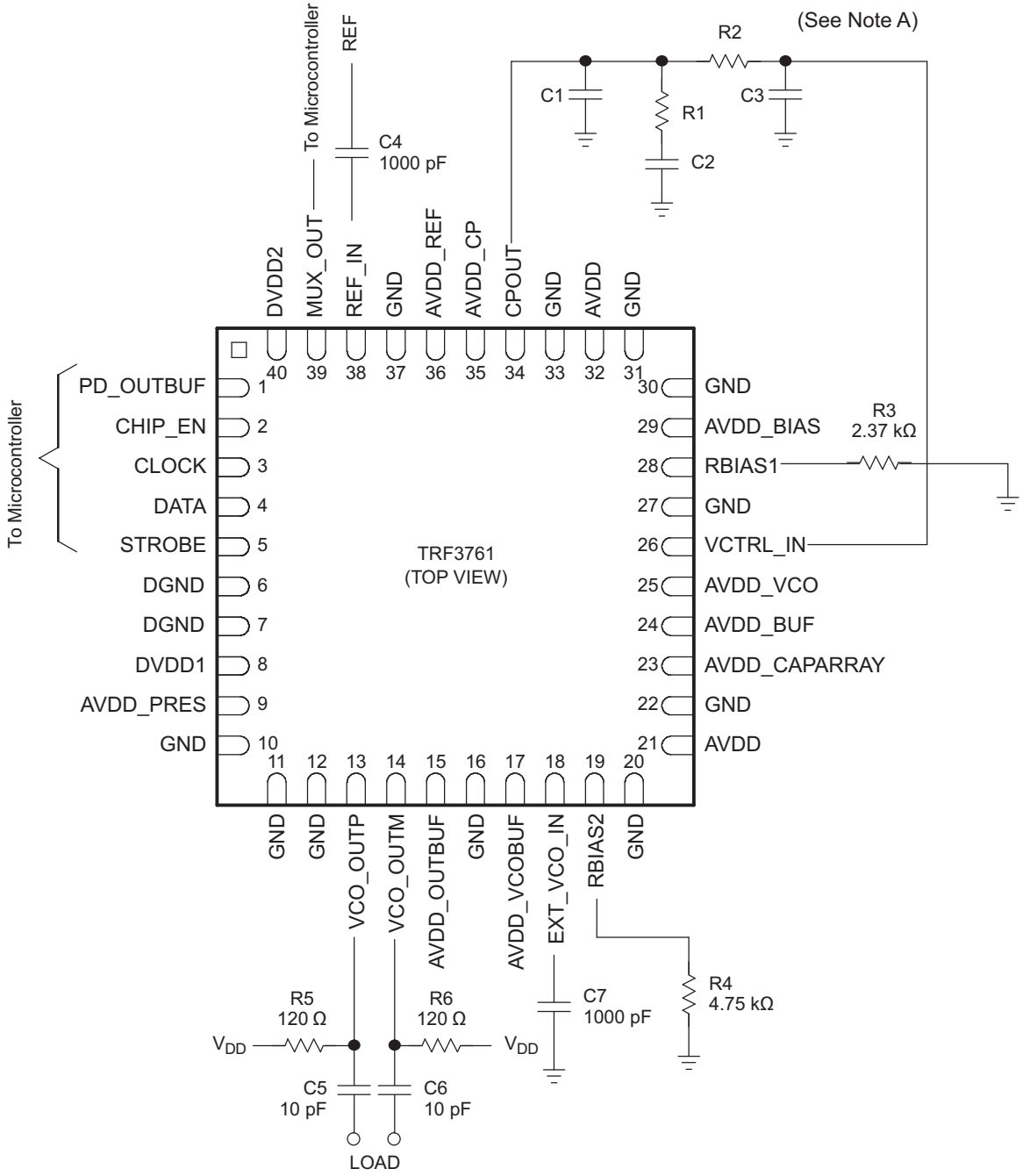
Application Schematic

Figure 87 shows a typical application schematic for the TRF3761. In this example, the output signal is taken differential using the 2 resistive pull-up resistors of the final output buffer. A single-ended and tuned load configuration is also available.

The loop filter components:

C1 = 303pF, R1 = 8.87kΩ, C2 = 1650pF, R2 = 3.4kΩ, C3 = 330pF

are typical ones used for the plots shown above. Those values can be optimized differently according to the requirements of the different applications.



A. Refer to the Application Information section Loop Filter Design.

Figure 87. TRF3761 Application Schematic

Loop Filter Design

Numerous methodologies and design techniques exist for designing optimized loop filters for particular applications. The loop filter design can affect the stability of the loop, the lock time, the bandwidth, the extra attenuation on the reference spurs, etc. The role of the loop filter is to integrate and lowpass the pulses of the charge pump and eventually yield an output tuning voltage that drives the VCO. Several filter topologies can be implemented, including both passive and active. In this section, a third-order passive filter is used. For this example, assume these several design parameters. The internal VCO has a value of 23MHz/V, meaning that in the linear region, changing the tuning voltage of the VCO by 1V induces a change of the output frequency of about 23MHz. It is known that N = 4500 and Fpfd = 200kHz from our previous example. It is assumed that current setting in register 1 <DB7:DB5> is set to 100 and sets a maximum current of 5.6mA.TI recommends an Icp of 5.6mA, which give the best spur performance, but can be changed for different application. In addition, the bandwidth of the loop filter must be determined. This is a critical consideration as it affects the lock time of the system. Assuming an approximate bandwidth of around 20kHz is required and that for stability a phase margin of about 45 degrees is desired, the following values for the components of the loop filter can be derived. There is almost an infinite number of solutions to the problem of designing the loop filter and the designer is called to make tradeoff decisions for each application. Texas Instruments has provided a loopfilter program in the product folder for the TRF3761.

Some terms are interchangeable and are described and equated here:

- F_{com} = F_{PDF} which identify the comparing frequency or phase detector frequency which is also equal to the system channel step size. F_{OUT} must be a multiple of F_{com}.
- F_{min} is the lower frequency of the design band.
- F_{max} is the upper frequency of the design band.
- F_{ref} is the reference frequency for the PLL. Fref must be a multiple of F_{com}.
- K_{vco} = Kv expressed in MHz per Volt (MHz/V) which is the gain of the VCO. The TRF3761 internal VCO has a Kv = 23MHz/V.
- I_{cp} is the charge pump current. The TRF3761 is typically set to 5.6mA.
- F_c is the loop filter bandwidth which should be no more than 1/10 F_{com}.
- ϕ is phase margin in degrees. Values should be between 30 and 70. The higher the phase margin the better the stability of the PLL but the slower the lock time. 45 degrees is a good tradeoff.
- T3/T1 in percent is the percentage of the poles in the loop filter. Usually set to 45%. The higher the value (closer to 100%) the more the spurs are attenuated, but peaking occurs in the pass band of the loop filter.

$$F_{OUT} = \sqrt{F_{min}F_{max}} \tag{8}$$

$$N = \frac{F_{OUT}}{F_{com}} \tag{9}$$

$$\varpi_C = 2\pi F_C \tag{10}$$

$$T1 = \frac{\left(\frac{1}{\cos\phi}\right) - \tan\phi}{\varpi_C\left(1 + \frac{T3}{T1}\right)} \tag{11}$$

$$T3 = \left(\frac{T3}{T1}\right)T_1 \tag{12}$$

$$T2 = \frac{1}{\varpi_C^2(T1+T3)} \tag{13}$$

$$C1 = \frac{T1}{T2} \times \frac{K_{VCO}K\phi}{\varpi_C^2 N} \times \left[\frac{1 + (\varpi_C T2)^2}{\left(1 + \varpi_C^2 T1^2\right)\left(1 + \varpi_C^2 T3^2\right)}\right]^{\frac{1}{2}} \tag{14}$$

$$C2 = C1\left(\frac{T2}{T1} - 1\right), \quad C3 = \frac{C1}{10} \tag{15}$$

$$R1 = \frac{T2}{C2}, \quad R2 = \frac{T3}{C3} \tag{16}$$

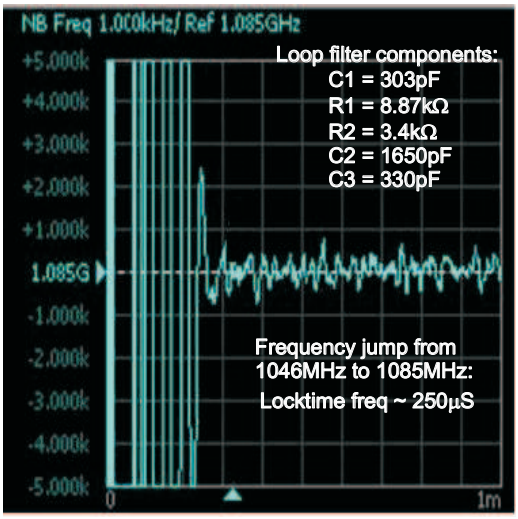


Figure 88. Frequency Locktime

Loop Filter Design Example

Given these parameters which were used for the lock time plot Figure 88:

- F_{min} = 2085 MHz
- F_{max} = 2175 MHz
- F_{com} = 400 KHz
- Icp = 4.2mA
- Kvco = 23 MHz
- Fc = 20 KHz
- Phase Margin = 45 degrees
- T3/T1 = 45%

Calculate F_{OUT} of design

$$F_{OUT} = \sqrt{F_{min}F_{max}} = 2130\text{MHz (rounded up)} \quad (17)$$

Next calculate N

$$N = \frac{F_{OUT}}{F_{com}} = 5325 \quad (18)$$

Then calculate ωc

$$\varpi_c = 2\pi F_c = 125.66 \times 10^3 \quad (19)$$

Now calculate T1-T3 to give the RC time constants.

$$T_1 = \frac{\left(\frac{1}{\cos\phi}\right) - \tan\phi}{\varpi_c\left(1 + \frac{T_3}{T_1}\right)} = 2.3 \times 10^{-6} \quad (20)$$

Use T1 to find T3

$$T_3 = \left(\frac{T_3}{T_1}\right)T_1 = 1 \times 10^{-6} \quad (21)$$

Then use T1 and T3 to find T2

$$T_2 = \frac{1}{\omega_C^2 (T_1 + T_3)} = 19.2 \times 10^{-6} \quad (22)$$

Now C1, C2, C3, R1, and R2 are calculated using T1, T2, and T3.

$$C1 = \frac{T_1}{T_2} \times \frac{K_{VCO} K\phi}{\omega_c^2 N} \times \left[\frac{1 + (\omega_c T_2)^2}{\left(1 + \omega_c^2 T_1^2\right)\left(1 + \omega_c^2 T_3^2\right)} \right]^{\frac{1}{2}} = 338.75pF \quad (23)$$

$$C2 = C1\left(\frac{T_2}{T_1} - 1\right) = 2524.14pF \quad (24)$$

$$C3 = \frac{C1}{10} = 33.87pF \quad (25)$$

Now using C2 and T2, find R2. Use C3 and T3 to find R3

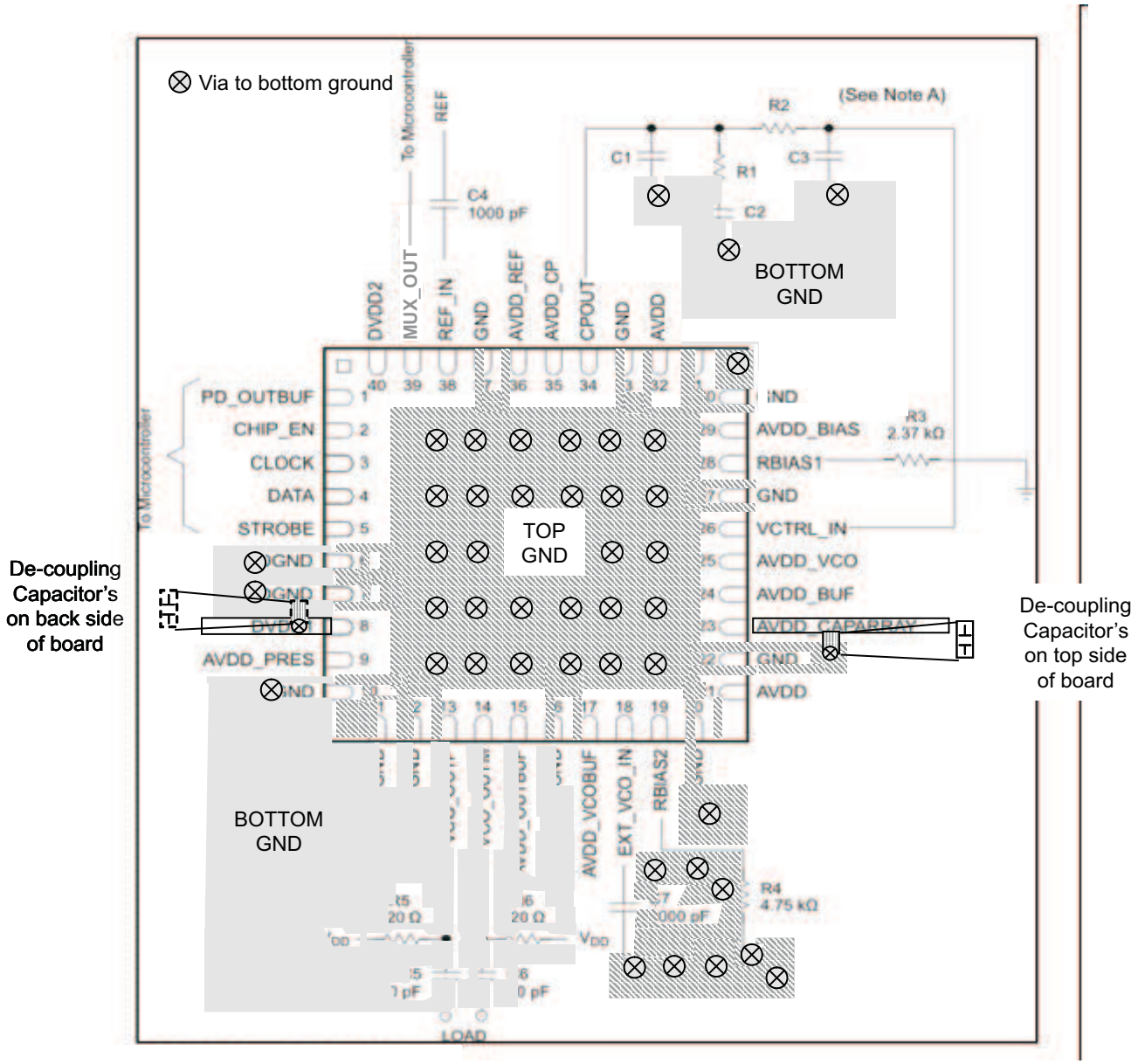
$$R2 = \frac{T_2}{C_2} = 7.61k\Omega \quad (26)$$

$$R3 = \frac{T_3}{C_3} = 30.2k\Omega \quad (27)$$

R2 x C3 can be scaled using T3, so if C3 = 330pF, then R2 = 3.03 kΩ => 3.4 kΩ in the loop filter. R1 × C2 can be scaled using T2. Scaling these values helps to improve the lock time. The actual values used in the lock time plot were optimized for lock time as well as using real valued components. The values in figure 62 were taken from the current EVM schematic.

Layout/PCB Considerations

This section of the design of the complete PLL is of paramount importance in achieving the desired performance. Wherever possible, a multi-layer PCB board should be used, with at least one dedicated ground plane. A dedicated power plane (split between the supplies if necessary) is also recommended. The impedance of all RF traces (the VCO output and feedback into the PLL) should be controlled to 50Ω. All small value (10pF and 0.1uF) decoupling capacitors should be placed as close to the device pins as possible. It is also recommended that both top and bottom layers of the circuit board be flooded with ground, with plenty of ground vias dispersed as appropriate. Because the digital lines are not in use during normal operation of the device and are only used to program the device on start up and during frequency changes the analog grounds (GND) and digital grounds (DGND) are tied to the same ground plane. The most sensitive part of any PLL is the section between the charge pump output and the input to the VCO. This includes the loop filter components, and the corresponding traces. The charge pump is a precision element of the PLL and any extra leakage on its path can adversely affect performance. Extra care should be given to ensure that parasitics are minimized in the charge pump output, and that the trace runs are short and optimized. Similarly, it is also recommend that extra care is taken in ensuring that any flux residue is thoroughly cleaned and moisture baked out of the PCB. From an EMI perspective, and since the synthesizer is typically a small portion of a bigger, complex circuit board, shielding is recommended to minimize EMI effects.



A. See the Application Information section for Loop Filter Design procedures.

Figure 89. TRF3761 Layout

Application Example for a High Performance RF Transmit Signal Chain

Much in the same way as described above, the TRF3761 is an ideal synthesizer to use in implementing a complete high performance RF transmitter chain such as the TSW3000 and TSW3003 Demonstration kits. Using a complete suite of high performance Texas Instruments components, a state-of-the-art transmitter can be implemented featuring excellent performance. Texas Instruments offers ideal solutions for the digital-to-analog conversion portion of transmitter as well as the analog and RF components needed to complete the transmitter. The baseband digital data is converted to I and Q signals through the dual DAC5687, which features a 16-bit interpolating dual digital-to-analog converter (DAC). The device incorporates a digital modulator, independent differential offset control, and I/Q amplitude control. The device is typically used in baseband mode or in low IF mode in conjunction with an analog quadrature modulator. The DAC5687, after filtering, feeds a TRF3703, which is a direct, upconversion IQ modulator. This device accepts a differential input voltage quadrature signal at baseband or low IF frequencies and outputs a modulated RF signal based on the LO drive frequency. The LO

drive input of the IQ modulator is generated by the TRF3761. The TRF3761 is a family of high performance, highly integrated frequency synthesizers, optimized for wireless infrastructure applications. The TRF3761 includes an integrated VCO and integer-N PLL. Different members of the TRF3761 family can be chosen for application specific VCO frequency ranges. In addition, the CDC7005 clocking solution can be used to clock the DAC and other portions of the transmitter. A block diagram of the proposed architecture is shown in Figure 90 and Figure 91. For more details, contact Texas Instruments directly.

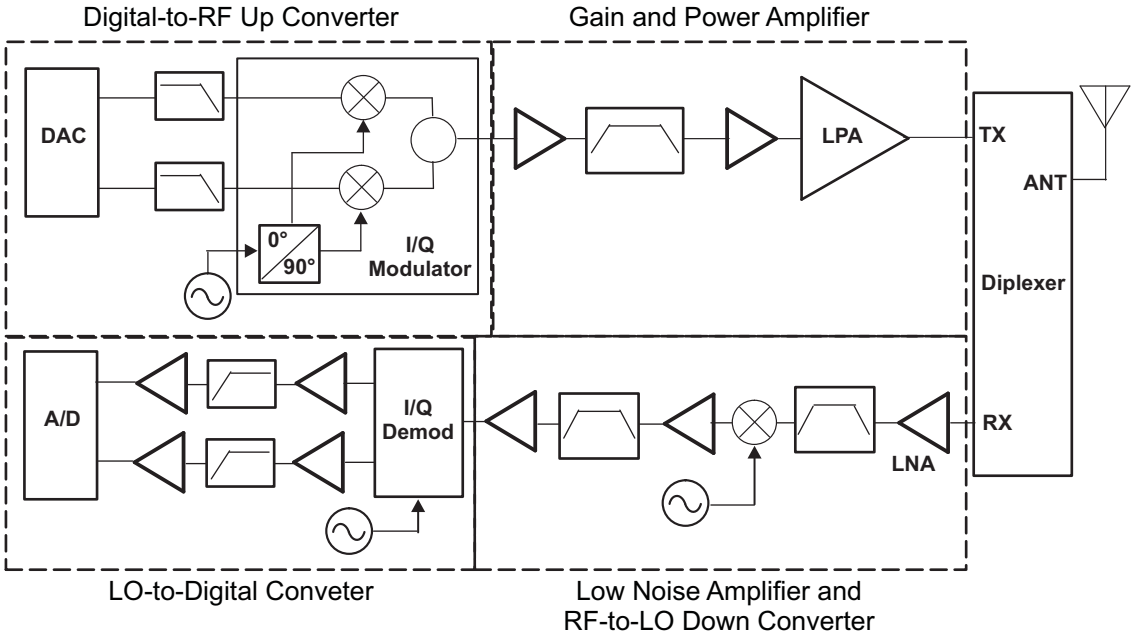


Figure 90. Transmit Chain Block Diagram

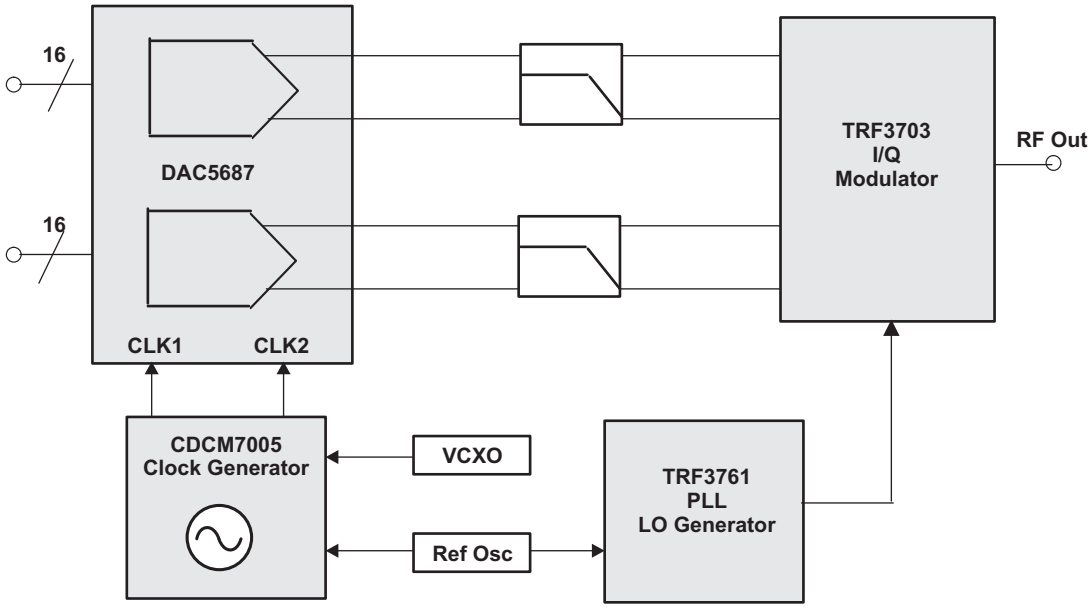


Figure 91. Transmit Chain Block Diagram

REVISION HISTORY

Changes from Revision I (March 2008) to Revision J **Page**

- Changed Figure 2 17
- Changed Figure 3 17
- Changed Figure 4 17
- Changed Figure 5 17
- Changed Figure 6 17
- Changed Figure 7 17
- Changed Figure 8 18
- Changed Figure 9 18
- Changed Figure 10 18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF3761-AIRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -A	Samples
TRF3761-AIRHARG4	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -A	Samples
TRF3761-AIRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -A	Samples
TRF3761-AIRHATG4	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -A	Samples
TRF3761-BIRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -B	Samples
TRF3761-BIRHARG4	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -B	Samples
TRF3761-BIRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -B	Samples
TRF3761-BIRHATG4	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -B	Samples
TRF3761-CIRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -C	Samples
TRF3761-CIRHATG4	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -C	Samples
TRF3761-DIRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -D	Samples
TRF3761-DIRHARG4	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -D	Samples
TRF3761-DIRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -D	Samples
TRF3761-DIRHATG4	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -D	Samples
TRF3761-EIRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -E	Samples
TRF3761-EIRHARG4	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -E	Samples
TRF3761-EIRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -E	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF3761-EIRHATG4	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -E	Samples
TRF3761-FIRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -F	Samples
TRF3761-FIRHARG4	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -F	Samples
TRF3761-FIRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -F	Samples
TRF3761-FIRHATG4	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -F	Samples
TRF3761-GIRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -G	Samples
TRF3761-GIRHARG4	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -G	Samples
TRF3761-GIRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -G	Samples
TRF3761-GIRHATG4	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -G	Samples
TRF3761-HIRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -H	Samples
TRF3761-HIRHARG4	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -H	Samples
TRF3761-HIRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -H	Samples
TRF3761-HIRHATG4	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -H	Samples
TRF3761-JIRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -J	Samples
TRF3761-JIRHATG4	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF3761 -J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

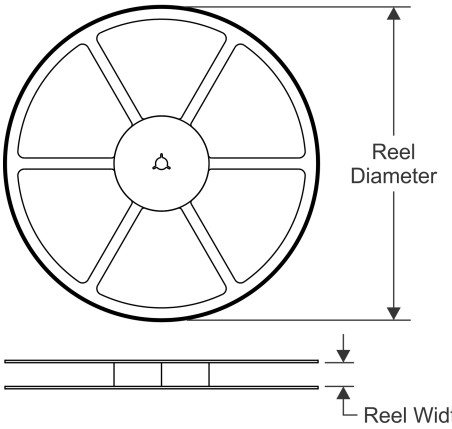
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

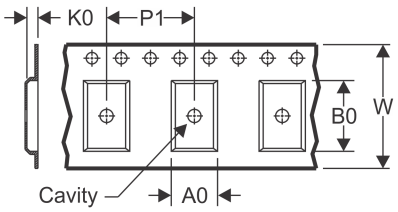
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

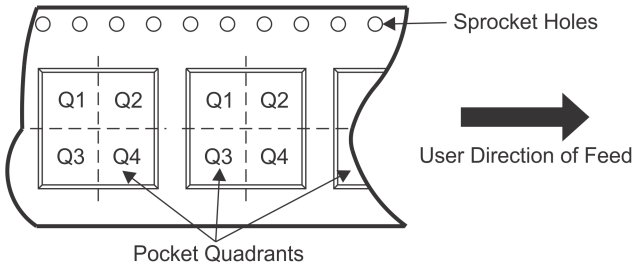


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

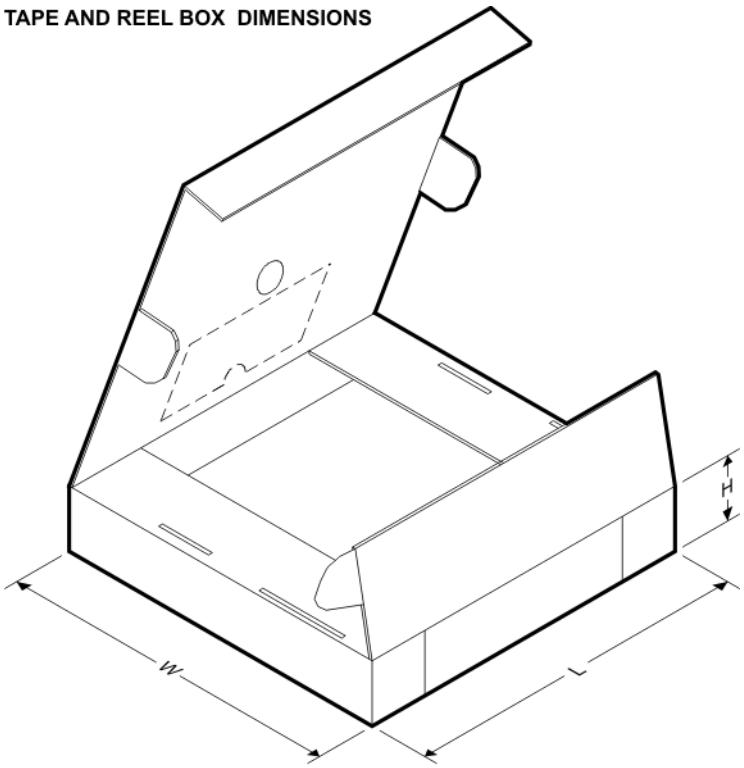
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF3761-AIRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-AIRHAT	VQFN	RHA	40	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-BIRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-BIRHAT	VQFN	RHA	40	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-CIRHAT	VQFN	RHA	40	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-DIRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-DIRHAT	VQFN	RHA	40	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-EIRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-EIRHAT	VQFN	RHA	40	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-FIRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-FIRHAT	VQFN	RHA	40	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-GIRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-GIRHAT	VQFN	RHA	40	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-HIRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-HIRHAT	VQFN	RHA	40	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TRF3761-JIRHAT	VQFN	RHA	40	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

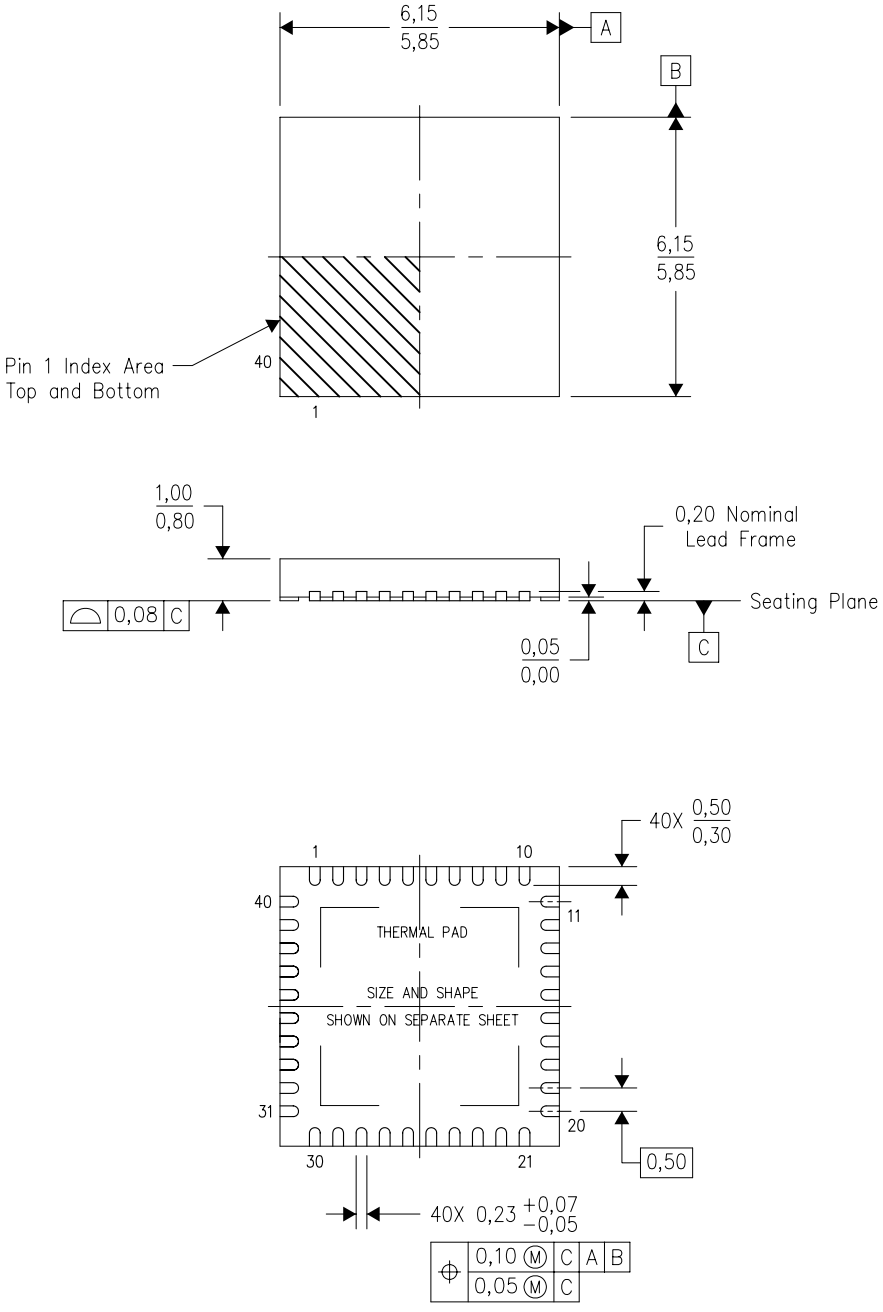
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF3761-AIRHAR	VQFN	RHA	40	2500	336.6	336.6	28.6
TRF3761-AIRHAT	VQFN	RHA	40	250	336.6	336.6	28.6
TRF3761-BIRHAR	VQFN	RHA	40	2500	336.6	336.6	28.6
TRF3761-BIRHAT	VQFN	RHA	40	250	336.6	336.6	28.6
TRF3761-CIRHAT	VQFN	RHA	40	250	336.6	336.6	28.6
TRF3761-DIRHAR	VQFN	RHA	40	2500	336.6	336.6	28.6
TRF3761-DIRHAT	VQFN	RHA	40	250	336.6	336.6	28.6
TRF3761-EIRHAR	VQFN	RHA	40	2500	336.6	336.6	28.6
TRF3761-EIRHAT	VQFN	RHA	40	250	336.6	336.6	28.6
TRF3761-FIRHAR	VQFN	RHA	40	2500	336.6	336.6	28.6
TRF3761-FIRHAT	VQFN	RHA	40	250	336.6	336.6	28.6
TRF3761-GIRHAR	VQFN	RHA	40	2500	336.6	336.6	28.6
TRF3761-GIRHAT	VQFN	RHA	40	250	336.6	336.6	28.6
TRF3761-HIRHAR	VQFN	RHA	40	2500	336.6	336.6	28.6
TRF3761-HIRHAT	VQFN	RHA	40	250	336.6	336.6	28.6
TRF3761-JIRHAT	VQFN	RHA	40	250	336.6	336.6	28.6

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

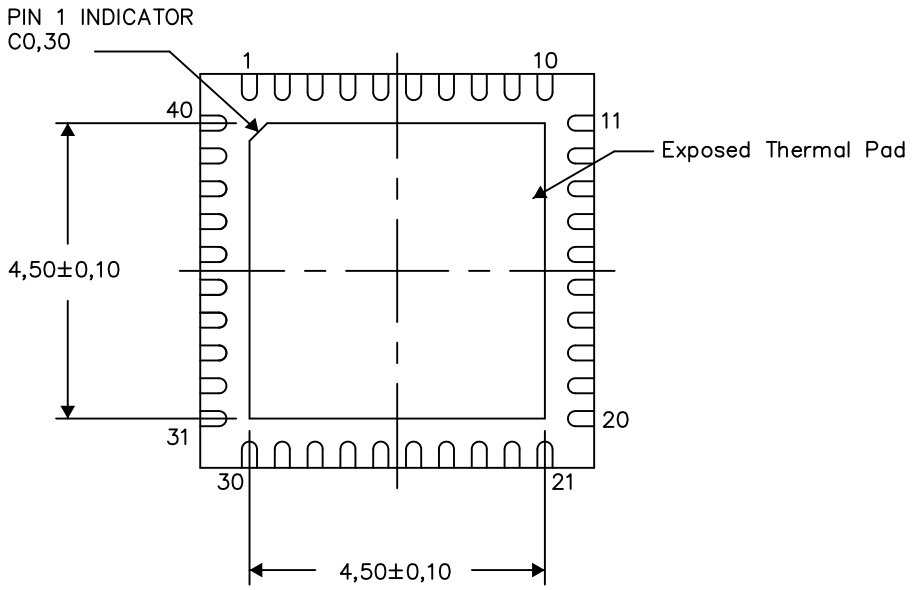
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206355–4/U 12/12

NOTES: A. All linear dimensions are in millimeters

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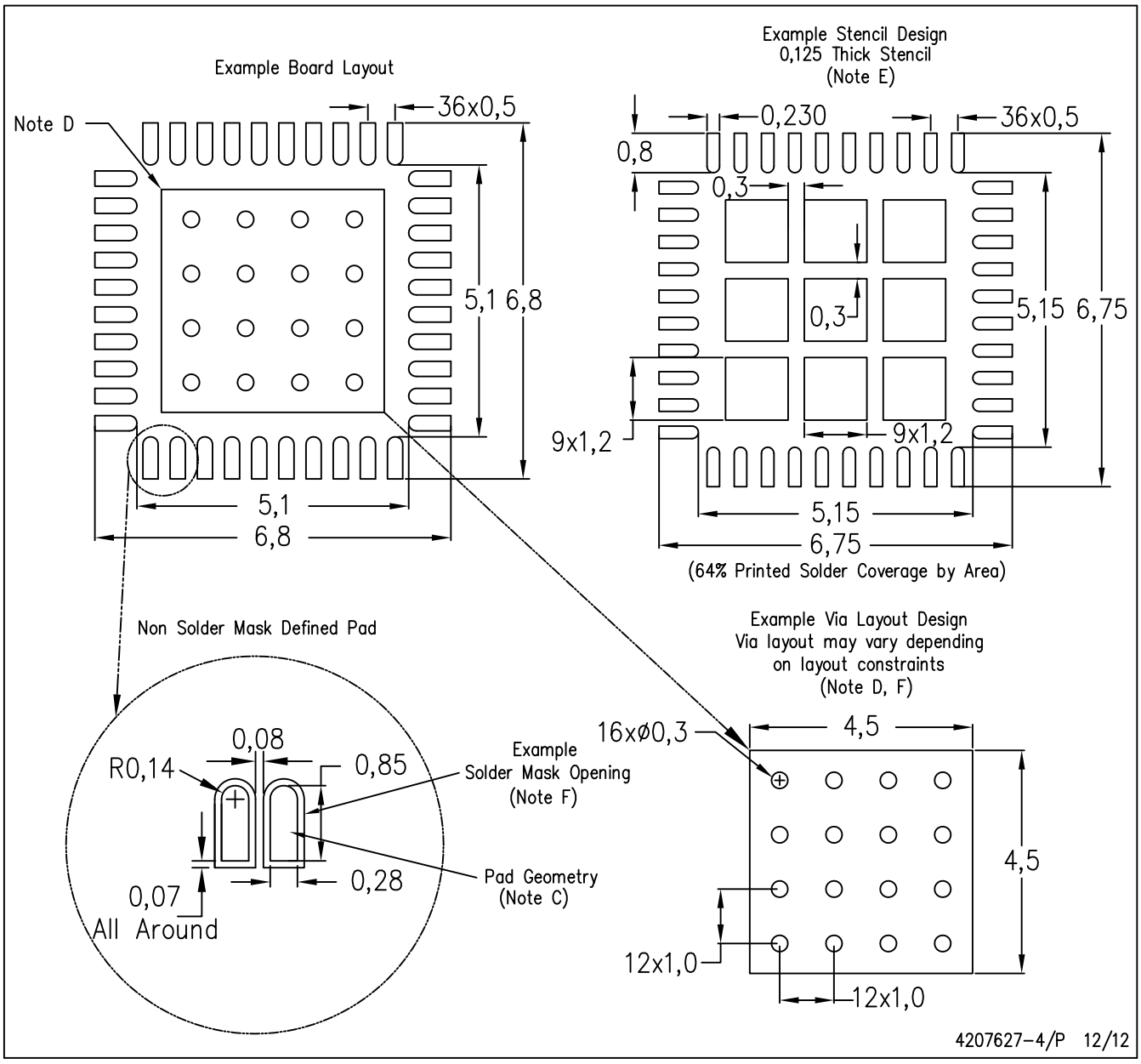

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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