Integer-N/Fractional-N PLL with Integrated VCO

Check for Samples: TRF3765

FEATURES

- **Output Frequencies: 300 MHz to 4.8 GHz**
- **Low-Noise VCO: –133 dBc/Hz (1-MHz Offset, f_{OUT} = 2.65 GHz)**
- **13-/16-Bit Reference/Feedback Divider**
- **25-Bit Fractional-N and Integer-N PLL**
- **Low RMS Jitter: 0.35 ps**
- **Input Reference Frequency Range: 0.5 MHz to 350 MHz**
- **Programmable Output Divide-by-1/-2/-4/-8**
- **Four Differential LO Outputs**
- **External VCO Input with Programmable VCO On/Off Control**

APPLICATIONS

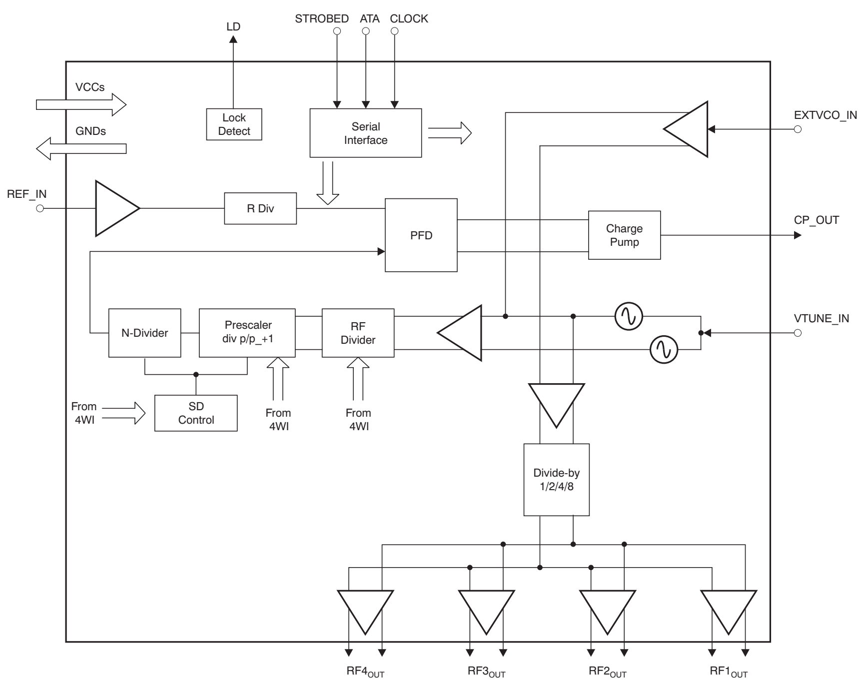
- **Wireless Infrastructure**
- **Wireless Local Loop**
- **Point-to-Point Wireless Access**
- **Wireless MAN Wideband Transceivers**

DESCRIPTION

The TRF3765 is a wideband Integer-N/Fractional-N frequency synthesizer with an integrated, wideband voltage-controlled oscillator (VCO). Programmable output dividers enable continuous frequency coverage from 300 MHz to 4.8 GHz. Four separate differential, open-collector RF outputs allow multiple devices to be driven in parallel without the need of external splitters.

The TRF3765 also accepts external VCO input signals and allows on/off control through a programmable control output. For maximum flexibility and wide reference frequency range, wide-range divide ratio settings are programmable and an off-chip loop filter can be used.

The TRF3765 is available in an RHB-32 QFN package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TRF3765	RHB-32	RHB	–40°C to +85°C	TRF3765IRHB	TRF3765IRHBT	Tape and Reel, 250
					TRF3765IRHBR	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
Supply voltage range(2)	All VCC pins except VCC_TK	–0.3 to +3.6	V
	VCC_TK	–0.3 to +5.5	V
Digital I/O voltage range		–0.3 to V_I + 0.5	V
Operating virtual junction temperature range, T_J		–40 to +150	°C
Operating ambient temperature range, T_A		–40 to +85	°C
Storage temperature range, T_{stg}		–40 to +150	°C
ESD ratings	Human body model, HBM	1000	V
	Charged device model, CDM	1500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{CC}	Power-supply voltage	3.0	3.3	3.6	V
VCC_TK	3.3-V to 5.5-V power-supply voltage	3.0	3.3	5.5	V
T_A	Operating ambient temperature range	–40		+85	°C
T_J	Operating virtual junction temperature range	–40		+150	°C

THERMAL INFORMATION

THERMAL METRIC(1)		TRF3765	UNITS
		RHB	
		32 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	31.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	21.6	
θ_{JB}	Junction-to-board thermal resistance	5.6	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	5.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

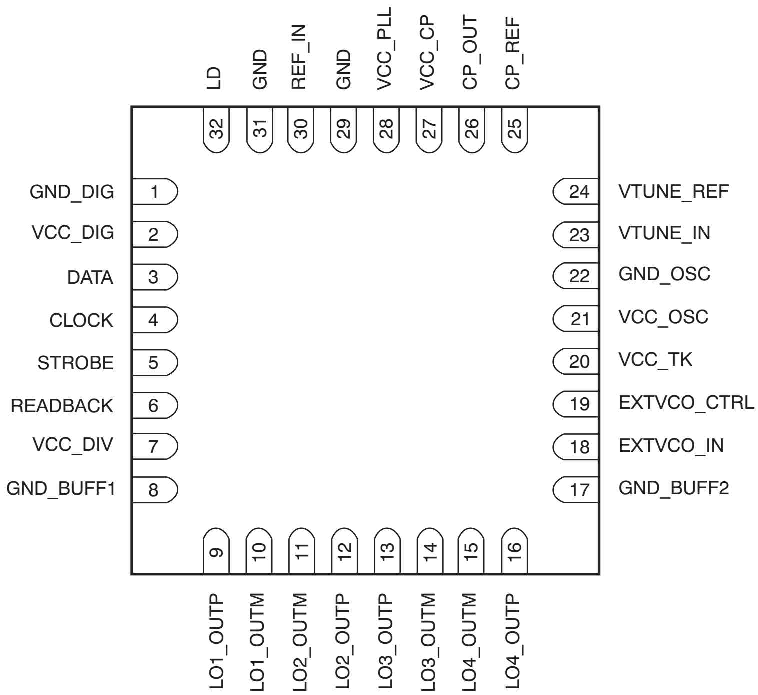
At T_A = +25°C and power supply = 3.3 V, unless otherwise noted.

PARAMETERS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PARAMETERS							
I_{CC}	Total supply current		Internal VCO, 1 output buffer on, divide-by-1		115		mA
			Internal VCO, 4 output buffers on, divide-by-1		190		mA
			Internal VCO, 1 output buffer on, divide-by-8		120		mA
			Internal VCO, 4 output buffers on, divide-by-8		182		mA
			External VCO mode, 1 output buffer on, divide-by-1		89		mA
DIGITAL INTERFACE							
V_{IH}	High-level input voltage			2	3.3		V
V_{IL}	Low-level input voltage			0		0.8	V
V_{OH}	High-level output voltage		Referenced to VCC_DIG	0.8 × V_{CC}			V
V_{OL}	Low-level output voltage		Referenced to VCC_DIG			0.2 × V_{CC}	V
REFERENCE OSCILLATOR PARAMETERS							
f_{REF}	Reference frequency			0.5[(1)]		350[(1)]	MHz
	Reference input sensitivity			0.2		3.3	V_{PP}
	Reference input impedance		Parallel capacitance, 10 MHz		2		pF
			Parallel resistance, 10 MHz		2500		Ω
PLL							
f_{PFD}	PFD frequency			0.5		65[(2)]	MHz
I_{CP_OUT}	Charge pump current		4WI programmable; ICP[4..0] = 00000[(3)]		1.94		mA
	In-band normalized phase noise floor		Integer mode		–221		dBc/Hz
INTERNAL VCO							
f_{VCO}	VCO frequency range		Divide-by-1	2400		4800	MHz
K_V	VCO gain		V_{CP} = 1 V		–65		MHz/V
	VCO free-running phase noise, f_{VCO} = 2650 MHz	VCC_TK = 3.3 V	At 10 kHz		–82		dBc/Hz
			At 100 kHz		–110		dBc/Hz
			At 1 MHz		–130		dBc/Hz
			At 10 MHz		–149		dBc/Hz
			At 40 MHz		–155		dBc/Hz
		VCC_TK = 5 V	At 10 kHz		–89		dBc/Hz
			At 100 kHz		–113		dBc/Hz
			At 1 MHz		–133		dBc/Hz
			At 10 MHz		–151		dBc/Hz
			At 40 MHz		–156		dBc/Hz
CLOSED-LOOP PLL/VCO							
	Integrated RMS jitter[(4)]		Fractional mode, f_{OUT} = 2.6 GHz, f_{PFD} = 30.72 MHz[(5)]		0.36		ps
			Integer mode, f_{OUT} = 2.6 GHz, f_{PFD} = 1.6 MHz		0.52		ps
RF OUTPUT/INPUT							
f_{OUT}	Output frequency range		Divide-by-1	2400		4800	MHz
			Divide-by-2	1200		2400	MHz
			Divide-by-4	600		1200	MHz
			Divide-by-8	300		600	MHz
P_{LO}	Output power[(6)]		Differential, divide-by-1, one output buffer on, maximum BUFOUT_BIAS		6.5		dBm
	External VCO input maximum frequency		20-dB gain loss, VCO pass-through, no PLL		9000		MHz
	External VCO input minimum frequency		20-dB gain loss, VCO pass-through, no PLL, divide-by-1		15		MHz
	External VCO input level				0		dBm

(1) See *Application Information* section for discussion of VCO calibration clock limitations on reference clock frequency.
(2) See *Application Information* section for discussion on PFD frequency selection and calibration logic frequency limitations.
(3) See the *4WI Register Descriptions* section for all possible programmable charge pump currents.
(4) Integrated from 1 kHz to 10 MHz.
(5) See *Application Information* section for information on loop filter characteristics.
(6) See *Application Information* section for external output buffers details.

DEVICE INFORMATION

RHB PACKAGE
QFN-32
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
CLOCK	4	I	Serial programming interface, clock input
CP_OUT	26	O	Charge pump output
CP_REF	25		Charge pump reference ground
DATA	3	I	Serial programming interface, data input
EXTVCO_CTRL	19	O	Digital control to enable/disable external VCO
EXTVCO_IN	18	I	External VCO input
GND	29		Ground
GND	31		Ground
GND_BUFF1	8		Output buffer ground
GND_BUFF2	17		Output buffer ground
GND_DIG	1		Digital ground
GND_OSC	22		VCO core ground
LD	32	O	Lock detector output
LO1_OUTM	10	O	LO1 output: negative terminal
LO1_OUTP	9	O	LO1 output: positive terminal
LO2_OUTM	11	O	LO2 output: negative terminal
LO2_OUTP	12	O	LO2 output: positive terminal
LO3_OUTM	14	O	LO3 output: negative terminal
LO3_OUTP	13	O	LO3 output: positive terminal
LO4_OUTM	15	O	LO4 output: negative terminal
LO4_OUTP	16	O	LO4 output: positive terminal

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
READBACK	6	O	Serial programming interface, readback
REF_IN	30	I	Reference signal input
STROBE	5	I	Serial programming interface, latch enable
VCC_CP	27		Charge pump power supply
VCC_DIG	2		Digital power supply
VCC_DIV	7		Divider power supply
VCC_OSC	21		VCO core power supply
VCC_PLL	28		PLL power supply
VCC_TK	20		VCO LC tank power supply
VTUNE_IN	23		VCO control voltage
VTUNE_REF	24		V_{TUNE} reference ground

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO1_OUTP (single-ended), PWD_BUFF2,3,4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

Table of Graphs

Open-Loop Phase Noise	vs Temperature(1)	Figure 1, Figure 2, Figure 3, Figure 4
Open-Loop Phase Noise	vs Voltage(1)	Figure 5, Figure 6, Figure 7, Figure 8
Open-Loop Phase Noise	vs Temperature(1)(2)	Figure 9, Figure 10, Figure 11, Figure 12
Open-Loop Phase Noise	vs Voltage(1)(2)	Figure 13, Figure 14, Figure 15, Figure 16
Closed-Loop Phase Noise	vs Temperature(3)	Figure 17, Figure 18, Figure 19, Figure 20, Figure 21, Figure 22, Figure 23
Closed-Loop Phase Noise	vs Temperature(2)(3)	Figure 24, Figure 25, Figure 26, Figure 27, Figure 28, Figure 29, Figure 30
Closed-Loop Phase Noise	vs Divide Ratio(3)	Figure 31
Closed-Loop Phase Noise	vs Divide Ratio(2)(3)	Figure 32
Closed-Loop Phase Noise	vs Temperature(4)	Figure 33, Figure 34, Figure 35, Figure 36, Figure 37, Figure 38, Figure 39
Closed-Loop Phase Noise	vs Temperature(2)(4)	Figure 40, Figure 41, Figure 42, Figure 43, Figure 44, Figure 45, Figure 46
Closed-Loop Phase Noise	vs Divide Ratio(4)	Figure 47
Closed-Loop Phase Noise	vs Divide Ratio(2)(4)	Figure 48
PFD Spurs	vs Temperature(4)	Figure 49
Multiples of PFD Spurs(4)		Figure 50, Figure 51, Figure 52
Multiples of PFD Spurs(4)(5)		Figure 53
Fractional Spurs	vs LO Divider(3)	Figure 54
Fractional Spurs	vs RF Divider and Prescaler(3)	Figure 55
Fractional Spurs	vs Temperature(3)	Figure 56
Multiples of PFD Spurs(3)		Figure 57
LO Harmonics(4)		Figure 58
Output Power with Multiple Buffers(4)		Figure 59, Figure 60
Output Power	vs Output Port(4)	Figure 61
Output Power	vs Buffer Bias(4)	Figure 62
VCO Gain (Kv)	vs Frequency	Figure 63

(1) VCO_TRIM = 32, VTUNE_IN = 1.1 V, CP_TRISTATE = 3 (3-state), and CAL_BYPASS = On.
(2) VCO_BIAS = 600 µA.
(3) Reference frequency = 61.44 MHz; PFD frequency = 30.72 MHz.
(4) Reference frequency = 40 MHz; PFD frequency = 1.6 MHz.
(5) Performance change at frequencies above 1500 MHz results from PLL_DIV_SEL changing from divide-by-1 to divide-by-2.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

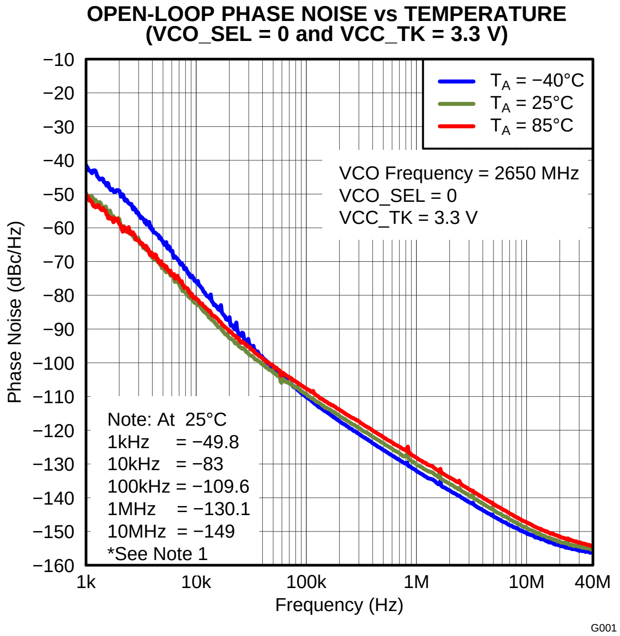


Figure 1.

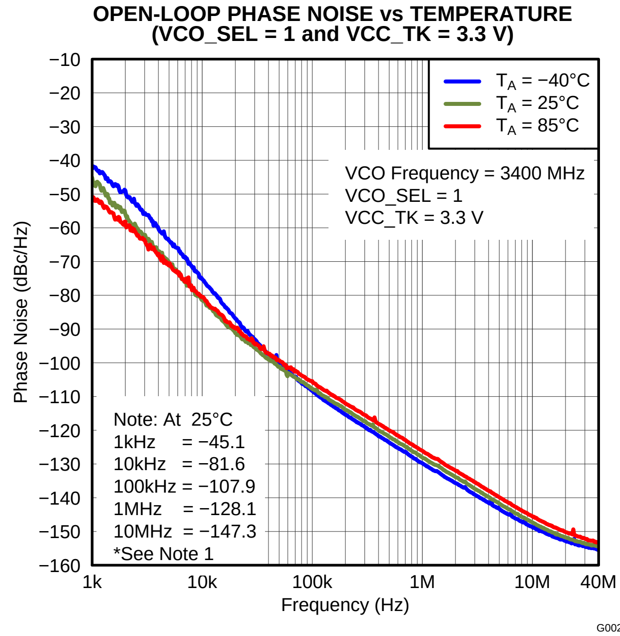


Figure 2.

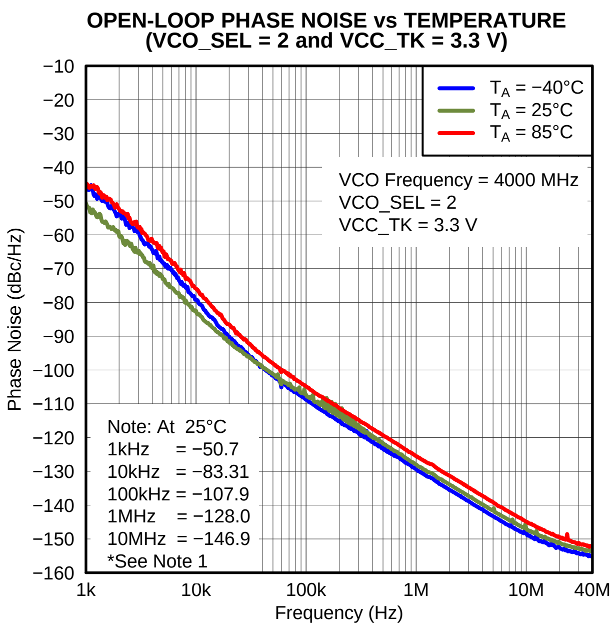


Figure 3.

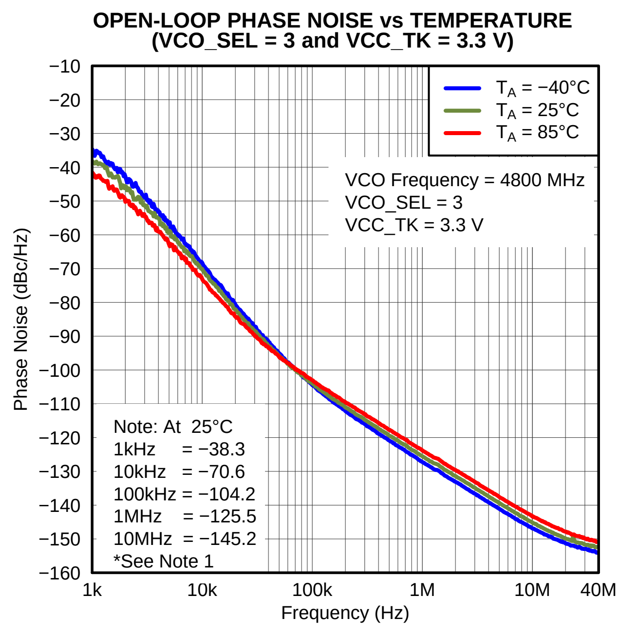


Figure 4.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

OPEN-LOOP PHASE NOISE vs VOLTAGE (VCO_SEL = 0)

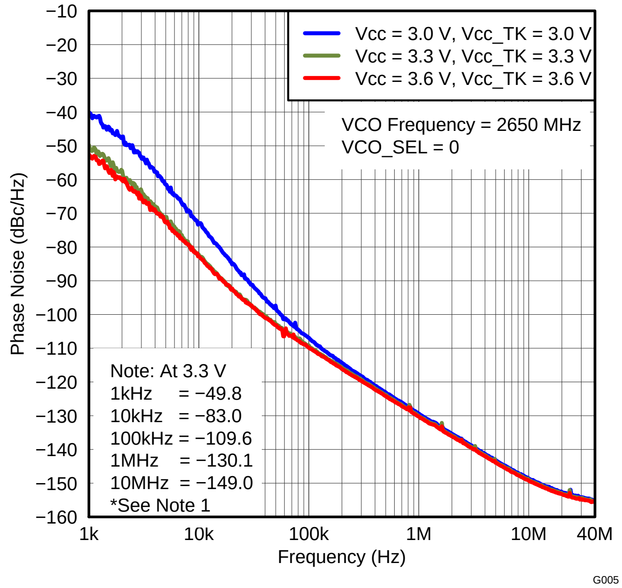


Figure 5.

OPEN-LOOP PHASE NOISE vs VOLTAGE (VCO_SEL = 1)

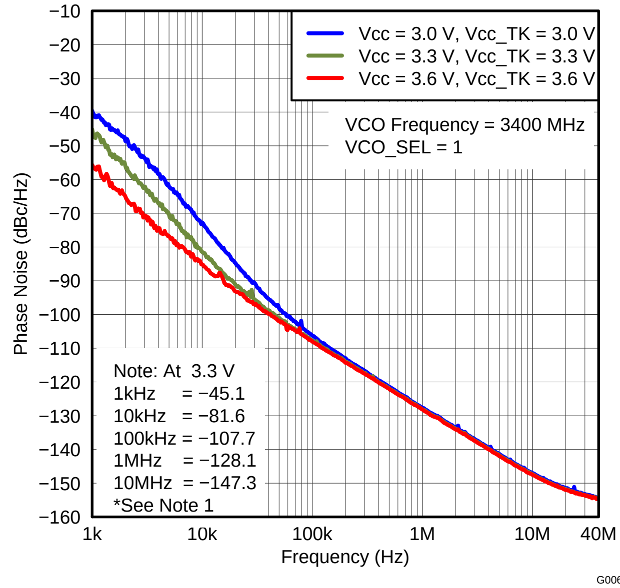


Figure 6.

OPEN-LOOP PHASE NOISE vs VOLTAGE (VCO_SEL = 2)

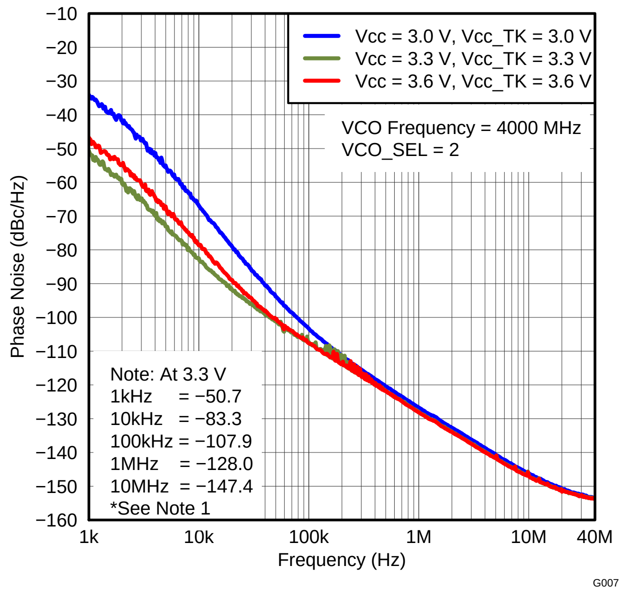


Figure 7.

OPEN-LOOP PHASE NOISE vs VOLTAGE (VCO_SEL = 3)

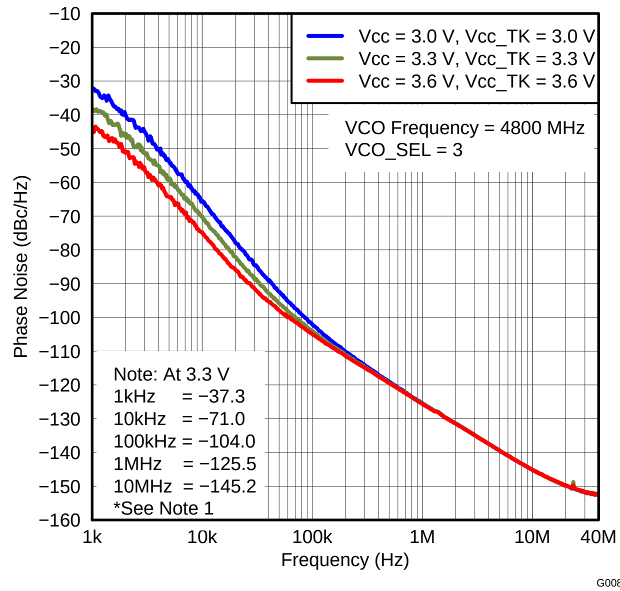


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

OPEN-LOOP PHASE NOISE vs TEMPERATURE (VCO_SEL = 0 and VCC_TK = 5 V)

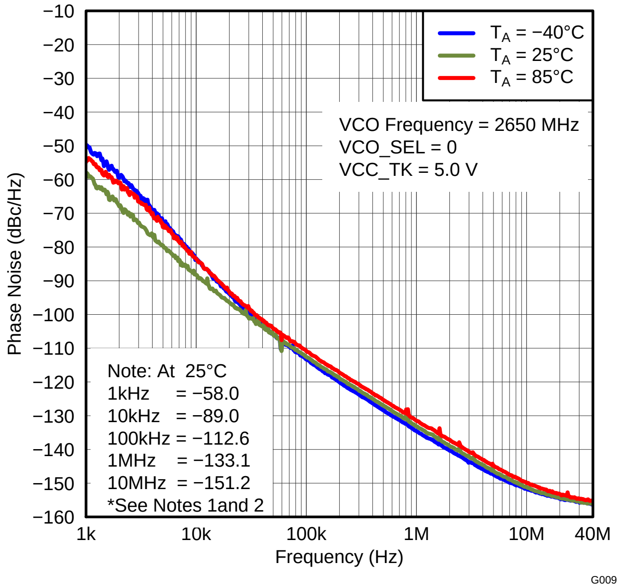


Figure 9.

OPEN-LOOP PHASE NOISE vs TEMPERATURE (VCO_SEL = 1 and VCC_TK = 5 V)

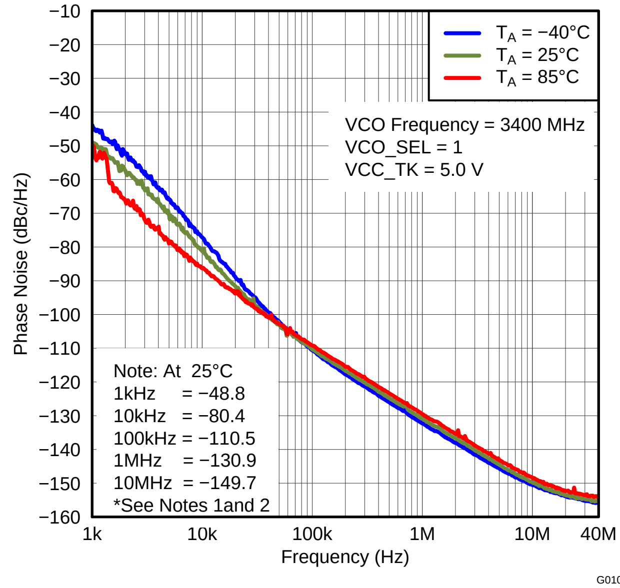


Figure 10.

OPEN-LOOP PHASE NOISE vs TEMPERATURE (VCO_SEL = 2 and VCC_TK = 5 V)

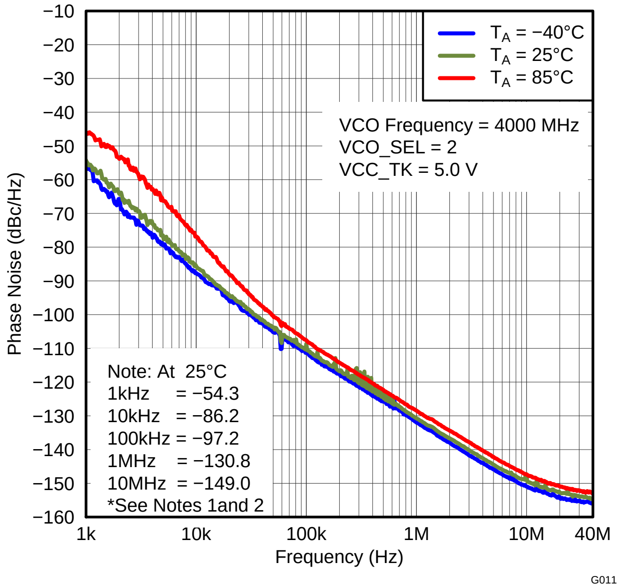


Figure 11.

OPEN-LOOP PHASE NOISE vs TEMPERATURE (VCO_SEL = 3 and VCC_TK = 5 V)

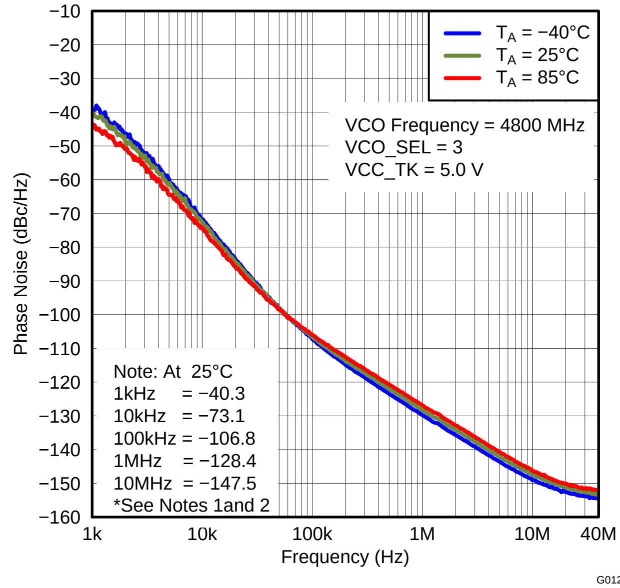


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

OPEN-LOOP PHASE NOISE vs VOLTAGE (VCO_SEL = 0)

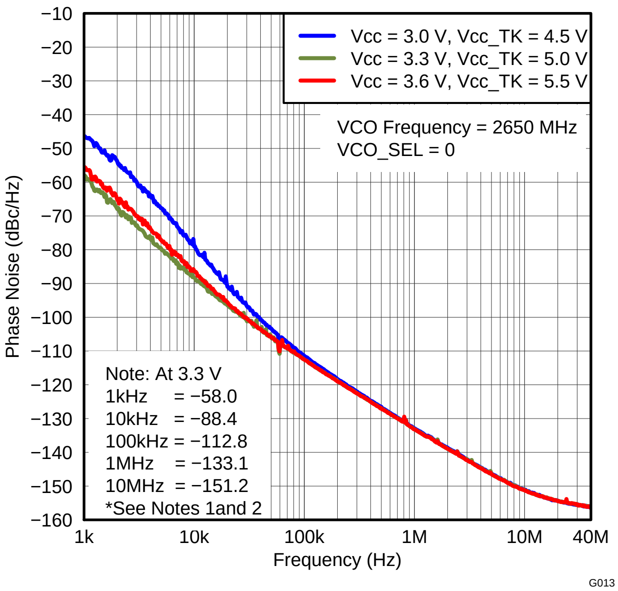


Figure 13.

OPEN-LOOP PHASE NOISE vs VOLTAGE (VCO_SEL = 1)

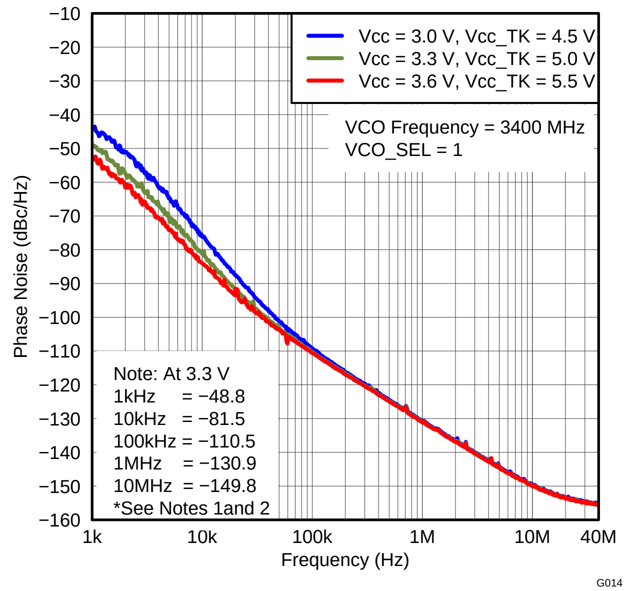


Figure 14.

OPEN-LOOP PHASE NOISE vs VOLTAGE (VCO_SEL = 2)

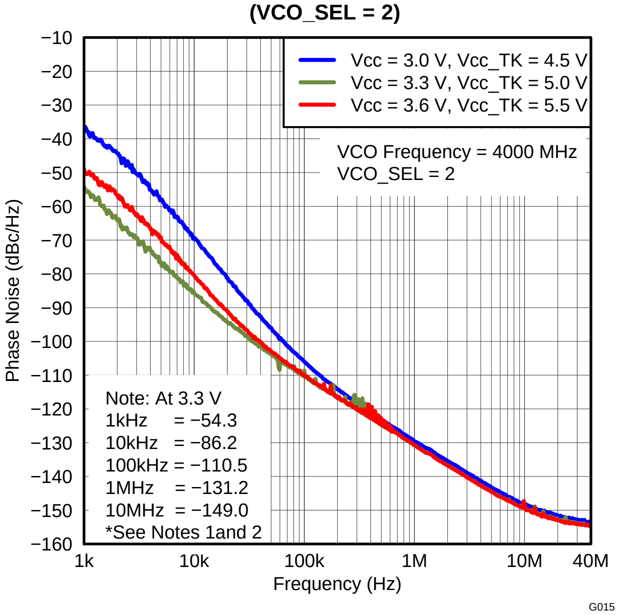


Figure 15.

OPEN-LOOP PHASE NOISE vs VOLTAGE (VCO_SEL = 3)

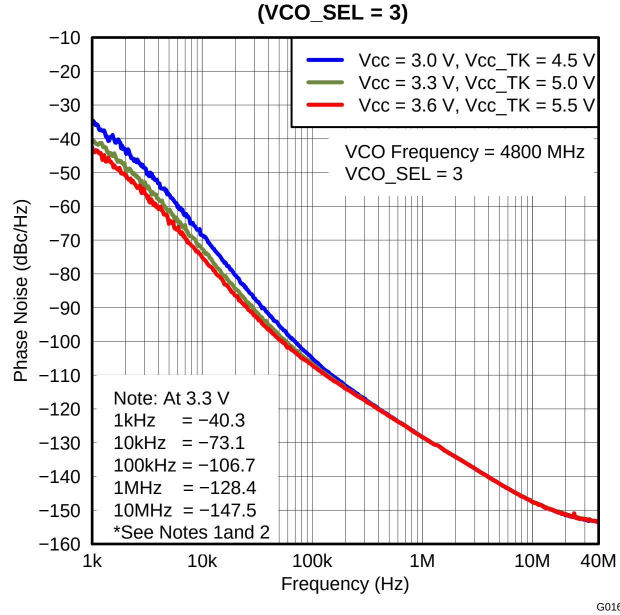


Figure 16.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (725 MHz, VCC_TK = 3.3 V, Fractional Mode)

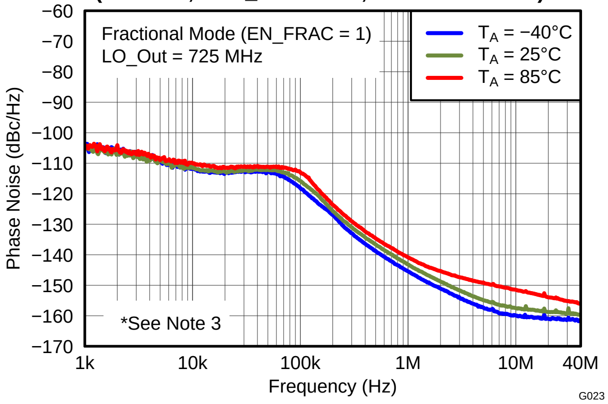


Figure 17.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (942.5 MHz, VCC_TK = 3.3 V, Fractional Mode)

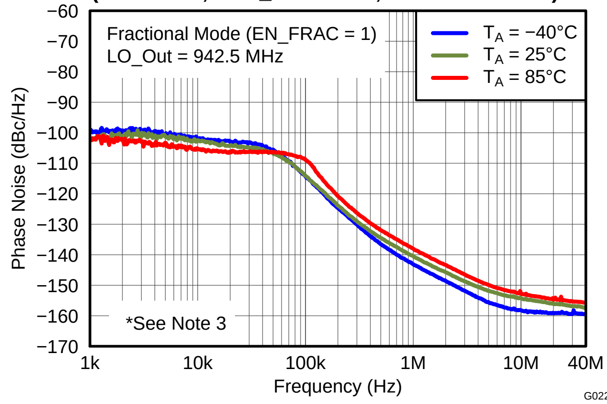


Figure 18.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (1880 MHz, VCC_TK = 3.3 V, Fractional Mode)

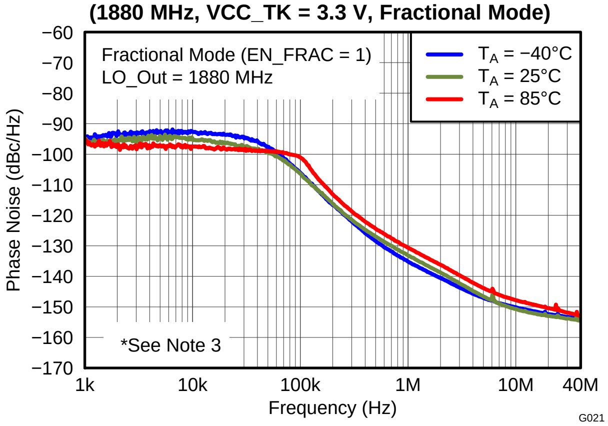


Figure 19.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (2120 MHz, VCC_TK = 3.3 V, Fractional Mode)

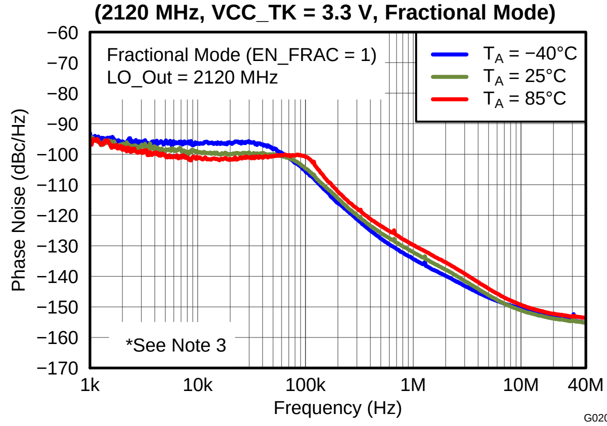


Figure 20.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (2650 MHz, VCC_TK = 3.3 V, Fractional Mode)

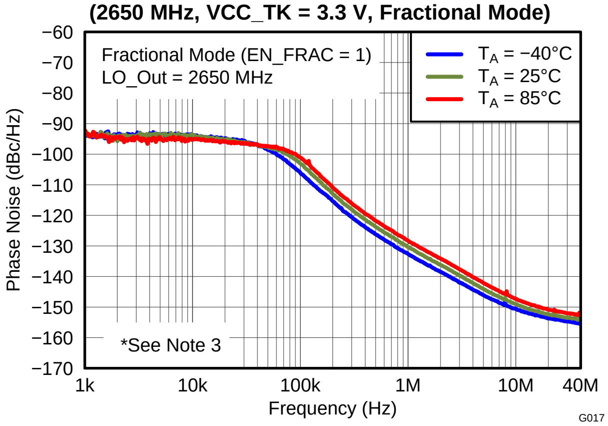


Figure 21.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (3500 MHz, VCC_TK = 3.3 V, Fractional Mode)

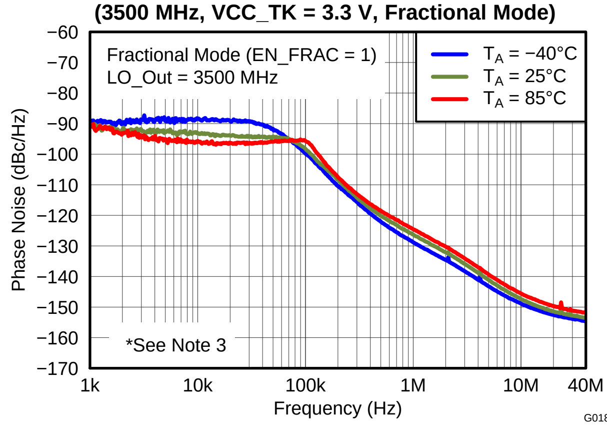


Figure 22.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (4750 MHz, VCC_TK = 3.3 V, Fractional Mode)

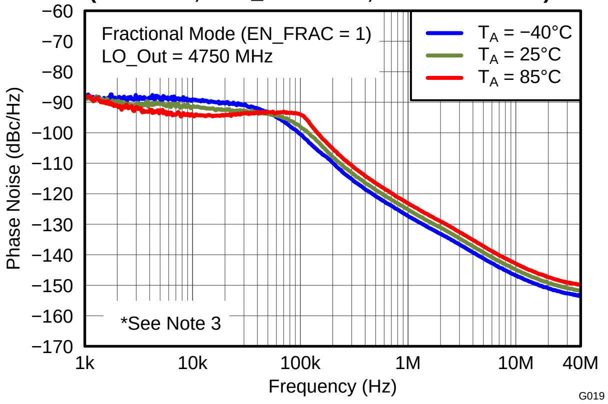


Figure 23.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (725 MHz, VCC_TK = 5 V, Fractional Mode)

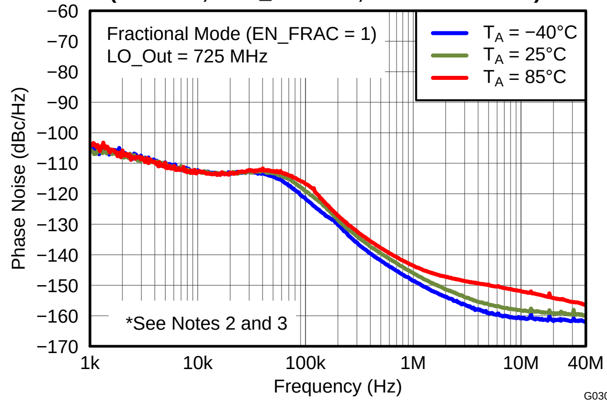


Figure 24.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (942.5 MHz, VCC_TK = 5 V, Fractional Mode)

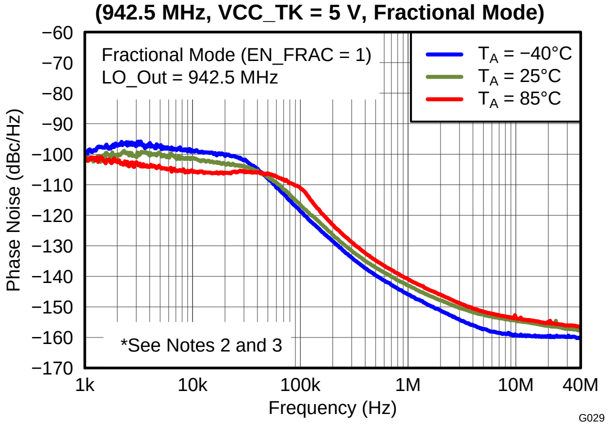


Figure 25.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (1880 MHz, VCC_TK = 5 V, Fractional Mode)

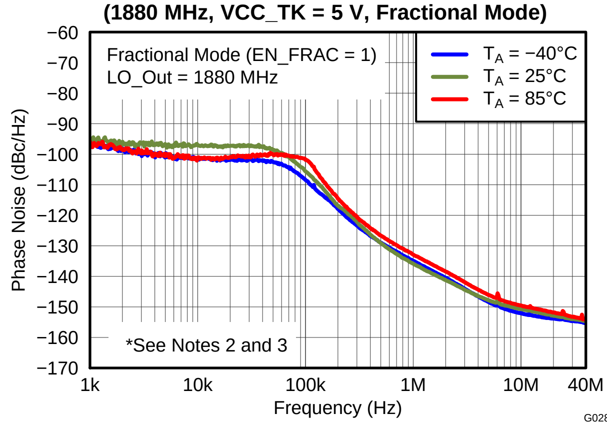


Figure 26.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (2120 MHz, VCC_TK = 5 V, Fractional Mode)

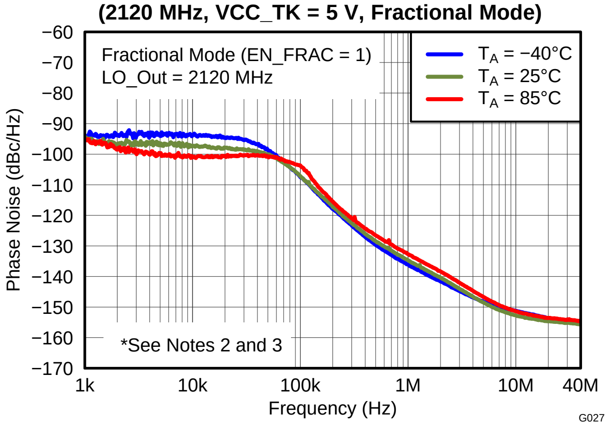


Figure 27.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (2650 MHz, VCC_TK = 5 V, Fractional Mode)

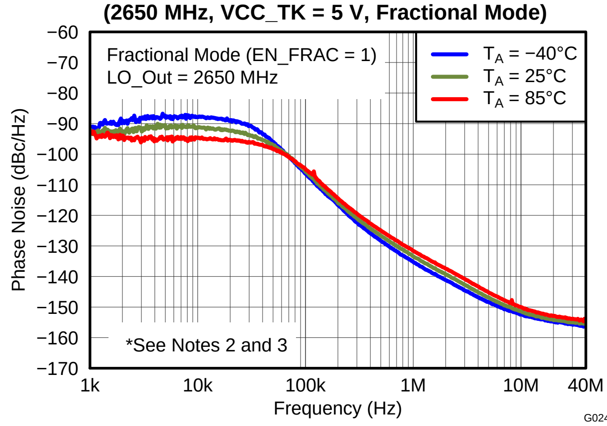


Figure 28.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (3500 MHz, VCC_TK = 5 V, Fractional Mode)

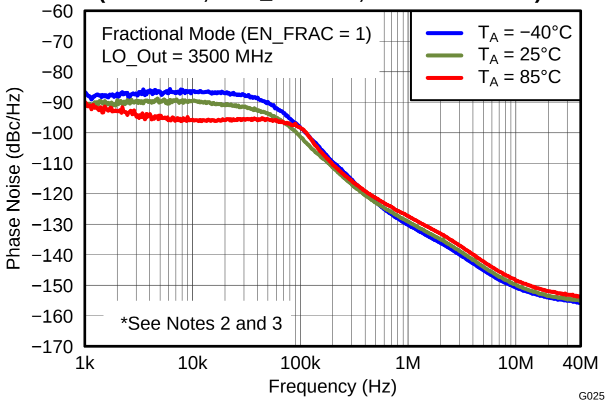


Figure 29.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (4750 MHz, VCC_TK = 5 V, Fractional Mode)

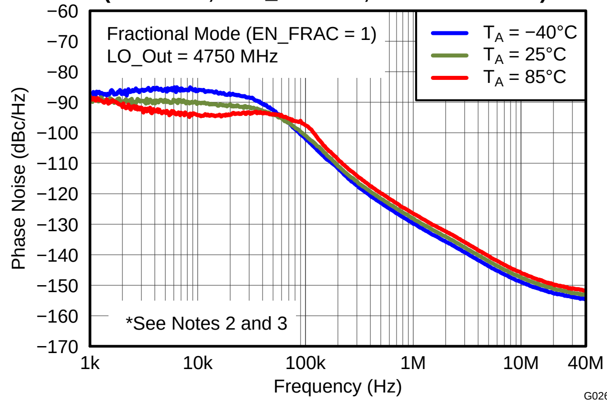


Figure 30.

CLOSED-LOOP PHASE NOISE vs DIVIDE RATIO (VCC_TK = 3.3 V, Fractional Mode)

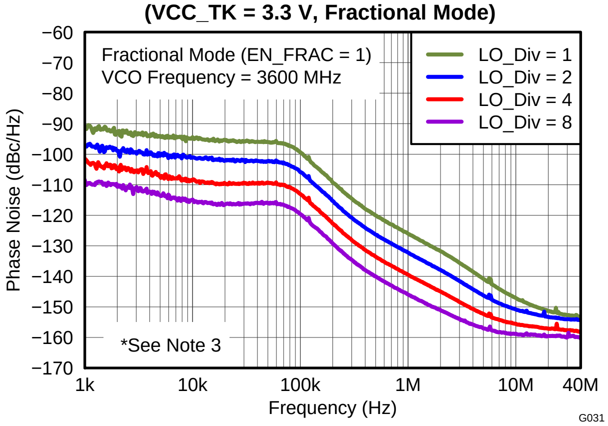


Figure 31.

CLOSED-LOOP PHASE NOISE vs DIVIDE RATIO (VCC_TK = 5 V, Fractional Mode)

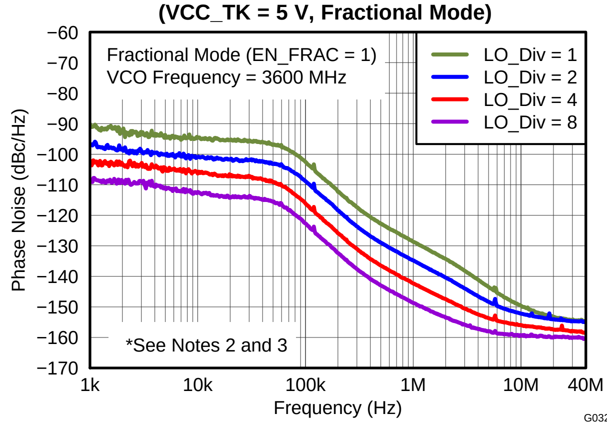


Figure 32.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (728 MHz, VCC_TK = 3.3 V, Integer Mode)

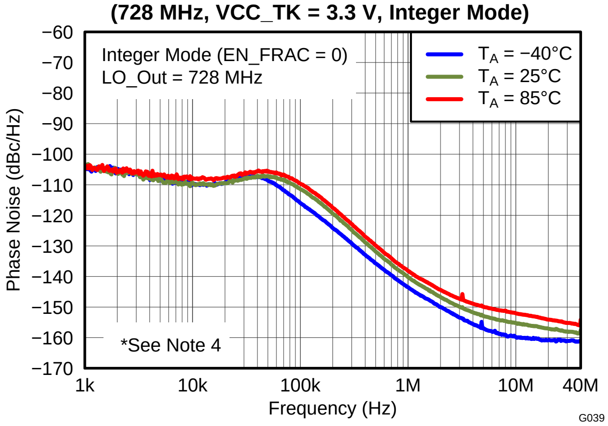


Figure 33.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (942.5 MHz, VCC_TK = 3.3 V, Integer Mode)

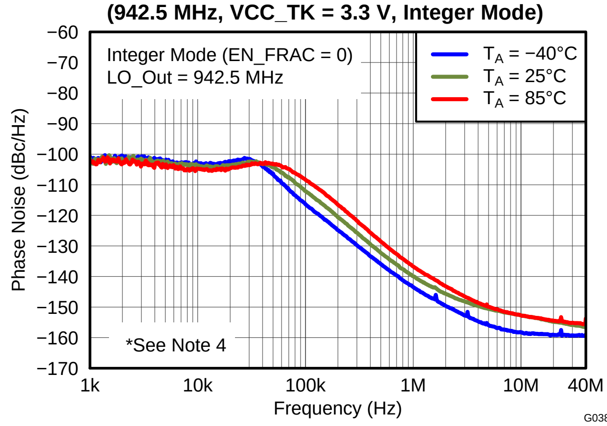


Figure 34.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (1842.5 MHz, VCC_TK = 3.3 V, Integer Mode)

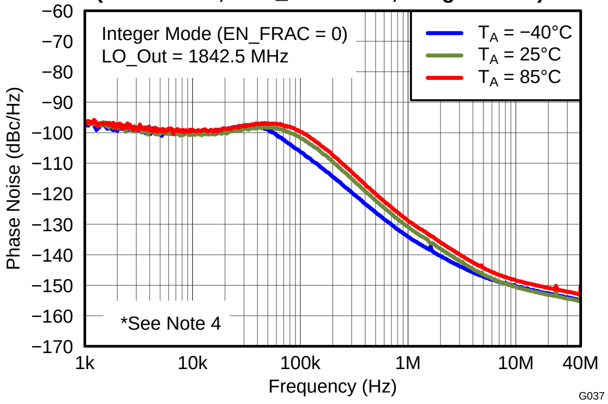


Figure 35.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (2140 MHz, VCC_TK = 3.3 V, Integer Mode)

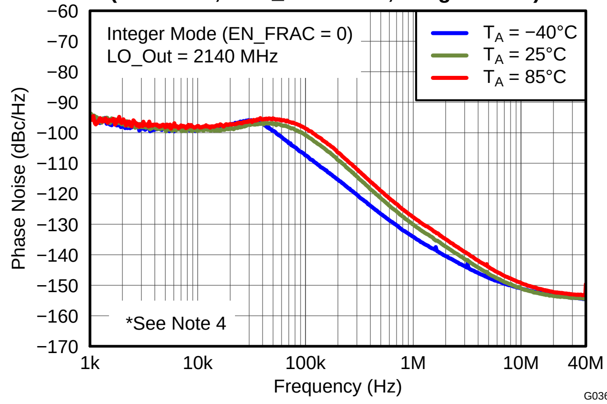


Figure 36.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (2600 MHz, VCC_TK = 3.3 V, Integer Mode)

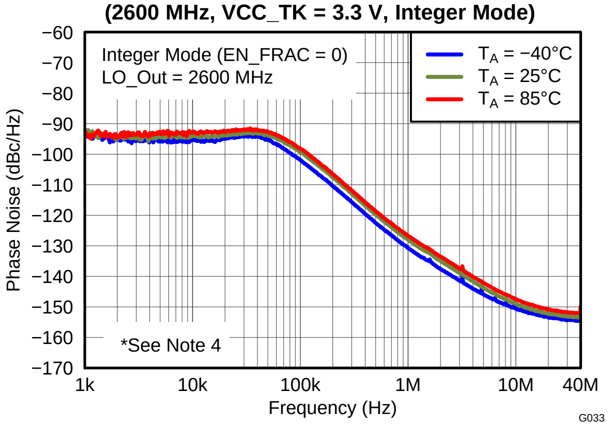


Figure 37.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (3500 MHz, VCC_TK = 3.3 V, Integer Mode)

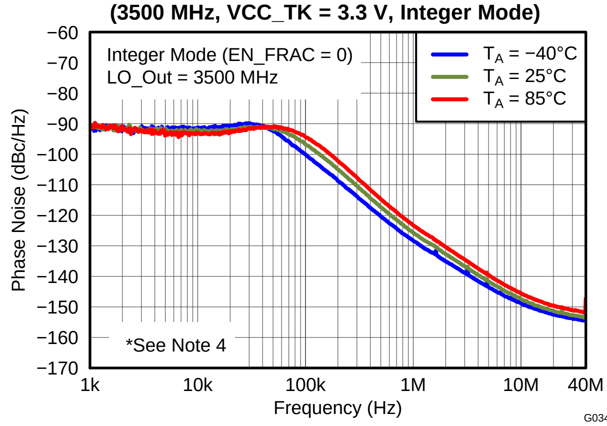


Figure 38.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (4800 MHz, VCC_TK = 3.3 V, Integer Mode)

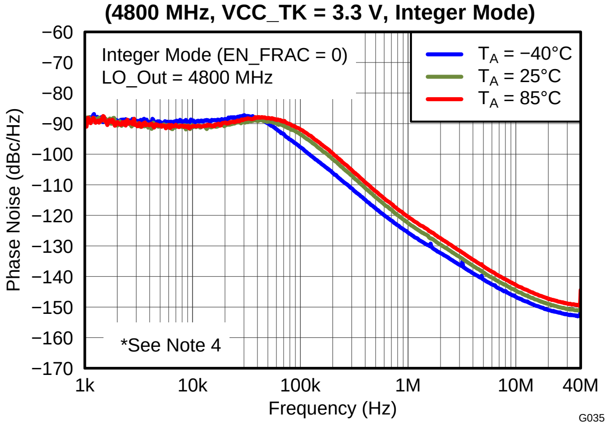


Figure 39.

CLOSED-LOOP PHASE NOISE vs TEMPERATURE (728 MHz, VCC_TK = 5 V, Integer Mode)

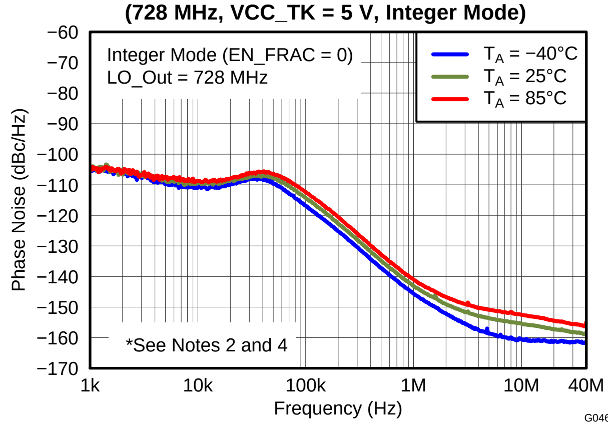


Figure 40.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

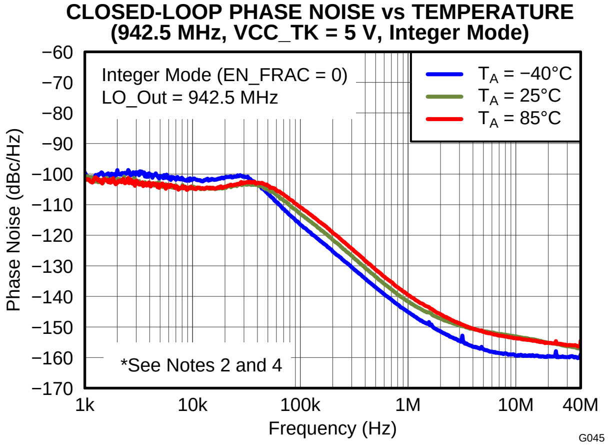


Figure 41.

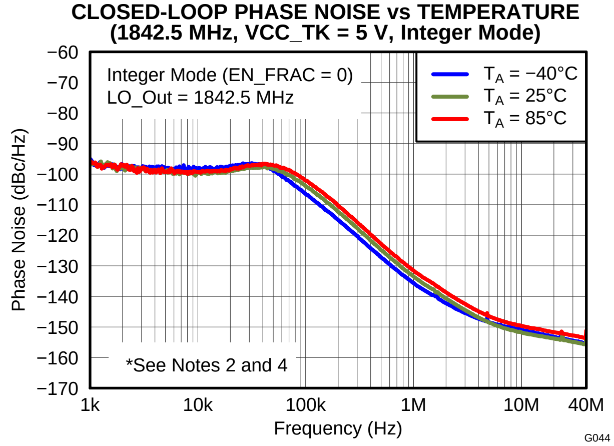


Figure 42.

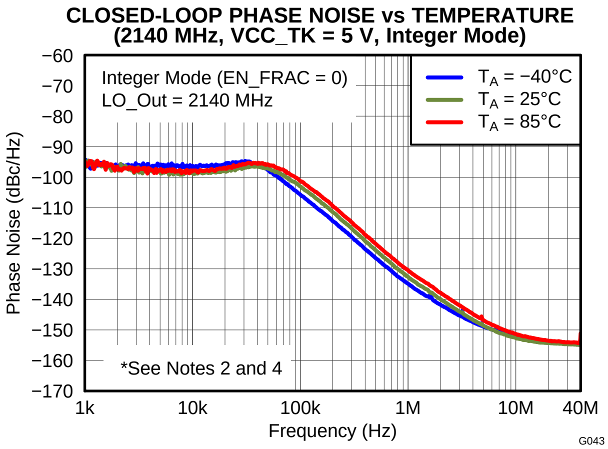


Figure 43.

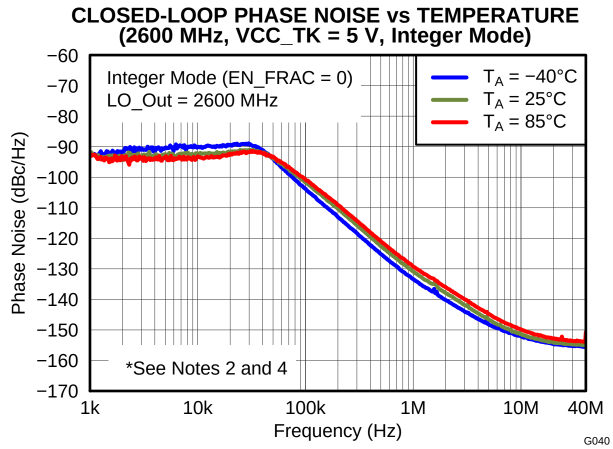


Figure 44.

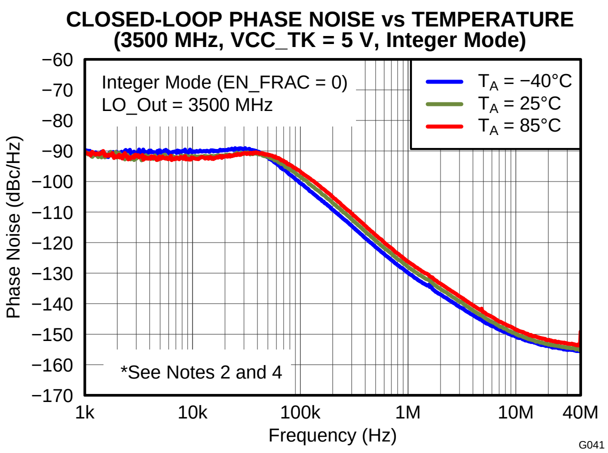


Figure 45.

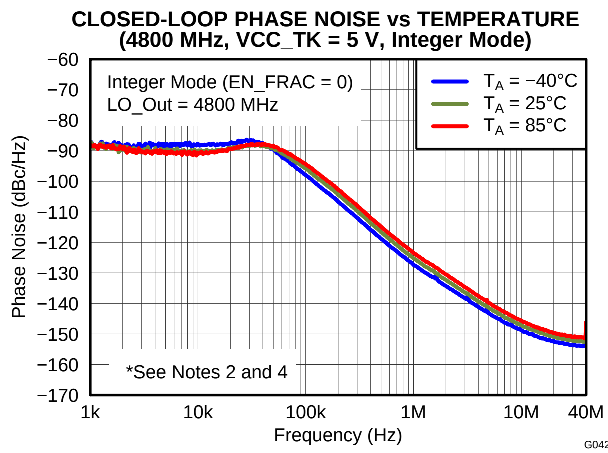


Figure 46.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

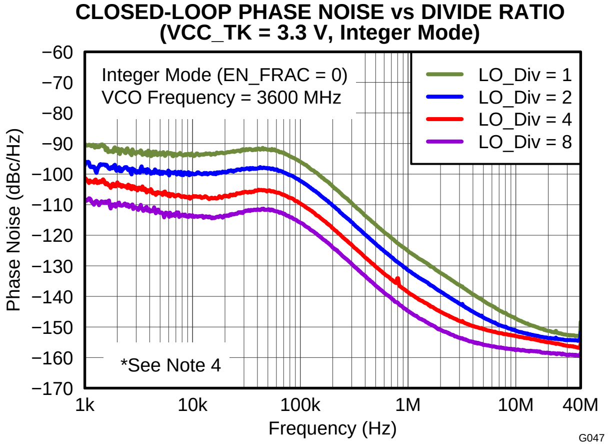


Figure 47.

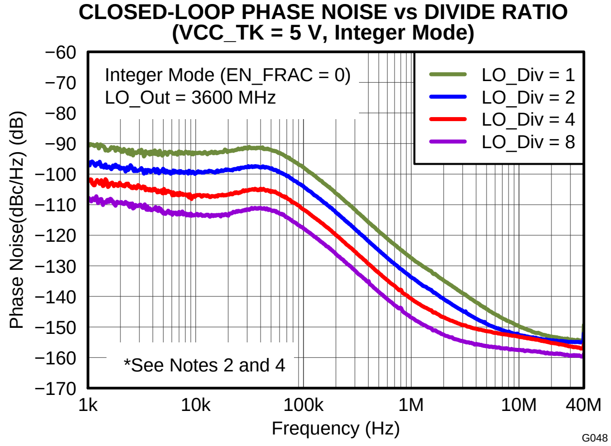


Figure 48.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

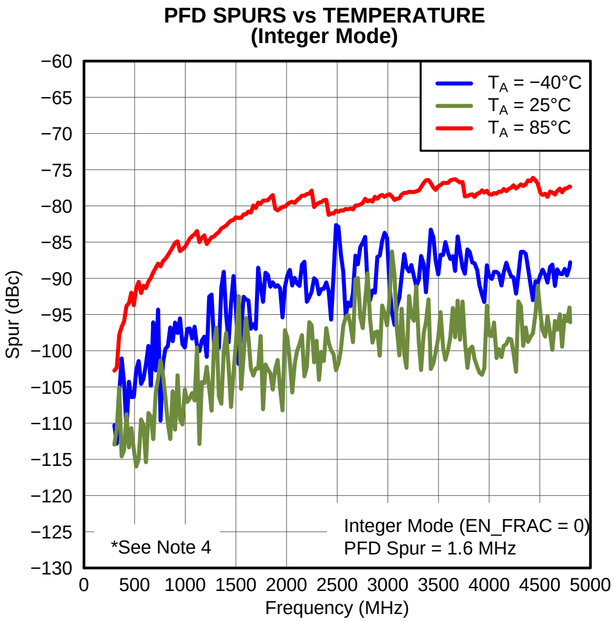


Figure 49.

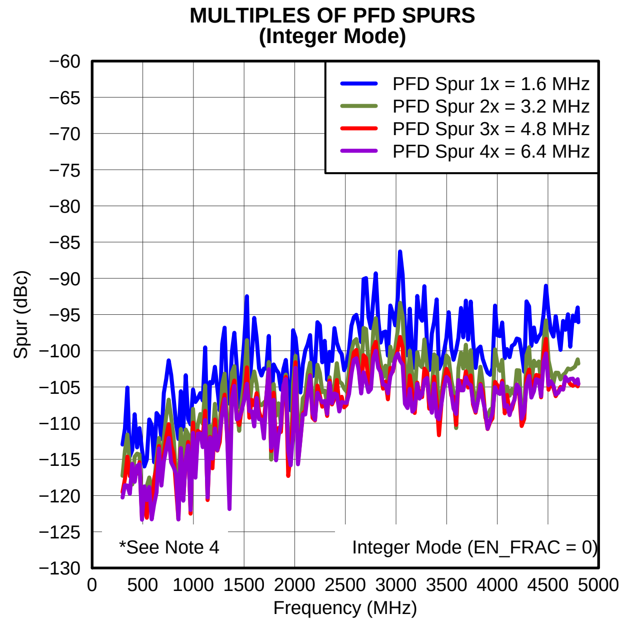


Figure 50.

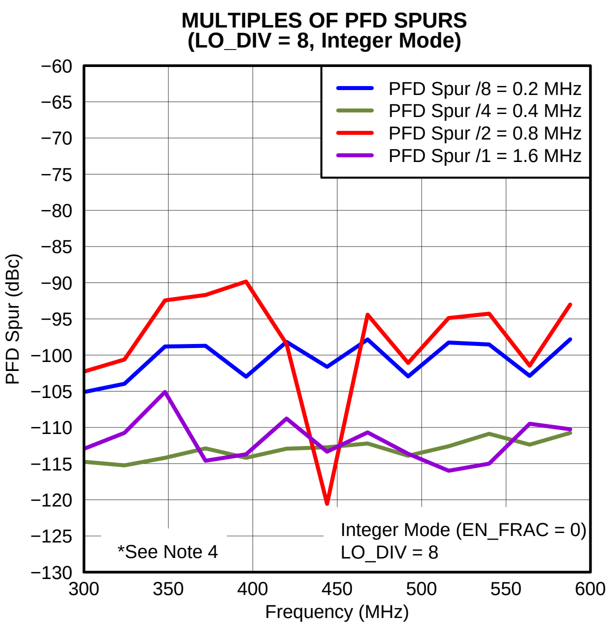


Figure 51.

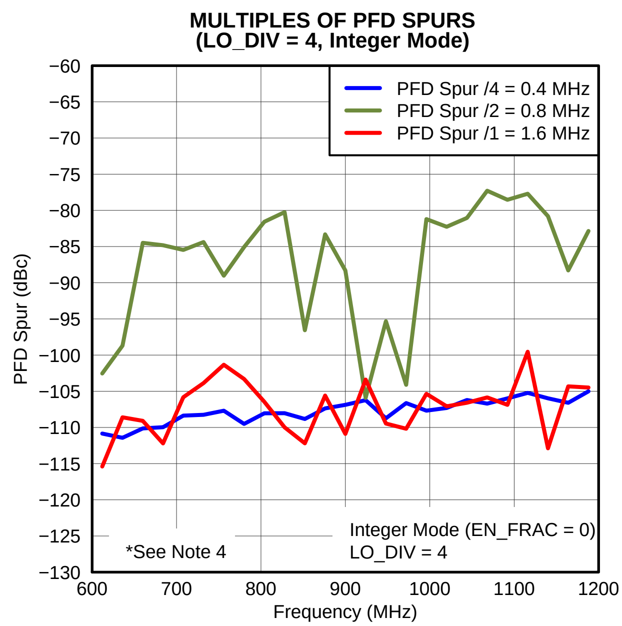


Figure 52.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

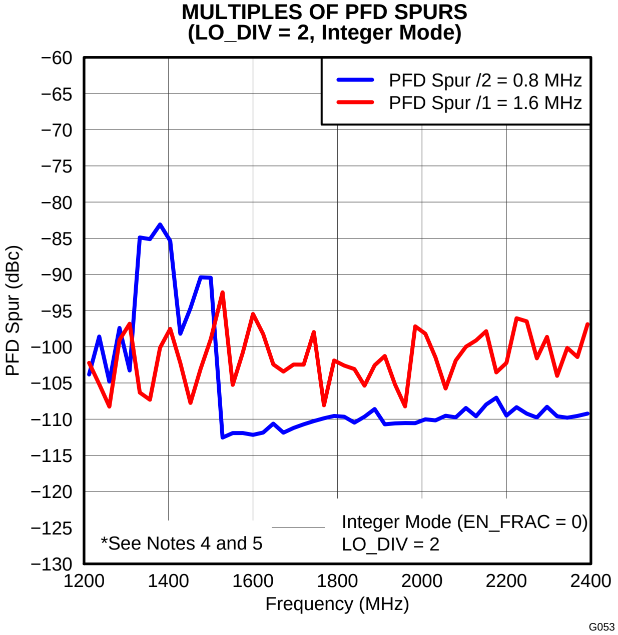


Figure 53.

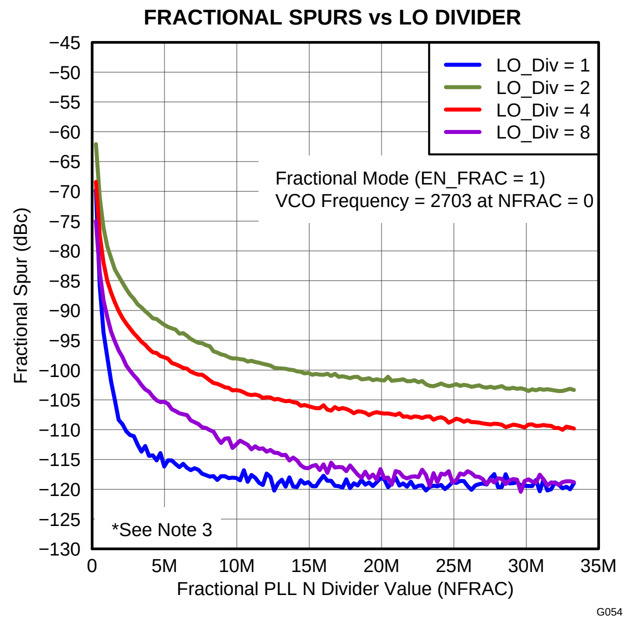


Figure 54.

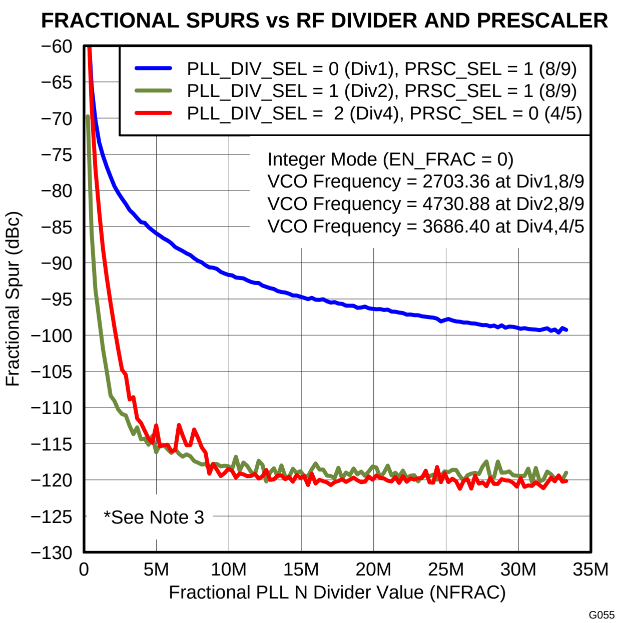


Figure 55.

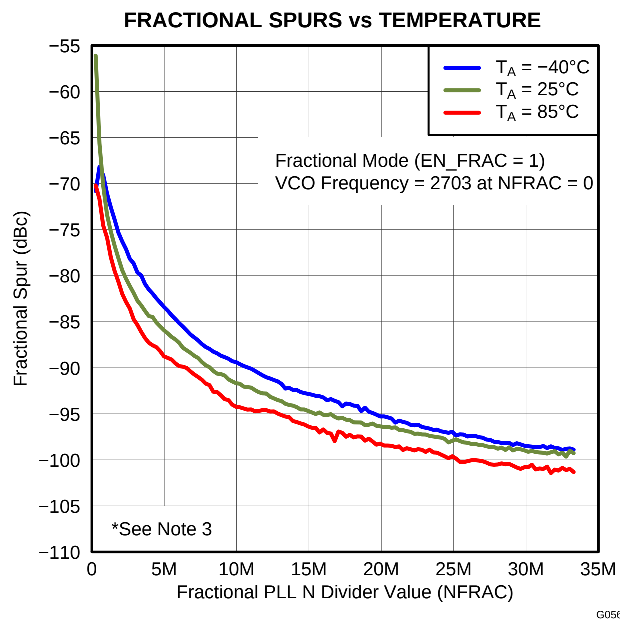


Figure 56.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

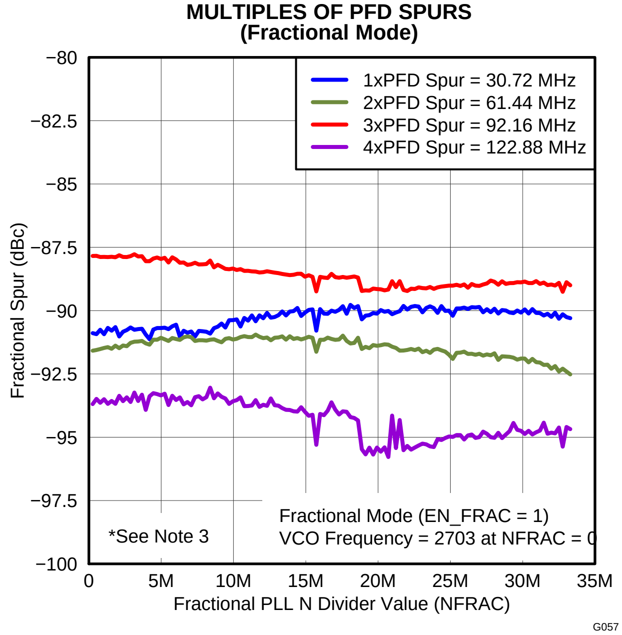


Figure 57.

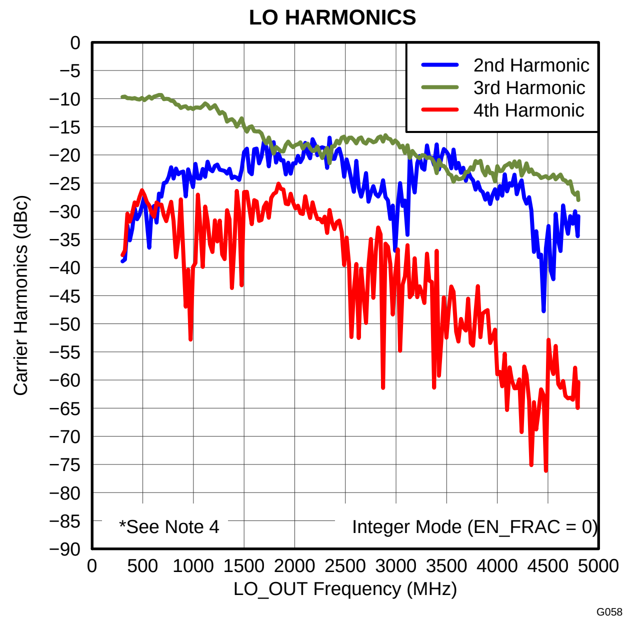


Figure 58.

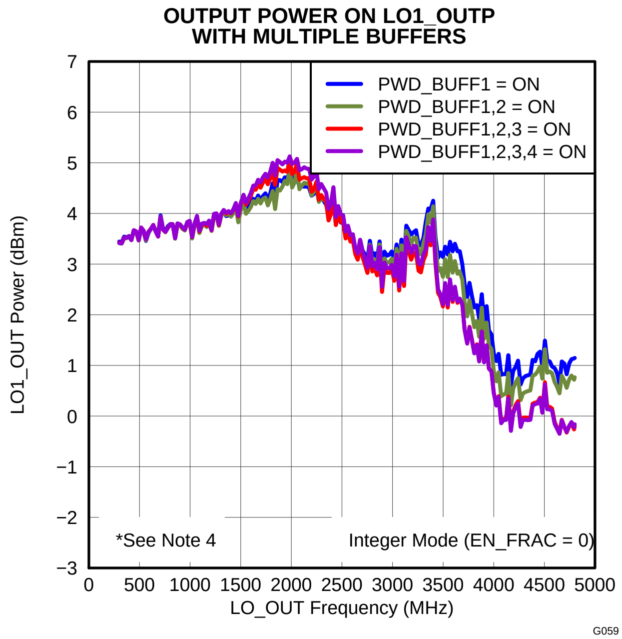


Figure 59.

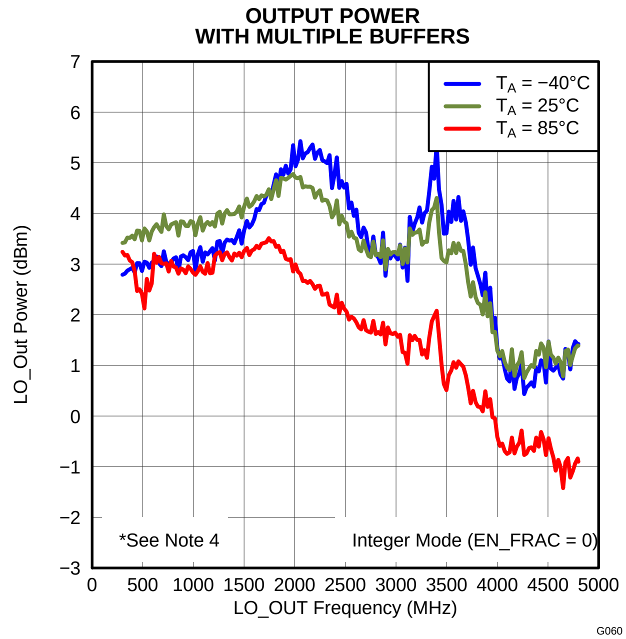


Figure 60.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = 3.3 V, VCC_TK = 3.3 V, LO_Out_1 (single ended), buffer 2, 3, 4 = off, VCO_BIAS = 400 µA; BUFOUT_BIAS = 600 µA, all other registers set per recommended programming in *Serial Programming Interface Register Definitions* section, and standard operating condition, unless otherwise noted.

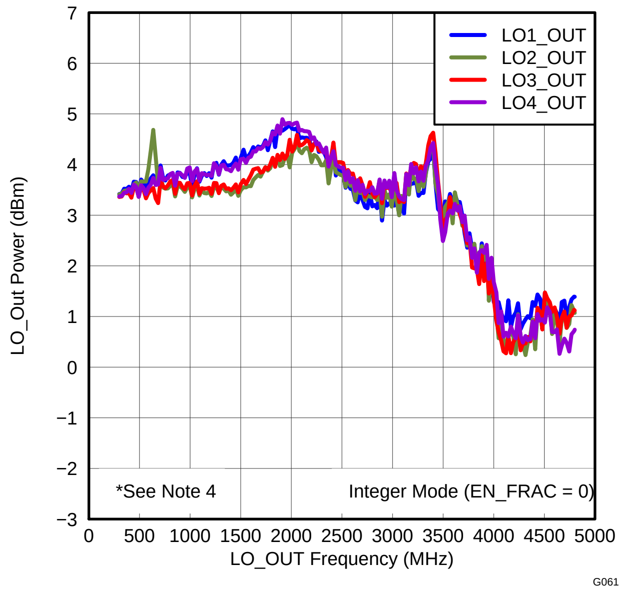


Figure 61.

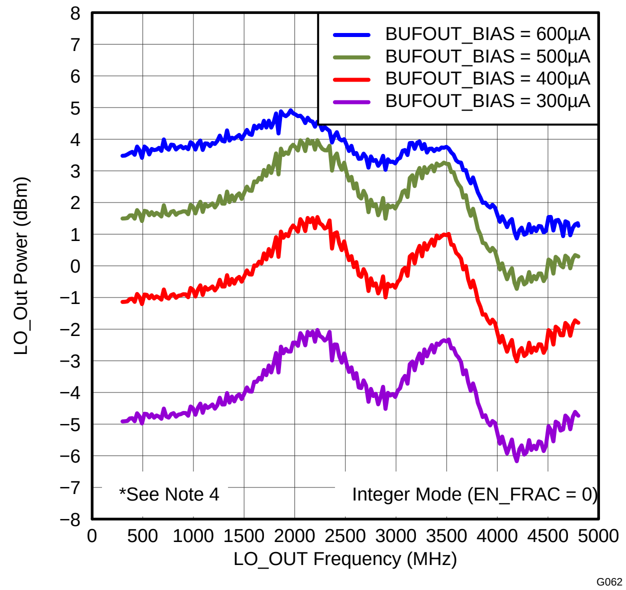


Figure 62.

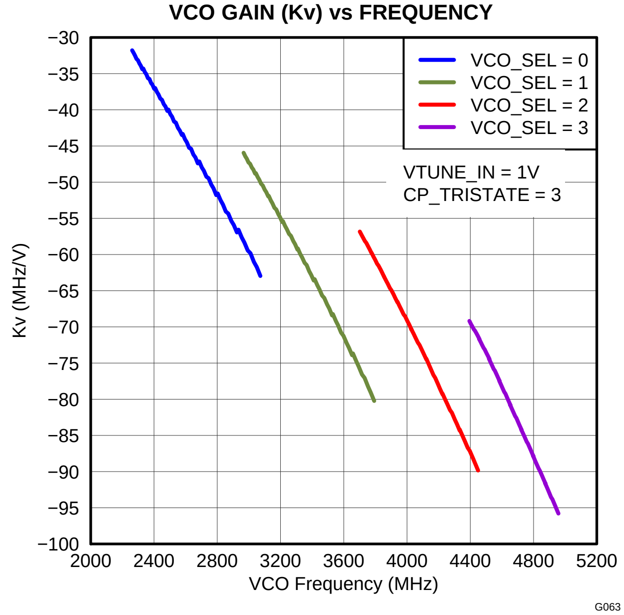


Figure 63.

SERIAL PROGRAMMING INTERFACE REGISTER DEFINITIONS

OVERVIEW

The TRF3765 features a four-wire serial programming interface (4WI) that controls an internal 32-bit shift register. There are a total of three signals that must be applied: the clock (CLOCK, pin 4); the serial data (DATA, pin 3); and the latch enable (STROBE, pin 5).

The serial data (DB0-DB31) are loaded least significant bit (LSB) first, and read on the rising edge of CLOCK. STROBE is asynchronous to the CLOCK signal; at its rising edge, the data in the shift register are loaded into the selected internal register. Figure 64 shows the timing for the 4WI. Table 1 lists the 4WI timing for the write operation.

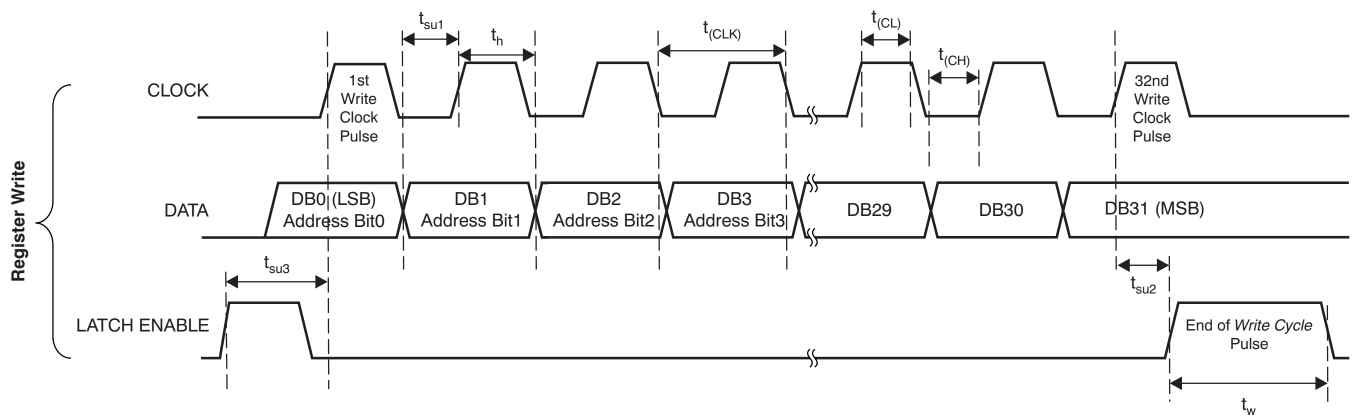


Figure 64. 4WI Timing Diagram

Table 1. 4WI Timing: Write Operation

PARAMETER		MIN	MAX	UNITS
t_h	Hold time, data to clock	20		ns
t_{su1}	Setup time, data to clock	20		ns
$t_{(CH)}$	Clock low duration	20		ns
$t_{(CL)}$	Clock high duration	20		ns
t_{su2}	Setup time, clock to enable	20		ns
$t_{(CLK)}$	Clock period	50		ns
t_w	Enable time	50		ns
t_{su3}	Setup time, latch to data	70		ns

PLL 4WI REGISTERS

Register 1

Table 2. PLL 4WI Register 1

REGISTER ADDRESS					REFERENCE CLOCK DIVIDER										
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

REF CLOCK DIV		RSV	REF INV	VCO NEG	CHARGE PUMP CURRENT					CP DOUBLE	VCO CAL CLK DIV/MULT				RSV
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

BIT NUMBER	BIT NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	1	Register address bits
Bit1	ADDR_1	0	
Bit2	ADDR_2	0	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	RDIV_0	1	13-bit Reference Divider value
Bit6	RDIV_1	0	
Bit7	RDIV_2	0	
Bit8	RDIV_3	0	
Bit9	RDIV_4	0	
Bit10	RDIV_5	0	
Bit11	RDIV_6	0	
Bit12	RDIV_7	0	
Bit13	RDIV_8	0	
Bit14	RDIV_9	0	
Bit15	RDIV_10	0	
Bit16	RDIV_11	0	
Bit17	RDIV_12	0	
Bit18	RSV	0	Reserved
Bit19	REF_INV	0	Invert Reference Clock polarity; 1 = use falling edge
Bit20	NEG_VCO	1	VCO polarity control; 1= negative slope (negative K_V)
Bit21	ICP_0	0	Program Charge Pump dc current, ICP 1.94 mA, B[25..21] = [00 000] 0.65 mA, B[25..21] = [11 111] 0.97 mA, default value, B[25..21] = [01 010]
Bit22	ICP_1	1	
Bit23	ICP_2	0	
Bit24	ICP_3	1	
Bit25	ICP_4	0	
Bit26	ICPDOUBLE	0	1 = Set ICP to double the current
Bit27	CAL_CLK_SEL_0	0	Multiplication or division factor to create VCO calibration clock from PFD frequency Fastest clock, B[25..21] = [00 000] Slowest clock, B[25..21] = [11 111]
Bit28	CAL_CLK _SEL_1	0	
Bit29	CAL_CLK _SEL_2	0	
Bit30	CAL_CLK _SEL_3	1	
Bit31	RSV	0	Reserved

CAL_CLK_SEL[3..0]: Set the frequency divider value used to derive the VCO calibration clock from the phase detector frequency. Table 3 shows the calibration clock scale factors.

Table 3. Calibration Clock Scale Factors

CAL_CLK_SEL	SCALING FACTOR
1111	1/128
1110	1/64
1101	1/32
1100	1/16
1011	1/8
1010	1/4
1001	1/2
1000	1
0110	2
0101	4
0100	8
0011	16
0010	32
0001	64
0000	128

ICP[4..0]: Set the charge pump current. Table 4 lists the charge pump current settings.

Table 4. Charge Pump Current Settings

ICP[4..0]	CURRENT (mA)
00 000	1.94
00 001	1.76
00 010	1.62
00 011	1.49
00 100	1.38
00 101	1.29
00 110	1.21
00 111	1.14
01 000	1.08
01 001	1.02
01 010	0.97
01 011	0.92
01 100	0.88
01 101	0.84
01 110	0.81
01 111	0.78
10 000	0.75
10 001	0.72
10 010	0.69
10 011	0.67
10 100	0.65
10 101	0.63
10 110	0.61
10 111	0.59
11 000	0.57
11 001	0.55
11 010	0.54
11 011	0.52
11 100	0.51
11 101	0.5
11 110	0.48
11 111	0.47

Register 2

Table 5. PLL 4WI Register 2

REGISTER ADDRESS					N-DIVIDER VALUE										
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

N-DIVIDER VALUE					PLL DIVIDER SETTING		PRE-SCALER SELECT	RSV	RSV	VCO SELECT		VCO SEL MODE	CAL ACCURACY		EN CAL
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

BIT NUMBER	BIT NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	0	Register address bits
Bit1	ADDR_1	1	
Bit2	ADDR_2	0	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	NINT_0	0	PLL N-divider division setting
Bit6	NINT_1	0	
Bit7	NINT_2	0	
Bit8	NINT_3	0	
Bit9	NINT_4	0	
Bit10	NINT_5	0	
Bit11	NINT_6	0	
Bit12	NINT_7	1	
Bit13	NINT_8	0	
Bit14	NINT_9	0	
Bit15	NINT_10	0	
Bit16	NINT_11	0	
Bit17	NINT_12	0	
Bit18	NINT_13	0	
Bit19	NINT_14	0	
Bit20	NINT_15	0	
Bit21	PLL_DIV_SEL0	1	Select division ratio of divider in front of prescaler
Bit22	PLL_DIV_SEL1	0	
Bit23	PRSC_SEL	1	Set prescaler modulus (0 → 4/5; 1 → 8/9)
Bit24	RSV	0	Reserved
Bit25	RSV	0	Reserved
Bit26	VCO_SEL_0	0	Selects between the four integrated VCOs 00 = lowest frequency VCO; 11= highest frequency VCO
Bit27	VCO_SEL_1	1	
Bit28	VCOSEL_MODE	0	Single VCO auto-calibration mode (1 = active)
Bit29	CAL_ACC_0	0	Error count during the cap array calibration Recommended programming [00].
Bit30	CAL_ACC_1	0	
Bit31	EN_CAL	0	Execute a VCO frequency auto-calibration. Set to '1' to initiate a calibration. Resets automatically.

PLL_DIV <1.0>: Select division ratio of divider in front of prescaler, according to Table 6.

Table 6. PLL_DIV Selection

PLL_DIV	FREQUENCY DIVIDER
00	1
01	2
10	4

VCOSEL_MODE: When VCOSEL_MODE is set to '1', the cap array calibration is executed on the VCO selected through bits VCO_SEL[1:0].

Register 3

Table 7. PLL 4WI Register 3

REGISTER ADDRESS					FRACTIONAL N-DIVIDER VALUE										
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

FRACTIONAL N-DIVIDER VALUE														RSV	RSV
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

BIT NUMBER	BIT NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	1	Register address bits
Bit1	ADDR_1	1	
Bit2	ADDR_2	0	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	NFRAC<0>	0	Fractional PLL N divider value 0 to 0.99999
Bit6	NFRAC<1>	0	
Bit7	NFRAC<2>	0	
Bit8	NFRAC<3>	0	
Bit9	NFRAC<4>	0	
Bit10	NFRAC<5>	0	
Bit11	NFRAC<6>	0	
Bit12	NFRAC<7>	0	
Bit13	NFRAC<8>	0	
Bit14	NFRAC<9>	0	
Bit15	NFRAC<10>	0	
Bit16	NFRAC<11>	0	
Bit17	NFRAC<12>	0	
Bit18	NFRAC<13>	0	
Bit19	NFRAC<14>	0	
Bit20	NFRAC<15>	0	
Bit21	NFRAC<16>	0	
Bit22	NFRAC<17>	0	
Bit23	NFRAC<18>	0	
Bit24	NFRAC<19>	0	
Bit25	NFRAC<20>	0	
Bit26	NFRAC<21>	0	
Bit27	NFRAC<22>	0	
Bit28	NFRAC<23>	0	
Bit29	NFRAC<24>	0	
Bit30	RSV	0	Reserved
Bit31	RSV	0	Reserved

Register 4

Table 8. PLL 4WI Register 4

REGISTER ADDRESS					PD PLL	POWER-DOWN PLL BLOCKS						POWER-DOWN OUTPUT BUFFERS			
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

EXT VCO		PLL TESTS CONTROL							ΔΣ MOD ORDER			ΔΣ MOD CONTROLS			EN FRACT MODE
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

BIT NUMBER	BIT NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	0	Register address bits
Bit1	ADDR_1	0	
Bit2	ADDR_2	1	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	PWD_PLL	0	Power-down all PLL blocks (1 = off)
Bit6	PWD_CP	0	When 1, charge pump is off
Bit7	PWD_VCO	0	When 1, VCO is off
Bit8	PWD_VCOMUX	0	Power-down the four VCO mux blocks (1 = off)
Bit9	PWD_DIV124	0	Power-down programmable RF divider in PLL feedback path (1 = off)
Bit10	PWD_PRESC	0	Power-down programmable prescaler (1 = off)
Bit11	PWD_LO_DIV	1	Power-down LO divider block (1 = off)
Bit12	PWD_BUFF_1	1	Power-down LO output buffer 1 (1 = off)
Bit13	PWD_BUFF_2	1	Power-down LO output buffer 2 (1 = off)
Bit14	PWD_BUFF_3	1	Power-down LO output buffer 3 (1 = off)
Bit15	PWD_BUFF_4	1	Power-down LO output buffer 4 (1 = off)
Bit16	EN_EXTVCO	0	Enable external VCO input buffer (1 = enabled)
Bit17	EXT_VCO_CTRL	0	Can be used to enable/disable an external VCO through pin EXTVCO_CTRL (1 = high).
Bit18	EN_ISOURCE	0	Enable offset current at Charge Pump output (to be used in Fractional mode only; 1 = on).
Bit19	LD_ANA_PREC_0	0	Control precision of analog lock detector 1 = low; 0 = high
Bit20	LD_ANA_PREC_1	0	
Bit21	CP_TRISTATE_0	0	Set the charge pump output into 3-state mode. Normal, B[22..21] = [00] Down, B[22..21] = [01] Up, B[22..21] = [10] 3-state, B[22..21] = [11]
Bit22	CP_TRISTATE_1	0	
Bit23	SPEEDUP	0	Speed up PLL block by bypassing bias stabilizer capacitors.
Bit24	LD_DIG_PREC	0	Lock detector precision (increases sampling time if set to 1)
Bit25	EN_DITH	1	Enable ΔΣ modulator dither (1 = on)
Bit26	MOD_ORD_0	0	ΔΣ modulator order (1 through 4). Not used in Integer mode. First order, B[27..26] = [00] Second order, B[27..26] = [01] Third order, B[27..26] = [10] Fourth order, B[27..26] = [11]
Bit27	MOD_ORD_1	1	
Bit28	DITH_SEL	0	Select dither mode for ΔΣ modulator (0 = pseudo-random; 1 = constant)
Bit29	DEL_SD_CLK_0	0	ΔΣ modulator clock delay. Not used in Integer mode. Min delay = 00; Max delay = 11
Bit30	DEL_SD_CLK_1	1	
Bit31	EN_FRAC	0	Enable Fractional mode (1 = fractional enabled)

Register 5

Table 9. PLL 4WI Register 5

REGISTER ADDRESS					VCO_R_TRIM			PLL_R_TRIM		VCO CURRENT				VCOBUF BIAS	
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

VCOMUX BIAS		OUTBUF BIAS		RSV	RSV	BIAS SEL	VCO CAL REF			VCOMUX AMPL		VCO BIAS VOLTAGE		RSV	EN_LD ISRC
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

BIT NUMBER	BIT NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	1	Register address bits
Bit1	ADDR_1	0	
Bit2	ADDR_2	1	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	VCOBIAS_RTRIM_0	0	VCO bias resistor trimming. Recommended programming [100].
Bit6	VCOBIAS_RTRIM_1	0	
Bit7	VCOBIAS_RTRIM_2	1	
Bit8	PLLBIAS_RTRIM_0	0	PLL bias resistor trimming. Recommended programming [10].
Bit9	PLLBIAS_RTRIM_1	1	
Bit10	VCO_BIAS_0	0	VCO bias reference current. 300 μA, B[13..10] = [00 00] 600 μA, B[13..10] = [11 11] Bias current varies directly with reference current Recommended programming: 400 μA, B[13..10] = [0101] with VCC_TK = 3.3 V 600 μA, B[13..10] = [1111] with VCC_TK = 5.0V
Bit11	VCO_BIAS_1	0	
Bit12	VCO_BIAS_2	0	
Bit13	VCO_BIAS_3	1	
Bit14	VCOBUF_BIAS_0	0	VCO buffer bias reference current. 300 μA, B[15..14] = [00] 600 μA, B[15..14] = [11] Bias current varies directly with reference current Recommended programming [10]
Bit15	VCOBUF _BIAS_1	1	
Bit16	VCOMUX_BIAS_0	0	VCO muxing buffer bias reference current. 300 μA, B[17..16] = [00] 600 μA, B[17..16] = [11] Bias current varies directly with reference current Recommended programming [10]
Bit17	VCOMUX _BIAS_1	1	
Bit18	BUFOUT_BIAS_0	1	PLL output buffer bias reference current. 300 μA, B[19..18] = [00] 600 μA, B[19..18] = [11] Bias current varies directly with reference current
Bit19	BUFOUT_BIAS_1	0	
Bit20	RSV	0	Reserved
Bit21	RSV	1	Reserved
Bit22	VCO_CAL_IB	0	Select bias current type for VCO calibration circuitry 0 = PTAT; 1 = constant over temperature. Recommended programming [0].
Bit23	VCO_CAL_REF_0	0	VCO calibration reference voltage trimming. 0.9 V, B[25..23] = [000] 1.4 V, B[25..23] = [111] Recommended programming 1.11 V, B[25..23] = [011]
Bit24	VCO_CAL_REF_1	0	
Bit25	VCO_CAL_REF_2	1	

BIT NUMBER	BIT NAME	RESET VALUE	DESCRIPTION
Bit26	VCO_AMPL_CTRL_0	0	Adjust the signal amplitude at the VCO mux input. [00] = maximum voltage swing [11] = minimum voltage swing Recommended programming [11]
Bit27	VCO_AMPL_CTRL_1	1	
Bit28	VCO_VB_CTRL_0	0	VCO core bias voltage control 1.2 V, B[29..28] = [00] 1.35 V, B[29..28] = [01] 1.5 V, B[29..28] = [10] 1.65 V, B[29..28] = [11] Recommended programming [01]
Bit29	VCO_VB_CTRL _1	1	
Bit30	RSV	0	Reserved
Bit31	EN_LD_ISOURCE	1	Enable monitoring of LD to turn on I_{SOURCE} when in frac-n mode (EN_FRAC=1). 0 = I_{SOURCE} set by EN_ISOURCE 1 = I_{SOURCE} set by LD Recommended programming [0]

Register 6

Table 10. PLL 4WI Register 6

REGISTER ADDRESS					RSV	RSV	VCO CAP ARRAY CONTROL						LD MODE	VCO TEST MODE	CAL BYPASS
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

MUX CONTROL			ISRC SINK	OFFSET CURRENT ADJUST			LO DIV		LO DIV BIAS		VCO MUX BIAS		DC OFF REF		VCO BIAS SEL
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

BIT NUMBER	BIT NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	0	Register address bits
Bit1	ADDR_1	1	
Bit2	ADDR_2	1	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	RSV	0	Reserved
Bit6	RSV	0	Reserved
Bit7	VCO_TRIM_0	0	VCO capacitor array control bits; used in manual cal mode
Bit8	VCO_TRIM_1	0	
Bit9	VCO_TRIM_2	0	
Bit10	VCO_TRIM_3	0	
Bit11	VCO_TRIM_4	0	
Bit12	VCO_TRIM_5	1	
Bit13	EN_LOCKDET	0	Initiate automatic calibration if LD indicates loss of lock. (1 = Initiate calibration if LD is low)
Bit14	VCO_TEST_MODE	0	Counter mode: measure maximum/minimum frequency of each VCO
Bit15	CAL_BYPASS	0	Bypass of VCO auto-calibration. When '1', VCO_TRIM and VCO_SEL bits are used to select the VCO and the capacitor array setting
Bit16	MUX_CTRL_0	1	Select signal for test output (pin 5, LD). [000] = Ground [001] = Lock detector [010] = NDIV counter output [011] = Ground [100] = RDIV counter output [101] = Ground [110] = A_counter output [111] = Logic high
Bit17	MUX_CTRL_1	0	
Bit18	MUX_CTRL_2	0	
Bit19	ISOURCE_SINK	0	Charge pump offset current polarity. 0 = source I_{SOURCE} current enabled by EN_ISOURCE. Recommended programming [0].

BIT NUMBER	BIT NAME	RESET VALUE	DESCRIPTION
Bit20	ISOURCE_TRIM_0	0	Adjust I_{SOURCE} bias current. Minimum value, ISOURCE_TRIM = 0, B[22..20] = [000] Maximum value, ISOURCE_TRIM = 7, B[22..20] = [111] I_{SOURCE} current enabled by EN_ISOURCE.
Bit21	ISOURCE_TRIM_1	0	
Bit22	ISOURCE_TRIM_2	1	
Bit23	LO_DIV_SEL_0	0	Adjust LO path divider Divide-by-1, [B24..23] = [00] Divide-by-2, [B24..23] = [01] Divide-by-4, [B24..23] = [10] Divide-by-8, [B24..23] = [11]
Bit24	LO_DIV_SEL_1	0	
Bit25	LO_DIV_IB_0	0	Adjust LO divider bias current. [B26..25] = [00] = 25 µA [01] = 37.5 µA [10] = 50 µA [11] = 62.5 µA
Bit26	LO_DIV_IB_1	0	
Bit27	DIV_MUX_REF<0>	0	Sets reference bias current of DIV_MUX buffer when bit 31=1; [00] = 500 µA [01] = 400 µA [10] = 300 µA [11] = 200 µA Recommended programming [10]
Bit28	DIV_MUX_REF<1>	1	
Bit29	DIV_MUX_OUT<0>	0	Set multiply factor for DIV_MUX_REF current. x16, B[30..29] = 00 x24, B[30..29] = 01 x32, B[30..29] = 10 x40, B[30..29] = 11 Recommended programming [10]
Bit30	DIV_MUX_OUT<1>	1	
Bit31	DIV_MUX_BIAS_OVRD	0	Overrides DIV_MUX auto-bias current control. When set to '1', DIV_MUX bias current is set by [B30..27].

READBACK MODE

Register 0 functions as a readback register. The TRF3765 implements the capability to read back the content of any serial programming interface register by initializing Register 0.

Each read-back operation consists of two phases: a write followed by the actual reading of the internal data. This sequence is described in the timing diagram (see Figure 65). During the write phase, a command is sent to TRF3765 Register 0 to set it to readback mode and to specify which register is to be read. In the proper reading phase, at each rising clock edge, the internal data are transferred to the READBACK pin where it can be read at the following falling edge (LSB first). The first clock after the latch enable STROBE, pin 5, goes high (that is, the end of the write cycle) is idle and the following 32 clock pulses transfer the internal register contents to the READBACK pin (pin 6).

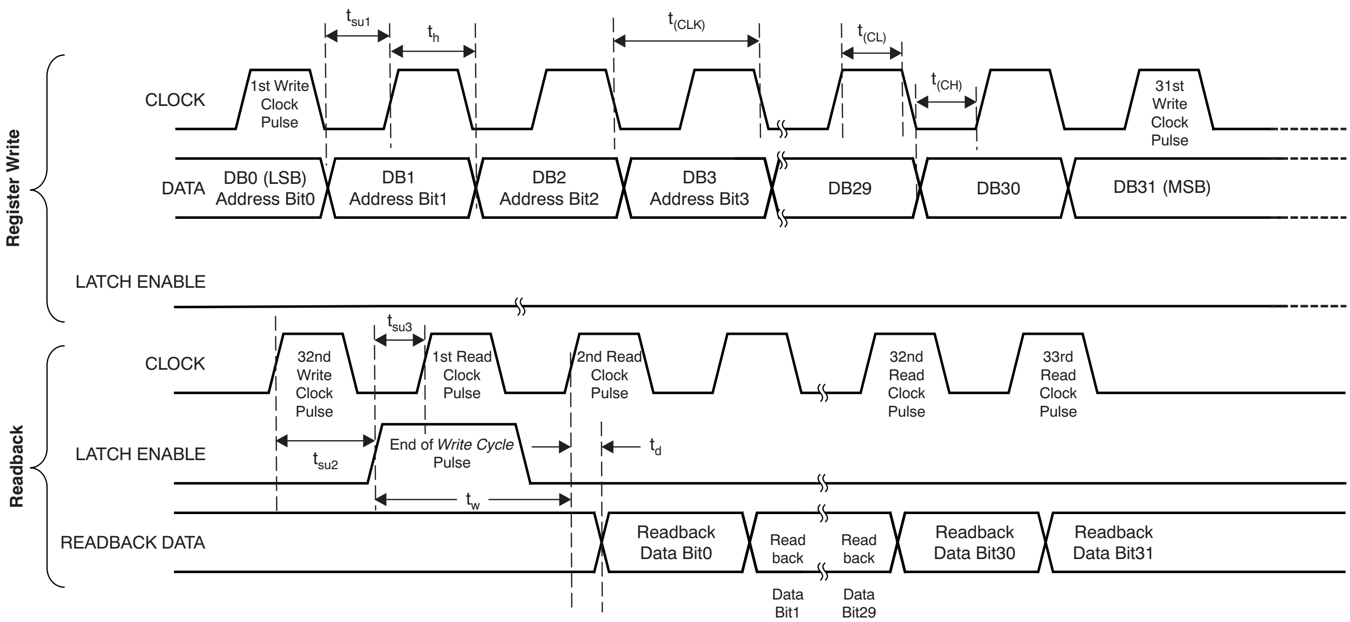


Figure 65. 4WI Readback Timing Diagram

Table 11 lists the readback timing parameters.

Table 11. Readback 4WI Timing

PARAMETER		MIN	MAX	UNITS	COMMENTS
Hold time, data to clock	t_h	20		ns	
Setup time, data to clock	t_{su1}	20		ns	
Clock low duration	$t_{(CH)}$	20		ns	
Clock high duration	$t_{(CL)}$	20		ns	
Setup time, clock to enable	t_{su2}	20		ns	
Setup time, enable to Readback clock	t_{su3}	20			
Delay time, clock to Readback data output	t_d	10		ns	
Enable time	t_w	50		ns	Equals Clock period
Clock period	$t_{(CLK)}$	50		ns	

READBACK FROM THE INTERNAL REGISTER BANKS

The TRF3765 integrates eight registers: Register 0 (000) to Register 7 (111). Registers 1 through 6 are used to set up and control the TRF3765 functions, Register 7 is used for factory functions, and Register 0 is used for the readback function.

Register 0 must be programmed with a specific command that sets the TRF3765 into readback mode and specifies the register to be read, according to the following parameters:

- Set B[31] to '1' to put TRF3765 into readback mode.
- Set B[30,28] equal to the address of the register to be read ('000' to '111').
- Set B27 to control the VCO frequency counter in VCO test mode.

REGISTER 0

Table 12. Register 0 Write

REGISTER ADDRESS					N/C										
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

N/C											COUNT_ MODE_ MUX_SEL	RB_REG			RB_ ENABLE
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

Register 0 Write

TYPE	BIT NUMBER	BIT NAME	RESET VALUE	DESCRIPTION
Address	Bit0	ADDR<0>	0	Register 0 to be programmed to set the TRF3765 into readback mode.
	Bit1	ADDR<1>	0	
	Bit2	ADDR<2>	0	
	Bit3	ADDR<3>	1	
	Bit4	ADDR<4>	0	
Data Field	Bit5	N/C	0	
	Bit6	N/C	0	
	Bit7	N/C	0	
	Bit8	N/C	0	
	Bit9	N/C	0	
	Bit10	N/C	0	
	Bit11	N/C	0	
	Bit12	N/C	0	
	Bit13	N/C	0	
	Bit14	N/C	0	
	Bit15	N/C	0	
	Bit16	N/C	0	
	Bit17	N/C	0	
	Bit18	N/C	0	
	Bit19	N/C	0	
	Bit20	N/C	0	
	Bit21	N/C	0	
	Bit22	N/C	0	
	Bit23	N/C	0	
	Bit24	N/C	0	
	Bit25	N/C	0	
	Bit26	N/C	0	
	Bit27	COUNT_MODE _MUX_SEL	0	Select Readback for VCO maximum frequency or minimum frequency. 0 = Maximum 1 = Minimum
	Bit28	RB_REG<0>	X	Three LSBs of the address for the register that is being read Register 1, B[30..28] = [000] Register 7, B[30..28] = [111]
	Bit29	RB_REG<1>	X	
	Bit30	RB_REG<2>	X	
	Bit31	RB_ENABLE	1	1 → Put the device into readback mode

Register 0 Read

Table 13. Register 0 Read

REGISTER ADDRESS					CHIP_ID	NOT USED						R_SAT_ERR	COUNT0-7/VCO_TRIM		
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

COUNT0-7/VCO_TRIM					COUNT8 / NU	COUNT9-10/VCO_SEL		COUNT11-17							COUNT MODE MUX_SEL
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

BIT NUMBER	BIT NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	0	Register address bits
Bit1	ADDR_1	0	
Bit2	ADDR_2	0	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	CHIP_ID	1	
Bit6	NU	x	
Bit7	NU	x	
Bit8	NU	x	
Bit9	NU	x	
Bit10	NU	x	
Bit11	NU	x	
Bit12	R_SAT_ERR	x	Error flag for calibration speed
Bit13	count_0/NU	x	B[30..13] = VCO frequency counter high when COUNT_MODE_MUX_SEL = 0 and VCO_TEST_MODE = 1 B[30..13] = VCO frequency counter low when COUNT_MODE_MUX_SEL = 1 and VCO_TEST_MODE = 1 B[20..15] = Autocal results for VCO_TRIM B[23..22] = Autocal results for VCO_SEL when VCO_TEST_MODE = 0
Bit14	count_1/NU	x	
Bit15	count_2/VCO_TRIM_0	x	
Bit16	count_3/VCO_TRIM_1	x	
Bit17	count_4/VCO_TRIM_2	x	
Bit18	count_5/VCO_TRIM_3	x	
Bit19	count_6/VCO_TRIM_4	x	
Bit20	count_7/VCO_TRIM_5	x	
Bit21	count_8/NU	x	
Bit22	count_9/VCO_sel_0	x	
Bit23	count_10/VCO_sel_1	x	
Bit24	count<11>	x	
Bit25	count<12>	x	
Bit26	count<13>	x	
Bit27	count<14>	x	
Bit28	count<15>	x	
Bit29	count<16>	x	
Bit30	count<17>	x	
Bit31	COUNT_MODE_MUX_SEL	x	0 = Minimum frequency 1 = Maximum frequency

APPLICATION INFORMATION

INTEGER AND FRACTIONAL MODE SELECTION

The PLL is designed to operate in either Integer mode or Fractional mode. If the desired local oscillator (LO) frequency is an integer multiple of the phase frequency detector (PFD) frequency, f_{PFD}, then Integer mode can be selected. The normalized in-band phase noise floor in Integer mode is lower than in Fractional mode. In Integer mode, the feedback divider is an exact integer, and the fraction is zero. While operating in Integer mode, the register bits corresponding to the fractional control are *don't care*.

In Fractional mode, the feedback divider fractional portion is non-zero on average. With 25-bit fractional resolution, RF stepsize $f_{PFD}/2^{25}$ is less than 1 Hz with a f_{PFD} up to 33 MHz. The appropriate fractional control bits in the serial register must be programmed.

PLL ARCHITECTURE

Figure 66 shows a block diagram of the PLL loop.

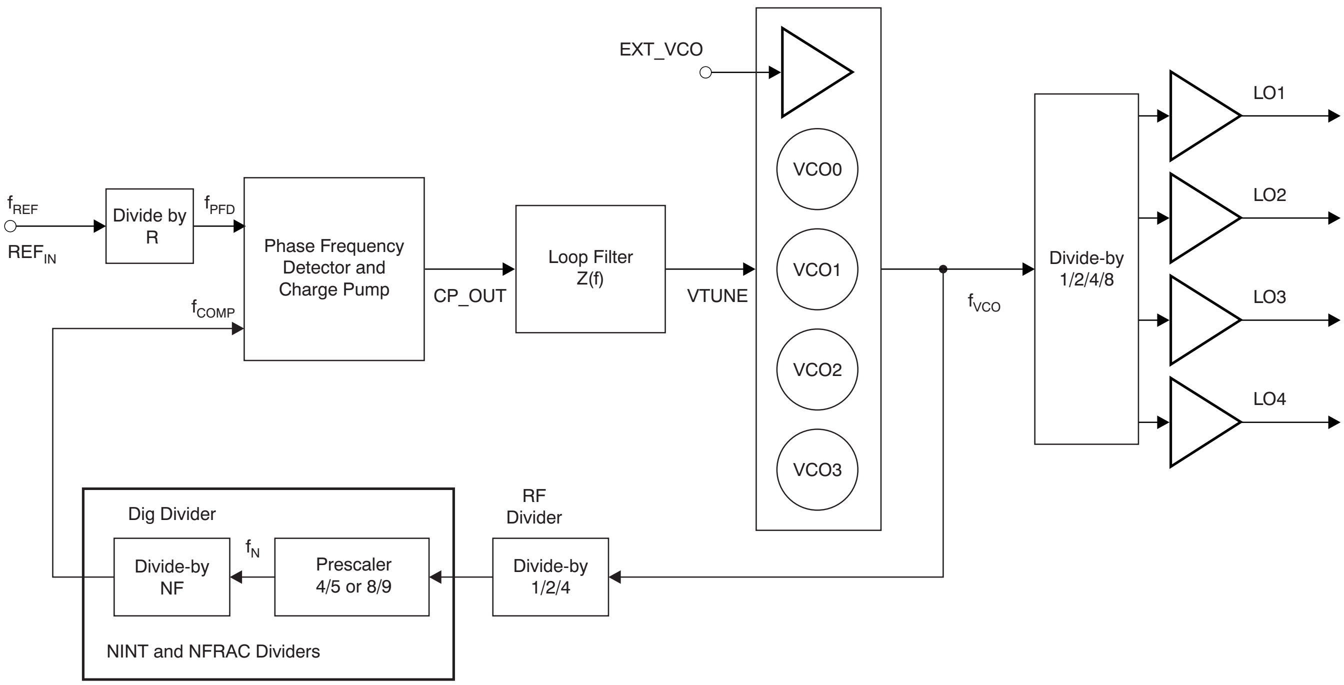


Figure 66. PLL Loop

The output frequency is given by Equation 1:

$$f_{VCO} = \frac{f_{REF}}{RDIV}\,(PLL\_DIV\_SEL)\left[NINT + \frac{NFRAC}{2^{25}}\right] \quad (1)$$

The rate at which phase comparison occurs is f_{REF}/RDIV. In Integer mode, the fractional setting is ignored and Equation 2 is applied.

$$\frac{f_{VCO}}{f_{PFD}} = NINT \times PLL\_DIV\_SEL \quad (2)$$

The feedback divider block consists of a programmable RF divider, a prescaler divider, and an NF divider. The prescaler can be programmed as either a 4/5 or an 8/9 prescaler. The NF divider includes an *A* counter and an *M* counter.

Selecting PLL Divider Values

Operation of the PLL requires the LO_DIV_SEL, RDIV, PLL_DIV_SEL, NINT, and NFRAC bits to be calculated. The LO or mixer frequency is related to f_{VCO} according to divide-by-1/-2/-4/-8 blocks and the operating range of f_{VCO}.

a. **LO_DIV_SEL**

$$\text{LO\_DIV\_SEL} = \begin{cases} 1 & 2400\text{ MHz} \le f_{RF} \le 4800\text{ MHz} \\ 2 & 1200\text{ MHz} \le f_{RF} \le 2400\text{ MHz} \\ 3 & 600\text{ MHz} \le f_{RF} \le 1200\text{ MHz} \\ 4 & 300\text{ MHz} \le f_{RF} \le 600\text{ MHz} \end{cases}$$

Therefore:

$$f_{VCO} = \text{LO\_DIV\_SEL} \times f_{RF}$$

b. **PLL_DIV_SEL**

Given f_{VCO}, select the minimum value for PLL_DIV_SEL so that the programmable RF divider limits the input frequency into the prescaler block, f_{PM}, to a maximum of 3000 MHz.

$$\text{PLL\_DIV\_SEL} = \min(1, 2, 4) \text{ such that } f_{PM} \le 3000\text{ MHz}$$

This calculation can be restated as Equation 3.

$$\text{PLL\_DIV\_SEL} = \text{Ceiling}\left(\frac{\text{LO\_DIV\_SEL} \times f_{RF}}{3000\text{ MHz}}\right) \tag{3}$$

Higher values of f_{PFD} correspond to better phase noise performance in Integer mode or Fractional mode. f_{PFD}, along with PLL_DIV_SEL, determines the f_{VCO} stepsize in Integer mode. Therefore, in Integer mode, select the maximum f_{PFD} that allows for the required RF stepsize, as shown by Equation 4.

$$f_{PFD} = \frac{f_{VCO,\ Stepsize}}{\text{PLL\_DIV\_SEL}} = \frac{f_{RF,\ Stepsize} \times \text{LO\_DIV\_SEL}}{\text{PLL\_DIV\_SEL}} \tag{4}$$

In Fractional mode, a small RF stepsize is accomplished through the Fractional mode divider. A large f_{PFD} should be used to minimize the effects of fractional controller noise in the output spectrum. In this case, f_{PFD} may vary according to the reference clock and fractional spur requirements; for example, f_{PFD} = 20 MHz.

c. **RDIV, NINT, NFRAC, PRSC_SEL**

$$\text{RDIV} = \frac{f_{REF}}{f_{PFD}}$$

$$\text{NINT} = \text{floor}\left(\frac{f_{VCO}\,\text{RDIV}}{f_{REF}\,\text{PLL\_DIV\_SEL}}\right)$$

$$\text{NFRAC} = \text{floor}\left(\left[\left(\frac{f_{VCO}\,\text{RDIV}}{f_{REF}\,\text{PLL\_DIV\_SEL}}\right) - \text{NINT}\right]2^{25}\right)$$

The P/(P+1) programmable prescaler is set to 8/9 or 4/5 through the PRSC_SEL bit. To allow proper fractional control, set PRSC_SEL according to Equation 5.

$$\text{PRSC\_SEL} = \begin{cases} \frac{8}{9} & \text{NINT} \geq 75 \text{ in Fractional Mode or NINT} \geq 72 \text{ in Integer mode} \\ \frac{4}{5} & 23 \leq \text{NINT} < 75 \text{ in Fractional mode or } 20 \leq \text{NINT} < 72 \text{ in Integer mode} \end{cases} \quad (5)$$

The PRSC_SEL limit at NINT < 75 applies to Fractional mode with third-order modulation. In Integer mode, the PRSC_SEL = 8/9 should be used with NINT as low as 72. The divider block accounts for either value of PRSC_SEL without requiring NINT or NFRAC to be adjusted. Then, calculate the maximum frequency to be input to the digital divider at f_N. Use the lower of the possible prescaler divide settings, P = (4,8), as shown by Equation 6.

$$f_{N,Max} = \frac{f_{VCO}}{\text{PLL\_DIV\_SEL} \times P} \quad (6)$$

Verify that the frequency into the digital divider, f_N, is less than or equal to 375 MHz. If f_N exceeds 375 MHz, choose a larger value for PLL_DIV_SEL and recalculate f_{PFD}, RDIV, NINT, NFRAC, and PRSC_SEL.

Setup Example for Integer Mode

Suppose the following operating characteristics are desired for Integer mode operation:

- f_{REF} = 40 MHz (reference input frequency)
- Step at RF = 2 MHz (RF channel spacing)
- f_{RF} = 1600 MHz (RF frequency)

The VCO range is 2400 MHz to 4800 MHz. Therefore:

- LO_DIV_SEL = 2
- f_{VCO} = LO_DIV_SEL × 1600 MHz = 3200 MHz

In order to keep the frequency of the prescaler below 3000 MHz:

- PLL_DIV_SEL = 2

The desired stepsize at RF is 2 MHz, so:

- f_{PFD} = 2 MHz
- f_{VCO}, stepsize = PLL_DIV_SEL × f_{PFD} = 4 MHz

Using the reference frequency along with the required f_{PFD} gives:

- RDIV = 20
- NINT = 800

NINT ≥ 75; therefore, select the 8/9 prescaler.

$f_{N,Max}$ = 3200 MHz/(2 × 8) = 200 MHz < 375 MHz

This example shows that Integer mode operation gives sufficient resolution for the required stepsize.

Setup Example for Fractional Mode

Suppose the following operating characteristics are desired for Fractional mode operation:

- f_{REF} = 40 MHz (reference input frequency)
- Step at RF = 5 MHz (RF channel spacing)
- f_{RF} = 1,600,000,045 Hz (RF frequency)

The VCO range is 2400 MHz to 4800 MHz. Therefore:

- LO_DIV_SEL = 2
- f_{VCO} = LO_DIV_SEL × 1,600,000,045 Hz = 3,200,000,090 Hz

In order to keep the frequency of the prescaler below 3000 MHz:

- PLL_DIV_SEL = 2

Using a typical f_{PFD} of 20 MHz:

- RDIV = 20
- NINT = 80
- NFRAC = 75

NINT ≥ 75; therefore, select the 8/9 prescaler.

$f_{N,Max}$ = 3200 MHz/(2 × 8) = 200 MHz < 375 MHz

The actual frequency at RF is:

- f_{RF} = 1600000044.9419 Hz

For a frequency error of –0.058 Hz.

Fractional Mode Setup

Optimal operation of the PLL in Fractional mode requires several additional register settings. Recommended values are listed in Table 14. Optimal performance may require tuning the MOD_ORD, ISOURCE_SINK, and ISOURCE_TRIM values according to the chosen frequency band.

Table 14. Fractional Mode Register Settings

REGISTER BIT	REGISTER ADDRESSING	RECOMMENDED VALUE
EN_ISOURCE	Reg4B18	1
EN_DITH	Reg4B25	1
MOD_ORD	Reg4B[27..26]	B[27..26] = [10]
DITH_SEL	Reg4B28	0
DEL_SD_CLK	Reg4B[30..29]	B[30..29] = [10]
EN_FRAC	Reg4B31	1
EN_LD_ISOURCE	Reg5B31	0
ISOURCE_SINK	Reg6B19	0
ISOURCE_TRIM	Reg6B[22..20]	B[22..20] = [100] or [111]; see Typical Characteristics
ICPDOUBLE	Reg1B26	0

SELECTING THE VCO AND VCO FREQUENCY CONTROL

To achieve a broad frequency tuning range, the TRF3765 includes four VCOs. Each VCO is connected to a bank of coarse tuning capacitors that determine the valid operating frequency of each VCO. For any given frequency setting, the appropriate VCO and capacitor array must be selected.

The device contains logic that automatically selects the appropriate VCO and capacitor bank. Set bit EN_CAL to initiate the calibration algorithm. During the calibration process, the device selects a VCO and a tuning capacitor state such that V_{TUNE} matches the reference voltage set by VCO_CAL_REF_n. Accuracy of the resulting tuning word is increased through bits CAL_ACC_n at the expense of increased calibration time. A calibration begins immediately when EN_CAL is set; as a result, all registers must contain valid values before a calibration is initiated.

The calibration logic is driven by a CAL_CLK clock derived from the phase frequency detector frequency scaled according to the setting in CAL_CLK_SEL. Faster CAL_CLK frequencies enable faster calibrations, but the logic is limited to clock frequencies up to 600 kHz. The flag R_SAT_ERR is evaluated during the calibration process to indicate calibration counter overflow errors, which occur if CAL_CLK runs too quickly. If R_SAT_ERR is set during a calibration, the resulting calibration is not valid and CAL_CLK_SEL must be used to slow the CAL_CLK. CAL_CLK frequencies should not be set below 0.05 MHz. Reference clock frequency is usually limited by the calibration logic. f_{REF} × CAL_CLK_SEL scaling factor > 0.01 MHz and f_{REF}/(CAL_CLK_SEL scaling factor × f_{PFD}) < 8000 are required. For example, with f_{REF} = 61.44 MHz, f_{PFD} = 30.72 MHz and CAL_CLK_SEL at 1/128, 61.44/128 = 0.5 > 0.01 and 61.44/(30.72 × 1/128) = 256 < 8000.

When VCOSEL_MODE is '0', the device automatically selects both the VCO and capacitor bank within 46 CAL_CLK cycles. When VCOSEL_MODE is '1', the device uses the VCO selected in VCO_SEL_0 and VCO_SEL_1 and automatically selects the capacitor array within 34 CAL_CLK cycles. The VCO and capacitor array settings that result from a calibration cannot be read from the VCO_SEL_n and VCO_TRIM_n bits in Registers 2 and 7. These settings can only be read from Register 0.

Automatic calibration can be disabled by setting CAL_BYPASS to '1'. In this manual calibration mode, the VCO is selected through register bits VCO_SEL_n, while the capacitor array is selected through register bits VCO_TRIM_n. Calibration modes are summarized in Table 15. After calibration is complete, the PLL is released from calibration mode and reaches phase lock.

Table 15. VCO Calibration Modes

CAL_BYPASS	VCOSEL_MODE	MAX CYCLES CAL_CLK	VCO	CAPACITOR ARRAY
0	0	46	Automatic	
0	1	34	VCO_SEL_n	Automatic
1	*don't care*	N/A	VCO_SEL_n	VCO_TRIM_n

During the calibration process, the TRF3765 scans through many frequencies. RF and LO outputs should be disabled until calibration is complete. At power-up, the RF and LO output are disabled by default. Once a calibration has been performed at a given frequency setting, the calibration remains valid over all operating temperature conditions.

EXTERNAL VCO

An external LO or VCO signal may be applied. EN_EXTVCO powers the input buffer and selects the buffered external signal instead of an internal VCO. Dividers, phase-frequency detector, and charge pump remain enabled and may be used to control V_{TUNE} or an external VCO. NEG_VCO must correspond to the sign of the external VCO tuning characteristic. EXT_VCO_CTRL = '1' asserts a logic 1 output level at the corresponding output pin. This configuration can be used to enable or disable the external VCO circuit or module.

VCO_TEST_MODE

Setting VCO_TEST_MODE forces the currently selected VCO to the edge of its frequency range by disconnecting the charge pump input from the phase detector and loop filter, and forcing its output high or low. The upper or lower edge of the VCO range is selected through COUNT_MODE_MUX_SEL.

VCO_TEST_MODE also reports the value of a frequency counter in COUNT, which can be read back in Register 0. COUNT reports the number of digital *N* divider cycles in the PLL, directly related to the period of f_N, that occur during each CAL_CLK cycle. Counter operation is initiated through the bit EN_CAL. Table 16 summarizes the settings for VCO_TEST_MODE.

Table 16. VCO_TEST_MODE Settings

VCO_TEST_MODE	COUNT_MODE_MUX_SEL	VCO OPERATION	REGISTER 0 B[30..13]
0	*Don't care*	Normal	B[30..24] = undefined B[23..22] = VCO_SEL selected during autocal B21 = undefined B[20..15] = VCO_TRIM selected during autocal B[14..13] = undefined
1	0	Max frequency	B[30..13] = Max frequency counter
1	1	Min frequency	B[30..13] = Min frequency counter

LOOP FILTER

Loop filter design is critical for achieving low closed-loop phase noise. Some typical loop filter component values are given in Table 17, referenced to designators in Figure 67. These loop filters are designed using a charge pump current of 1.94 mA to minimize noise.

Table 17. Typical Loop Filter Components

f_{PFD} (MHz)	C1 (pF)	C2 (pF)	R2 (kΩ)	C3 (pF)	R3 (kΩ)	C4 (pF)	R4 (kΩ)
1.6	47	560	10	4.7	5	open	0
30.72	2200	22000	0.47	220	0.47	220	0.47

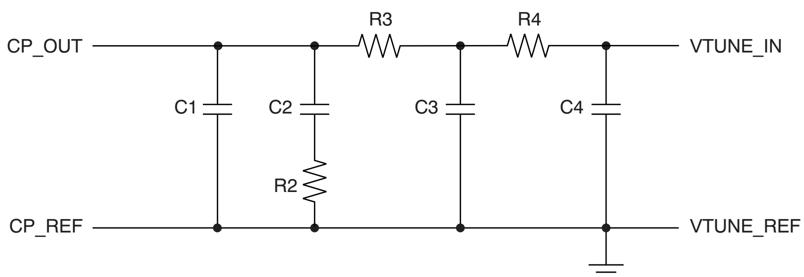


Figure 67. Loop Filter Component Reference Designators

LOCK DETECT

The lock detect signal is generated in the phase frequency detector by comparing the VCO target phase against the VCO actual phase. When the two compared phase signals remain aligned for several clock cycles, an internal signal goes high. The precision of this comparison is controlled through the LD_ANA_PREC bits. This internal signal is then averaged and compared against a reference voltage to generate the LD signal. The number of averages used is controlled through LD_DIG_PREC. Therefore, when the VCO is frequency locked, LD is high. When the VCO frequency is not locked, LD may pulse high or exhibit periodic behavior.

By default, the internal lock detect signal is made available on the LD terminal. Register bits MUX_CTRL_n can be used to control a multiplexer to output other diagnostic signals on the LD output. The LD control signals are shown in Table 18. Table 19 shows the LD Control Signal Mode settings.

Table 18. LD Control Signals

ADJUSTMENT	REGISTER BITS	BIT ADDRESSING
Lock detect precision	LD_ANA_PREC_0	Reg4B19
Unlock detect precision	LD_ANA_PREC_1	Reg4B20
LD averaging count	LD_DIG_PREC	Reg4B24
Diagnostic output	MUX_CTRL_n	Reg6B[18..16]

Table 19. LD Control Signal Mode Settings

CONDITION	RECOMMENDED SETTINGS
Integer mode	LD_ANA_PREC_0 = 0 LD_ANA_PREC_1 = 0 LD_DIG_PREC = 0
Fractional mode	LD_ANA_PREC_0 = 1 LD_ANA_PREC_1 = 1 LD_DIG_PREC = 0

LO DIVIDER

The LO divider is shown in Figure 68. It frequency divides the VCO output. Only one of the dividers operates at a time, and the appropriate output is selected by a mux. DIVn bits are controlled through LO_DIV_SEL_n. The output is buffered and provided on output pins LOn_OUT_P and LOn_OUT_N. Outputs are phase-locked but not phase-matched. The output level is controlled through BUFOUT_BIAS.

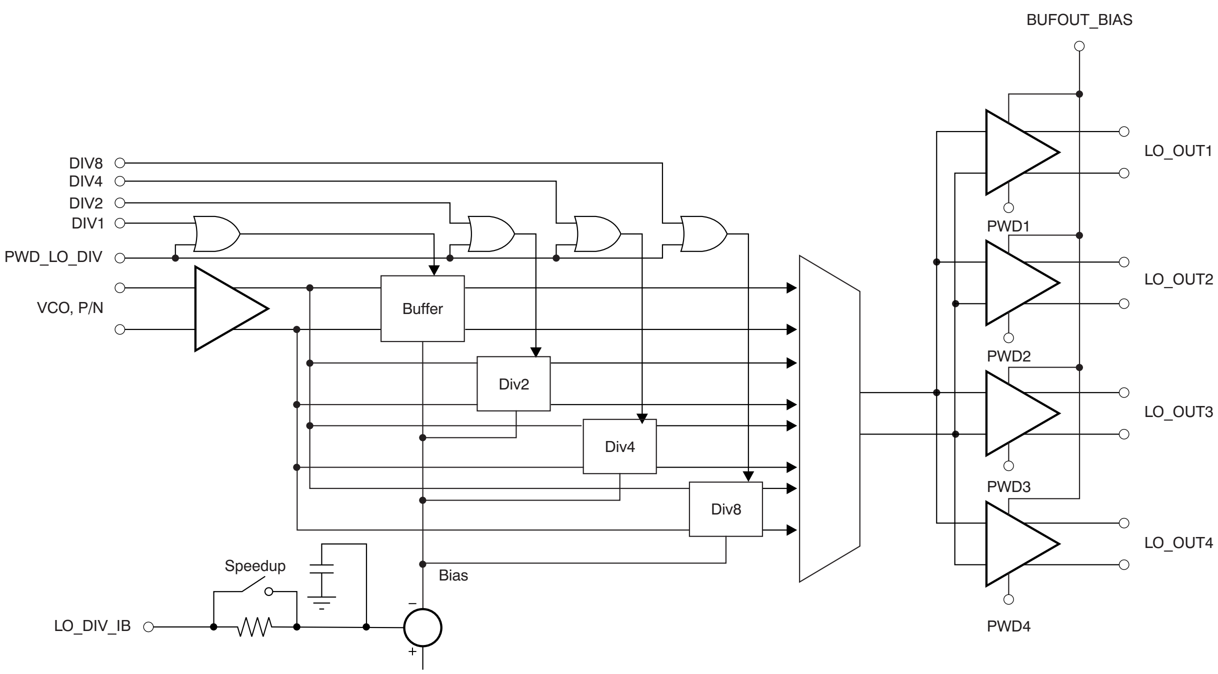


Figure 68. LO Divider

LO_DIV_IB determines the bias level for the divider blocks. The SPEEDUP control is used to bypass a stabilization resistor and reach the final bias level faster after a change in the divider selection. SPEEDUP should be disabled during normal operation.

POWER-SUPPLY DISTRIBUTION

Power-supply distribution for the TRF3765 is shown in Table 20. Proper isolation and filtering of the supplies are critical for low phase noise operation of the device. Each supply pin should be supplied with local decoupling capacitance and isolated with a ferrite bead.

Table 20. Power-Supply Distribution

PIN	SUPPLY	BLOCKS
2	VCC_DIG	Fractional divider
		N-Divider
7	VCC_DIV	LO_OUT buffers
		LO 1/2/4/8 divider
20	VCC_TK	VCO tank
21	VCC_OSC	VCO bias
27	VCC_CP	Charge pump
28	VCC_PLL	4WI
		LD
		Prescaler
		REF_IN buffer
		ISource
		RF-Divider
		R-Divider

APPLICATION SCHEMATIC

Figure 69 illustrates a typical application schematic for the TRF3765. Table 21 lists the pin termination requirements and interfacing for the circuit.

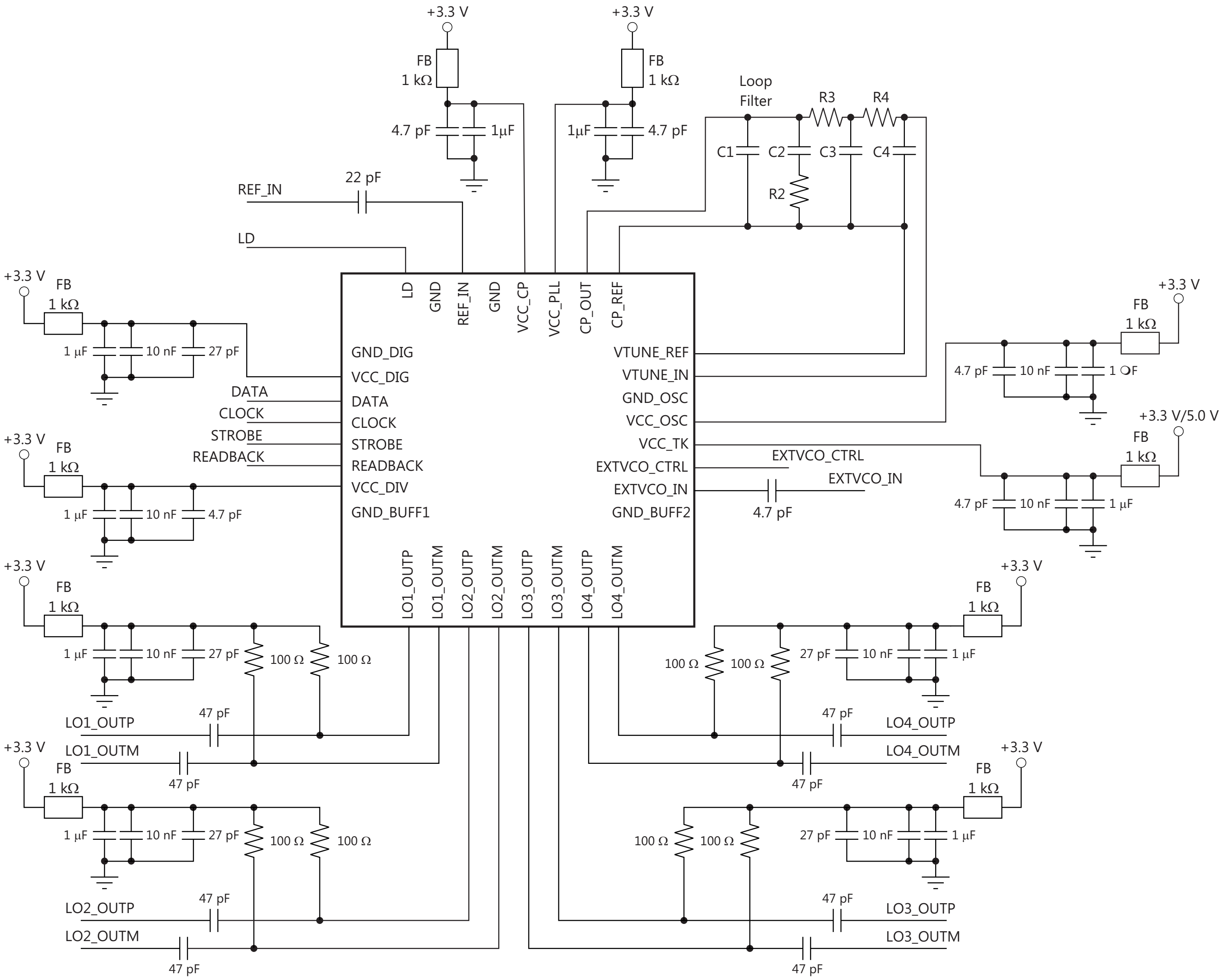


Figure 69. TRF3765 Application Schematic

Table 21. Pin Termination Requirements and Interfacing

PIN	NAME	DESCRIPTION
3	DATA	4WI data input: digital input, high impedance
4	CLOCK	4WI clock input: digital input, high impedance
5	STROBE	4WI latch enable: digital input, high impedance
6	READBACK	Readback output; digital output pins can source or sink up to 8 mA of current
9 through 16	LO_OUT	Local oscillator output: open-collector output. A pull-up resistor is required, normally ac-coupled. Any unused output differential pairs may be left open.
18	EXTVCO_IN	External local oscillator input: high impedance, normally ac-coupled
19	EXTVCO_CTRL	Power-down control pin for optional external VCO; digital output pins can source or sink up to 8 mA of current
30	REF_IN	Reference clock input: high impedance, normally ac-coupled
32	LD	Lock detector digital output, as configured by MUX_CTRL; digital output pins can source or sink up to 8 mA of current

APPLICATION LAYOUT

Layout of the application board significantly impacts the analog performance of the TRF3765 device. Noise and high-speed signals should be prevented from leaking onto power-supply pins or analog signals. Follow these recommendations:

1. Place supply decoupling capacitors physically close to the device, on the same side of the board. Each supply pin should be isolated with a ferrite bead.
2. Maintain a continuous ground plane in the vicinity of the device and as return paths for all high-speed signal lines. Place reference plane vias or decoupling capacitors near any signal line reference transition.
3. The pad on the bottom of the device must be electrically grounded. Connect GND pins directly to the pad on the surface layer. Connect the GND pins and pad directly to surface ground where possible.
4. Power planes should not overlap each other or high-speed signal lines.
5. Isolate REF_IN routing from loop filter lines, control lines, and other high-speed lines.

See Figure 70 for an example of critical component layout (for the top PCB layer).

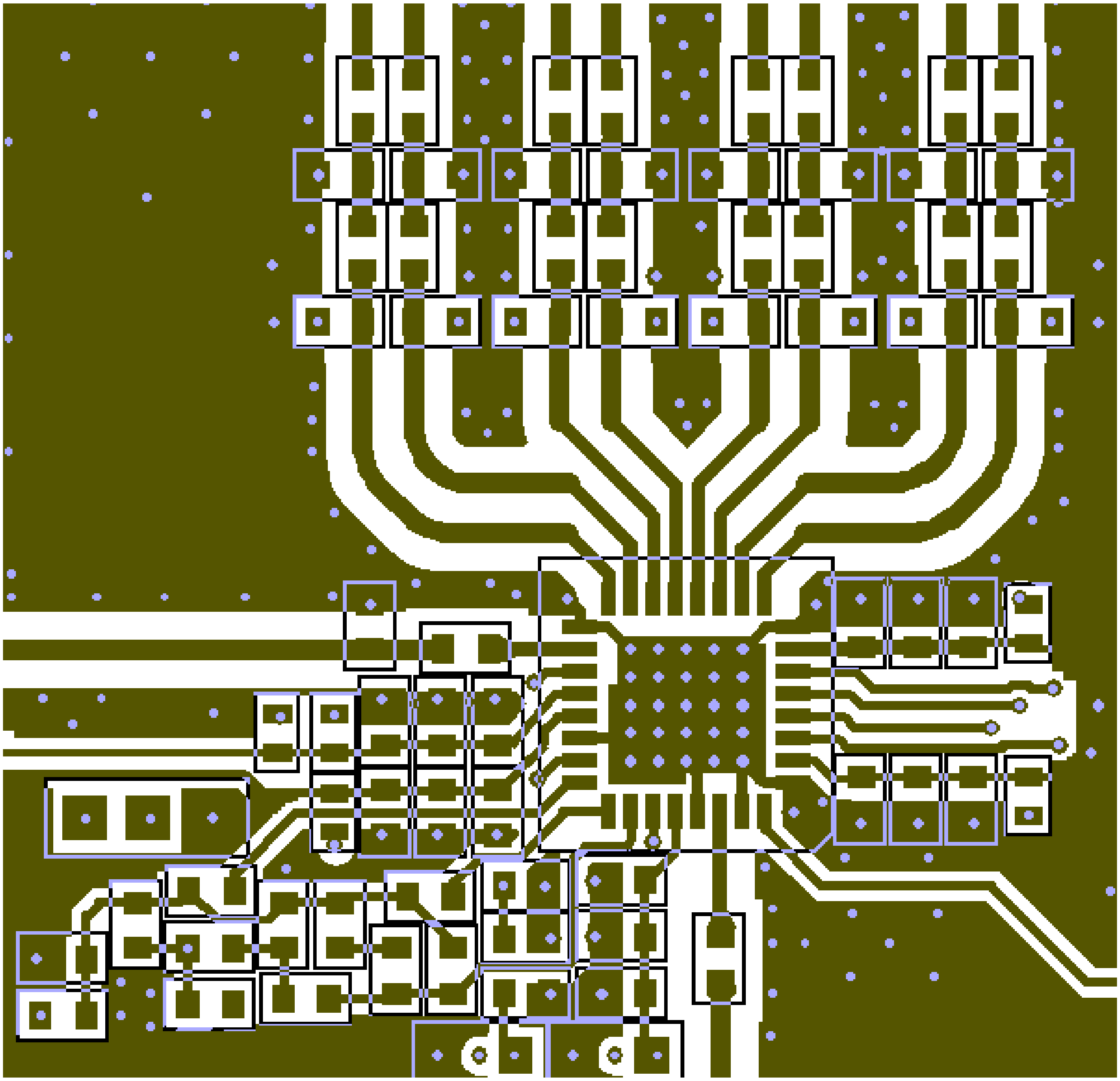


Figure 70. Layout of Critical TRF3765 Components

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2011) to Revision C **Page**

- Changed Reference Oscillator Parameters, *Reference input impedance* parameter rows in Electrical Characteristics table 3

Changes from Revision C (December 2011) to Revision D **Page**

- Changed the Description of Bit25 and Bit26 in Register 6 30
- Changed the Description of Bit27 and Bit28 in Register 6 30
- Changed the Bit Name of Bit31 From: DIV_MUX_BIAS_OVRT To: DIV_MUX_BIAS_OVRD in Register 6 30
- Changed VCC_OSC From: +3.3V/5.0V To: +3.3V, and VCC_TK From: +3.3V To: +3.3V/5.0V in Figure 69 42

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF3765IRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TRF3765 IRHB	Samples
TRF3765IRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TRF3765 IRHB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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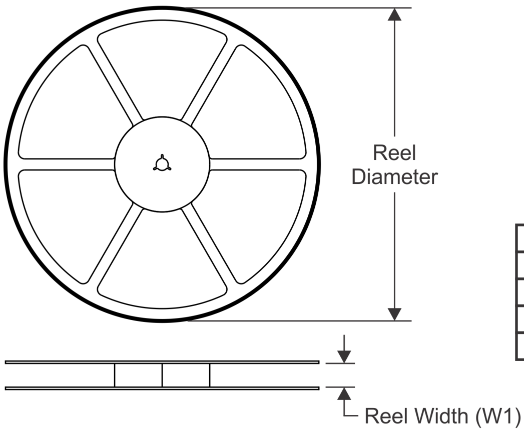
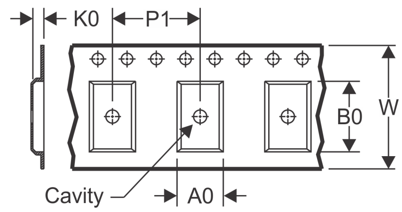
TAPE AND REEL INFORMATION

REEL DIMENSIONS

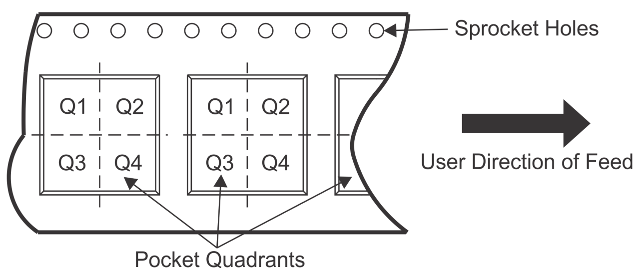


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

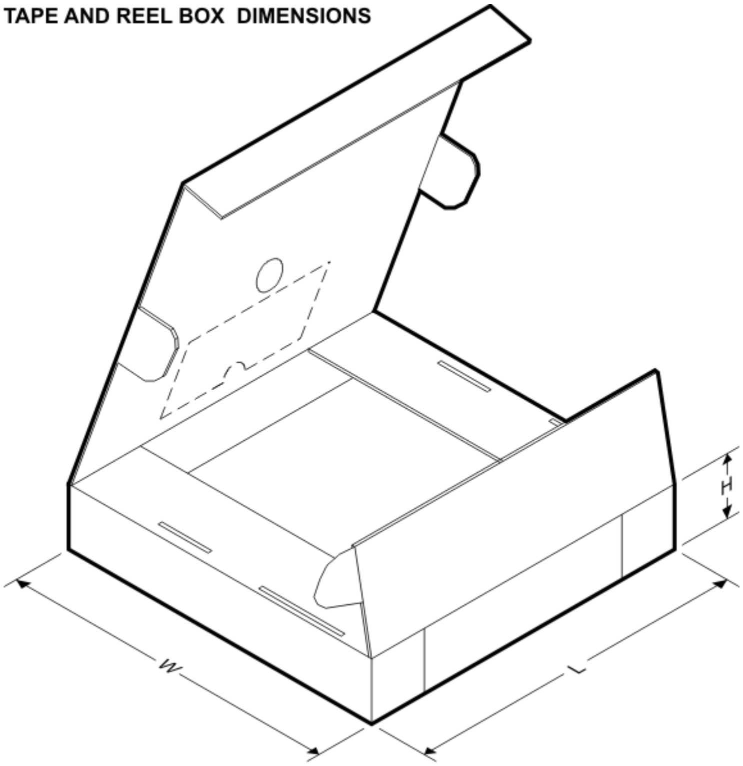
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF3765IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRF3765IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

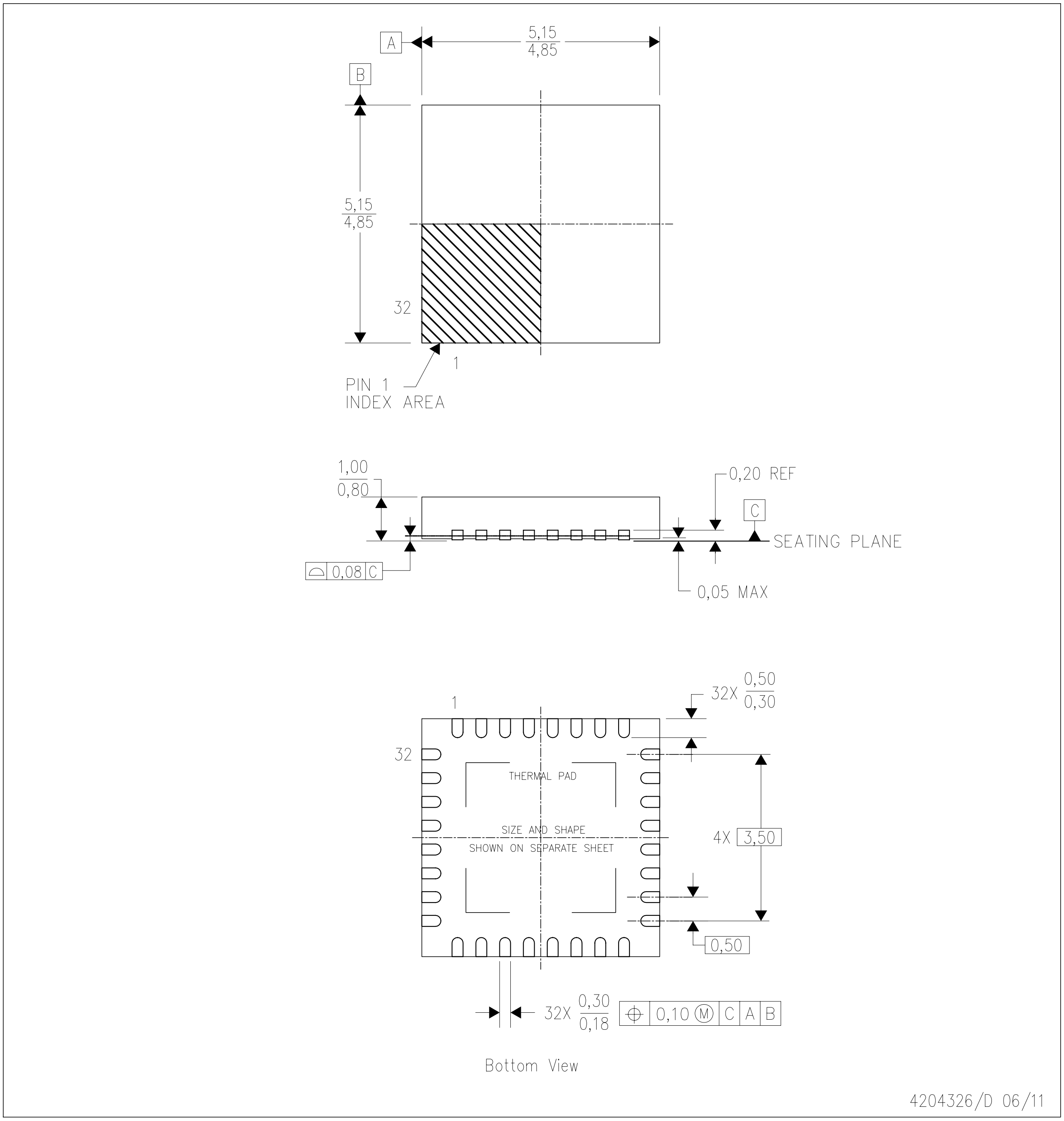
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF3765IRHBR	VQFN	RHB	32	3000	338.1	338.1	20.6
TRF3765IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

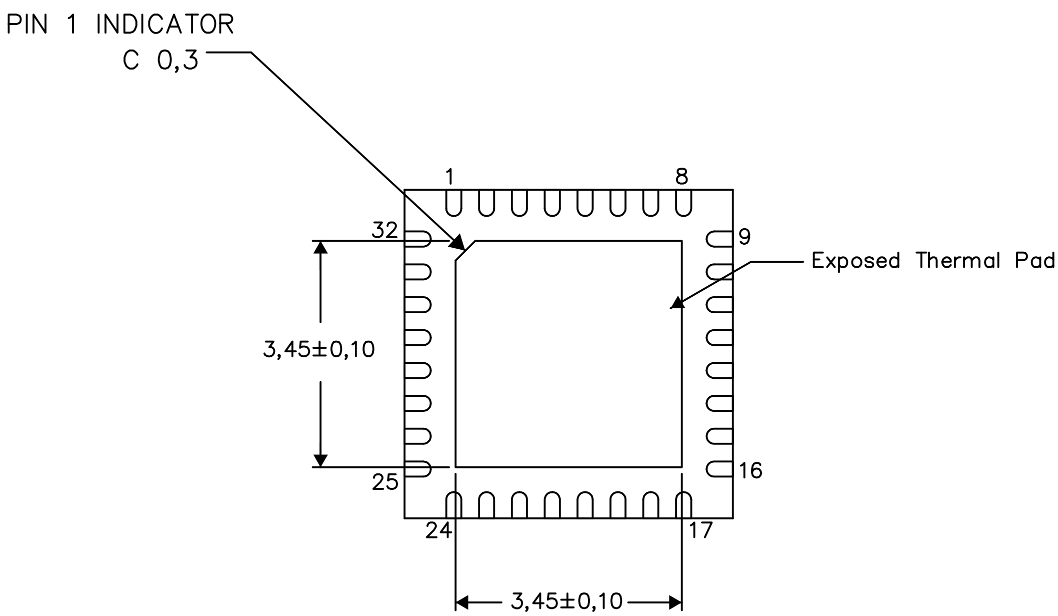
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



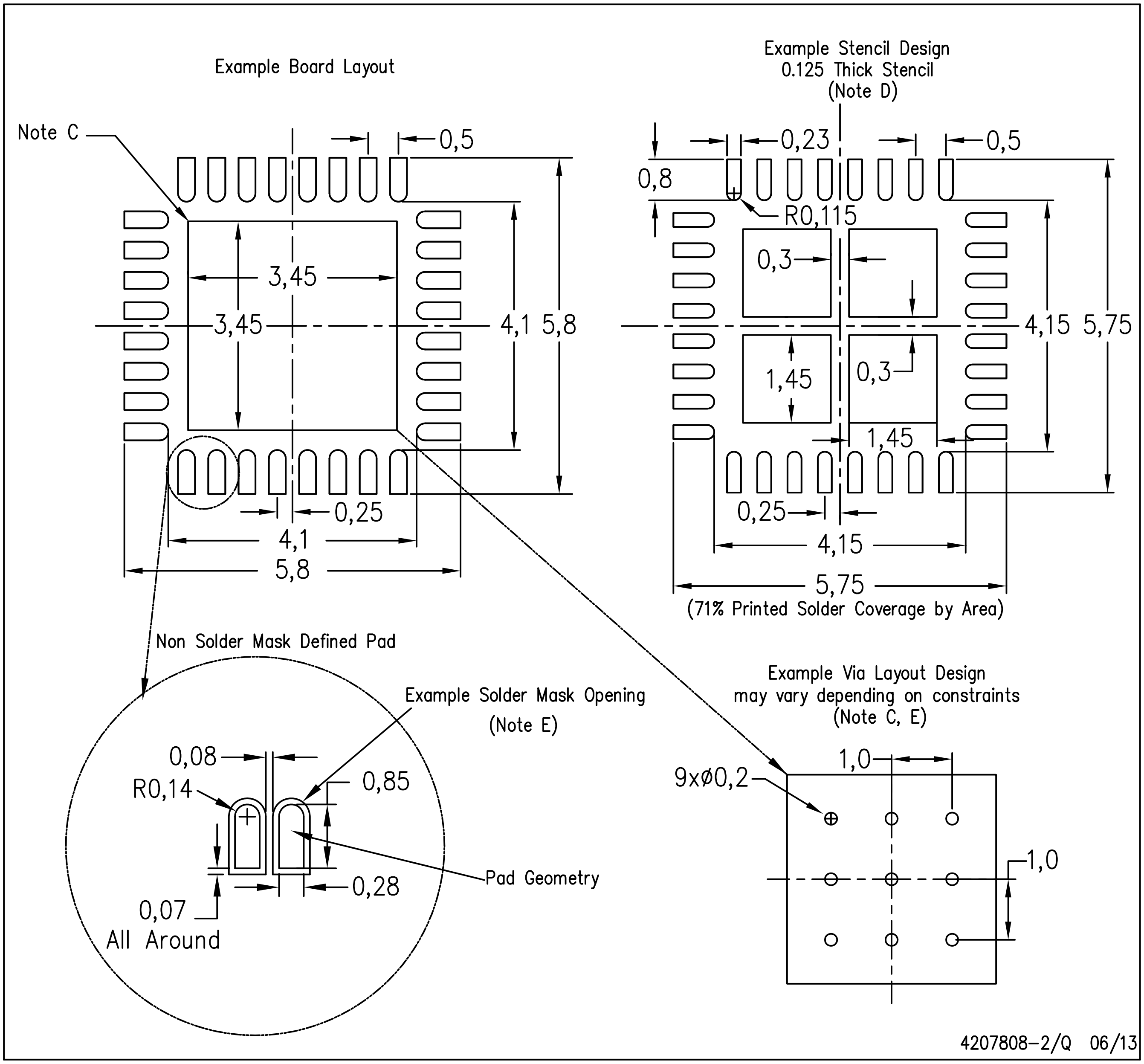
Bottom View

Exposed Thermal Pad Dimensions

4206356-2/Y 06/13

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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