±6 V/+12 V, 5 Ω, LOW r_{ON} SINGLE SPDT ANALOG SWITCH

Check for Samples: TS12A12511

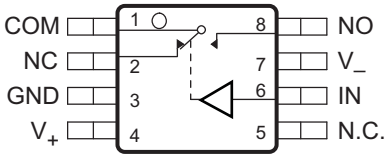
FEATURES

- ±2.7 V to ±6 V Dual Supply
- 2.7 V to 12 V Single Supply
- 5-Ω (typ) ON-State Resistance
- 1.6-Ω (typ) ON-State Resistance Flatness
- 3.3-V, 5-V Compatible Digital Control Inputs
- Rail-to-Rail Analog Signal Handling
- Fast t_{ON}, t_{OFF} Times
- Tiny 8-Lead SOT-23, 8-Lead MSOP, and QFN-8 Packages
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

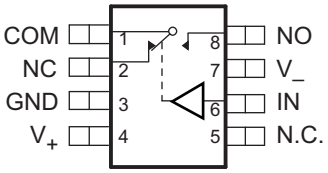
APPLICATIONS

- Automatic Test Equipment
- Power Routing
- Communication Systems
- Data Acquisition Systems
- Sample-and-Hold Systems
- Relay Replacement
- Battery-Powered Systems

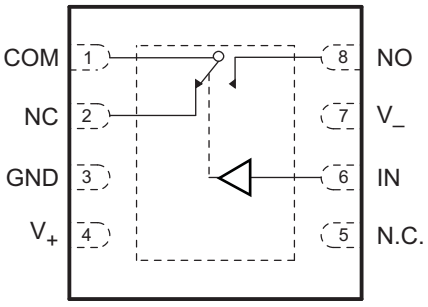
DGK PACKAGE
(TOP VIEW)



DCN PACKAGE
(TOP VIEW)



DRJ PACKAGE
(TOP VIEW)



N.C. – Not internally connected
NC – Normally closed
NO – Normally open

The Exposed Thermal Pad must be electrically connected to V_ or left floating.

DESCRIPTION/ORDERING INFORMATION

The TS12A12511 is a single-pole double-throw (SPDT) analog switch capable of passing signals with swings of 0 to 12 V or –6 V to 6 V. This switch conducts equally well in both directions when it is on. It also offers a low ON-state resistance of 5 Ω (typical), which is matched to within 1 Ω between channels. The max current consumption is <1 µA and –3 dB bandwidth is >93 MHz. The TS12A12511 exhibits break-before-make switching action, preventing momentary shorting when switching channels. This device is available packaged in an 8-lead MSOP, 8-lead SOT-23, and a 8-pin QFN.

Table 1. ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	MSOP – DGK	Tape and reel	TS12A12511DGKR	2US
	QFN – DRJ	Tape and reel	TS12A12511DRJR	ZVE
	SOT – DCN	Tape and reel	TS12A12511DCNR	NFH

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

TRUTH TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	On	Off
H	Off	On

ABSOLUTE MAXIMUM RATINGS(1)

T_A = 25°C (unless otherwise noted).

			MIN	MAX	UNIT
V_+ to V_-				13	V
V_+ to GND			–0.3	13	V
V_- to GND			–6.5	0.3	V
$V_{I/O}$	Analog inputs		V_- – 0.5	V_+ + 0.5	V
I_{IN}	Digital inputs			±30	mA
$I_{I/O}$	Peak current	NC, NO, or COM		±100	mA
	Continuous current	NC, NO, or COM		±50	mA
T_{stg}	Storage temperature range		–65	150	°C
T_A	Operating temperature range		–40	85	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE RATINGS

				UNIT
θ_{JA}	Package thermal impedance	DCN package	220	°C/W
		DGK package	173	
		DRJ package	103	

ELECTRICAL CHARACTERISTICS
±5-V Dual Supply

V_+ = 5 V ± 10%, V_- = -5 V ± 10%, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A= 25°C			T_A= –40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Analog Switch									
Analog signal range						V_-		V_+	V
ON-state resistance	r_{ON}	V_{NC} = -4.5 V to +4.5 V or V_{NO} = –4.5 V to 4.5 V, I_{COM} = –10 mA; see Figure 12		5			5	8	Ω
ON-state resistance match between channels	Δr_{ON}	V_{NC} = -4.5 V to +4.5 V or V_{NO} = -4.5 V to +4.5 V, I_{COM} = –10 mA		1	1.2			1.6	Ω
ON-state resistance flatness	$r_{ON(flat)}$	V_{NC} = -3.3 V to +3.3 V or V_{NO} = -3.3 V to +3.3 V, I_{COM} = –10 mA		1.6	2.2			2.2	Ω
Leakage Currents									
OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} = -4.5 V to +4.5 V or V_{NO} = -4.5 V to +4.5V V_{COM} = -4.5 V to +4.5 V; see Figure 13		±0.5	±1			±50	nA
ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} = -4.5 V to +4.5 V or V_{NO} = -4.5 V to +4.5 V V_{COM} = open; see Figure 14		±0.5	±1			±50	nA
Digital Inputs									
High-level input voltage	V_{INH}					2.4		V_+	V
Low-level input voltage	V_{INL}					0		0.8	V
Input current	I_{INL}, I_{INH}	V_{IN} = V_{INL} or V_{INH}		0.005				±1	µA
Control input capacitance	C_{IN}			2.5					pF
Dynamic(1)									
Turn-ON time	t_{ON}	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see Figure 16		80	95			115	ns
Turn-OFF time	t_{OFF}	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V		41	50			56	ns
Break-before-make time delay	t_{BBM}	R_L = 300 Ω, C_L = 35 pF, V_{NC} = V_{NO} = 3.3 V; see Figure 17		36		18			ns
Charge injection	Q_C	V_{NC} = V_{NO} = 0 V, R_{GEN} = 0 Ω, C_L = 1 nF; see Figure 18		26					pC
OFF isolation	O_{ISO}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 19		–70					dB
Channel-to-channel crosstalk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 20		–70					dB
Bandwidth –3 dB	BW	R_L = 50 Ω, C_L = 5 pF; see Figure 21		93					MHz
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 15pF, VNO = 1V_{RMS}, f = 20 kHz; see Figure 22		0.004					%
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	f = 1 MHz; see Figure 15		14					pF
COM, NC, NO ON capacitance	$C_{COM(ON)}$, $C_{NC(ON)}$, $C_{NO(ON)}$	f = 1 MHz; see Figure 15		60					pF
Supply									
Positive supply current	I_+			0.03				1	µA

(1) Ensured by design, not subject to production test.

ELECTRICAL CHARACTERISTICS
12-V Single Supply

V_+ = 12 V ± 10%, V_- = 0 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A= 25°C			T_A= –40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Analog Switch									
Analog signal range						0		V_+	V
ON-state resistance	r_{on}	V_{NC} =0 V to 10.8 V or V_{NO} = 0 V to 10.8 V, I_{COM} = –10 mA, see Figure 12		5			5	8	Ω
ON-state resistance match between channels	Δr_{on}	V_{NC} = 0 V to 10.8 V or V_{NO} = 0 V to 10.8 V, I_{COM} = –10 mA		1.6	2.4			2.6	Ω
ON-state resistance flatness	$r_{on(flat)}$	V_{NC} = 3.3 V to 7V or V_{NO} = 3.3 V to 7 V, I_{COM} = –10 mA		1.7			1.8	3.2	Ω
Leakage Currents									
OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} = 0 V to 10.8 V or V_{NO} = 0 V to 10.8 V, V_{COM} = 0 V to 10.8 V; see Figure 13		±0.5	±10			±50	nA
ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} = 0 V to 10.8V or V_{NO} = 0 V to 10.8 V, V_{COM} = open; see Figure 14		±0.5	±10			±50	nA
Digital Inputs									
High-level input voltage	V_{INH}					5		V_+	V
Low-level input voltage	V_{INL}					0		0.8	V
Input current	I_{INL}, I_{INH}	V_{IN} = V_{INL} or V_{INH}		±0.005				±0.1	µA
Digital input capacitance	C_{IN}			2.7					pF

ELECTRICAL CHARACTERISTICS
12-V Single Supply (continued)

V_+ = 12 V ± 10%, V_- = 0 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A= 25°C			T_A= –40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic(1)									
Turn-ON time	t_{ON}	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see Figure 16		56	85			110	ns
Turn-OFF time	t_{OFF}	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see Figure 16		25	30			31	ns
Break-before-make time delay	t_{BBM}	R_L = 300 Ω, C_L = 35 pF, V_{NC} = V_{NO} = 3.3 V; see Figure 17		30		19			ns
Charge injection	Q_C	R_{GEN} = V_{NC} = V_{NO} = 0 V, R_{GEN} = 0 Ω, C_L = 1 nF; see Figure 18		491					pC
OFF isolation	O_{ISO}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 19		–70					dB
Channel-to-channel crosstalk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 20		–70					dB
Bandwidth –3 dB	BW	R_L = 50 Ω, C_L = 5 pF, see Figure 21		122					MHz
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 15pF, V_{NO} = 1V_{RMS}, f = 20 kHz; see Figure 22		0.04					%
NC, NO OFF capacitance	$C_{NC(OFF)}$, $CI_{NO(OFF)}$	f = 1 MHz, see Figure 15		14					pF
COM, NC, NO ON capacitance	$C_{COM(ON)}$, $C_{NC(ON)}$, $C_{NO(ON)}$	f = 1 MHz, see Figure 15		55					pF
Supply									
Positive supply current	I_+			0.07				1	µA

(1) Ensured by design, not subject to production test.

ELECTRICAL CHARACTERISTICS
5-V Single Supply

V_+ = 5 V ± 10%, V_- = 0 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A= 25°C			T_A= –40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Analog Switch									
Analog signal range						0		V_+	V
ON-state resistance	r_{on}	V_{NC} =0 V to 4.5 V or V_{NO} = 0 V to 4.5 V, I_{COM} = –10 mA; see Figure 12		8	10			12.5	Ω
ON-state resistance match between channels	Δr_{on}	V_{NC} =0 V to 4.5 V or V_{NO} = 0 V to 4.5 V, I_{COM} = –10 mA		1	1.1			1.5	Ω
ON-state resistance flatness	$r_{on(flat)}$	V_{NC} =0 V to 4.5 V or V_{NO} = 0 V to 4.5 V, I_{COM} = –10 mA		1.3			1.3	2	Ω
Leakage Currents									
OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} =0 V to 4.5 V or V_{NO} = 0 V to 4.5 V, V_{COM} = 0 V to 4.5 V; see Figure 13		±0.5	±1			±50	nA
ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} = 0 V to 4.5V or V_{NO} = 0 V to 4.5 V, V_{COM} = open; see Figure 14		±0.5	±1			±50	nA
Digital Inputs									
High-level input voltage	V_{INH}					2.4		V_+	V
Low-level input voltage	V_{INL}					0		0.8	V
Input current	I_{INL}, I_{INH}	V_{IN} = V_{INL} or V_{INH}		0.01				±0.1	µA
Digital input capacitance	C_{IN}			2.8					pF

ELECTRICAL CHARACTERISTICS
5-V Single Supply (continued)

V_+ = 5 V ± 10%, V_- = 0 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A= 25°C			T_A= –40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic(1)									
Turn-ON time	t_{ON}	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see Figure 16		119	145			178	ns
Turn-OFF time	t_{OFF}	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see Figure 16		38	47			95.2	ns
Break-before-make time delay	t_{BBM}	R_L = 300 Ω, C_L = 35 pF, V_{NC} = V_{NO} = 3.3 V; see Figure 17		79		44			ns
Charge injection	Q_C	V_{GEN} = V_{NC} = V_{NO} = 0 V, R_{GEN} = 0 Ω, C_L = 1 nF; see Figure 18		65					pC
OFF isolation	O_{ISO}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 19		–70					dB
Channel-to-channel crosstalk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 20		–70					dB
Bandwidth –3 dB	BW	R_L = 50 Ω, see Figure 21		152					MHz
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 15 pF, V_{NO} = 1 VRMS, f = 20 kHz; see Figure 22		0.04					%
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	f = 1 MHz, see Figure 15		15					pF
COM, NC, NO ON capacitance	$C_{COM(ON)}$, $C_{NC(ON)}$, $I_{NO(ON)}$	f = 1 MHz, see Figure 15		55					pF
Power Requirements									
V_+ supply current	I_+	V_{IN} = 0 V or V_+		0.02				1	µA

(1) Ensured by design, not subject to production test.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Pin Function Descriptions

TERMINAL		DESCRIPTION
NAME	NO.	
1	COM	Common terminal. Can be an input or output.
2	NC	Normally closed. Can be an input or output.
3	GND	Ground (0 V) reference
4	V_+	Most positive power supply
5	N.C.	No connect. Not internally connected.
6	IN	Logic control input
7	V_-	Most negative power supply. This pin is only used in dual-supply applications and should be tied to ground in single-supply applications.
8	NO	Normally open. Can be an input or output.

TYPICAL PERFORMANCE CHARACTERISTICS

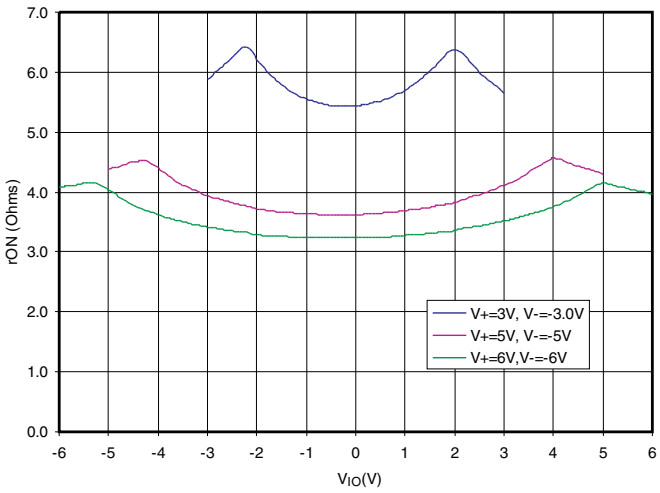


Figure 1. r_{ON} vs V_{IO}

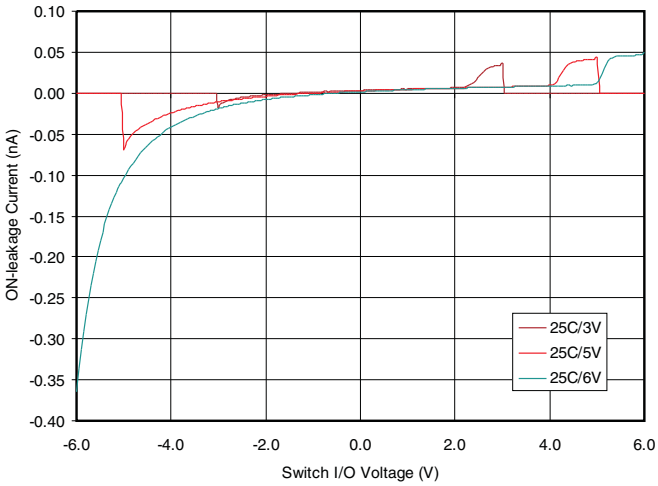


Figure 2. Leakage Current vs I/O voltage (Switch ON)

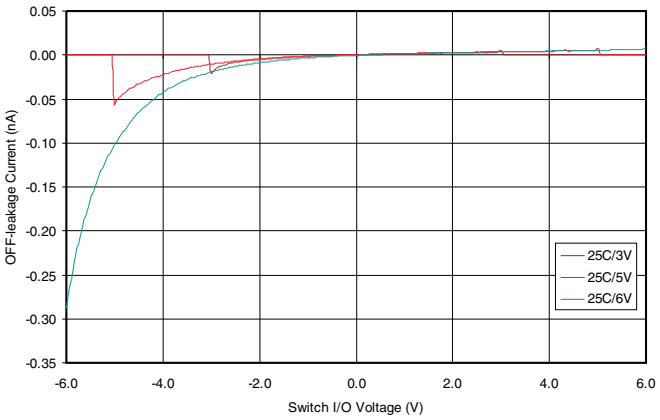


Figure 3. Leakage Current vs I/O Voltage (Switch OFF)

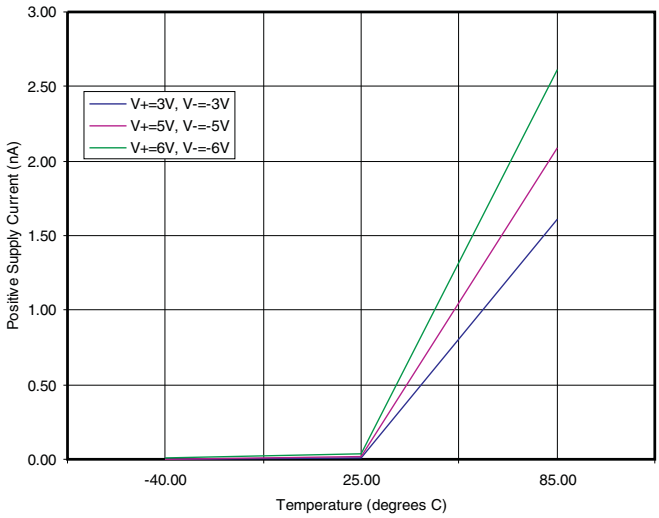


Figure 4. Positive Supply Current vs Temperature

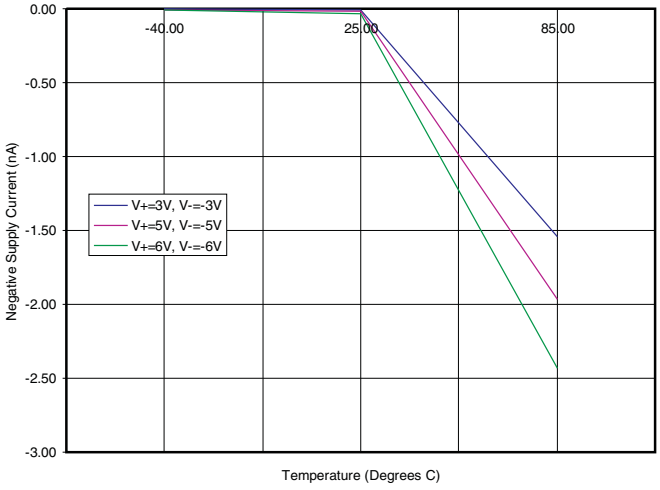


Figure 5. Negative Supply Current vs Temperature

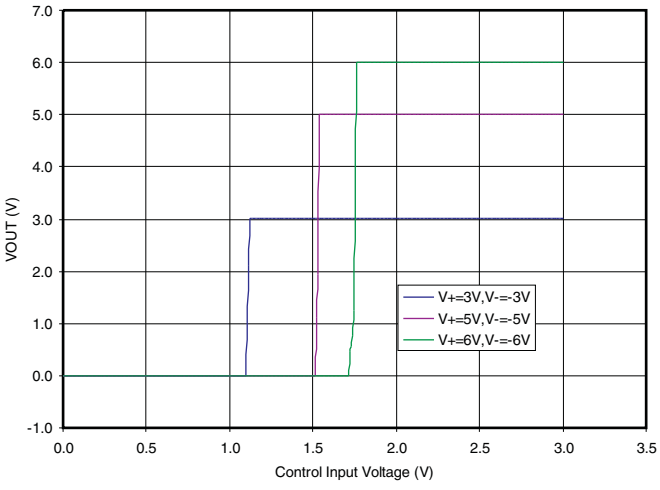


Figure 6. Control Input (IN) Threshold Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

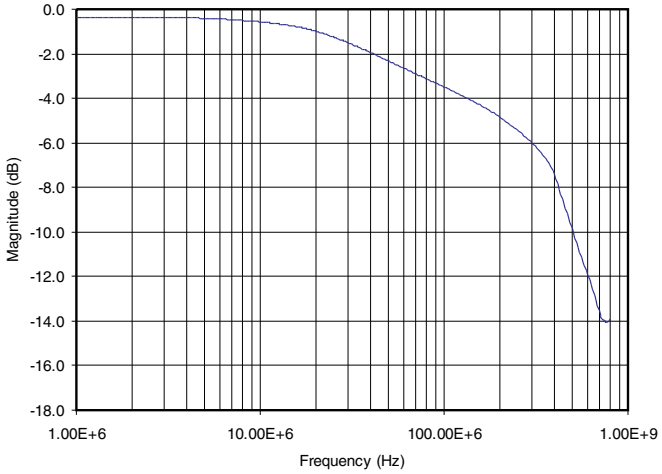


Figure 7. Bandwidth Dual Supply (±5V)

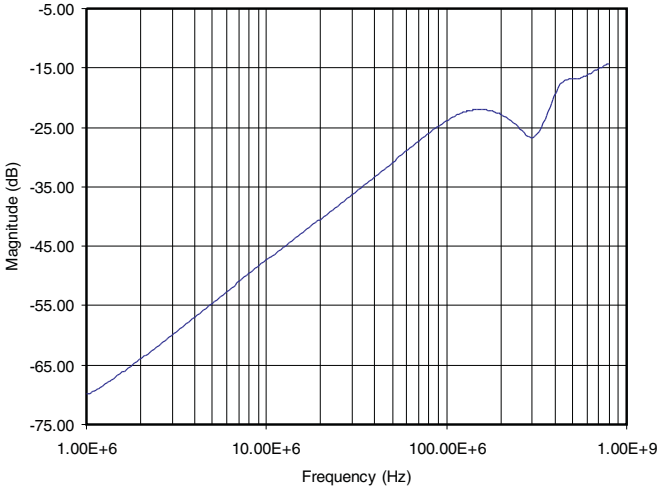


Figure 8. Off Isolation vs Frequency Dual Supply (±5v)

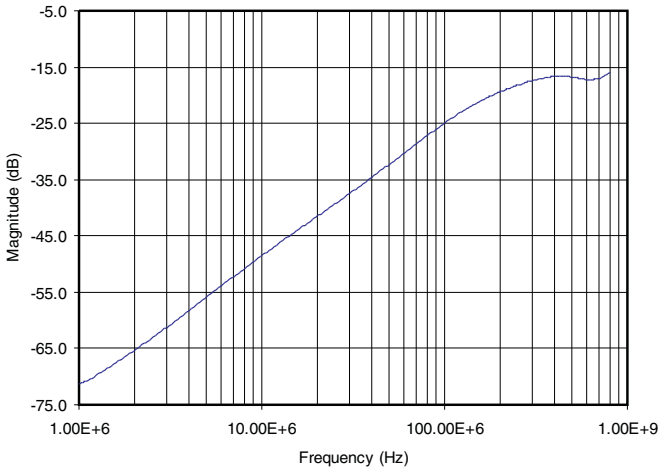


Figure 9. Crosstalk vs Frequency Dual Supply (±5V)

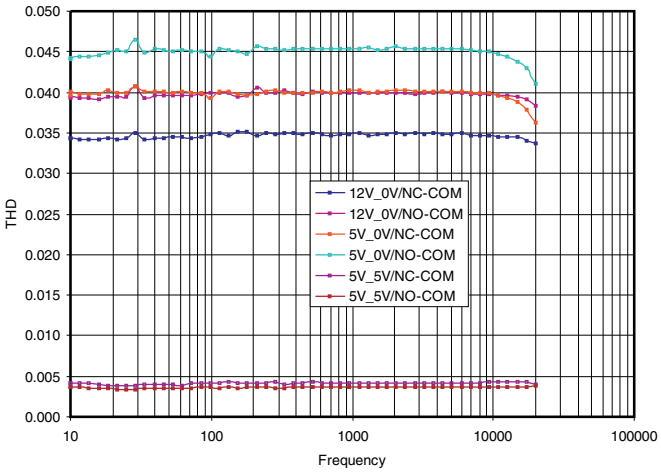


Figure 10. THD+N (%) vs Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

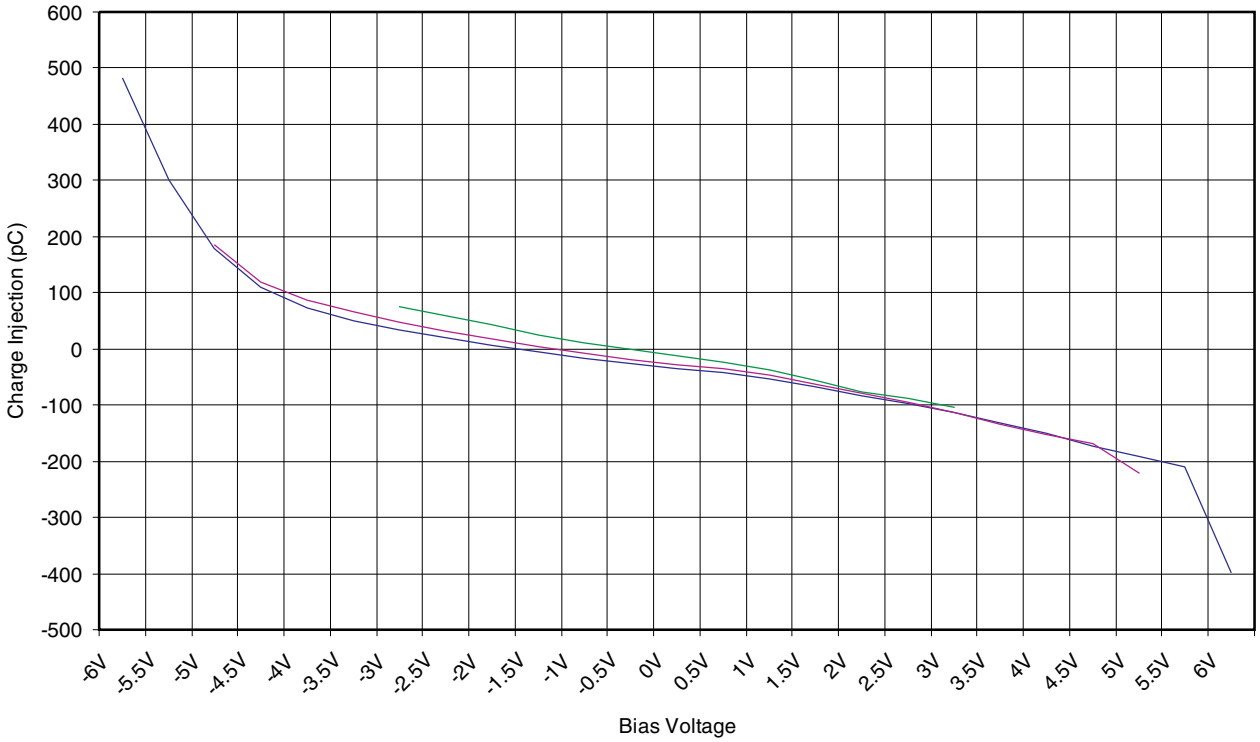


Figure 11. Charge Injection vs Bias Voltage

TEST CIRCUITS

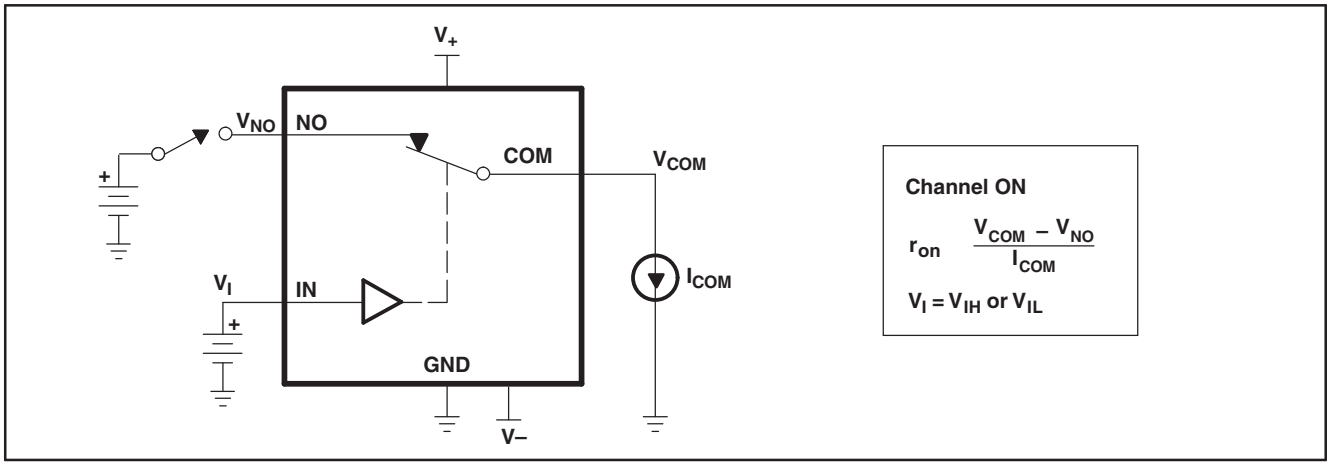


Figure 12. ON-State Resistance

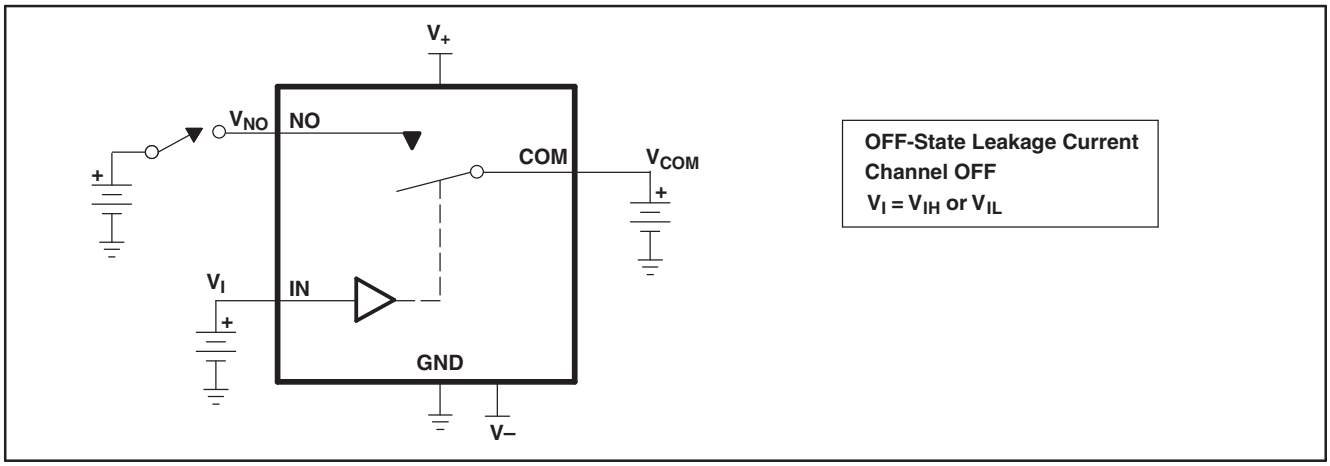


Figure 13. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$)

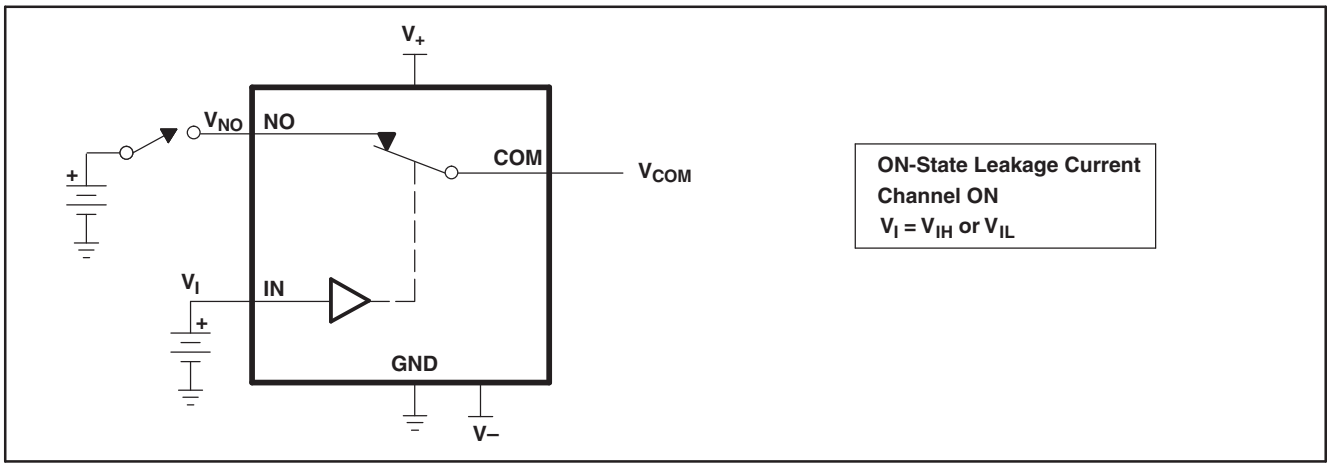


Figure 14. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

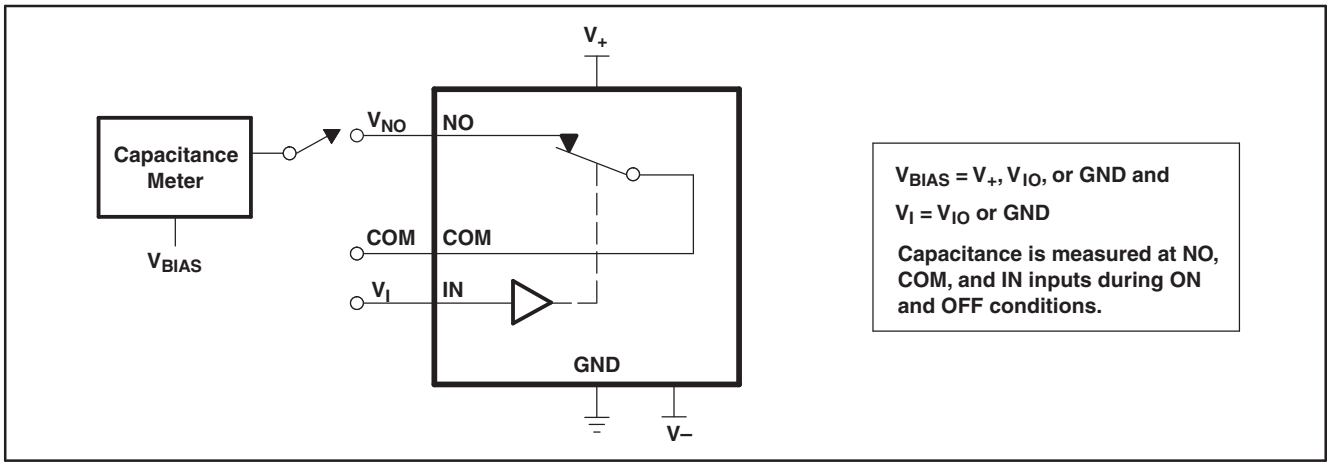
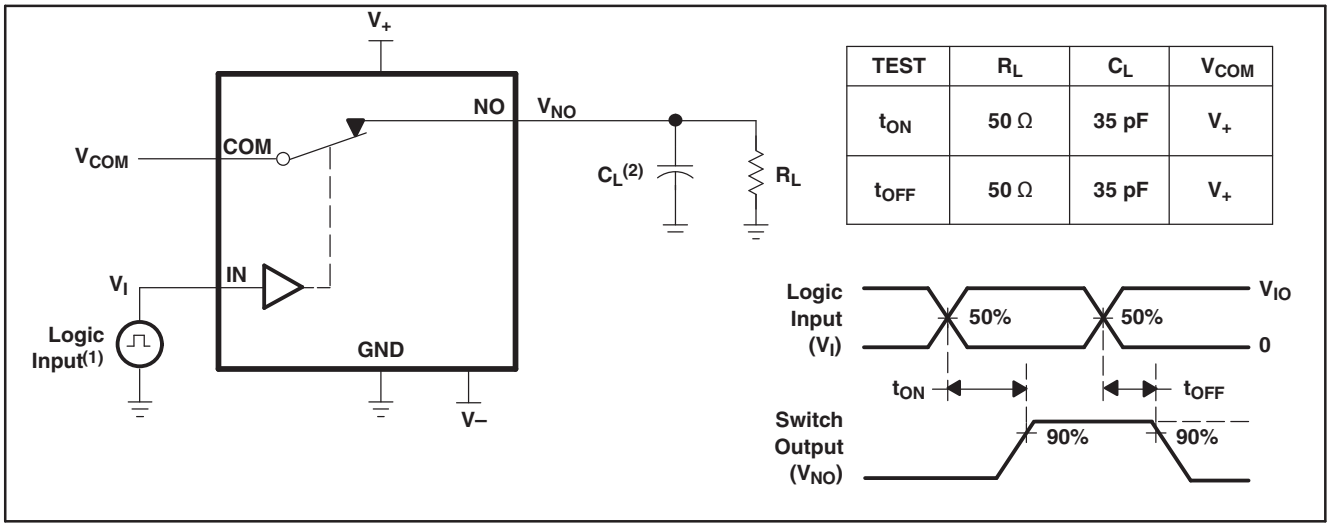


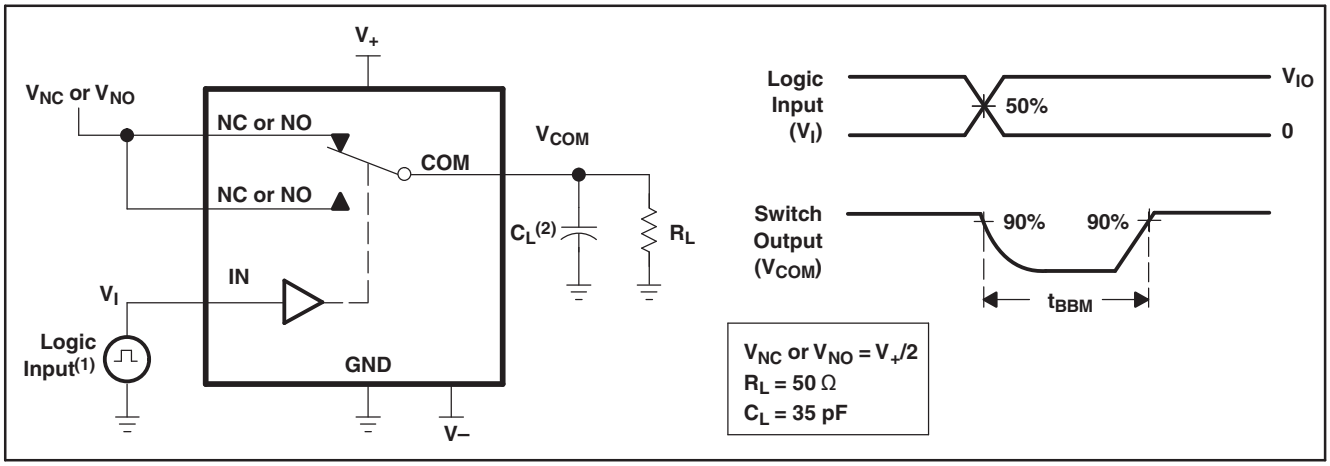
Figure 15. Capacitance ($C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

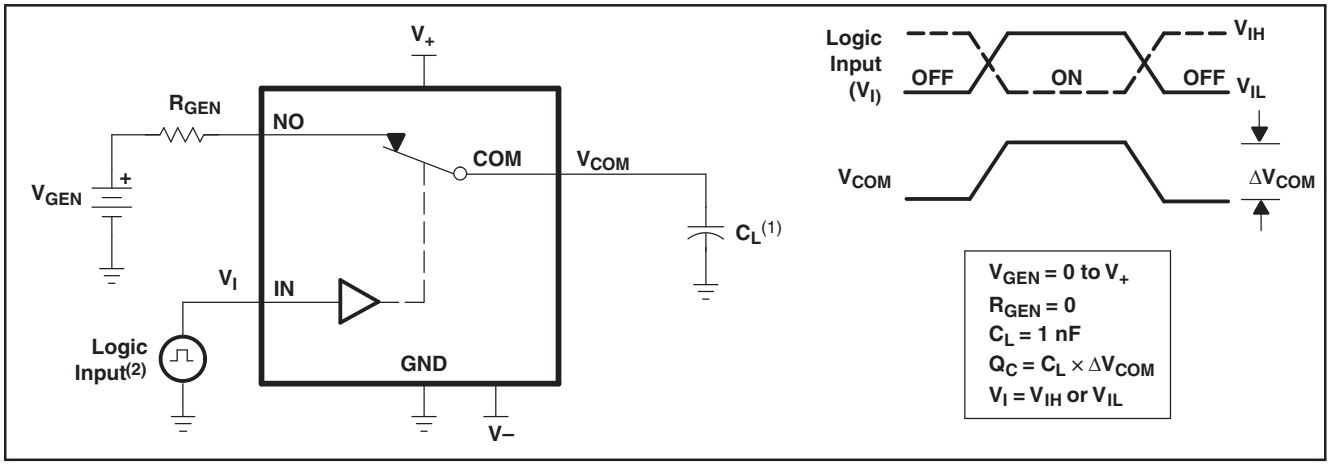
(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 16. Turn-ON (t_{ON}) and Turn-OFF Time (t_{OFF})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 17. Break-Before-Make Time Delay (t_{BBM})



(1) C_L includes probe and jig capacitance.
(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 18. Charge Injection (Q_C)

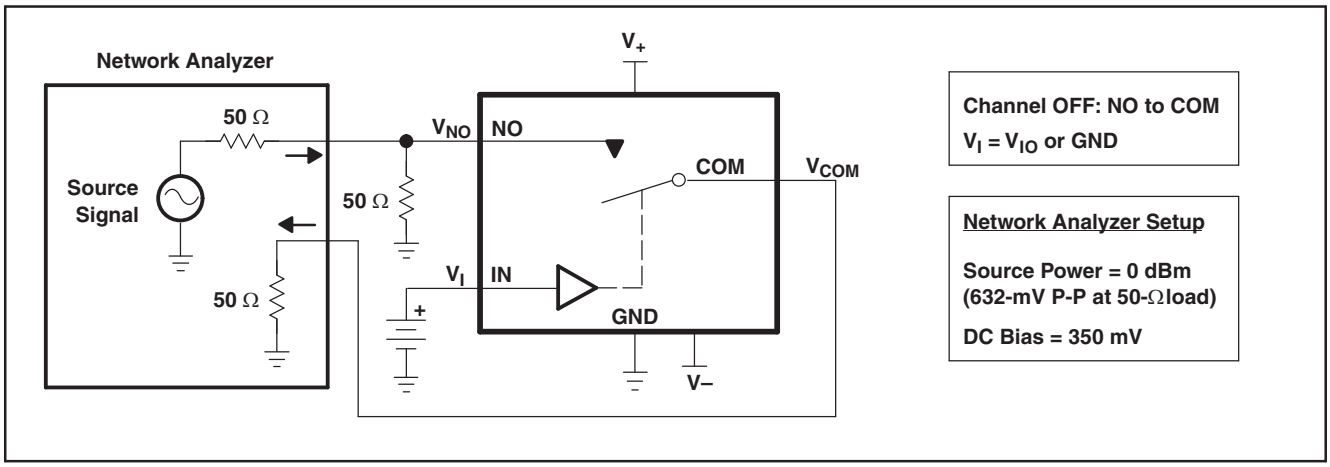


Figure 19. OFF Isolation (O_{ISO})

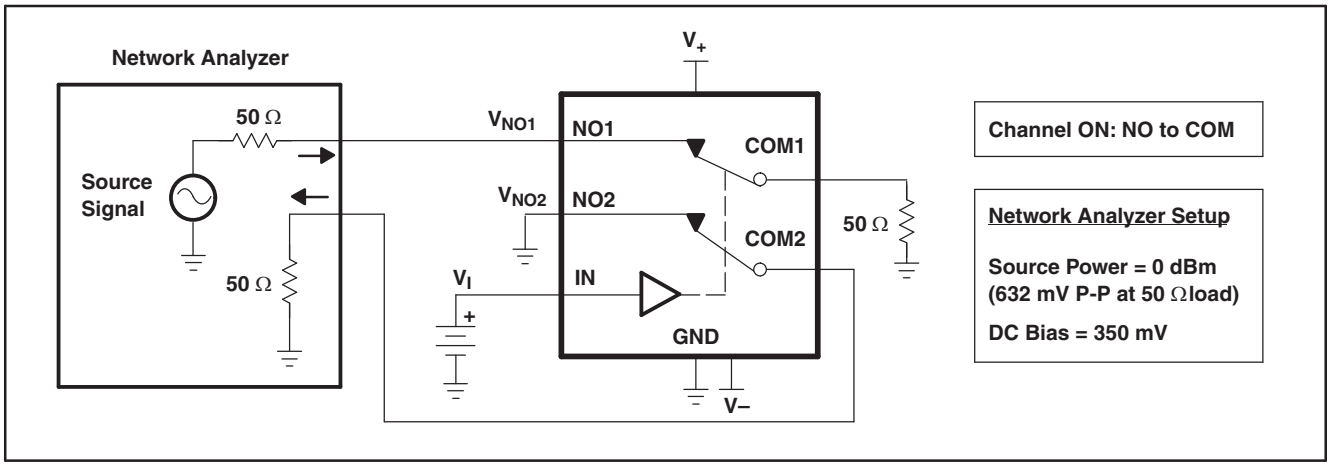


Figure 20. Channel-to-Channel Crosstalk (X_{TALK})

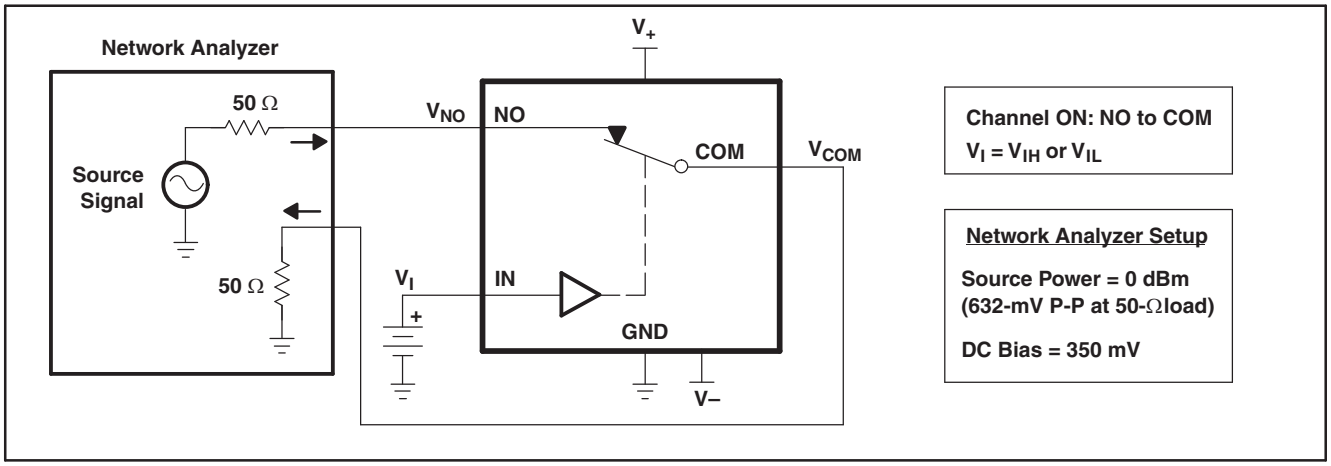
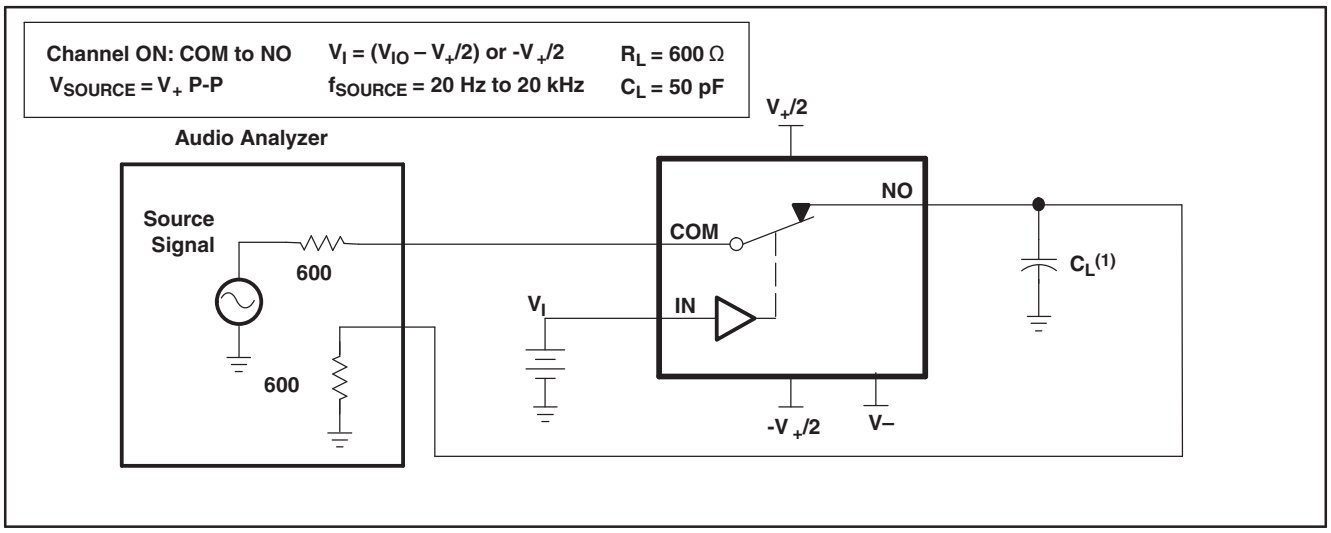


Figure 21. Bandwidth (BW)



(1) C_L includes probe and jig capacitance.

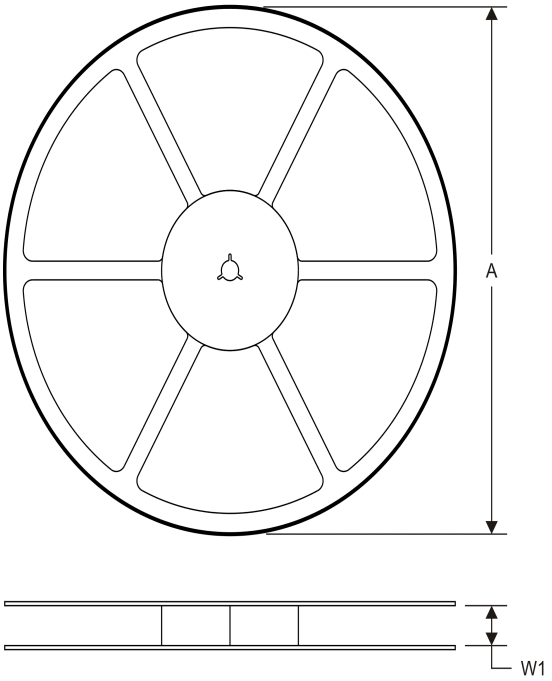
Figure 22. Total Harmonic Distortion

REVISION HISTORY

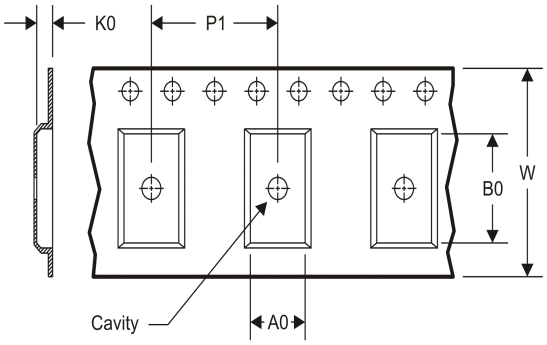
Changes from Revision A (May 2010) to Revision B	Page
• Deleted preview status from DGK and DCN packages.	1

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



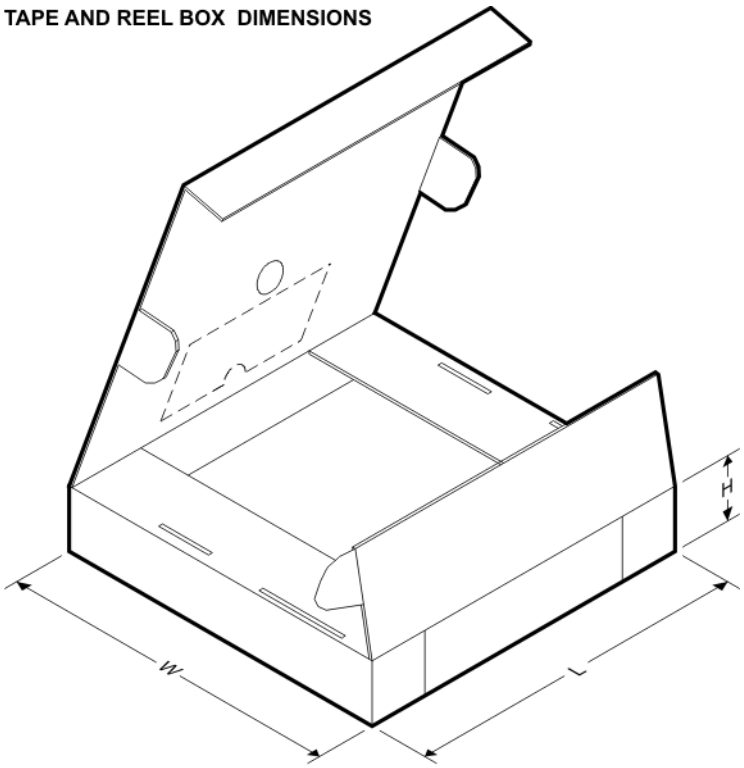
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS12A12511DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS12A12511DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS12A12511DRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

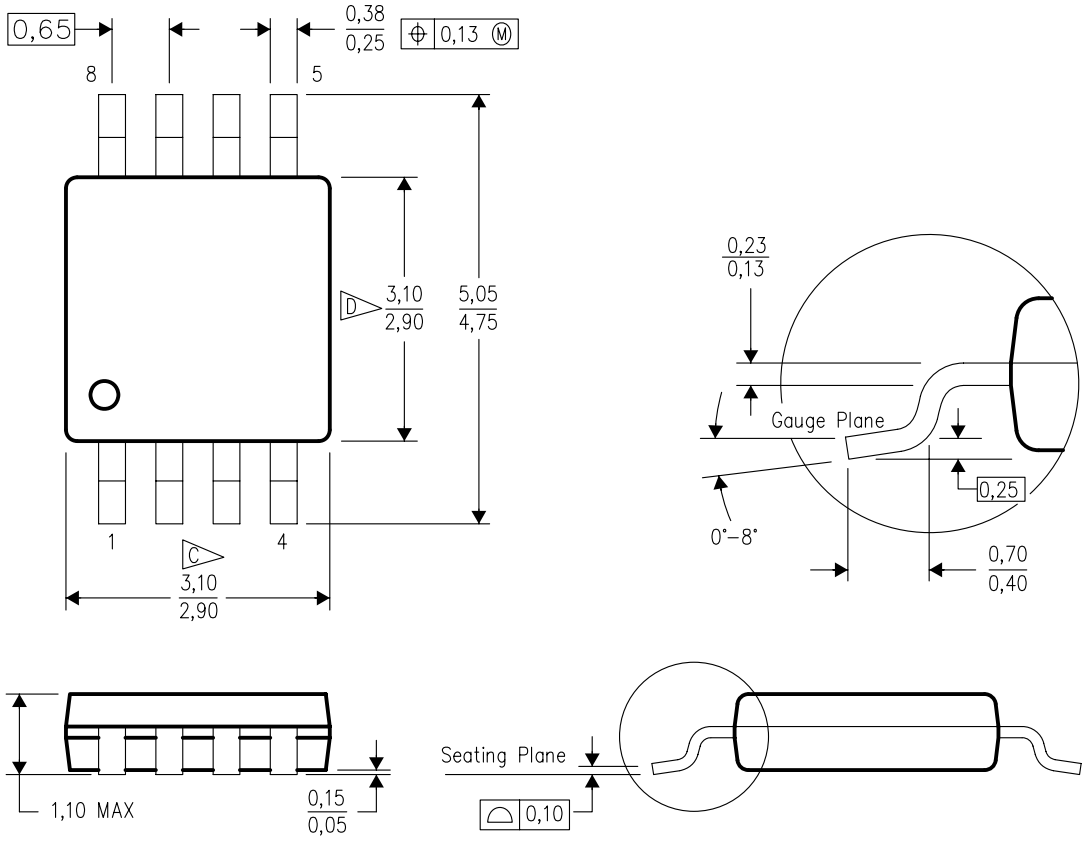
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS12A12511DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TS12A12511DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TS12A12511DRJR	SON	DRJ	8	1000	210.0	185.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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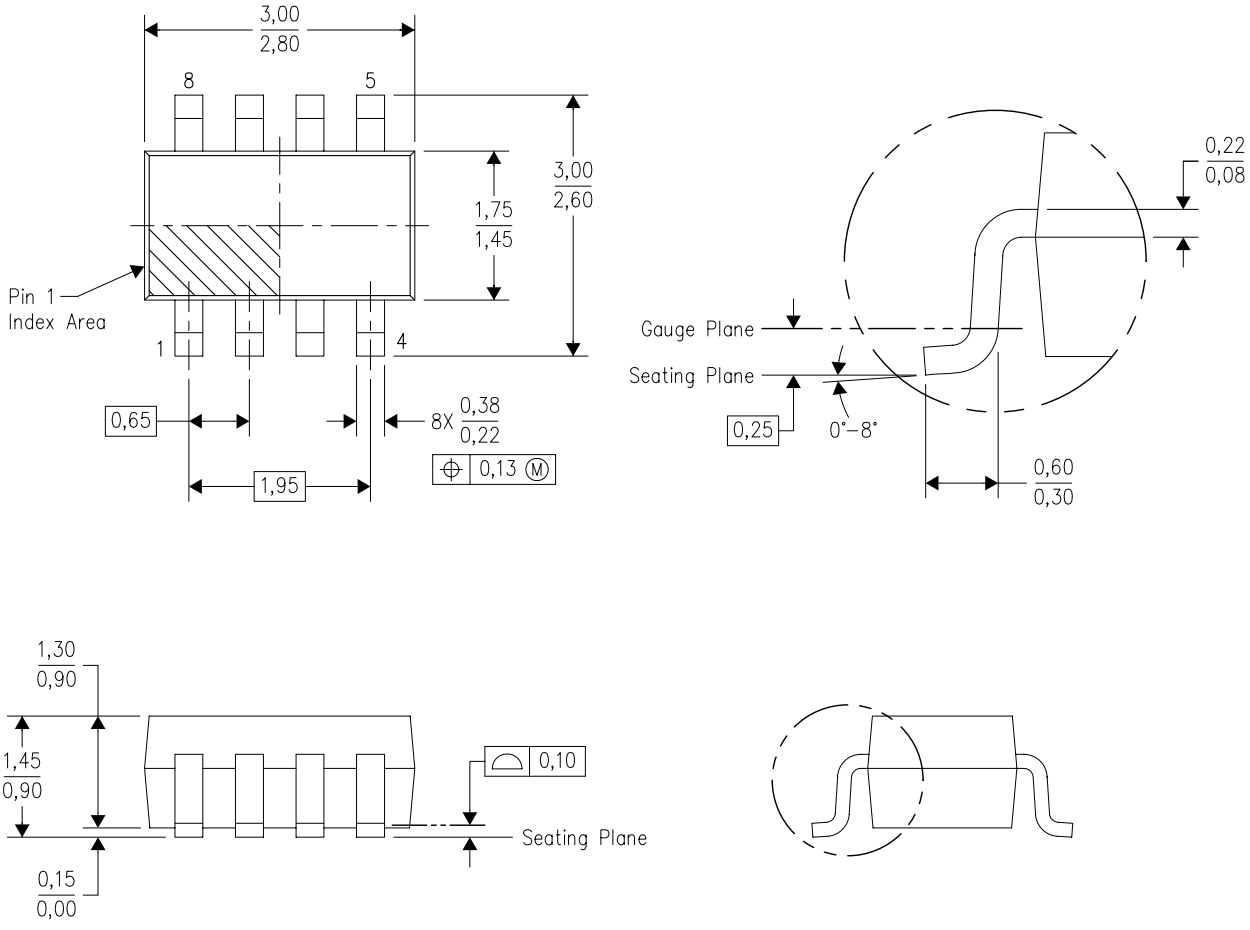
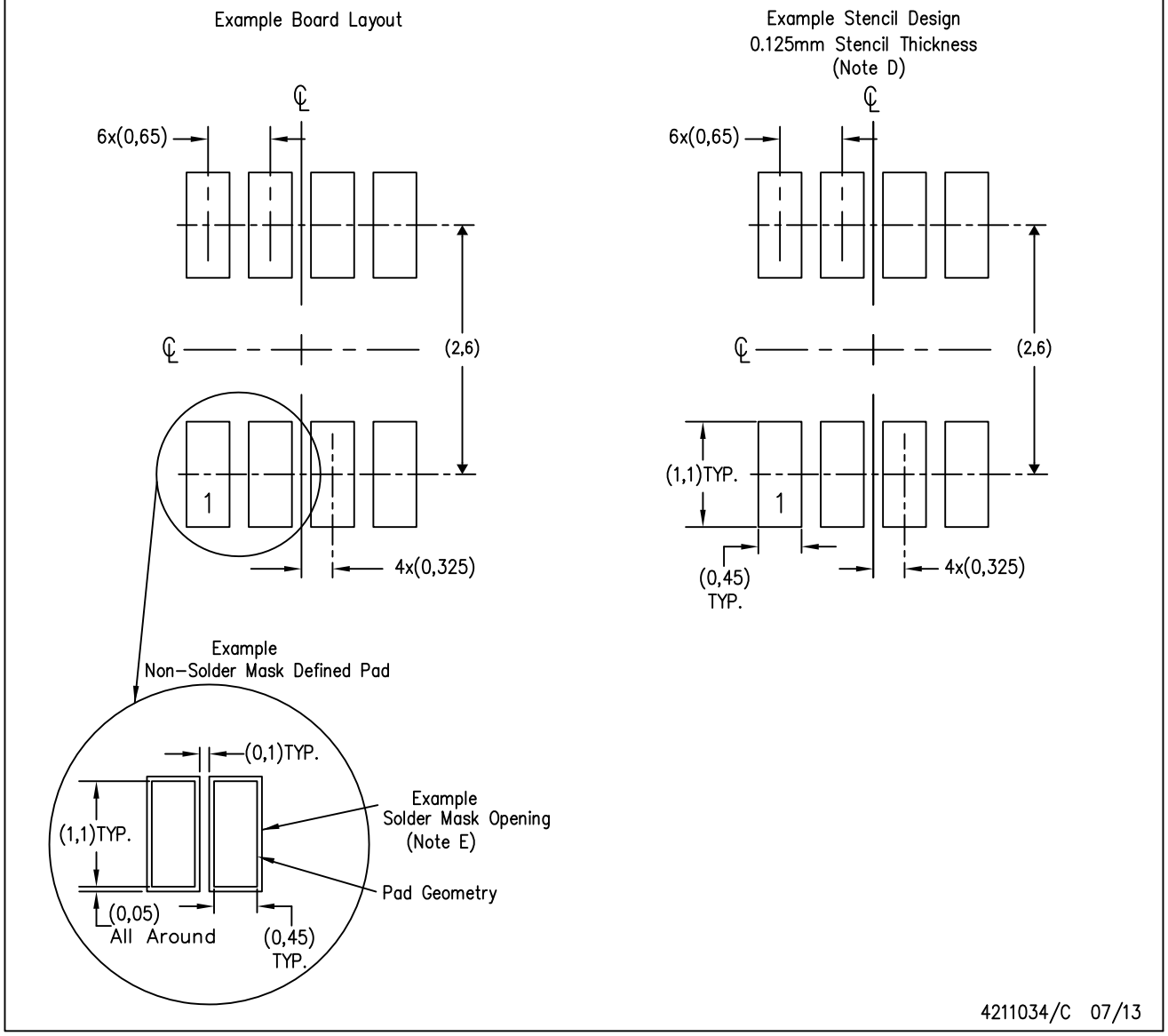
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



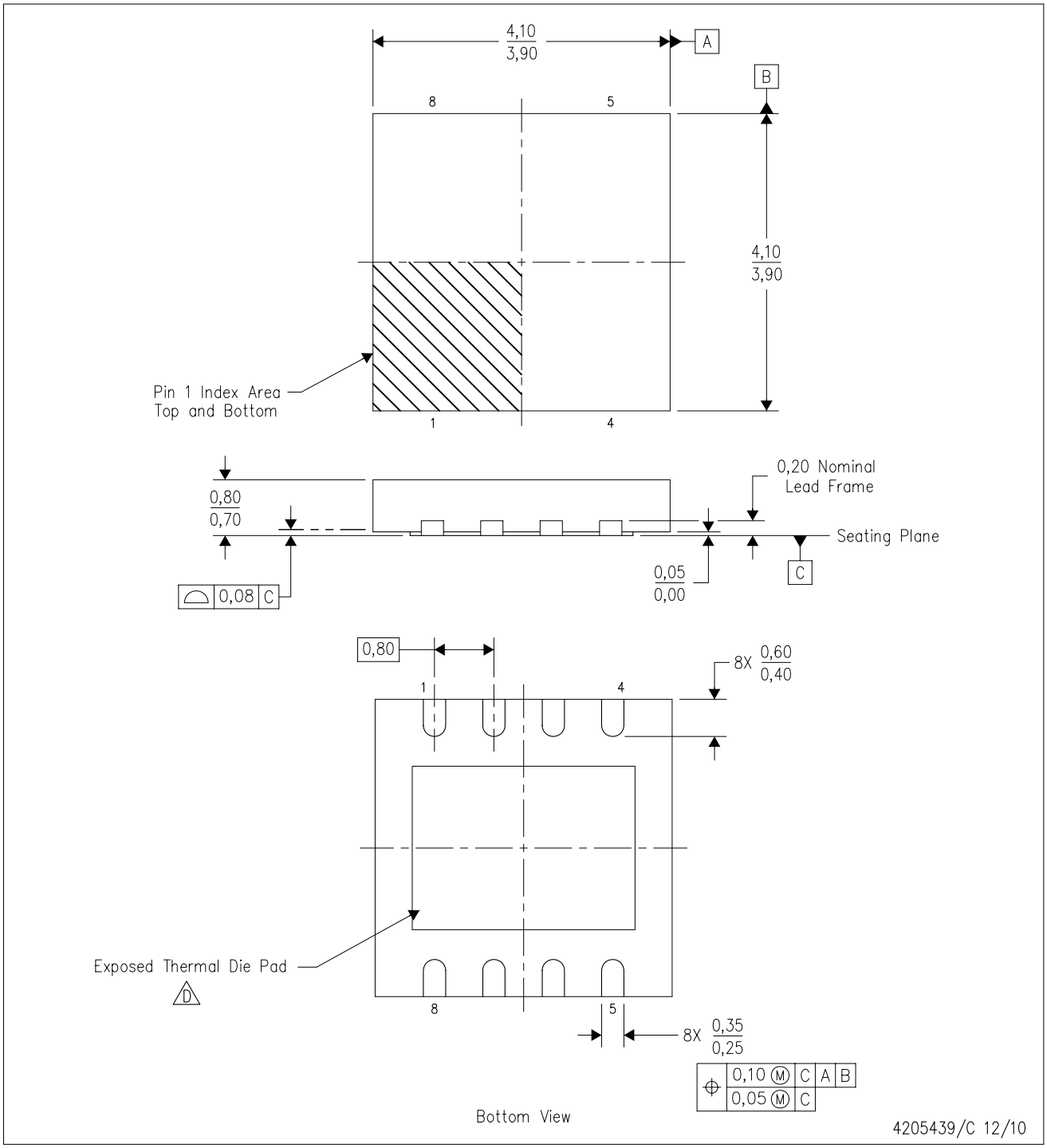
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–229 variation WGGB.

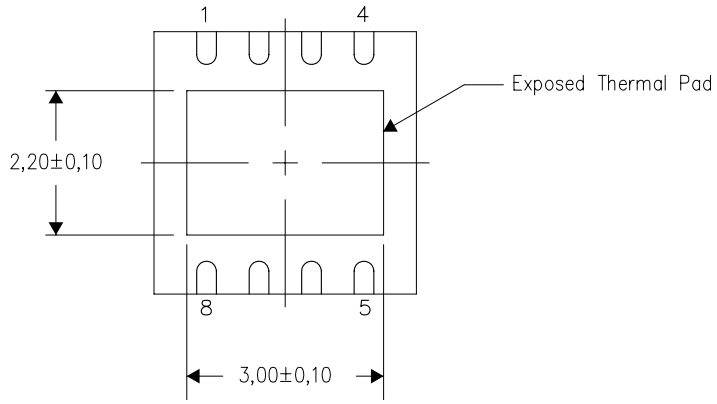
DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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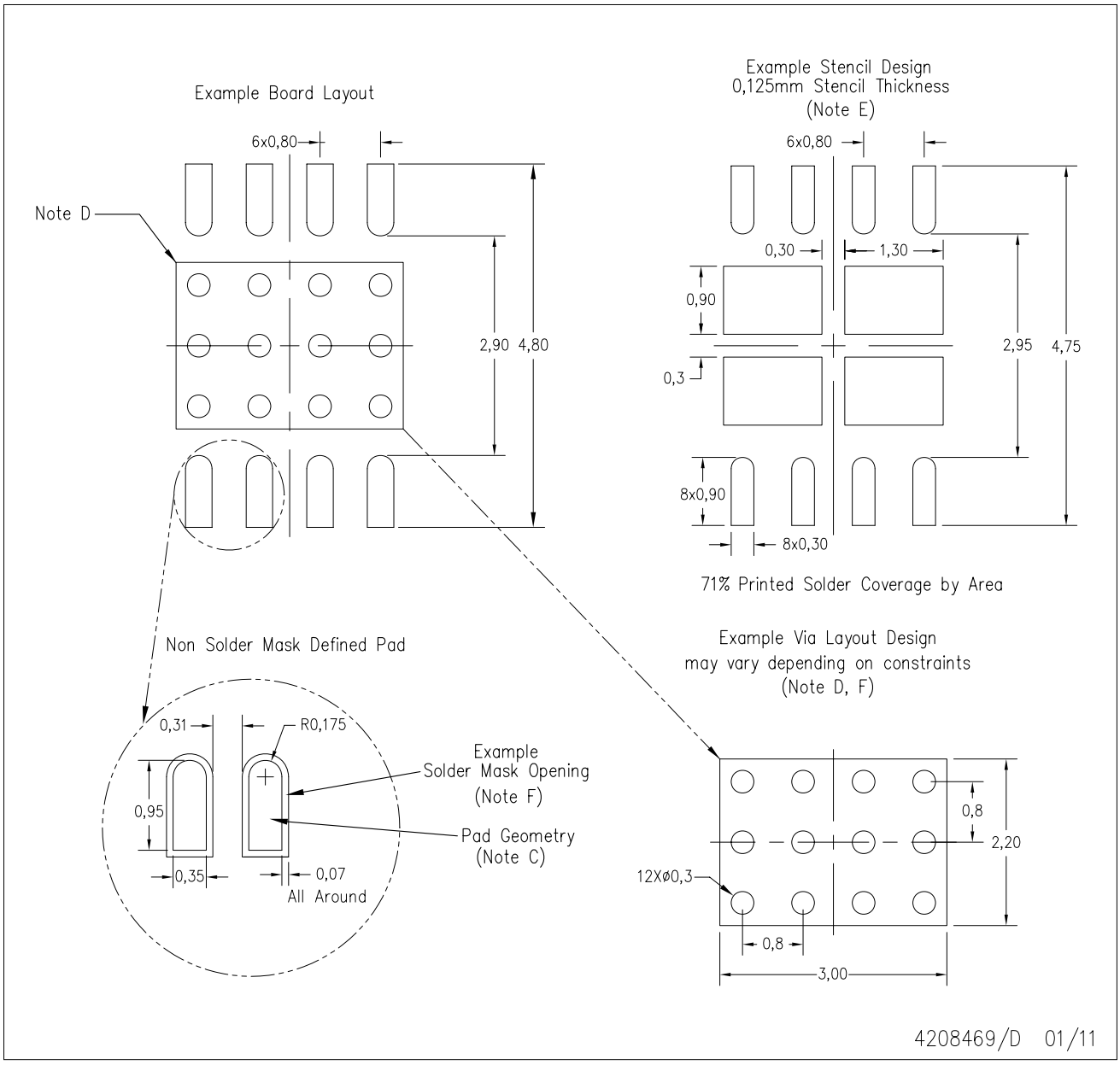
NOTE: All linear dimensions are in millimeters

DRJ (S–PWSON–N8) SMALL PACKAGE OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

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