2 X 2 Crosspoint Switch for Audio Applications

Check for Samples: **TS3A26746E**

## FEATURES

- **Ultra Low R_{ON} for GND Switch (80-mΩ typical)**
- **R_{ON} for MIC Switch <10-Ω**
- **3.0V to 3.6V V+ Operation**
- **Control Input is 1.8-V Logic Compatible**
- **6-bump, 0.5mm pitch CSP Package (1.45mm × 0.95mm × 0.5mm)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **500-V Charged-Device Model (C101)**
- **ESD Performance (SLEEVE, RING2)**
  - **±8-kV Contact Discharge (IEC 61000-4-2)**

APPLICATIONS

- **Cellular phones**
- **PDAs**
- **Portable Instrumentation**
- **Digital Still Cameras**
- **Portable Navigation Devices**

PINOUT
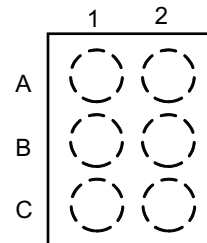
DESCRIPTION

The TS3A26746E is a 2 × 2 cross-point switch that is used to interchange the Ground and MIC connections on a headphone connector. The Ground switch has an ultra low R_{ON} of <0.1Ω to minimize voltage drop across it, preventing undesired increases in headphone ground reference voltage. The switch state is controlled via the SEL input. When SEL=High, GND is connected to RING2 and MIC is connected to SLEEVE. When SEL=Low, GND is connected to SLEEVE and MIC is connected to RING2. An internal 100k pull-up resistor on the SEL input sets the default state of the switch.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
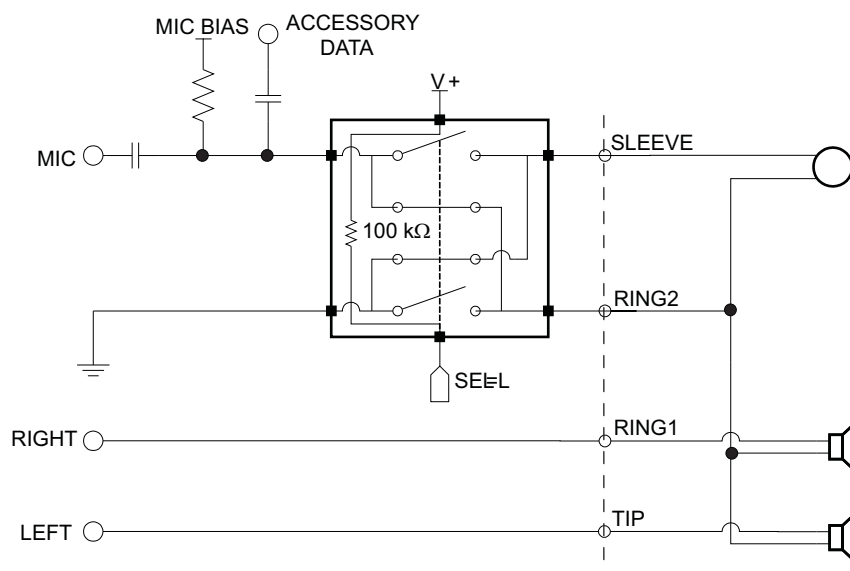
⚠️ These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.
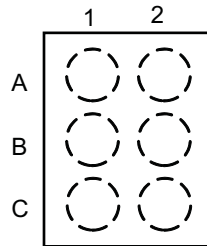
TYPICAL APPLICATION BLOCK DIAGRAM
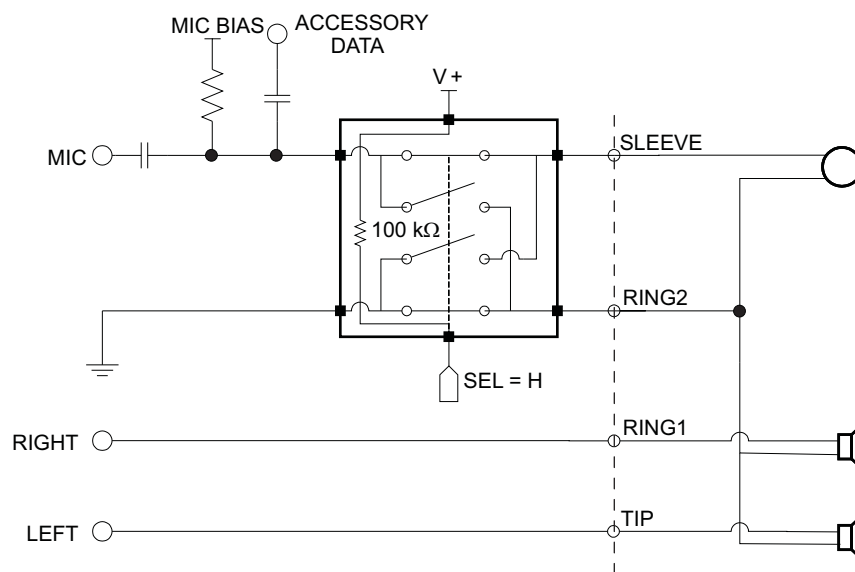
Figure 1. Standard Headphone Configuration (SEL=H)

Figure 2. Alternate Headphone Configuration (SEL=L)

PINOUT

TERMINAL ASSIGNMENTS

	1	2
A	SEL	V+
B	MIC	SLEEVE
C	GND	RING2

PIN FUNCTIONS

BALL #	PIN NAME	PIN TYPE	DESCRIPTION
A1	SEL	Input	Control Input
A2	V+	Power	Supply Voltage
B1	MIC	I/O	MIC
B2	SLEEVE	I/O	Sleeve Connection on Headphone Jack
C1	GND	Ground	Ground
C2	RING2	I/O	2nd Ring Connection on Headphone Jack

Table 1. FUNCTION TABLE

SEL	MIC to SLEEVE, GND to RING2	MIC to RING2, GND to SLEEVE
L	OFF	ON
H	ON	OFF

ABSOLUTE MAXIMUM RATINGS[(1)(2)]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range[(3)]		−0.3	4.0	V
V_{MIC} V_{SLEEVE} V_{RING2}	Analog voltage range[(3)]		−0.3	4.0	V
I_K	Analog port diode current	V_{MIC}, V_{SLEEVE}, V_{RING2} < 0 V	−50		mA
V_I	Digital input voltage range		−0.3	4.0	V
I_{IK}	Digital input clamp current[(3)]	V_I < 0 V	−50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		−100		mA
θ_{JA}	Package thermal impedance[(4)]	YZP package		102	°C/W
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY[(1)]

V_+ = 3 V to 3.6 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
MIC SWITCH									
V_{MIC}, V_{SLEEVE}, V_{RING2}	Analog signal range					0		V+	V
r_{on}	ON-state resistance	$0 \leq V_{SLEEVE}$ or $V_{RING2} \leq V_+$, $I_{MIC} = -32$ mA	Switch ON	25°C	3 V		5	8	Ω
				Full				10	
$r_{on(flat)}$	ON-state resistance flatness	$0 \leq V_{SLEEVE}$ or $V_{RING2} \leq V_+$, $I_{MIC} = -32$ mA	Switch ON	25°C	3 V		1	2.3	Ω
				Full				2.5	
$I_{SLEEVE(OFF)}$, $I_{RING2(OFF)}$	SLEEVE, RING2 OFF leakage current	V_{SLEEVE} or $V_{RING2} = 1$ V, $V_{MIC} = 3$ V, or V_{SLEEVE} or $V_{RING2} = 3$ V, $V_{MIC} = 1$ V	Switch OFF	25°C	3.6 V	−0.5	0.05	0.5	µA
				Full		−2		2	
$I_{MIC(OFF)}$	MIC OFF leakage current	V_{SLEEVE} or $V_{RING2} = 3$ V, $V_{MIC} = 1$ V, or V_{SLEEVE} or $V_{RING2} = 1$ V, $V_{MIC} = 3$ V	Switch OFF	25°C	3.6 V	−1	0.1	1	µA
				Full		−2		2	
$I_{SLEEVE(ON)}$, $I_{RING2(ON)}$	SLEEVE, RING2 ON leakage current	V_{SLEEVE} or $V_{RING2} = 1$ V, V_{MIC} = Open, or V_{SLEEVE} or $V_{RING2} = 3$ V, V_{MIC} = Open	Switch ON	25°C	3.6 V	−2	0.5	2	µA
				Full		−2		2	
$I_{MIC(ON)}$	MIC ON leakage current	V_{SLEEVE} or V_{RING2} = Open V, $V_{MIC} = 1$ V, or V_{SLEEVE} or V_{RING2} = Open, $V_{MIC} = 3$ V	Switch ON	25°C	3.6 V	−2	0.5	2	µA
				Full		−2		2	
GND SWITCH									
r_{on}	ON-state resistance	I_{SLEEVE} or $I_{RING2} = +32$ mA, $V_{GND} = 0$ V, $I_{GND} = -32$ mA	Switch ON	25°C	3 V		0.08	0.09	Ω
				Full				0.11	
$I_{SLEEVE(OFF)}$, $I_{RING2(OFF)}$	SLEEVE, RING2 OFF leakage current	V_{SLEEVE} or $V_{RING2} = 3$V and $V_{GND} = 0$ V	Switch OFF	25°C	3.6 V	−0.5	0.05	0.5	µA
				Full		−1		1	
$I_{SLEEVE(PWROFF)}$, $I_{RING2(PWROFF))}$		V_{SLEEVE} or $V_{RING2} = 0$ to 3.6 V and V_{GND} = 0 V	Switch OFF	25°C	0 V	−1	0.5	1	µA
				Full		−10		10	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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Product Folder Links :TS3A26746E

ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY[1] (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
DIGITAL CONTROL INPUTS (SEL)									
V_{IH}	Input logic high			Full	3.6 V	1.2		3.6	V
V_{IL}	Input logic low			Full	3.6 V	0		0.4	V
I_{IH}	Input logic high leakage current	$V_I = V_+$		25°C	3.6 V	−1	0.05	1	µA
				Full		−2		2	
I_{IL}	Input logic low leakage current	$V_I = 0$ V		25°C	3.6 V	−38	−36	−34	µA
				Full		−45		−30	
DYNAMIC									
t_{ON}	Turn-on time	$V_{MIC} = V_+$, $R_L = 50$ Ω	$C_L = 35$ pF	25°C	3.3 V		150	200	ns
				Full	3 V to 3.6 V			250	
t_{OFF}	Turn-off time	$V_{MIC} = V_+$, $R_L = 50$ Ω	$C_L = 35$ pF	25°C	3.3 V		5	10	ns
				Full	3 V to 3.6 V			15	
t_{BBM}	Break-before-make time	$V_{MIC} = V_+$		25°C	3.3 V	70		330	ns
				Full	3 V to 3.6 V			330	
C_{MIC}	MIC capacitance	SEL=High		25°C	3.3 V		100	140	pF
		SEL=Low		25°C	3.3 V		100	140	pF
C_{SLEEVE}	SLEEVE / RING2 capacitance	SEL=High		25°C	3.3 V		100	140	pF
		SEL=Low		25°C	3.3 V		100	140	pF
C_I	Digital input capacitance	$V_I = V_+$ or 0 V		25°C	3.3 V		4.0		pF
THD	Total harmonic distortion	$R_L = 1$k Ω, V = 30 mVPP	f = 20 Hz to 20 kHz	25°C	3.3 V		0.01%		
SUPPLY									
V+	Power Supply Voltage					3.0	3.3	3.6	V
I_+	Positive supply current	$V_I = V_+$		25°C	3.6 V		0.01	1	µA
				Full				5	
		$V_I = 0$ V		25°C			40	41	µA
				Full				50	

OPERATIONAL CHARACTERISTICS
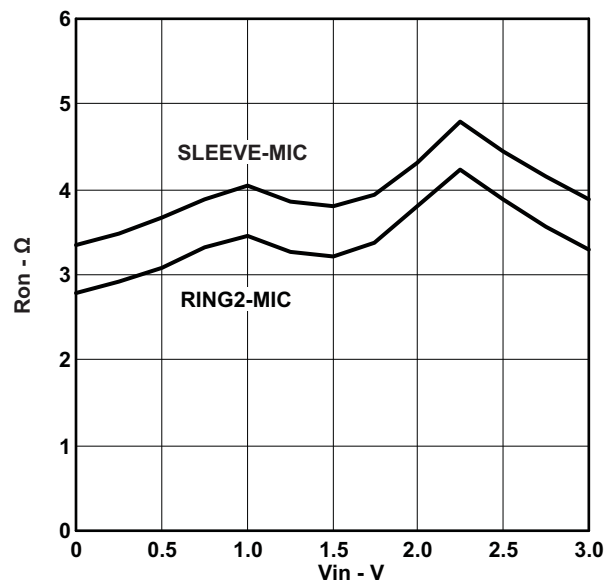
Figure 3. R_{ON} vs V_{IN} (MIC Switch)

PARAMETER MEASRUMENT INFORMATION

TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V+
t_{OFF}	50 Ω	35 pF	V+
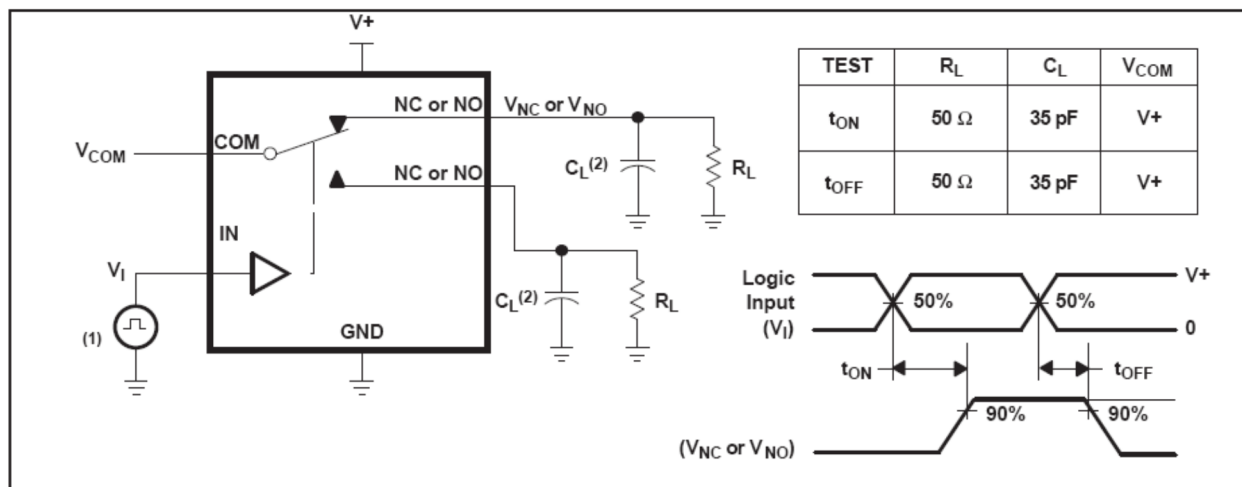
A.   All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 4. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

Product Folder Links : *TS3A26746E*

PARAMETER MEASRUMENT INFORMATION (continued)
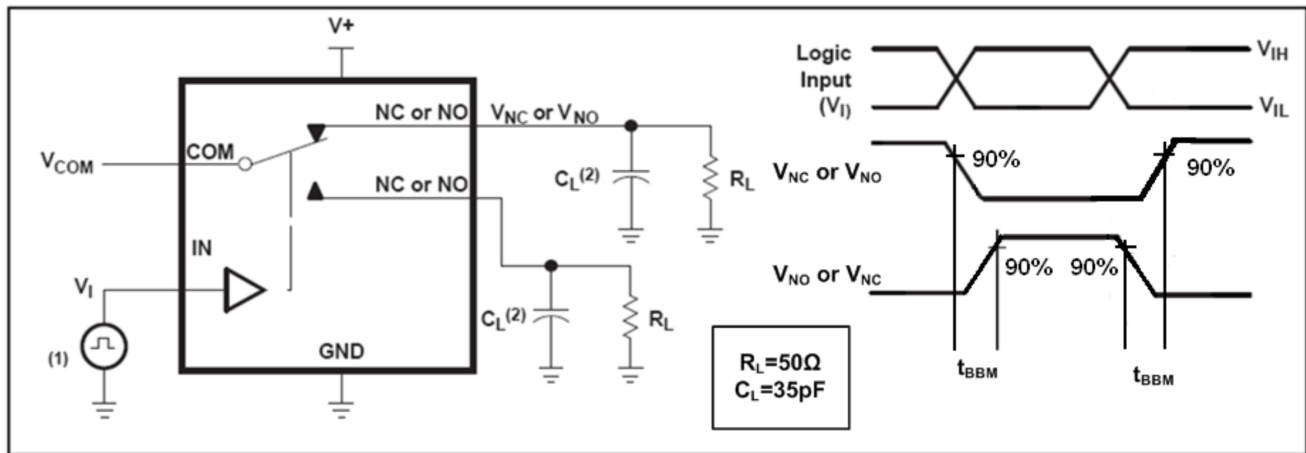
A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 5. Break-Before-Make Time (t_{BBM})

REVISION HISTORY

Changes from Revision B (November 2011) to Revision C   **Page**

- Replaced 1 page preview with full document. 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A26746EYZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
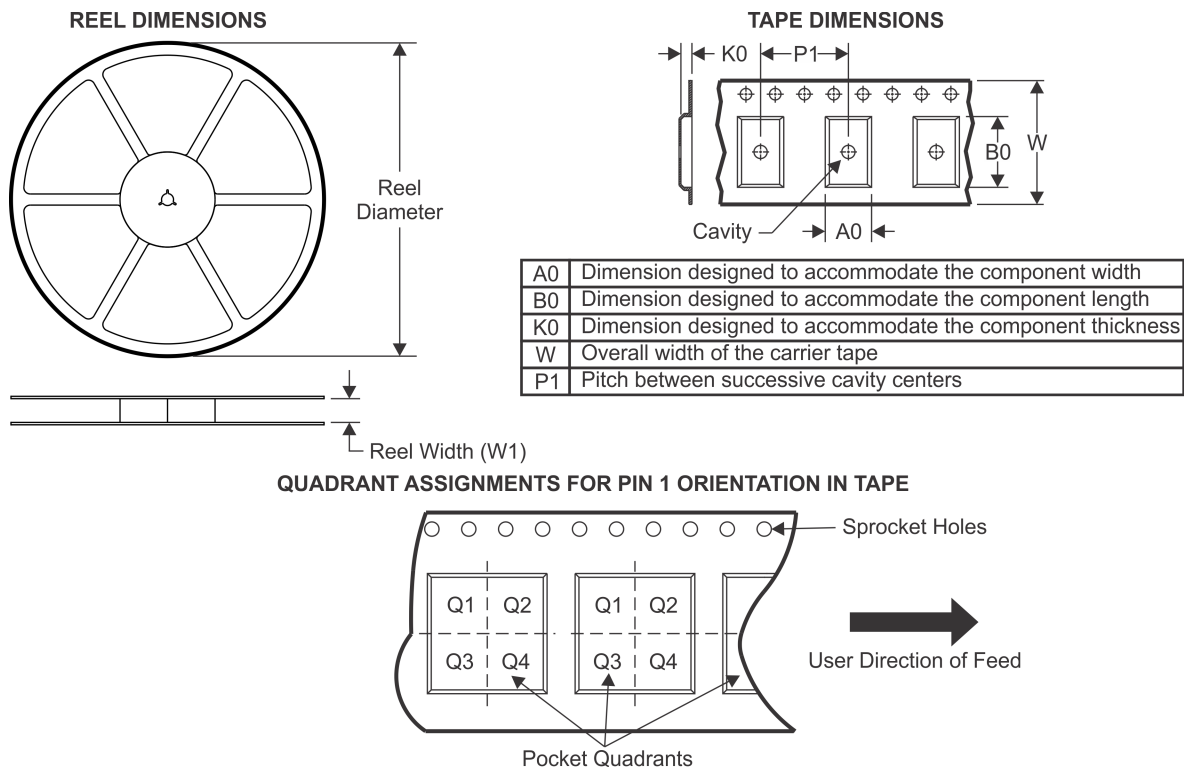
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A26746EYZPR	DSBGA	YZP	6	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A26746EYZPR	DSBGA	YZP	6	3000	182.0	182.0	17.0

YZP (R−XBGA−N6)   DIE−SIZE BALL GRID ARRAY

Ball A1 Index Area

Bottom View

6X ∅ 0,25 / 0,21

⊕ ∅ 0,015 Ⓜ C A B

0,50 Max

0,19 / 0,15

0,05 C

Seating Plane

C

D: Max = 1.338 mm, Min =1.277 mm

E: Max = 0.838 mm, Min =0.777 mm

4204741−4/M   11/13
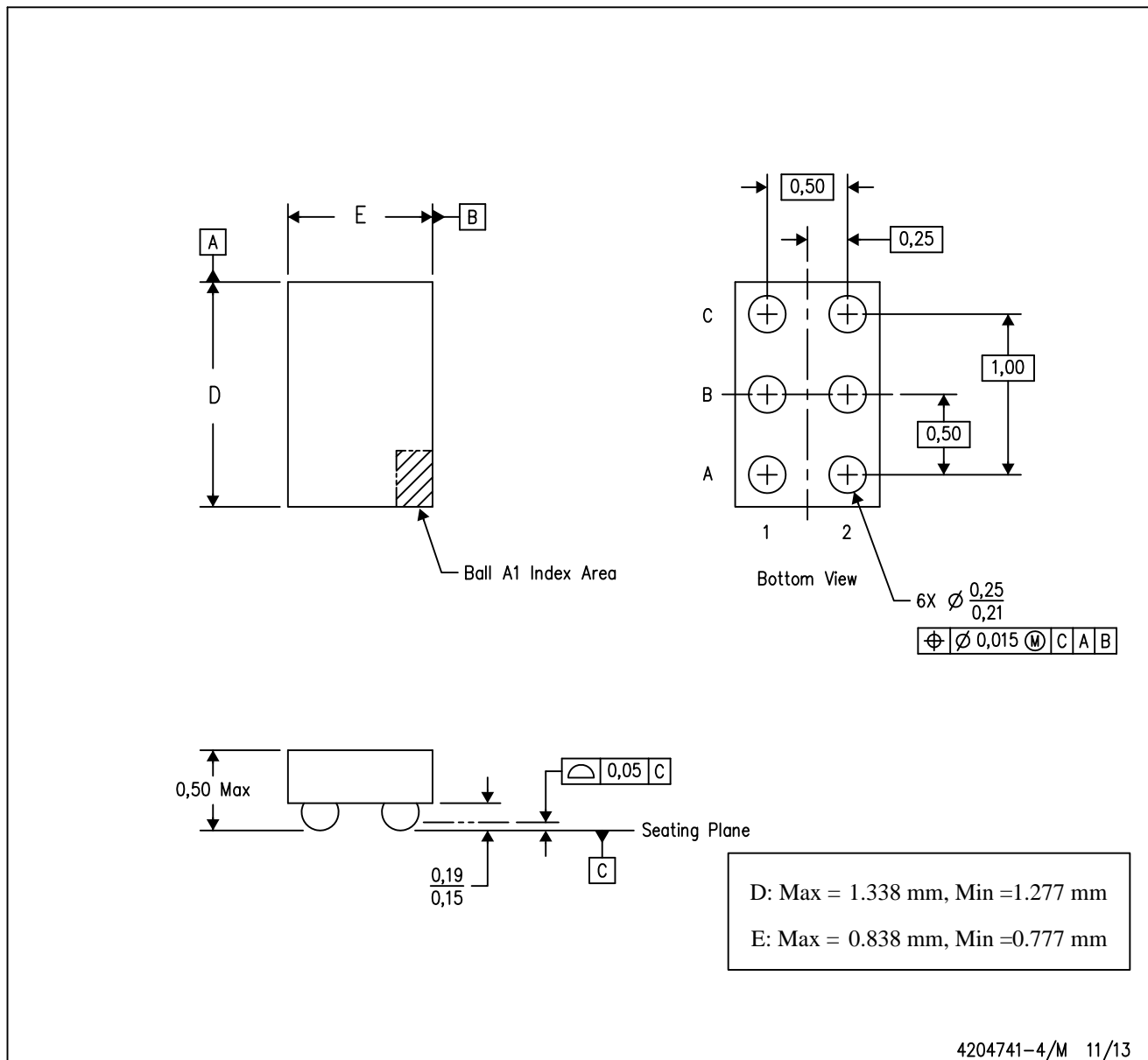
NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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