12-Channel 1:2 MUX/DEMUX with1.8V Compatible Control and Power-Down Mode

Check for Samples: TS3DV642

FEATURES

- **Switch Type: 2:1 or 1:2**
- **Differential Bandwidth (–3dB)**
  - **Port A – 6.9 GHz Typical**
  - **Port B – 7.5 GHz Typical**
- **Ron**
  - **Port A – 6.5 Ω Typical**
  - **Port B – 8.2 Ω Typical**
- **Con at 1GHz: 0.5 pF Typ**
- **V_{CC} Range, 2.6 V–4.5 V**
- **I/O Voltage range, 0 V–5 V**
- **Special Features**
  - **I_{OFF} Protection Prevents Current Leakage in Powered Down State (V_{CC} = 0 V)**
- **ESD Performance**
  - **2 kV Human Body Model (A114B, Class II)**
  - **1 kV Charged Device Model (C101)**
- **42-pin QFN Package (9 x 3.5 mm, 0.5 mm Pitch)**

APPLICATIONS

- **HDMI 1.4b with support for 4k2k up to 30 Hz**
- **DVI 1.0 Signal Switching**
- **DisplayPort 1.2a Signal Switching**
- **General Purpose TMDS Signal Switching**
- **General Purpose LVDS Signal Switching**
- **General Purpose High Speed Signal Switching**

DESCRIPTION

The TS3DV642 is a 12 channels 1:2 or 2:1 bi-directional multiplexer/demultiplexer. The TS3DV642 operates from a 2.6 to 4.5 V supply, making it suitable for battery-powered applications. It offers low and flat ON-state resistance as well as low I/O capacitance which allow it to achieve a typical bandwidth of up to 7.5 GHz. The device provides the high bandwidth necessary for HDMI and DisplayPort applications.

The TS3DV642 offers a power-down mode, in which all channels become high-Z and the device operates with minimal power.

TYPICAL APPLICATION DIAGRAM

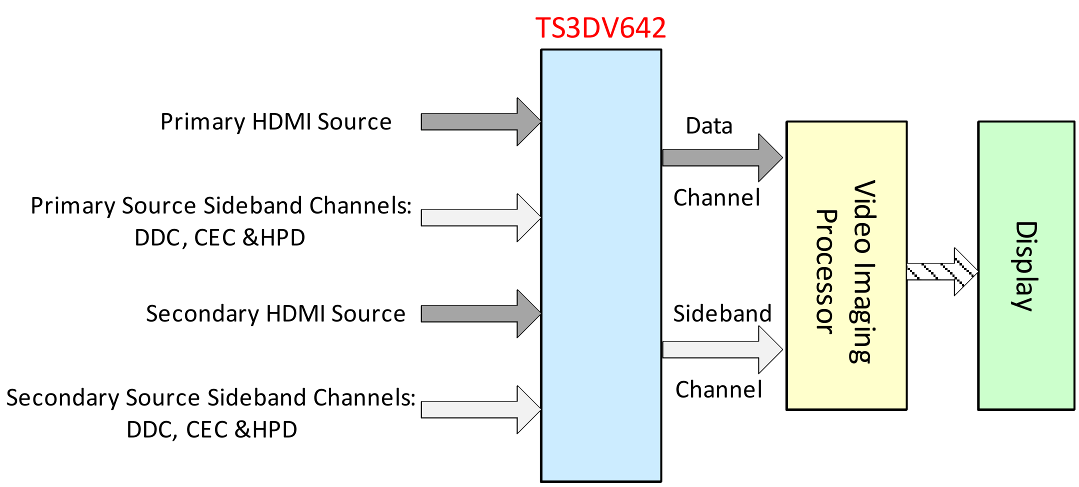


Figure 1. Typical 2:1 HDMI Demux Application

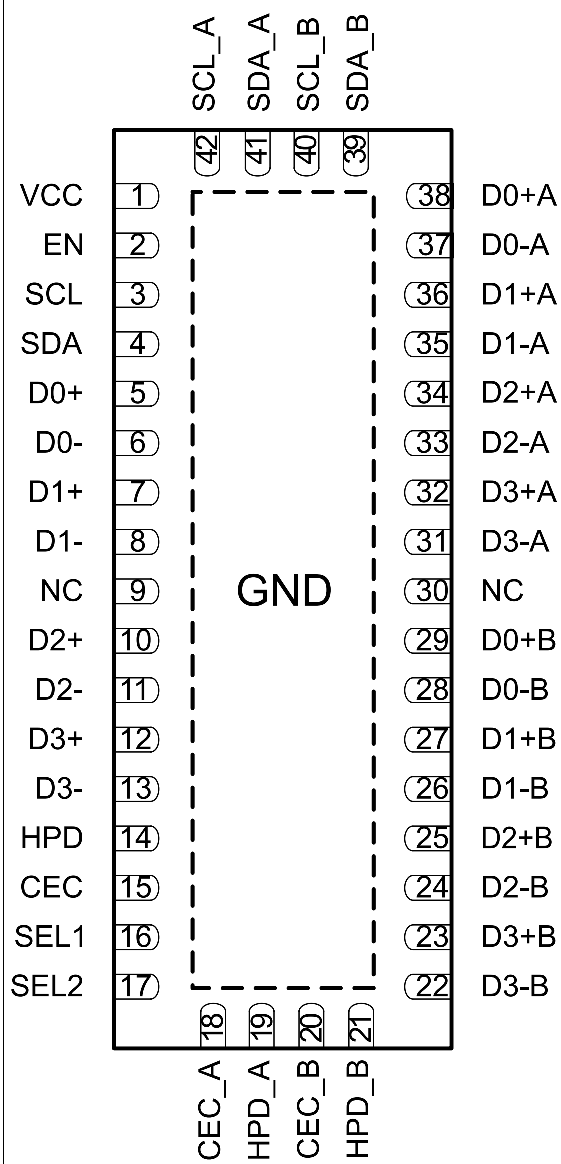
ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN DESCRIPTION



PIN		I/O Type	DESCRIPTION
NAME	NUMBER		
VCC	1	Power	Supply Voltage
GND	PowerPad	GND	Ground
SEL1	16	I	Select Input 1
SEL2	17	I	Select Input 2
EN	2	I	Output Enable
D0+A	38	I/O	Port A, Lane 0, +ve signal
D0–A	37	I/O	Port A, Lane 0, –ve signal
D1+A	36	I/O	Port A, Lane 1, +ve signal
D1-A	35	I/O	Port A, Lane 1, –ve signal
D2+A	34	I/O	Port A, Lane 2, +ve signal
D2–A	33	I/O	Port A, Lane 2,–ve signal
D3+A	32	I/O	Port A, Lane 3, +ve signal
D3–A	31	I/O	Port A, Lane 3, –ve signal
SCL_A	42	I/O	Port A, DDC Clock
SDA_A	41	I/O	Port A, DDC Data
HPD_A	19	I/O	Port A, Hot Plug Detects
CEC_A	18	I/O	Port A, Consumer Electronics Control
D0+B	29	I/O	Port B, Lane 0, +ve signal
D0–B	28	I/O	Port B, Lane 0, –ve signal
D1+B	27	I/O	Port B, Lane 1, +ve signal
D1–B	26	I/O	Port B, Lane 1, –ve signal
D2+B	25	I/O	Port B, Lane 2, +ve signal
D2–B	24	I/O	Port B, Lane 2,–ve signal
D3+B	23	I/O	Port B, Lane 3, +ve signal
D3–B	22	I/O	Port B, Lane 3, –ve signal
SCL_B	40	I/O	Port B, DDC Clock
SDA_B	39	I/O	Port B, DDC Data
HPD_B	21	I/O	Port B, Hot Plug Detects
CEC_B	20	I/O	Port B, Consumer Electronics Control
D0+	5	I/O	Common Port, Lane 0, +ve signal
D0–	6	I/O	Common Port, Lane 0, –ve signal
D1+	7	I/O	Common Port, Lane 1, +ve signal
D1–	8	I/O	Common Port, Lane 1, –ve signal
D2+	10	I/O	Common Port, Lane 2, +ve signal
D2–	11	I/O	Common Port, Lane 2, –ve signal
D3+	12	I/O	Common Port, Lane 3, +ve signal
D3–	13	I/O	Common Port, Lane 3,–ve signal
SCL	3	I/O	Common Port, DDC Clock
SDA	4	I/O	Common Port, DDC Data
HPD	14	I/O	Common Port, Hot Plug Detects
CEC	15	I/O	Common Port, Consumer Electronics Control
NC	9, 30	NC	No Connect

LOGIC DIAGRAM

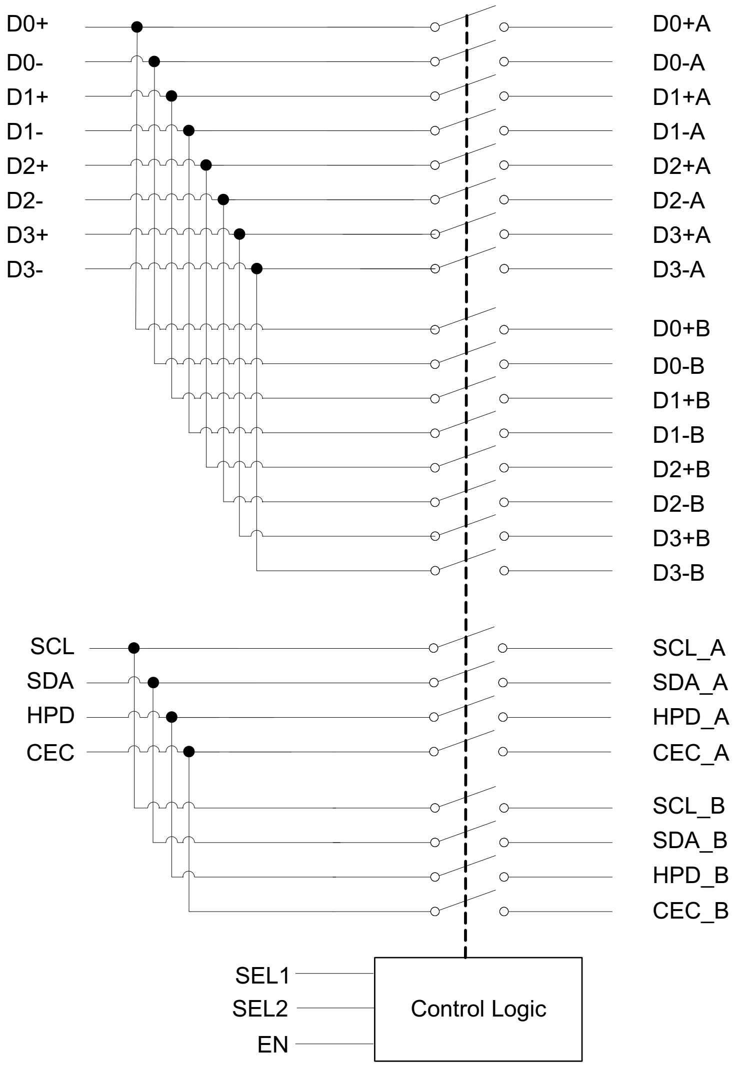


Table 1. Functional Table

EN	SEL1	SEL2	FUNCTION
L	X	X	Switch Disabled. All Channel Hi-Z.
H	L	L	D0+/D0– to D0+A/D0–A ON. All the other channels Hi-Z.
H	L	H	D0+/D0– to D0+B/D0–B ON. All the other channels Hi-Z.
H	H	L	Channel A Enabled. Channel B Hi-Z.
H	H	H	Channel B Enabled. Channel A Hi-Z.

SYSTEM DIAGRAMS FOR DISPLAYPORT APPLICATION

The following two diagrams described two typical DisplayPort applications with the use of TS3DV642. The first one describes a docking application, while the second one describes muxing between two graphic controllers. Note that the TS3DV642 is not designed for passing signals with negative swings; the high speed signals need to be properly DC biased (usually ~1V from the graphic controller side) before being passed to the TS3DV642.

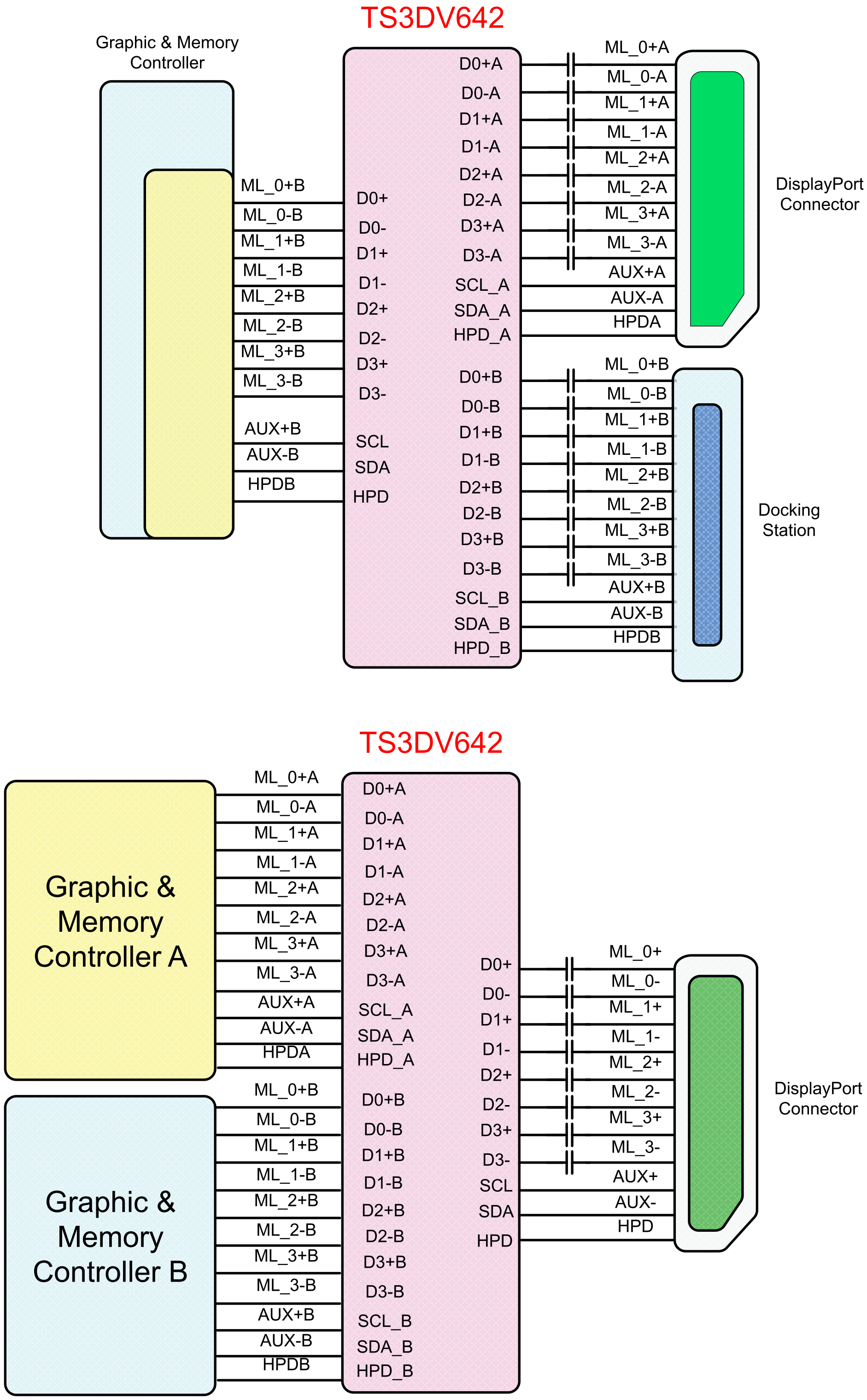


Figure 2. Typical Display Port Application

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	5.5	V
$V_{I/O}$	Analog voltage range[2][3][4]	All I/O	–0.5	5.5	V
V_{IN}	Digital input voltage range[2][3]	SEL1, SEL2,EN	–0.5	5.5	V
$I_{I/OK}$	Analog port diode current	$V_{I/O}$ < 0		–50	mA
I_{IK}	Digital input clamp current	V_{IN} < 0		–50	mA
$I_{I/O}$	On-state switch current[5]		–128	128	mA
θ_{JA}	Package thermal impedance[6]	RUA package		29	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS[1]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.6	4.5	V
$V_{I/O}$	Input/Output voltage	0	5.5	V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused control inputs of the device must be held at VDD or GND to ensure proper device operation. Refer to the *TI application report, Implications of Slow or Floating CMOS Inputs,* literature number SCBA004.

ELECTRICAL CHARACTERISTICS

PARAMETER			TEST CONDITIONS[1]	MIN	TYP[2]	MAX	UNIT
PORT A							
R_{ON}	ON-state resistance	D0 to D3	V_{CC} = 3 V, 1.5 V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = –40 mA		6.5	9.5	Ω
		SCL, SDA, HPD, CEC			6	9.5	Ω
$R_{ON(flat)}$[3]	ON-state resistance flatness	All I/O	V_{CC} = 3 V, $V_{I/O}$ = 1.5 V and V_{CC}, $I_{I/O}$ = –40 mA		1.5		Ω
ΔR_{ON}[4]	On-state resistance match between high-speed channels	D0 to D3	VCC = 3 V, 1.5 V ≤ VI/O ≤ V_{CC}, $I_{I/O}$ = –40 mA		0.4	1	Ω
I_{OFF}	Leakage under power off	All outputs	V_{CC} = 0 V, $V_{I/O}$ = 0 to 3.6 V, V_{IN} = 0 V to 5.5 V			±10	µA
PORT B							
R_{ON}	ON-state resistance	D0 to D3	V_{CC} = 3 V, 1.5 V ≤ $V_{I/O}$ ≤ V_{CC}, II/O = -40 mA		8.2	10.5	Ω
		SCL, SDA, HPD, CEC			6	9.5	Ω
$R_{ON(flat)}$[3]	ON-state resistance flatness	All I/O	V_{CC} = 3 V, $V_{I/O}$ = 1.5 V and V_{CC}, $I_{I/O}$ = –40 mA		1.5		Ω
ΔR_{ON}[4]	On-state resistance match between high-speed channels	D0 to D3	V_{CC} = 3 V, 1.5 V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = –40 mA		0.4	1	Ω
I_{OFF}	Leakage under power off	All outputs	V_{CC} = 0 V, $V_{I/O}$ = 0 V to 3.6 V, V_{IN} = V to 5.5 V			±10	µA

(1) V_I, V_O, I_I, and I_O refer to I/O pins, V_{IN} refers to the control inputs
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C
(3) $R_{ON(FLAT)}$ is the difference of R_{ON} in a given channel at specified voltages.
(4) ΔR_{ON} is the difference of RON from center port to any other ports.

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER			TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
DIGITAL INPUTS (SEL1, SEL2, EN)							
V_{IH}	High-level control input voltage	SEL1, SEL2, EN		1.4			V
V_{IL}	Low-level control input voltage	SEL1, SEL2, EN				0.5	V
I_{IH}	Digital input high leakage current	SEL1, SEL2, EN	V_{CC} = 3.6 V , V_{IN} = V_{DD}			±10	µA
I_{IL}	Digital input low leakage current	SEL1, SEL2, EN	V_{CC} = 3.6 V, V_{IN} = GND			±10	µA
SUPPLY							
I_{CC}	VCC supply current		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Normal Operation Mode, EN = H		50		µA
I_{CC}, PD	VCC supply current in power-down mode		V_{CC} = 3.6 V, $I_{I/O}$ = 0, EN = L		6		µA

SWITCHING CHARACTERISTICS

over recommended operation free-air temperature range, V_{CC} = 3.3 V± 0.3 V (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{ON} (2)	Switch turn-on time		All I/O	See Figure 3			100	µs
t_{SWITCH} (3)	Switching time between channels		All I/O	See Figure 4		20		µs
t_{pd}	Propagation Delay	Port A	D0 to D3	See Figure 5		30		ps
			SCL, SDA, HPD, CEC			30		
		Port B	D0 to D3			40		
			SCL, SDA, HPD, CEC			30		
t_{SKEW}	Inter-pair Skew	Port A	D0 to D3	Between +ve and –ve signals of each lane		2		ps
		Port B				2		
	Intra-pair Skew	Port A		Between lane 0, 1, 2, or 3		2		
		Port B				6		

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(2) t_{ON} is the time it takes the output to recover after enabling switches
(3) t_{SWITCH} is the time it takes for the output to recover after the state is changed

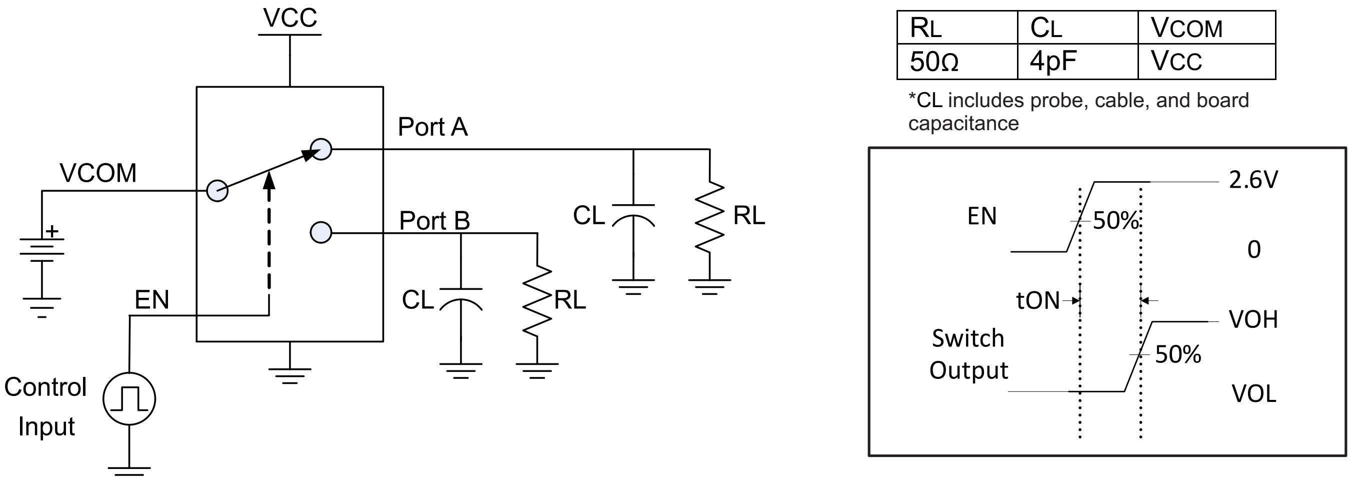
DYNAMIC CHARACTERISTICS

Over recommended operation free-air temperature range, V_{CC} = 3.3V ± 0.3V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
C_{IN}	Digital input capacitance		f = 1 MHz, V_{IN} = 0 V		6		pF
Coff	Switch OFF capacitance		f = 1 GHz, $V_{I/O}$ = 0 V, Output is open, Switch is OFF		0.3		pF
Con	Switch ON capacitance		f = 1 GHz, $V_{I/O}$ = 0 V, Output is open, Switch is ON		0.5		pF
Xtalk	Differential Crosstalk		R_L = 50 Ω at 1.7 GHz (See Figure 6)		–40		dB
			R_L = 50 Ω at 2.7 GHz (See Figure 7)		–40		
OISO	Differential Off Isolation		R_L = 50 Ω at 1.7 GHz (See Figure 7)		–23		dB
			R_L = 50 Ω at 2.7 GHz (See Figure 7)		–28		
IL	Insertion Loss		Port A at DC		–0.75		dB
			Port B at DC		–1		dB
BW	Differential Bandwidth (–3 dB)	Port A	R_L = 50 Ω, All channels (See Figure 8)		6.9		GHz
		Port B	R_L = 50 Ω, All channels (See Figure 8)		7.5		

(1) All Typical Values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.

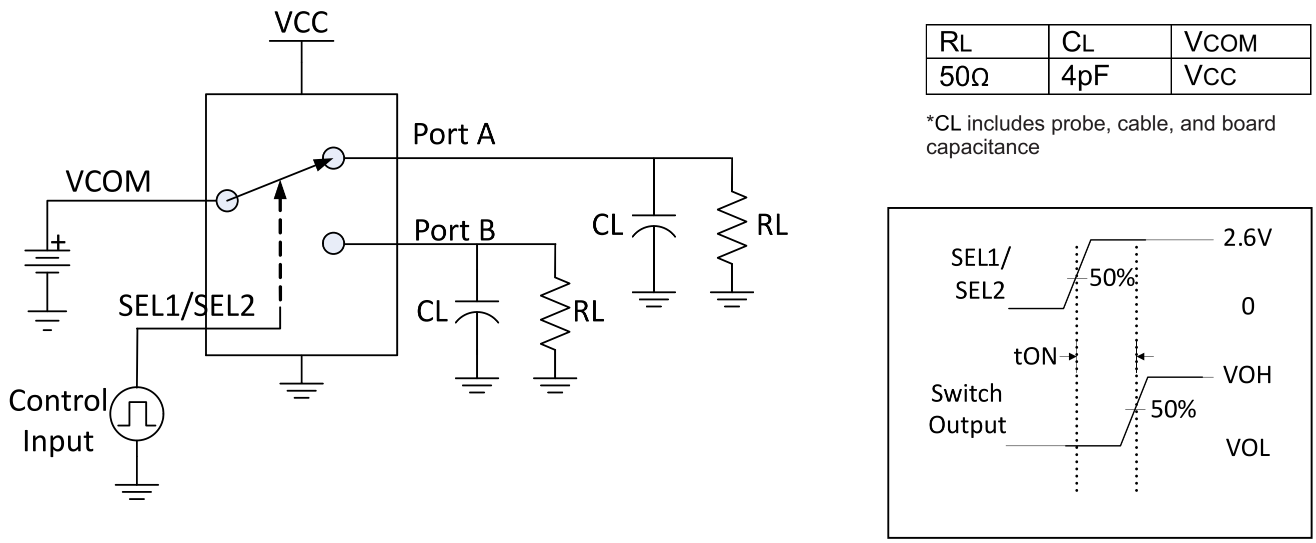
PARAMETER MEASUREMENT INFORMATION



RL	CL	VCOM
50Ω	4pF	VCC

*CL includes probe, cable, and board capacitance

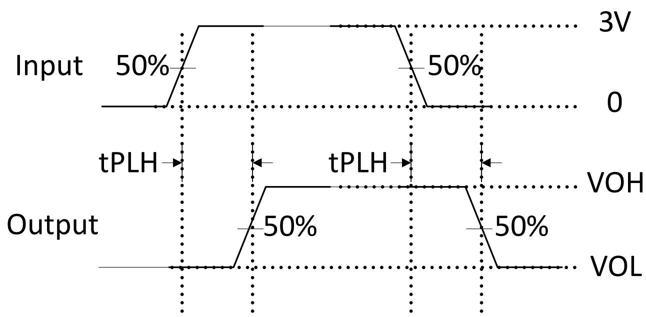
Figure 3. Switch Turn-On Time (t_{ON})



RL	CL	VCOM
50Ω	4pF	VCC

*CL includes probe, cable, and board capacitance

Figure 4. Switching Time Between Channels (t_{SWITCH})



$$tpd = (tPLH + tPLH) / 2$$

Figure 5. Propagation Delay (t_{pd})

PARAMETER MEASUREMENT INFORMATION (continued)

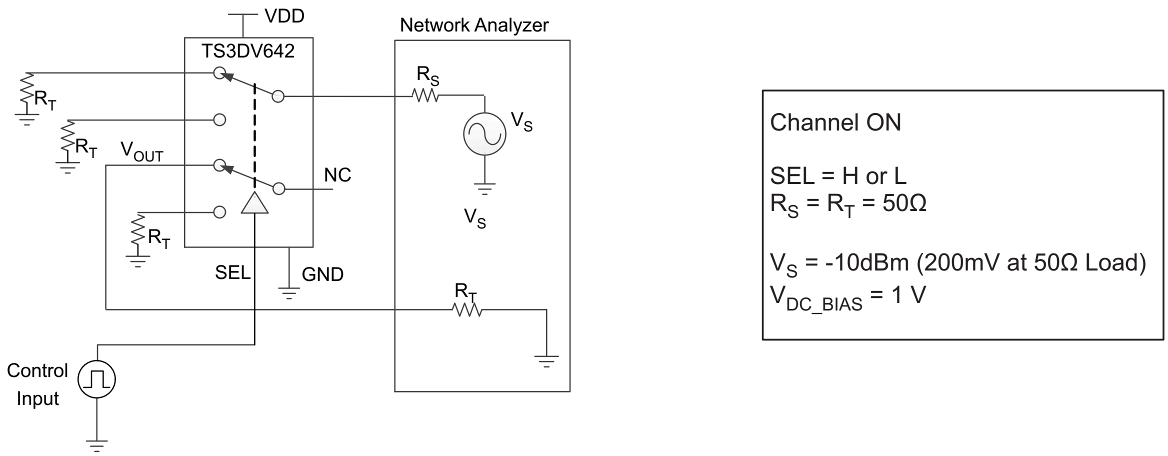


Figure 6. Crosstalk (Xtalk)

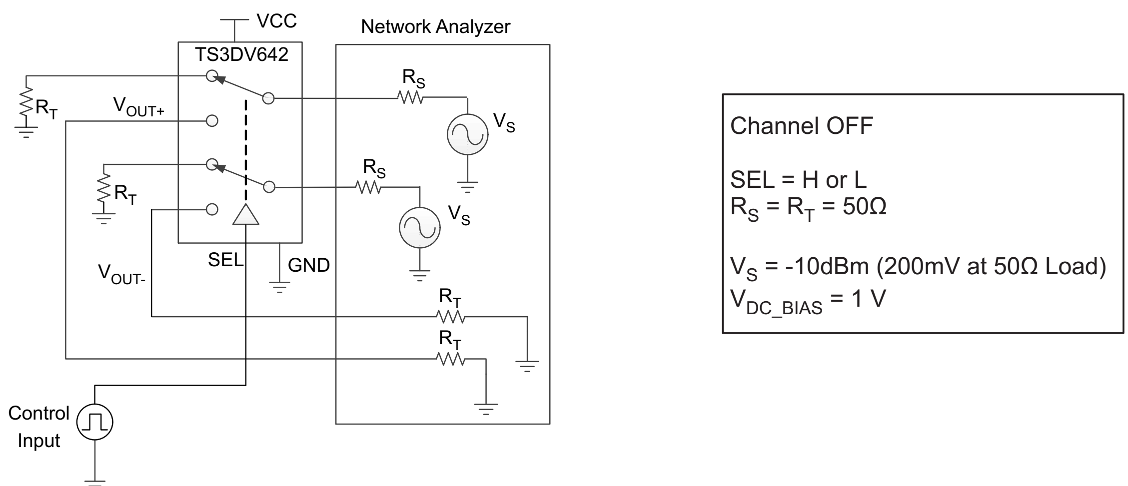


Figure 7. Differential Off-Isolation (OISO)

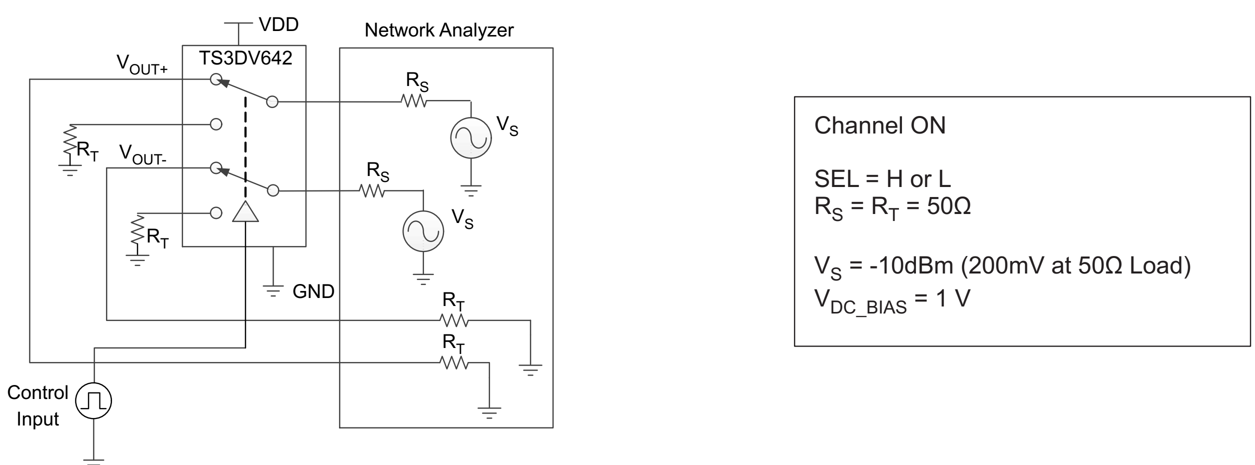


Figure 8. Differential Bandwidth (BW)

TYPICAL CHARACTERISTICS

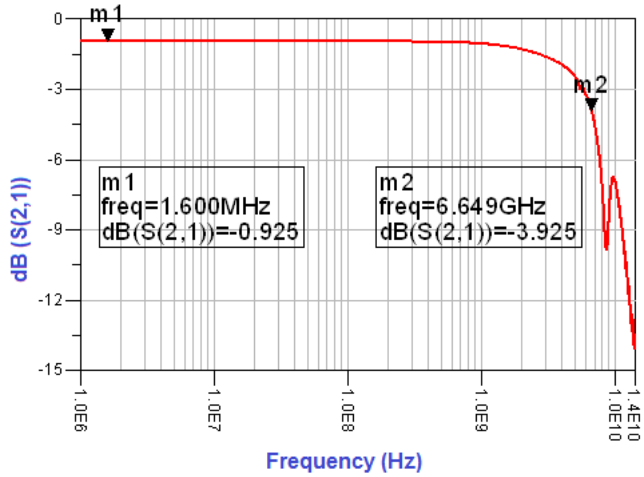


Figure 9. Differential S21 vs Frequency for Port A

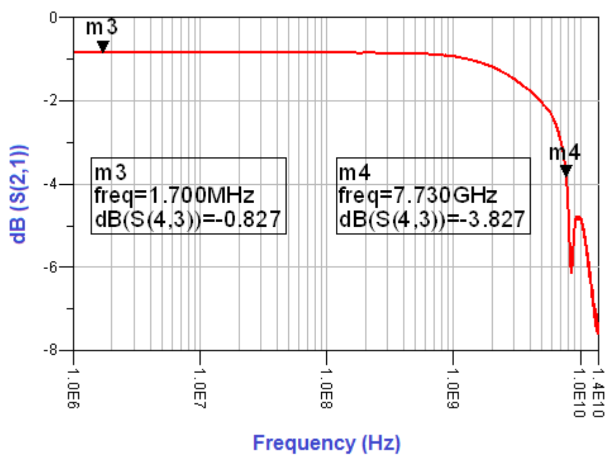


Figure 10. Differential S21 vs Frequency for Port B

TYPICAL CHARACTERISTICS (continued)

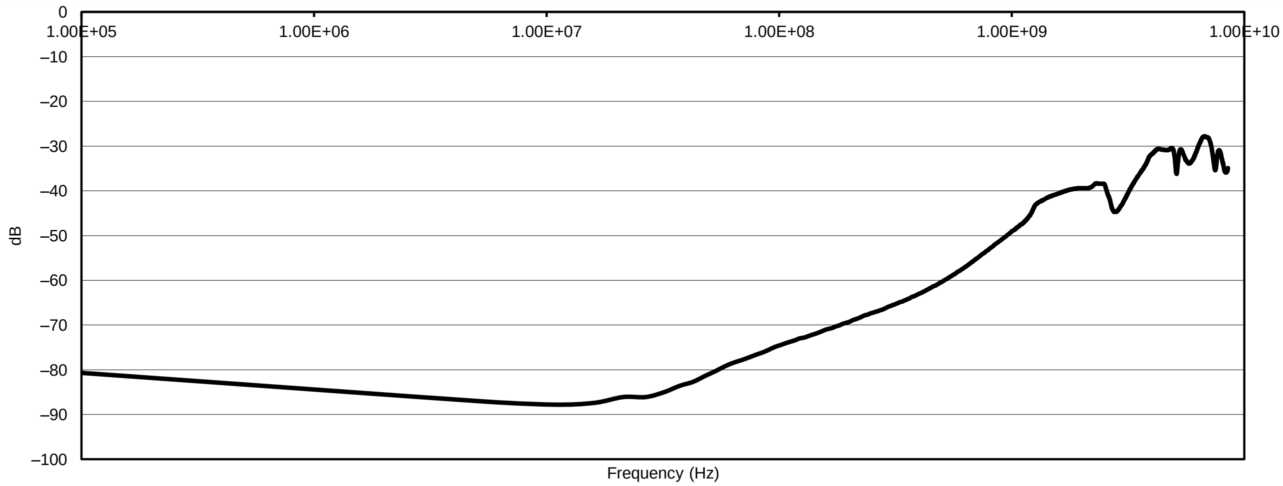


Figure 11. XTALK Port A

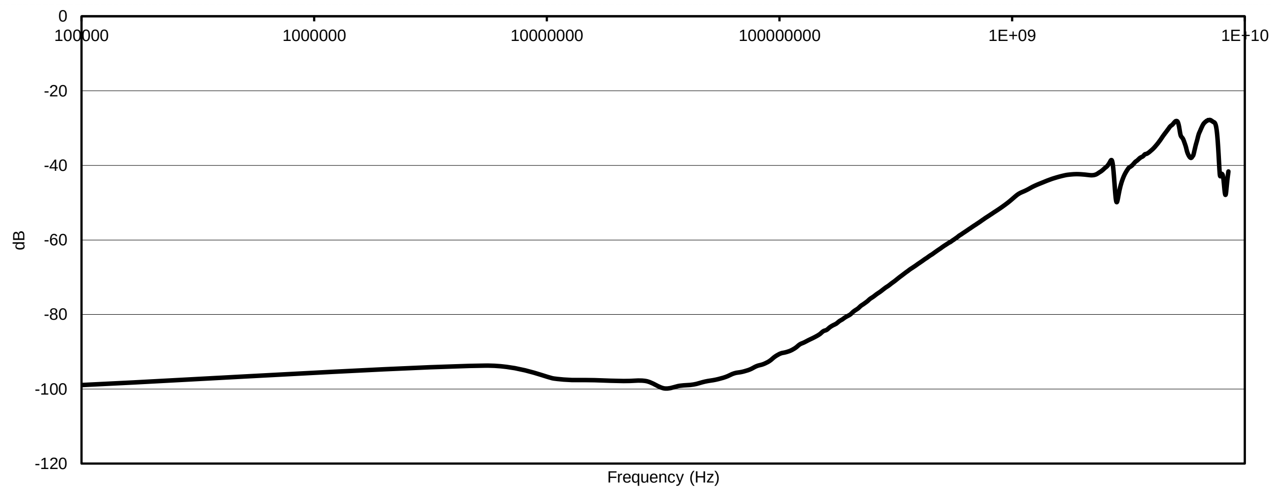


Figure 12. XTALK Port B

TYPICAL CHARACTERISTICS (continued)

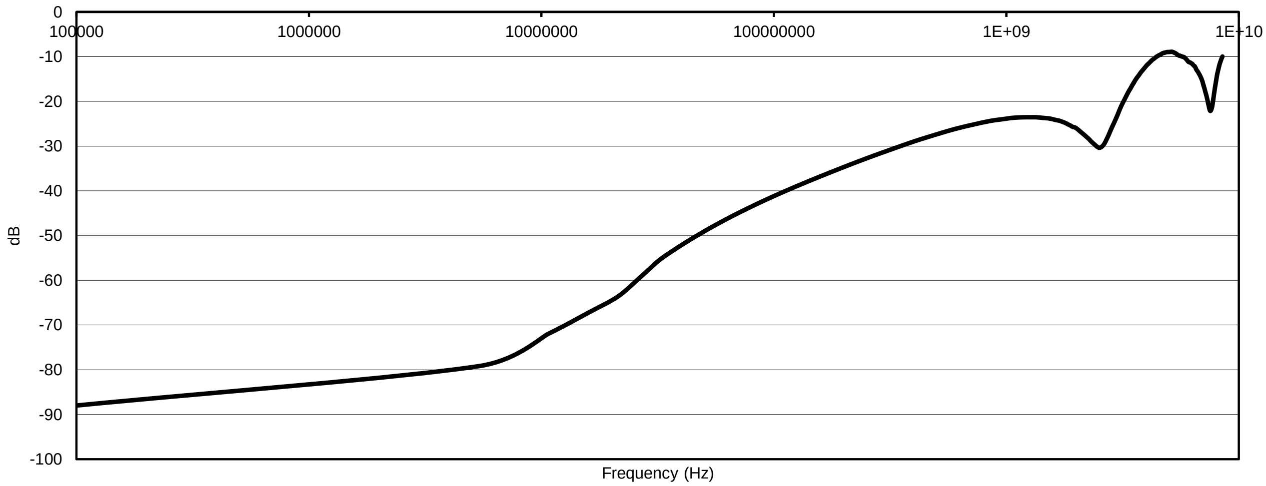


Figure 13. OIRR Port A

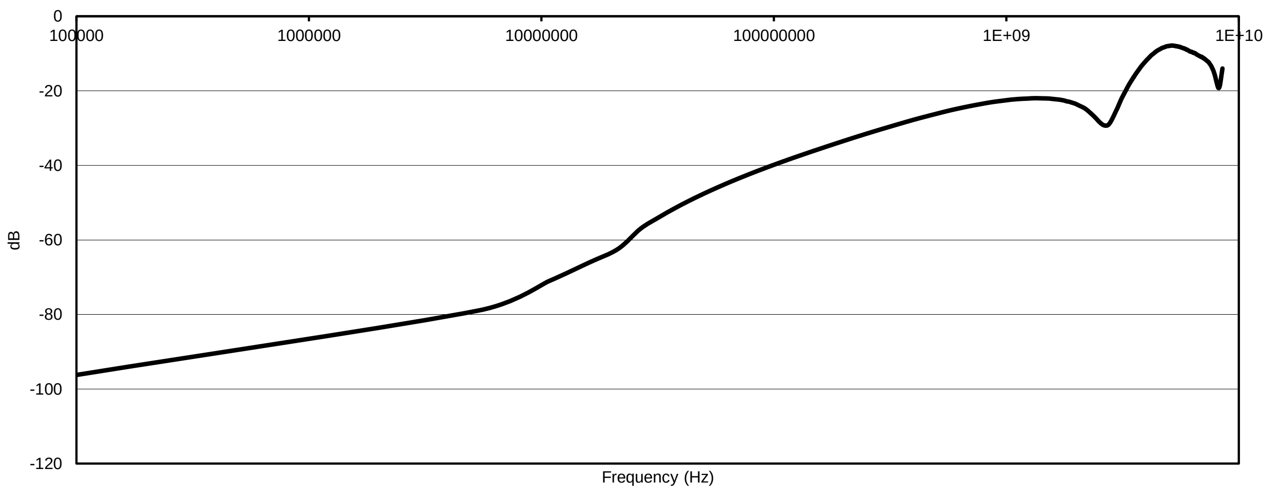


Figure 14. OIRR Port B

TYPICAL CHARACTERISTICS (continued)

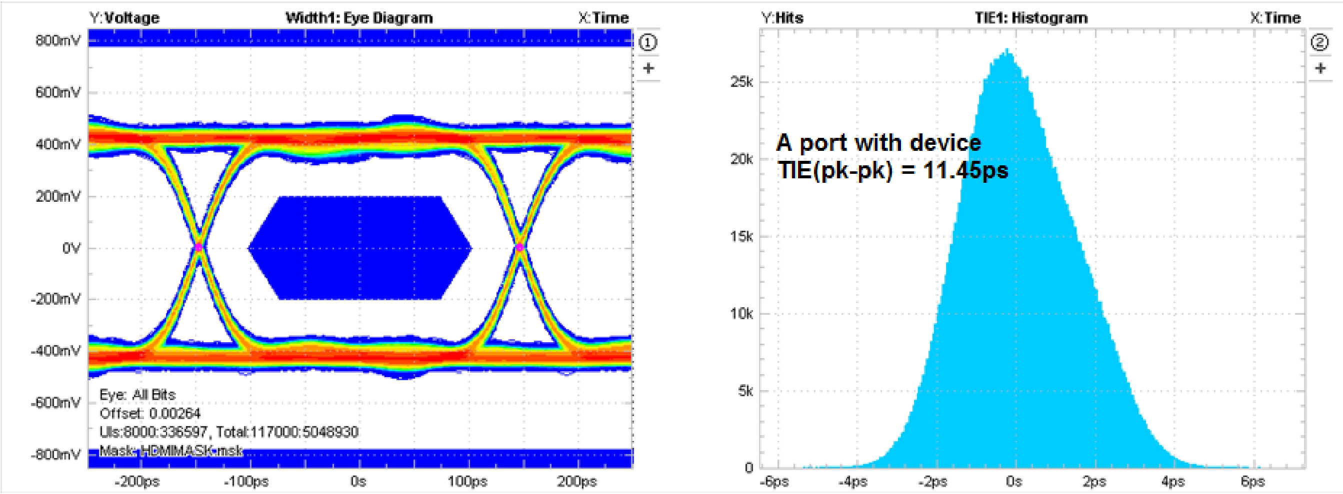


Figure 15. Eye Pattern and Time Interval Error Histogram: 3.4 Gbps Port A, With Device

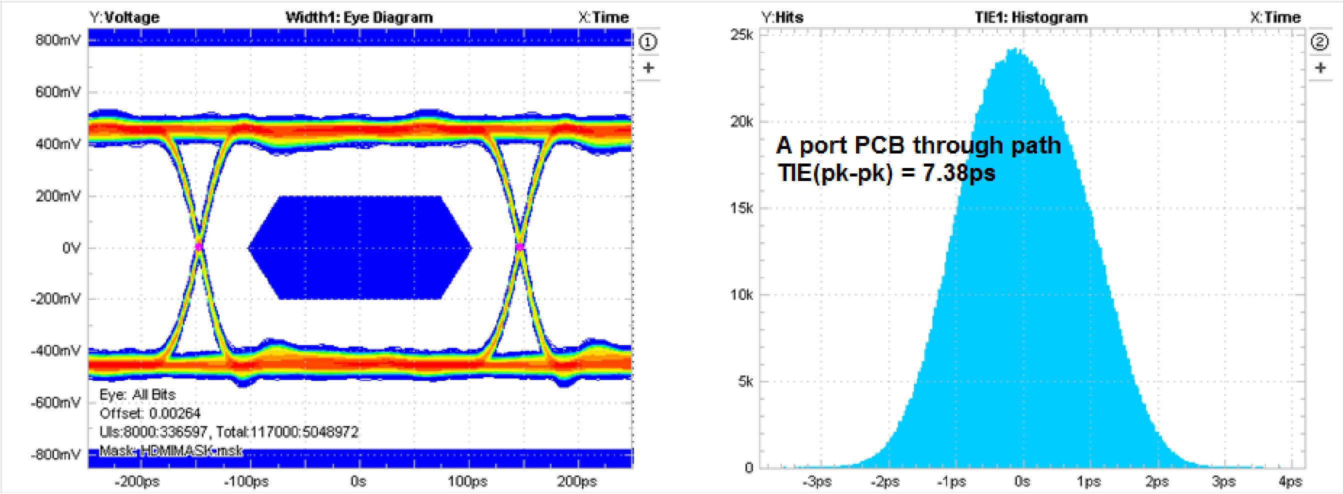


Figure 16. Eye Pattern and Time Interval Error Histogram: 3.4 Gbps Port A, No Device

TYPICAL CHARACTERISTICS (continued)

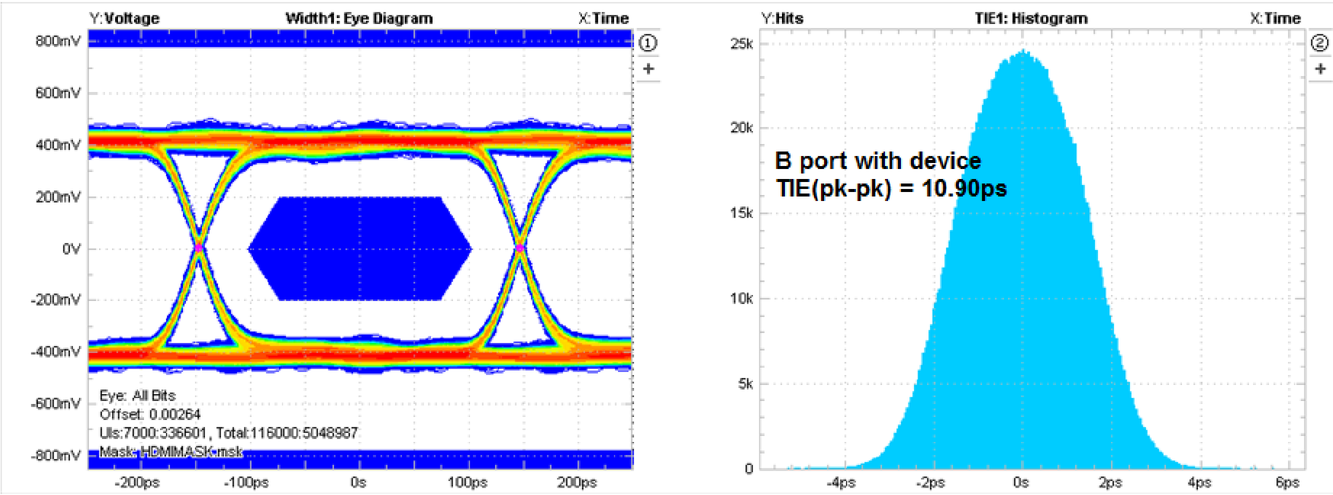


Figure 17. Eye Pattern and Time Interval Error Histogram: 3.4 Gbps Port B, With Device

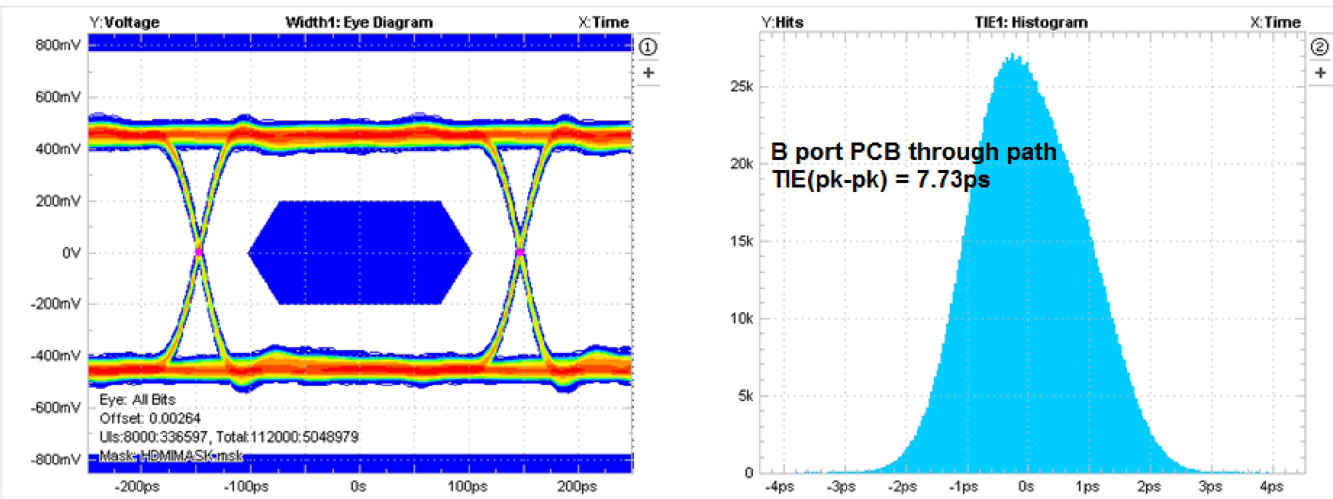


Figure 18. Eye Pattern and Time Interval Error Histogram: 3.4 Gbps Port B, No Device

REVISION HISTORY

Changes from Original (May 2013) to Revision A	Page
• Changed Feature From: Con: 4 pF Typ To: Con at 1GHz: 0.5 pF Typ	1
• Removed the Ordering Information table.	1
• Added the SYSTEM DIAGRAMS FOR DISPLAYPORT APPLICATION Section.	4

Changes from Revision A (July 2013) to Revision B	Page
• Changed Application From: HDMI 1.4/DVI 1.0 Signal Switching To: HDMI 1.4b with support for 4k2k up to 30 Hz	1
• Added Application: DVI 1.0 Signal Switching	1
• Changed Application From: DisplayPort 1.2 Signal Switching To: DisplayPort 1.2a Signal Switching	1
• Added Eye Pattern and Time Interval Error Histogram graphics, Figure 15 to Figure 18	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DV642A0RUAR	ACTIVE	WQFN	RUA	42	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		SD642A0	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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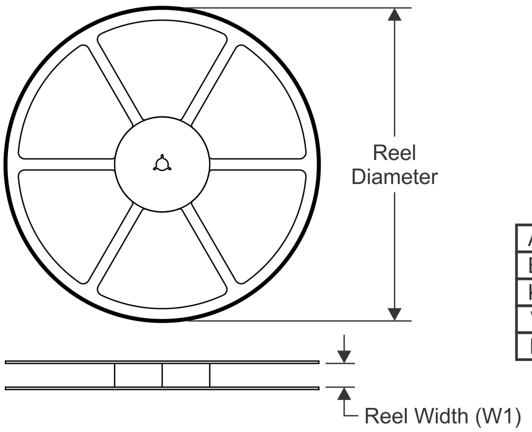
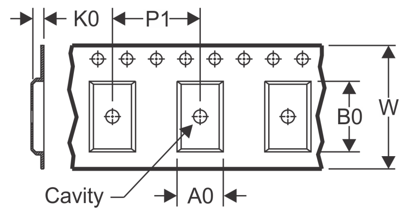
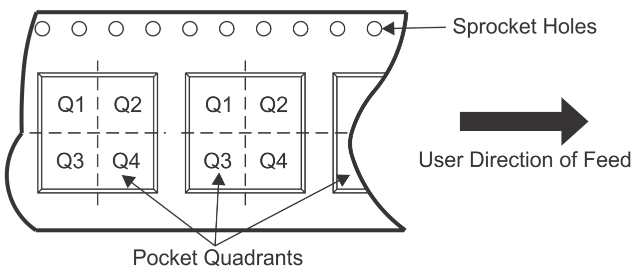
TAPE AND REEL INFORMATION





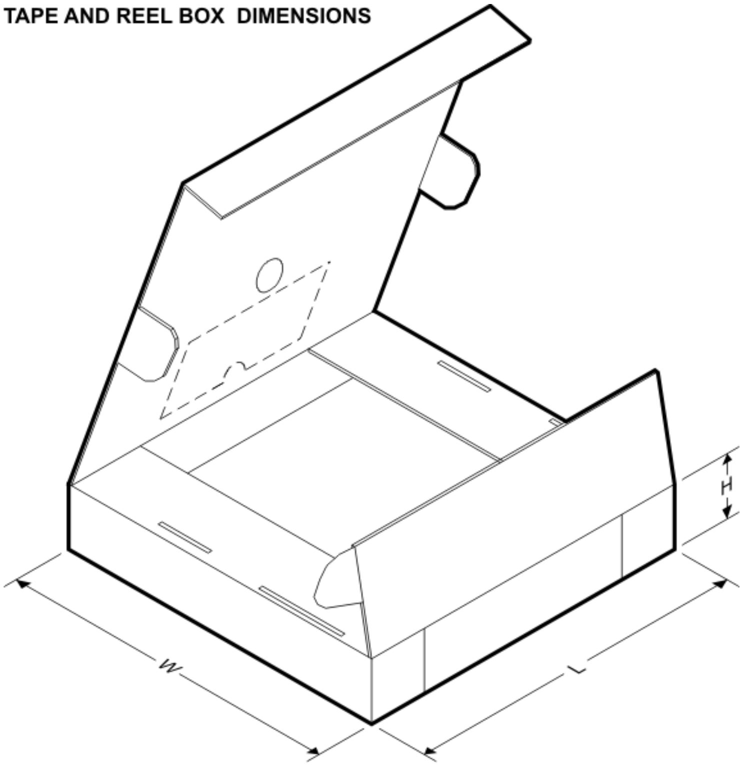
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV642A0RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

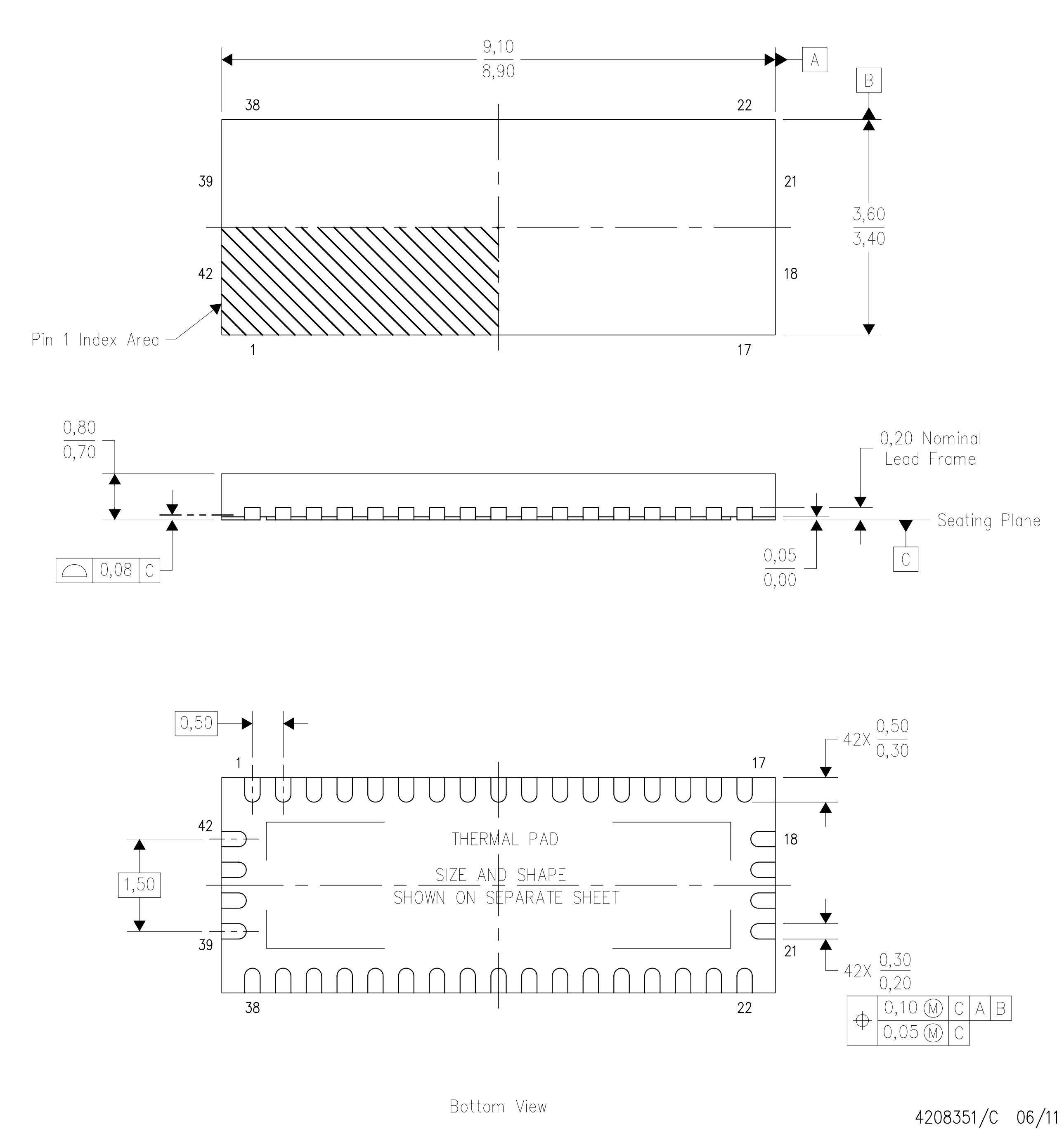
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV642A0RUAR	WQFN	RUA	42	3000	367.0	367.0	38.0

RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

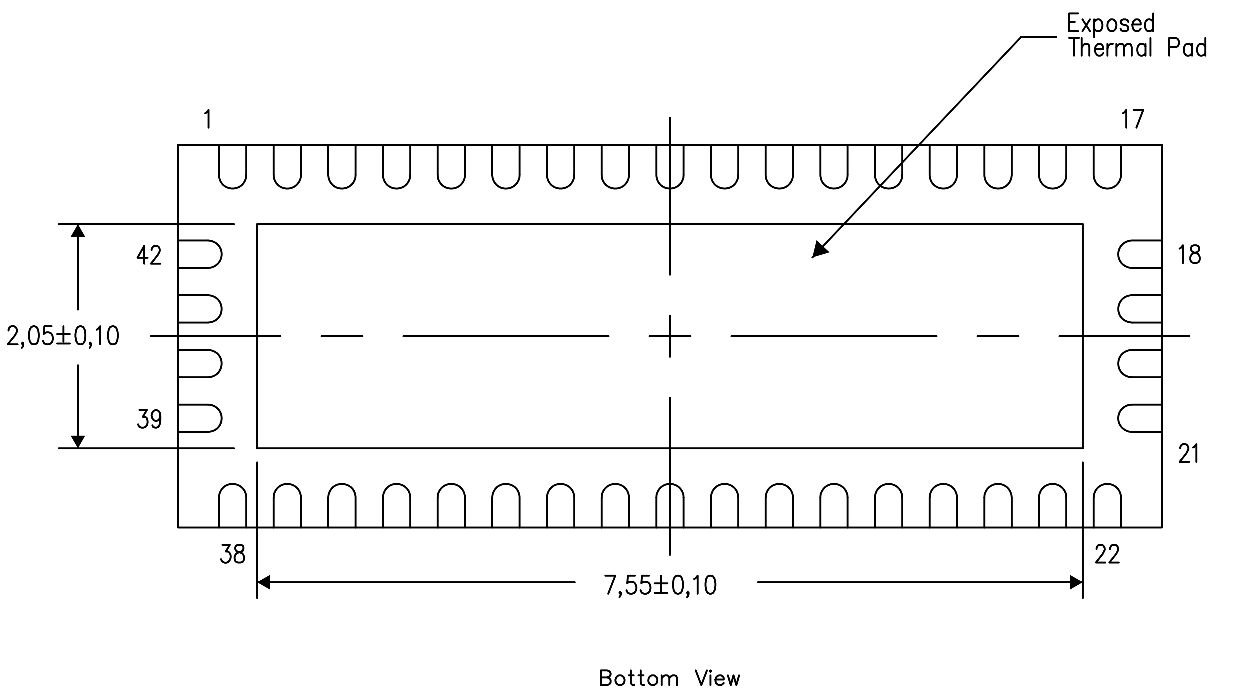
RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

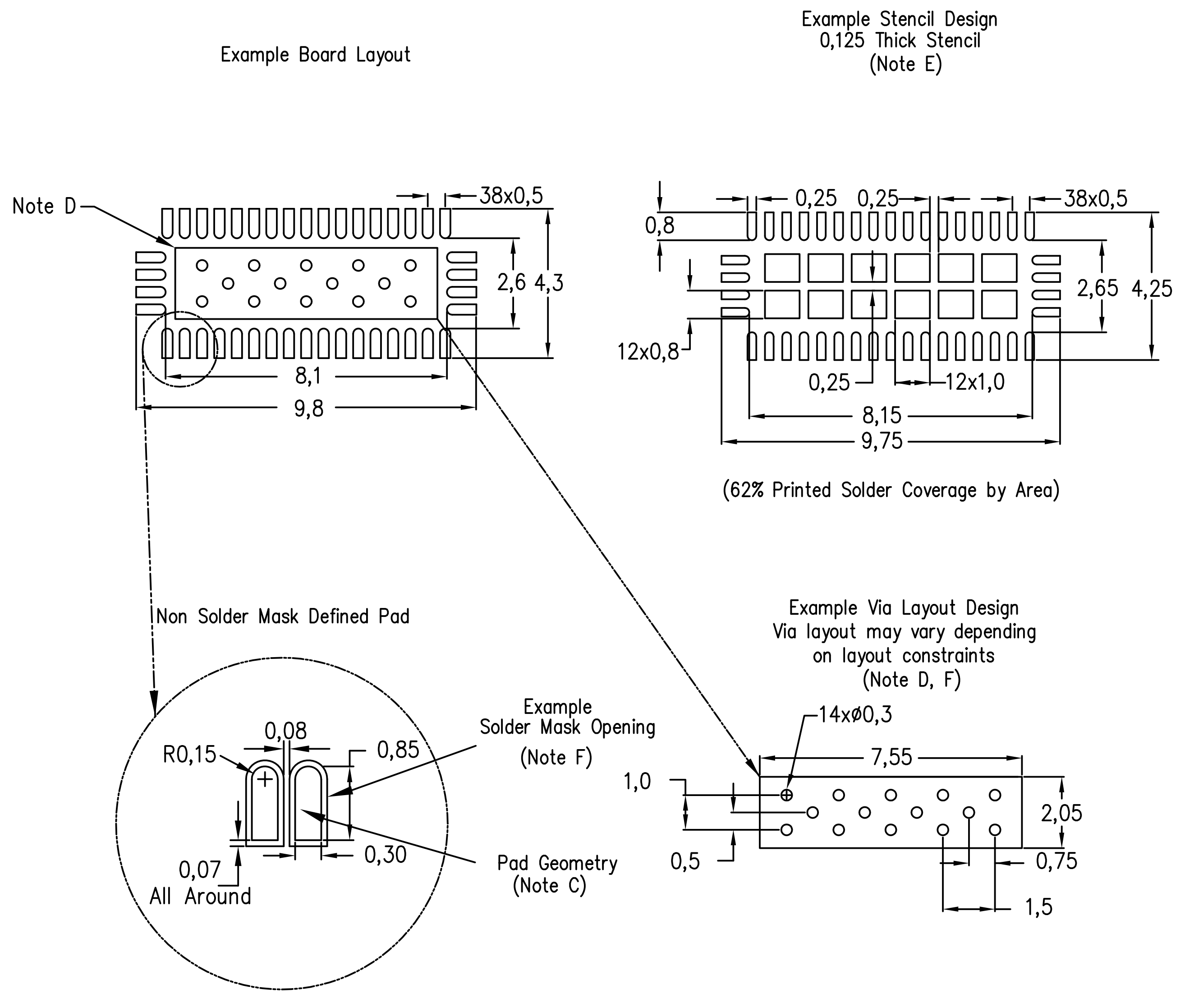


Exposed Thermal Pad Dimensions

4208352/E 01/13

NOTE: All linear dimensions are in millimeters

RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD



4210129/D 01/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.