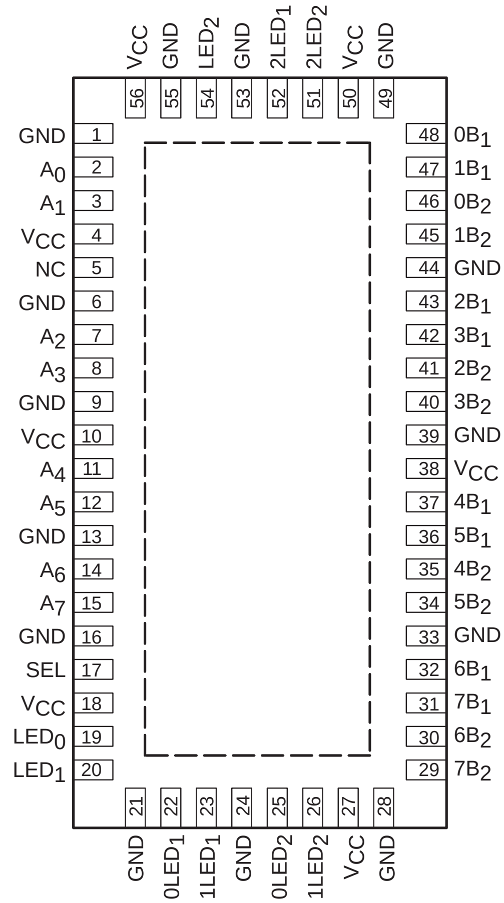
- **Wide Bandwidth (BW > 1100 MHz Typ)**
- **Low Crosstalk (X_{TALK} = −37 dB Typ)**
- **Low Bit-to-Bit Skew ($t_{sk(o)}$ = 100 ps Max)**
- **Low and Flat ON-State Resistance (r_{on} = 4 Ω Typ, $r_{on(flat)}$ = 0.5 Ω Typ)**
- **Low Input/Output Capacitance (C_{ON} = 8 pF Typ)**
- **Rail-to-Rail Switching on Data I/O Ports (0 to 5 V)**
- **V_{CC} Operating Range From 3 V to 3.6 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Applications**
  - **10/100/1000 Base-T Signal Switching**
  - **Differential (LVDS, LVPECL) Signal Switching**
  - **Audio/Video Switching**
  - **Hub and Router Signal Switching**

TQFN PACKAGE
(TOP VIEW)



description/ordering information

The TS3L500 is a 16-bit to 8-bit multiplexer/demultiplexer LAN switch with a single select (SEL) input. SEL controls the data path of the multiplexer/demultiplexer. The device provides additional I/Os for switching status indicating LED signals.

The device provides a low and flat ON-state resistance (r_{on}) and an excellent ON-state resistance match. Low input/output capacitance, high bandwidth, low skew, and low crosstalk among channels make this device suitable for various LAN applications, such as 10/100/1000 Base-T.

This device can be used to replace mechanical relays in LAN applications. It also can be used to route signals from a 10/100 Base-T ethernet transceiver to the RJ-45 LAN connectors in laptops or in docking stations.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TQFN	Tape and reel	TS3L500RHUR	TK500

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

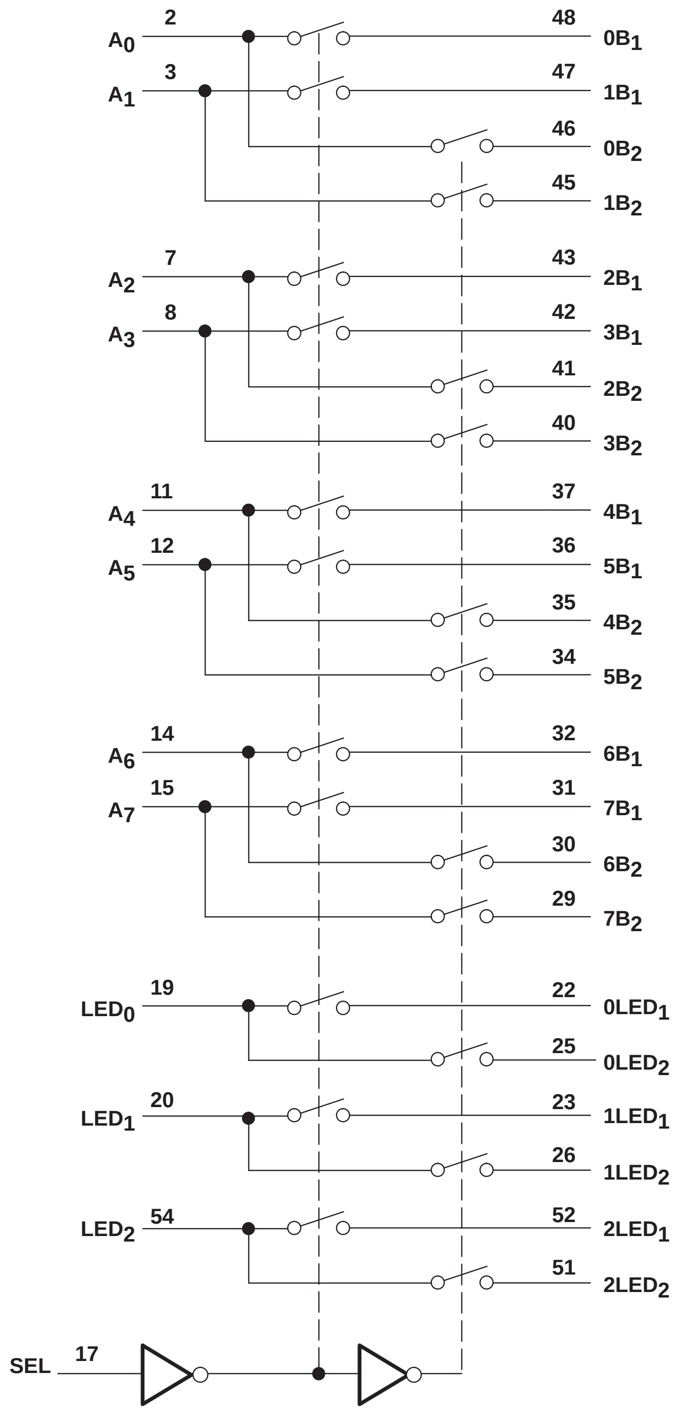
FUNCTION TABLE

INPUT SEL	INPUT/OUTPUT A_n	FUNCTION
L	nB_1	$A_n = nB_1$, $LED_x = XLED_1$
H	nB_2	$A_n = nB_2$, $LED_x = XLED_2$

PIN DESCRIPTION

NAME	DESCRIPTION
A_n	Data I/O
nB_m	Data I/O
SEL	Select input
LED_x	LED I/O port
$XLED_m$	LED I/O port

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . −0.5 V to 7 V
Control input clamp current, I_{IK} (V_{IN} < 0) . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0) . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . ±128 mA
Continuous current through V_{CC} or GND terminals . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5) . . . . 31.8°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground, unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage (SEL)	2	5.5	V
V_{IL}	Low-level control input voltage (SEL)	0	0.8	V
$V_{I/O}$	Input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics for 1000 Base-T ethernet switching over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)†

PARAMETER		TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{IK}	SEL	V_{CC} = 3.6 V,	I_{IN} = −18 mA				−0.7	−1.2	V
I_{IH}	SEL	V_{CC} = 3.6 V,	V_{IN} = V_{CC}					±1	μA
I_{IL}	SEL	V_{CC} = 3.6 V,	V_{IN} = GND					±1	μA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0,	Switch ON or OFF			250	500	μA
C_{IN}	SEL	f = 1 MHz,	V_{IN} = 0				2	2.5	pF
C_{OFF}	B port	V_I = 0,	f = 1 MHz,	Outputs open,	Switch OFF		2.5	4	pF
C_{ON}		V_I = 0,	f = 1 MHz,	Outputs open,	Switch ON		8	9	pF
r_{on}		V_{CC} = 3 V,	1.5 V ≤ V_I ≤ V_{CC},	I_O = −40 mA			4	6	Ω
$r_{on(flat)}$§		V_{CC} = 3 V,	V_I = 1.5 V and V_{CC},	I_O = −40 mA			0.5		Ω
Δr_{on}¶		V_{CC} = 3 V,	1.5 V ≤ V_I ≤ V_{CC},	I_O = −40 mA			0.4	1	Ω

† V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
‡ All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
§ $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
¶ Δr_{on} is the difference of r_{on} from center (A_4, A_5) ports to any other port.

electrical characteristics for 10/100 Base-T ethernet switching over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)†

PARAMETER		TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{IK}	SEL	V_{CC} = 3.6 V,	I_{IN} = −18 mA				−0.7	−1.2	V
I_{IH}	SEL	V_{CC} = 3.6 V,	V_{IN} = V_{CC}					±1	μA
I_{IL}	SEL	V_{CC} = 3.6 V,	V_{IN} = GND					±1	μA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0,	Switch ON or OFF			250	500	μA
C_{IN}	SEL	f = 1 MHz,	V_{IN} = 0				2	2.5	pF
C_{OFF}	B port	V_I = 0,	f = 1 MHz,	Outputs open,	Switch OFF		2.5	4	pF
C_{ON}		V_I = 0,	f = 1 MHz,	Outputs open,	Switch ON		8		pF
r_{on}		V_{CC} = 3 V,	1.25 V ≤ V_I ≤ V_{CC},	I_O = −10 mA to −30 mA			4	6	Ω
$r_{on(flat)}$§		V_{CC} = 3 V,	V_I = 1.25 V and V_{CC},	I_O = −10 mA to −30 mA			0.5		Ω
Δr_{on}¶		V_{CC} = 3 V,	1.25 V ≤ V_I ≤ V_{CC},	I_O = −10 mA to −30 mA			0.4	1	Ω

† V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
‡ All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
§ $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
¶ Δr_{on} is the difference of r_{on} from center (A_4, A_5) ports to any other port.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted) (see Figures 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{pd}‡	A or B	B or A		0.25		ns
t_{PZH}, t_{PZL}	SEL	A or B	0.5		15	ns
t_{PHZ}, t_{PLZ}	SEL	A or B	0.9		9	ns
$t_{sk(o)}$§	A or B	B or A		50	100	ps
$t_{sk(p)}$¶				50	150	ps

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
‡ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
§ Output skew between center port (A_4 to A_5) to any other port
¶ Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$

dynamic characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP†	UNIT
X_{TALK}	R_L = 100 Ω,	f = 250 MHz,	See Figure 8	−37	dB
O_{IRR}	R_L = 100 Ω,	f = 250 MHz,	See Figure 9	−37	dB
BW	R_L = 100 Ω,	See Figure 7		1100	MHz

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

OPERATING CHARACTERISTICS

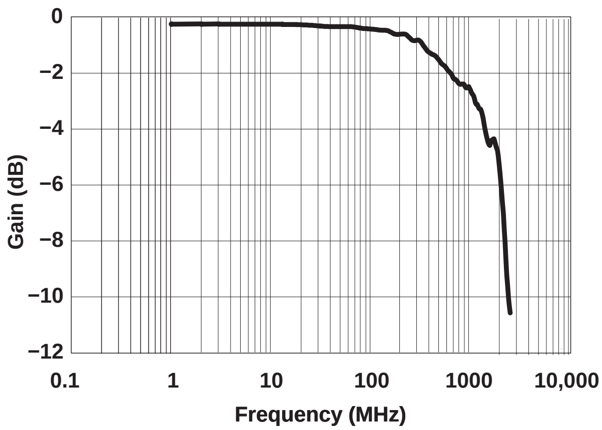


Figure 1. Gain vs Frequency

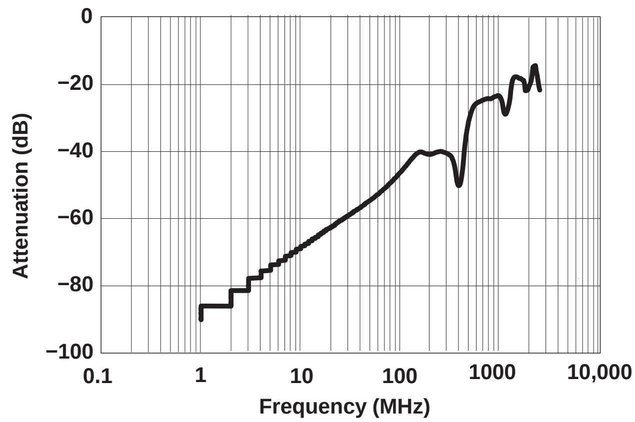


Figure 2. OFF Isolation vs Frequency

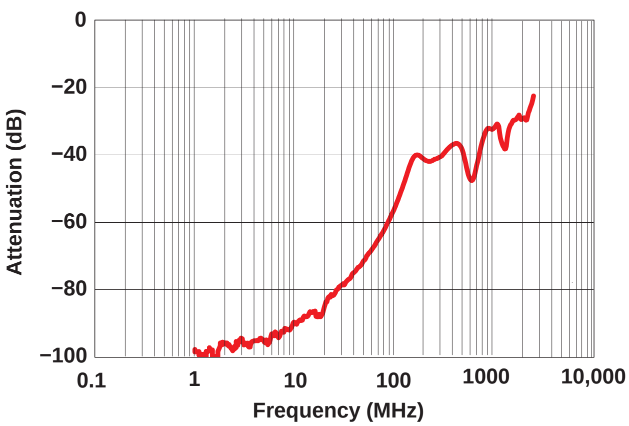


Figure 3. Crosstalk vs Frequency

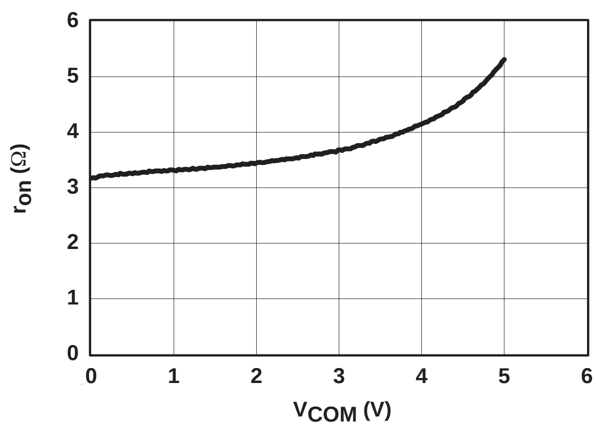
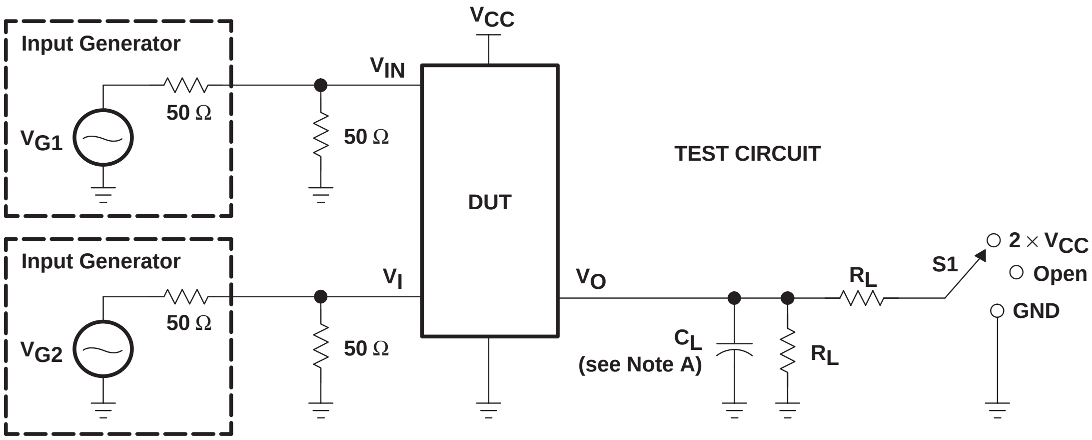
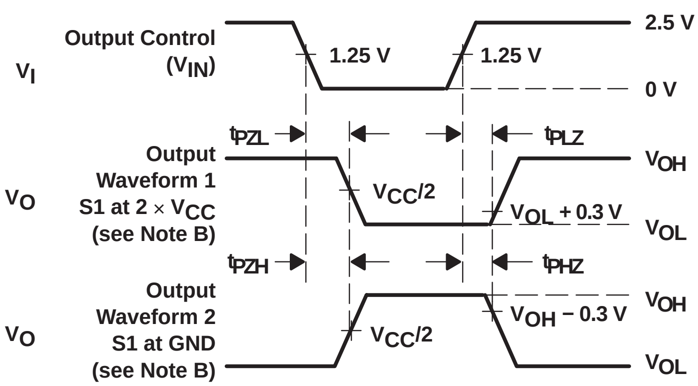


Figure 4. r_{on} (Ω) vs V_{com} (V)

PARAMETER MEASUREMENT INFORMATION
Enable and Disable Times



TEST	V_{CC}	S1	R_L	V_{in}	C_L	V_{Δ}
t_{PLZ}/t_{PZL}	3.3 V ± 0.3 V	2 × V_{CC}	200 Ω	GND	10 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V ± 0.3 V	GND	200 Ω	V_{CC}	10 pF	0.3 V

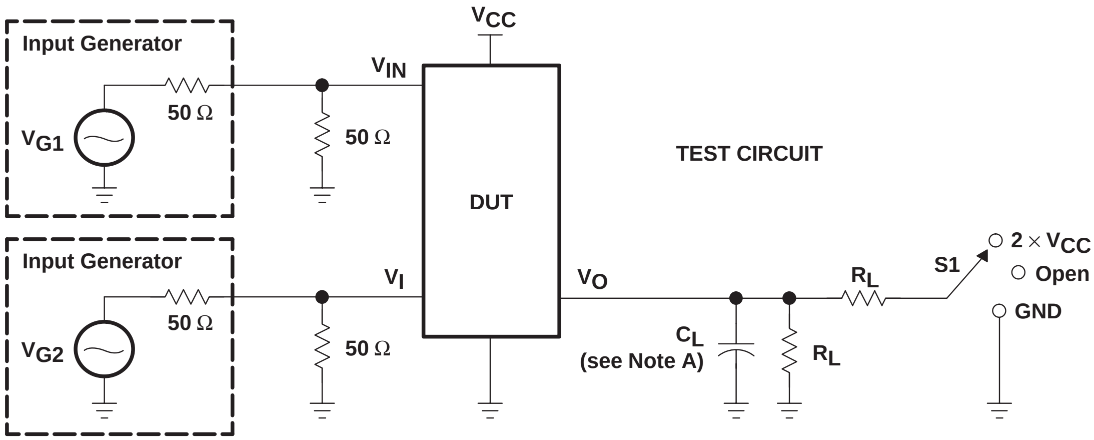


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

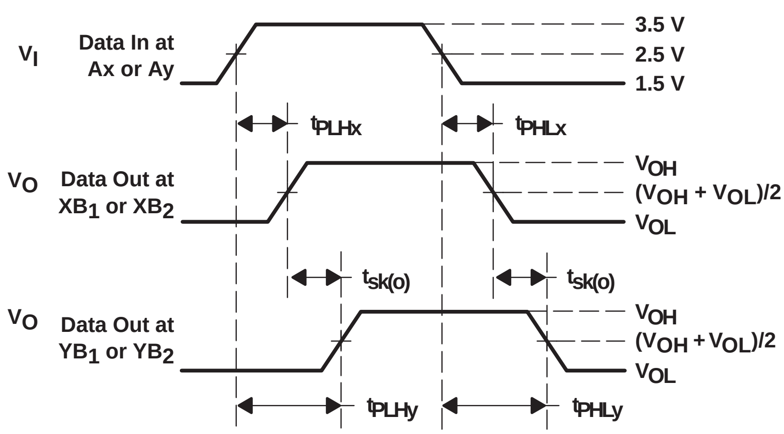
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 5. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
Skew

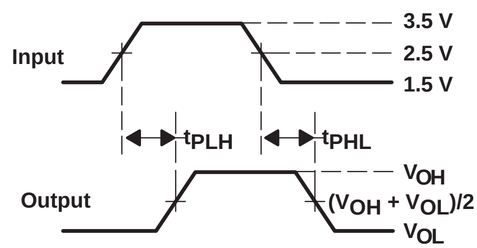


TEST	V_{CC}	S1	R_L	V_{in}	C_L
$t_{sk(o)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{CC} or GND	10 pF
$t_{sk(p)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{CC} or GND	10 pF



$t_{sk(o)} = |t_{PLHy} - t_{PLHx}|$ or $|t_{PHLy} - t_{PHLx}|$

VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)



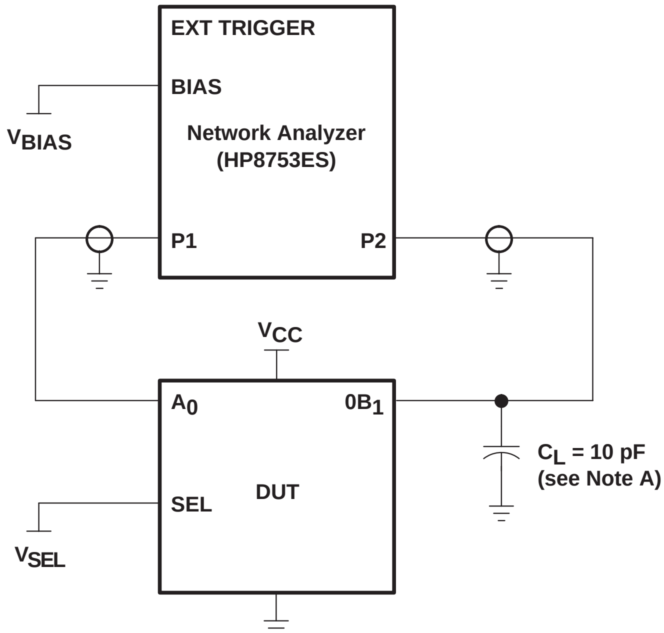
$t_{sk(p)} = |t_{PHL} - t_{PLH}|$

VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 6. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

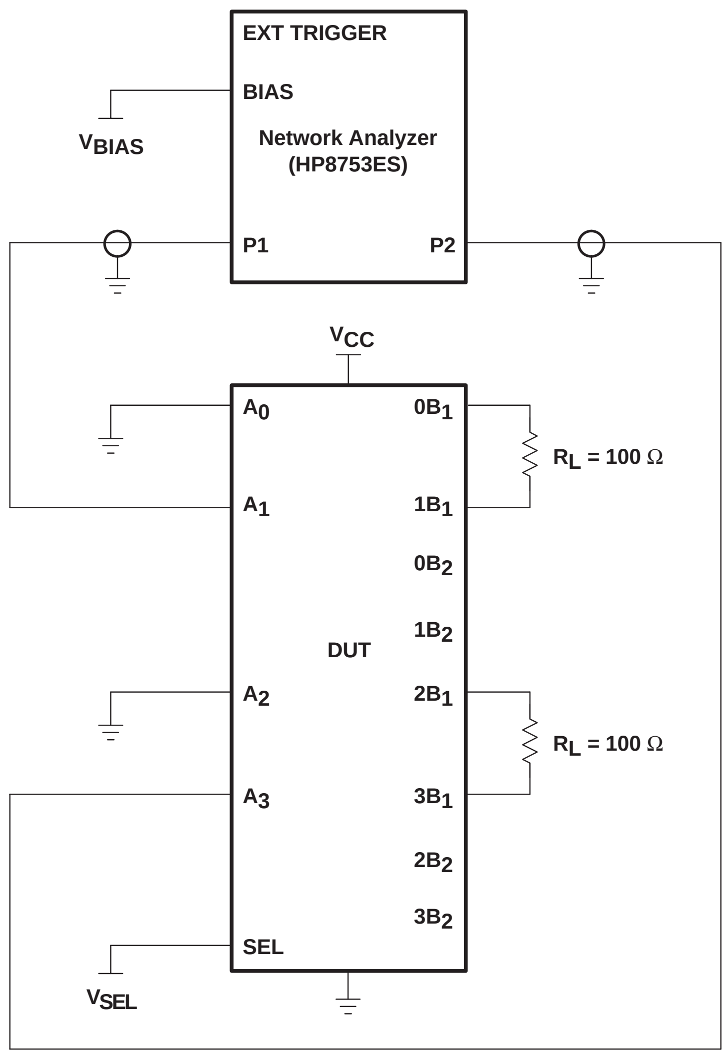
Figure 7. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 and A_0 is the input, the output is measured at $0B_1$. All unused analog I/O ports are left open.

HP8753ES setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

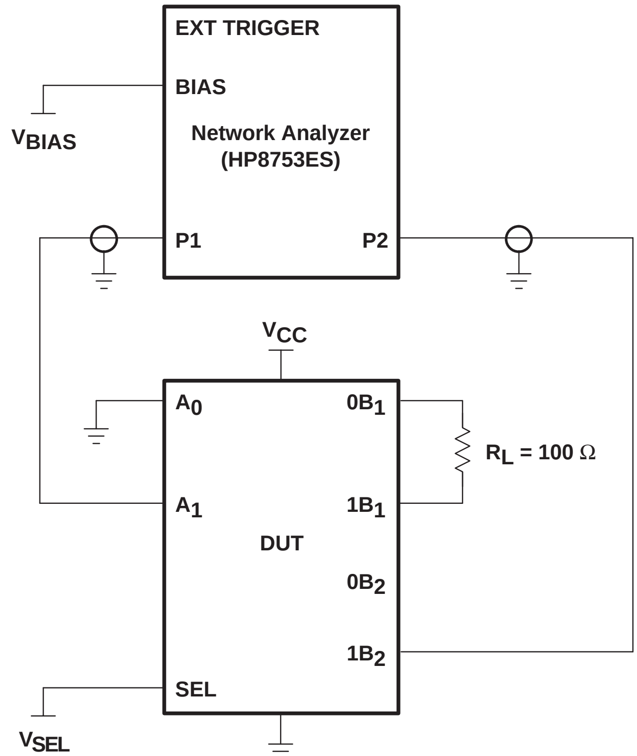
Figure 8. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{SEL} = 0 and A_0 is the input, the output is measured at $1B_1$. All unused analog input (A) ports are connected to GND, and output (B) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

Figure 9. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when $V_{SEL} = V_{CC}$ and A_0 is the input, the output is measured at $0B_2$. All unused analog input (A) ports are left open, and output (B) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TS3L500RHUR	ACTIVE	WQFN	RHU	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3L500RHURG4	ACTIVE	WQFN	RHU	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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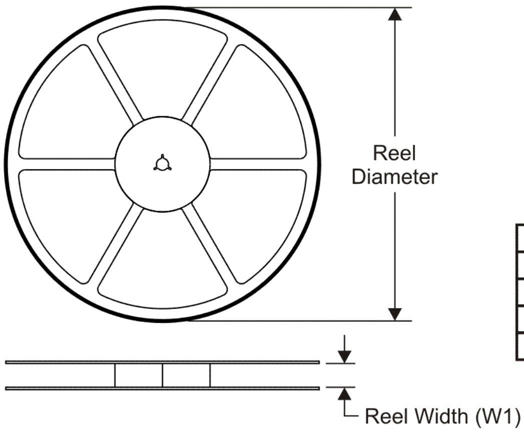
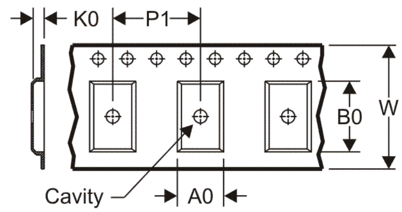
TAPE AND REEL INFORMATION

REEL DIMENSIONS

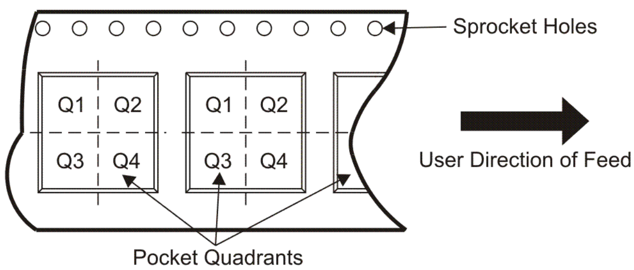


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

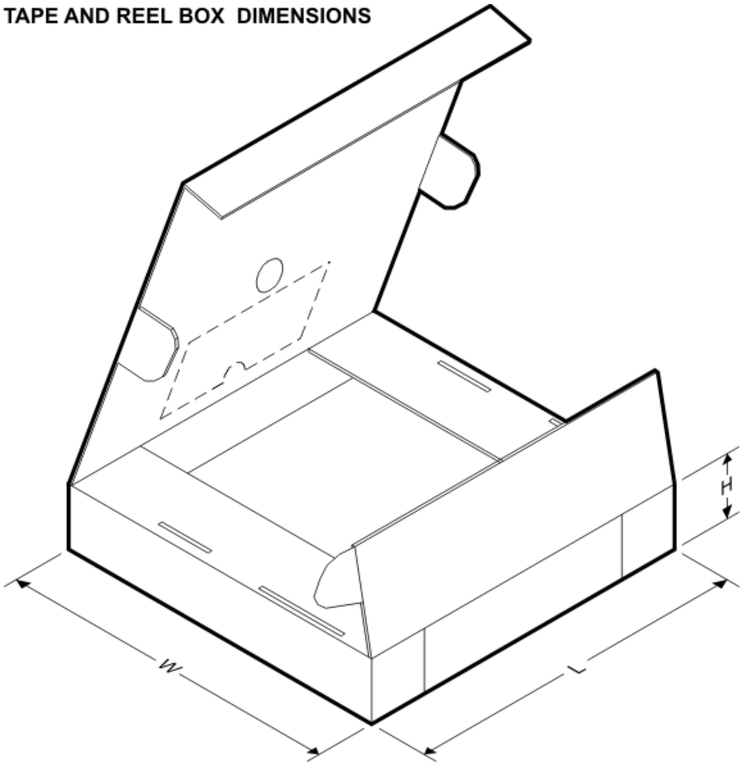
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3L500RHUR	WQFN	RHU	56	2000	330.0	24.4	5.3	11.3	1.0	12.0	24.0	Q1

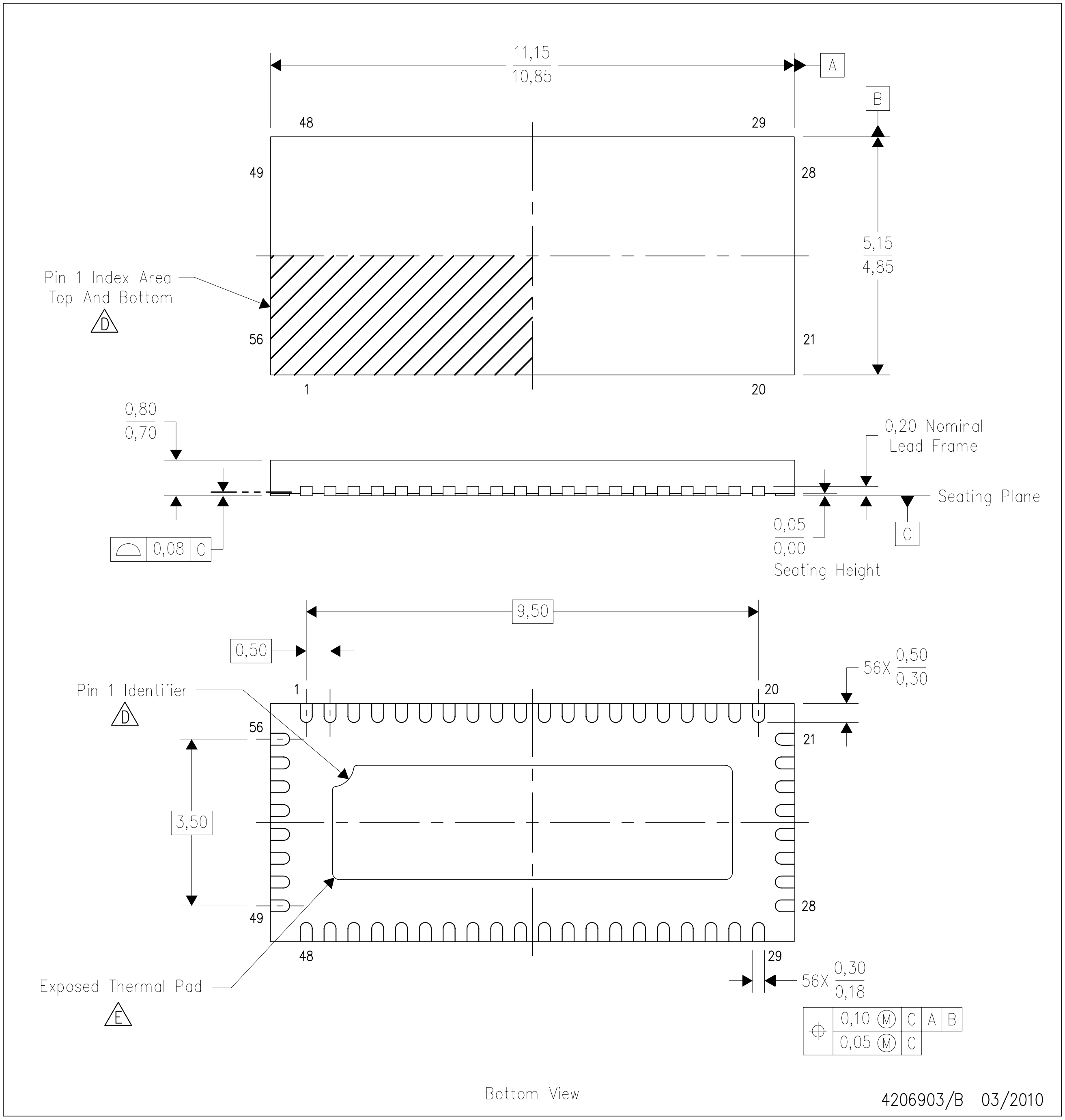
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3L500RHUR	WQFN	RHU	56	2000	346.0	346.0	35.0

RHU (R-PWQFN-N56) PLASTIC QUAD FLATPACK NO-LEAD



Notes:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- E. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- F. JEDEC MO–220 package registration is pending.

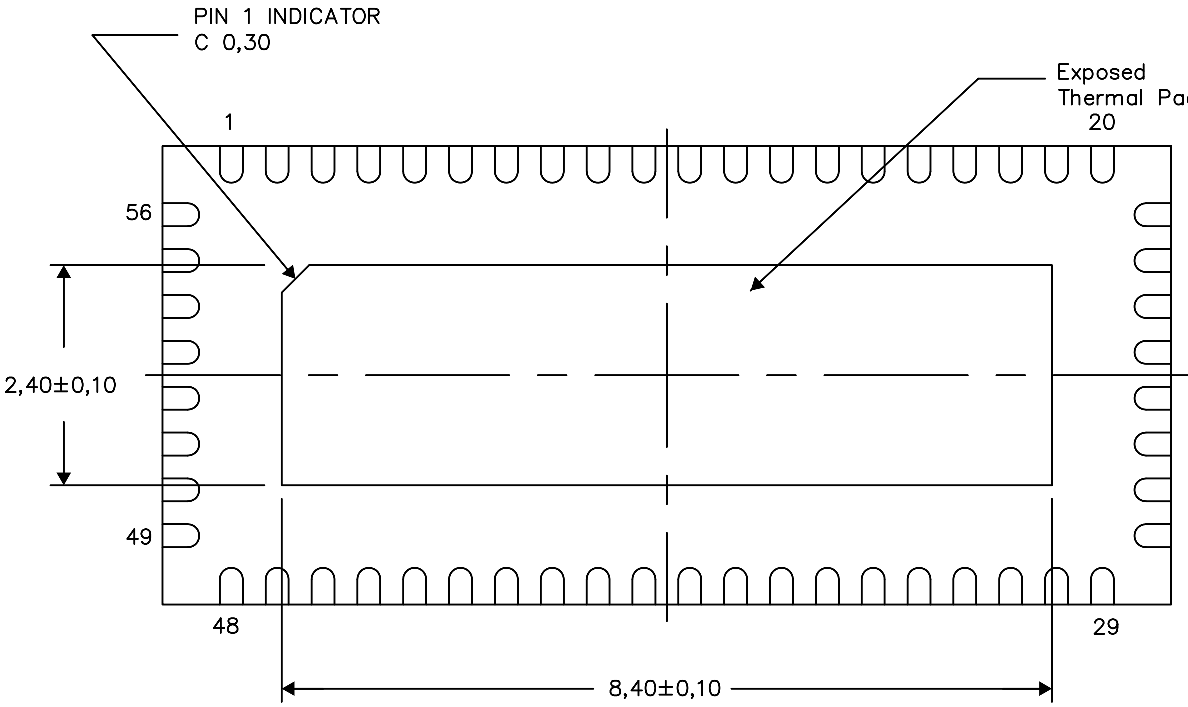
RHU (R–PWQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



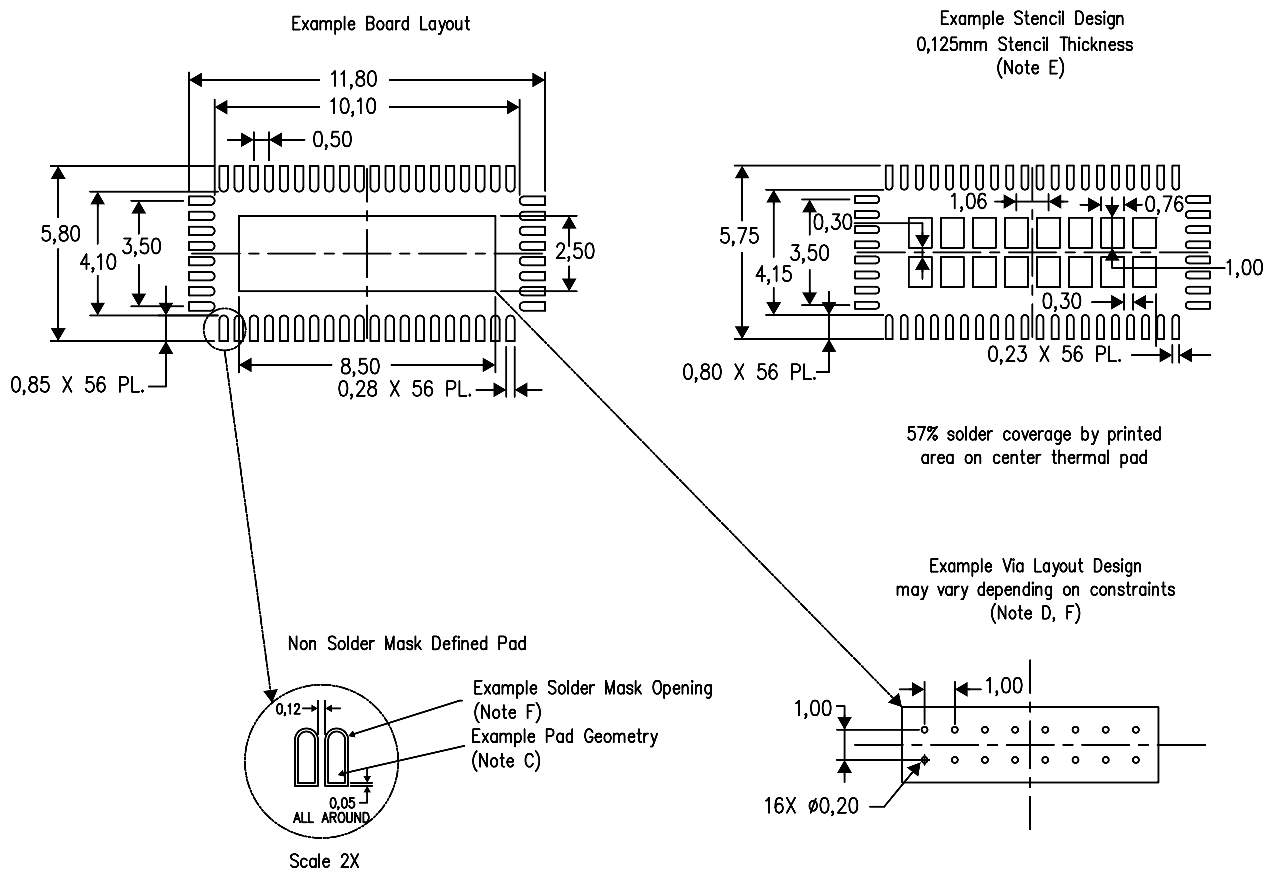
Bottom View

Exposed Thermal Pad Dimensions

4206904/E 12/12

NOTE: All linear dimensions are in millimeters

RHU (R–PWQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



4208257/D 12/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

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