0.9-Ω DUAL SPST ANALOG SWITCH
5-V/3.3-V 2-CHANNEL ANALOG SWITCH

Check for Samples: TS5A23167

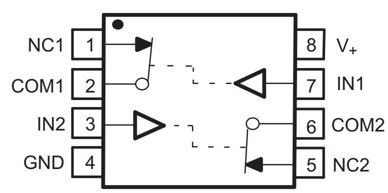
FEATURES

- Isolation in Powered-Off Mode, $V_+ = 0$
- Low ON-State Resistance (0.9 Ω)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model(A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

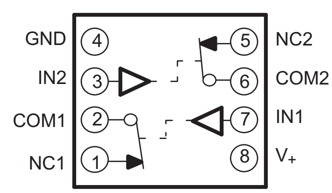
APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals

SSOP OR VSSOP PACKAGE
(TOP VIEW)



YZP PACKAGE
(BOTTOM VIEW)



DESCRIPTION/ORDERING INFORMATION

The TS5A23167 is a dual single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	TS5A23167YZPR	J87
	SSOP – DCT	Tape and reel	TS5A23167DCTR	JAP_
	VSSOP – DCU (Pb-free)	Tape and reel	TS5A23167DCUR	JAP_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The acutal top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

SUMMARY OF CHARACTERISTICS(1)

Configuration	Dual Single Pole Single Throw (2 × SPST)
Number of channels	2
ON-state resistance (r_{on})	0.9 Ω
ON-state resistance match (Δr_{on})	0.1 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.25 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	7.5 ns/9 ns
Charge injection (Q_C)	6 pC
Bandwidth (BW)	150 MHz
OFF isolation (O_{ISO})	–62 dB at 1 MHz
Crosstalk (X_{TALK})	–85 dB at 1 MHz
Total harmonic distortion (THD)	0.005%
Leakage current ($I_{COM(OFF)}$)	±20 nA
Power-supply current (I_+)	0.1 μA
Package option	8-pin VSSOP
	8-pin YZP

(1) $V_+ = 5$ V, $T_A = 25°C$

FUNCTION TABLE

IN	NC TO COM, COM TO NC
L	ON
H	OFF

Absolute Maximum Ratings(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		–0.5	6.5	V
V_{NC} V_{COM}	Analog voltage range(3) (4) (5)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{COM} < 0	–50		mA
I_{NC} I_{COM}	On-state switch current	V_{NC}, V_{COM} = 0 to V_+	–200	200	mA
	On-state peak switch current(6)		–400	400	
V_I	Digital input voltage range(3) (4)		–0.5	6.5	V
I_{IK}	Digital clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
θ_{JA}	Package thermal impedance(7)	DCT package		220	°C/W
		DCU package		227	
		YZP package		102	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle.
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 5-V Supply(1)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.9	1.1	Ω
				Full				1.2	
ON-state resistance	r_{on}	V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.75	0.9	Ω
				Full				1	
ON-state resistance match between channels	Δr_{on}	V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.04	0.1	Ω
				Full				0.1	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.2		Ω
		V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C			0.15	0.25	
				Full				0.25	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 4.5 V, or V_{NC} = 4.5 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	0 V	4	20	nA
				Full		–150		150	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–10	0.2	10	μA
				Full		–50		50	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 4.5 V, or V_{COM} = 4.5 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	0 V	4	20	nA
				Full		–150		150	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 5.5 V, V_{NC} = 5.5 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–10	0.2	10	μA
				Full		–50		50	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 4.5 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	5.5 V	–5	0.4	5	nA
				Full		–50		50	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 4.5 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	5.5 V	–5	0.4	5	nA
				Full		–50		50	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		2.4		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 5-V Supply(1) (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	1	4.5	7.5	ns
				Full	4.5 V to 5.5 V	1		9	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	4.5	8	11	ns
				Full	4.5 V to 5.5 V	3.5		13	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0 ,	C_L = 1 nF, See Figure 21	25°C	5 V		6		pC
NC OFF capacitance	$C_{NC(OFF)}$	V_{NC} = V_+ or GND, Switch OFF,	See Figure 16	25°C	5 V		19		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 16	25°C	5 V		18		pF
NC ON capacitance	$C_{NC(ON)}$	V_{NC} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		35.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		35.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	5 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	5 V		150		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	5 V		–62		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 20	25°C	5 V		–85		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	5 V		0.005		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.1	μA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 3.3-V Supply(1)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		1.3	1.6	Ω
				Full				1.8	
ON-state resistance	r_{on}	V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		1.1	1.5	Ω
				Full				1.7	
ON-state resistance match between channels	Δr_{on}	V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		0.04	0.1	Ω
				Full				0.1	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		0.3		Ω
		V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C			0.15	0.25	
				Full				0.25	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 3 V, or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–5	0.5	5	nA
				Full		–50		50	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–5	0.1	5	µA
				Full		–25		25	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 3 V, or V_{COM} = 3 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–5	0.5	5	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 3.6 V, V_{NC} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–5	0.1	5	µA
				Full		–25		25	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 3 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		2		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 3.3-V Supply(1) (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	1.5	5	9.5	ns
				Full	3 V to 3.6 V	1.0		10	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	4.5	8.5	11	ns
				Full	3 V to 3.6 V	3		12.5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 21	25°C	3.3 V		6		pC
NC OFF capacitance	$C_{NC(OFF)}$	$V_{NC} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		18.5		pF
NC ON capacitance	$C_{NC(ON)}$	$V_{NC} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		36		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		36		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	3.3 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	3.3 V		150		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	3.3 V		–62		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 20	25°C	3.3 V		–85		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	3.3 V		0.01		%
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V		0.001	0.05	μA
				Full				0.3	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 2.5-V Supply(1)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}				2.3 V	0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		1.8	2.4	Ω
				Full				2.6	
ON-state resistance	r_{on}	V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		1.2	2.1	Ω
				Full				2.4	
ON-state resistance match between channels	Δr_{on}	V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.04	0.15	Ω
				Full				0.15	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.7		Ω
		V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C			0.4	0.6	
				Full				0.6	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 3 V, or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	2.7 V	–5	0.3	5	nA
				Full		–50		50	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–2	0.05	2	µA
				Full		–15		15	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 3 V, or V_{COM} = 3 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	2.7 V	–5	0.3	5	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 3.6 V, V_{NC} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–2	0.05	2	µA
				Full		–15		15	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 3 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1.8		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 2.5-V Supply(1) (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	4.5	8	12.5	ns
				Full	2.3 V to 2.7 V	3		15	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 21	25°C	2.5 V		4		pC
NC OFF capacitance	$C_{NC(OFF)}$	V_{NC} = V_+ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		18.5		pF
NC ON capacitance	$C_{NC(ON)}$	V_{NC} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		36.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		36.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	2.5 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	2.5 V		150		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	2.5 V		–62		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 20	25°C	3.3 V		–85		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	2.5 V		0.02		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		0.001	0.02	μA
				Full				0.25	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 1.8-V Supply(1)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted))

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		4.2	25	Ω
				Full				30	
ON-state resistance	r_{on}	V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		1.6	3.9	Ω
				Full				4.0	
ON-state resistance match between channels	Δr_{on}	V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		0.04	0.2	Ω
				Full				0.2	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NC} \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		2.8		Ω
		V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C			4.1	22	
				Full				27	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 3 V, or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	–5		5	nA
				Full		–50		50	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–2		2	μA
				Full		–10		10	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 3 V, or V_{COM} = 3 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	–5		5	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 3.6 V, V_{NC} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	–2		2	μA
				Full		–10		10	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–2		2	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 3 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–2		2	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1.5		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 1.8-V Supply[1] (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted))

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	1.8 V	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	1.8 V	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 21	25°C	1.8 V		2		pC
NC OFF capacitance	$C_{NC(OFF)}$	$V_{NC} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		18.5		pF
NC ON capacitance	$C_{NC(ON)}$	$V_{NC} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		36.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		36.5		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	1.8 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	1.8 V		150		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	1.8 V		–62		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 20	25°C	1.8 V		–85		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz See Figure 22	25°C	1.8 V		0.055		%
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V		0.001	0.01	µA
				Full				0.15	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

TYPICAL PERFORMANCE

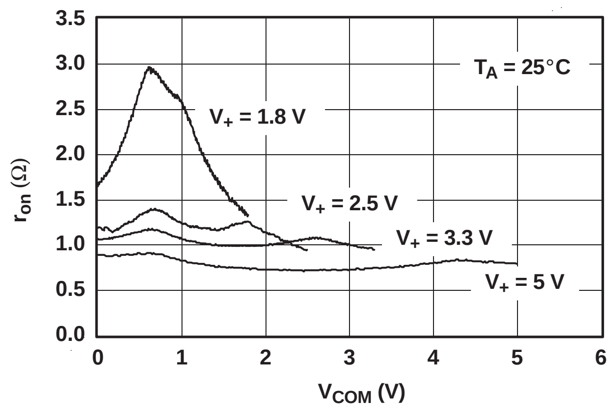


Figure 1. r_{on} **vs** V_{COM}

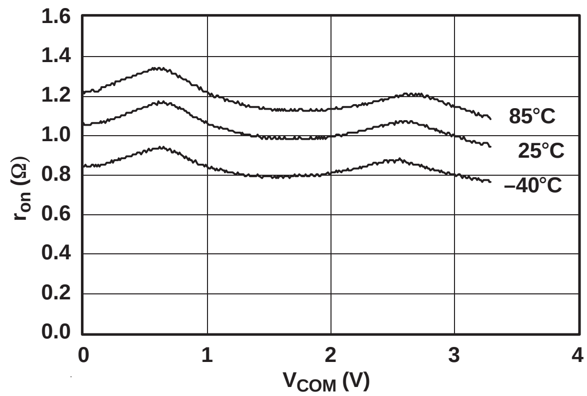


Figure 2. r_{on} **vs** V_{COM} **(V_+ = 3.3 V)**

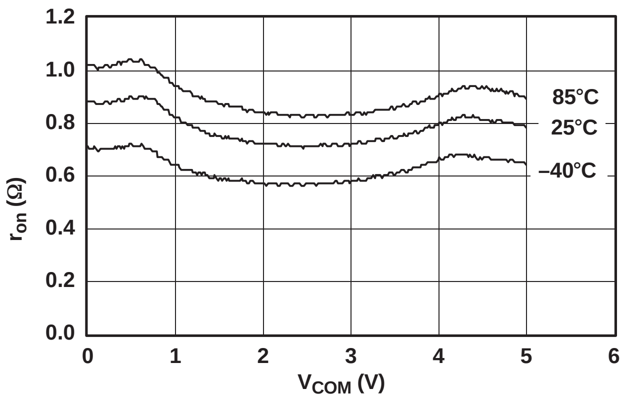


Figure 3. r_{on} **vs** V_{COM} **(V_+ = 5 V)**

TYPICAL PERFORMANCE

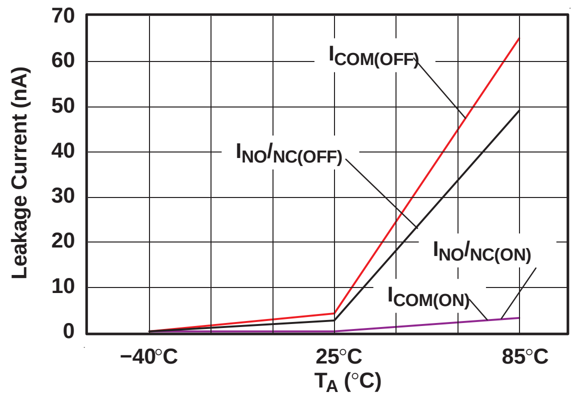


Figure 4. Leakage Current vs Temperature (V_+ = 5 V)

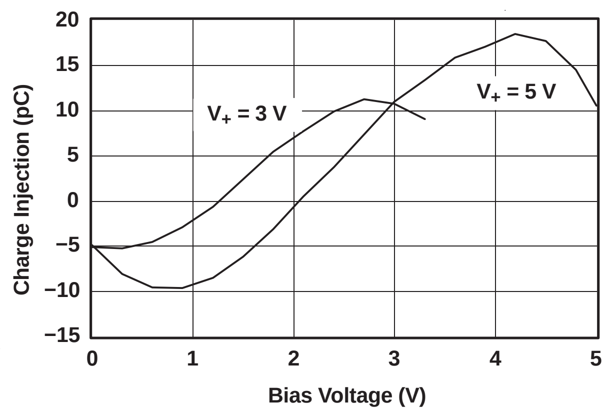


Figure 5. Charge Injection (Q_C) vs V_{COM}

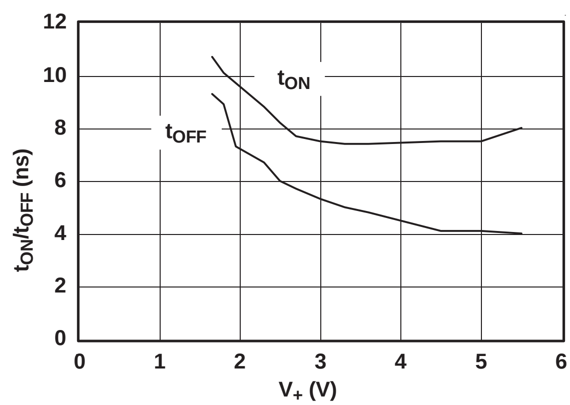


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

TYPICAL PERFORMANCE

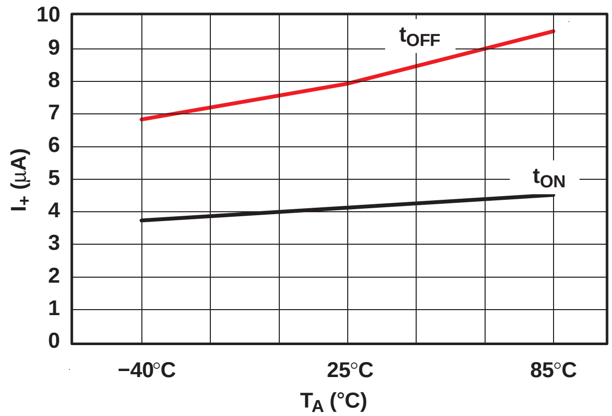


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

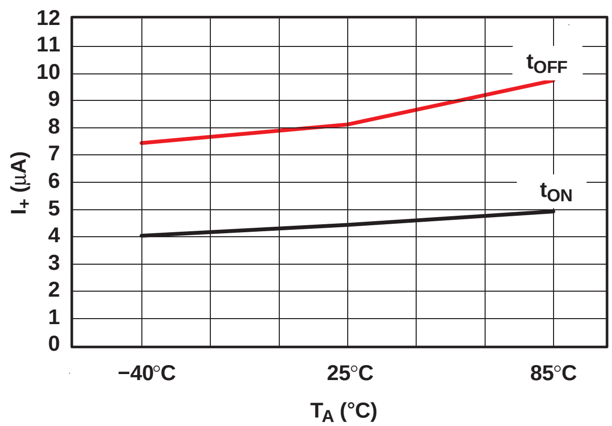


Figure 8. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

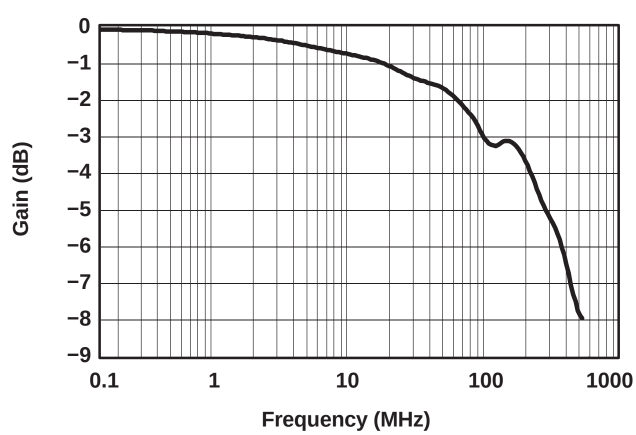


Figure 9. Bandwidth (Gain vs Frequency) (V_+ = 5 V)

TYPICAL PERFORMANCE

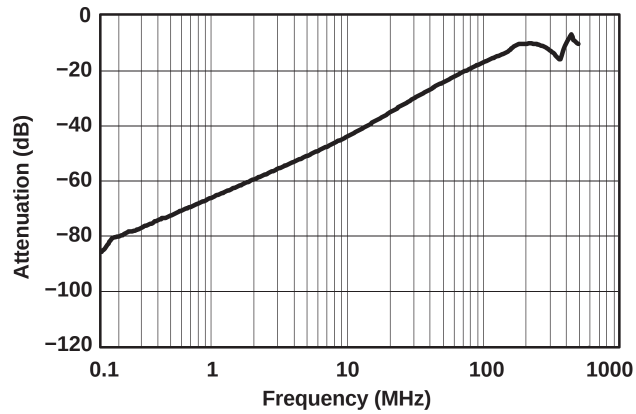


Figure 10. OFF Isolation vs Frequency

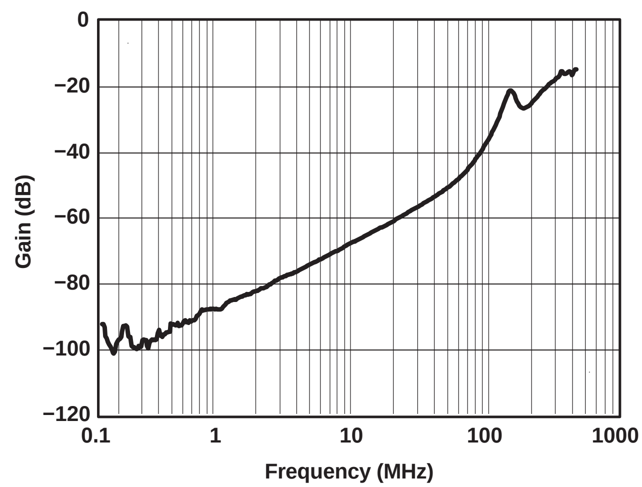


Figure 11. Gain vs Frequency

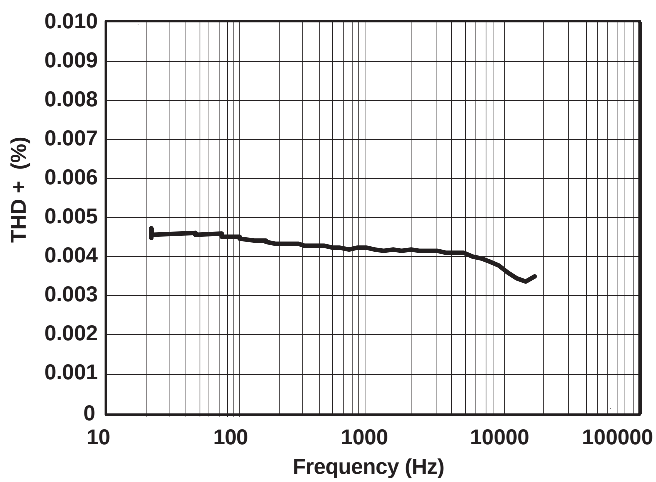


Figure 12. Total Harmonic Distortion vs Frequency (V_+ = 5 V)

TYPICAL PERFORMANCE

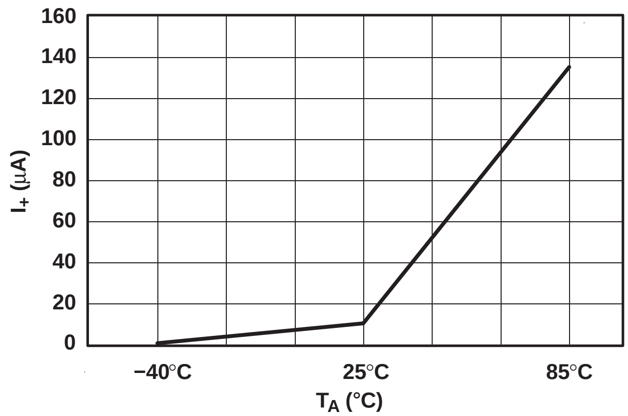


Figure 13. Power-Supply Current vs Temperature (V_+ = 5 V)

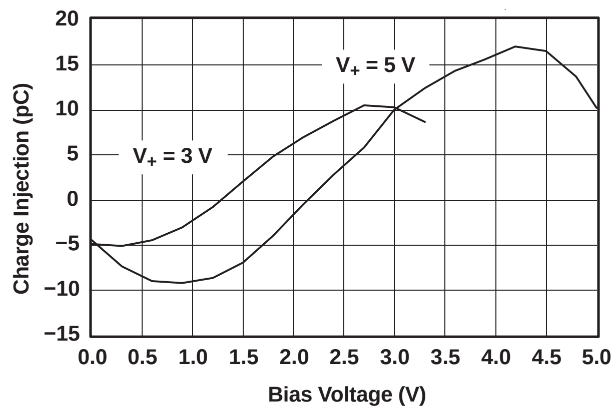


Figure 14. Charge Injection (Q_C) vs V_{COM}

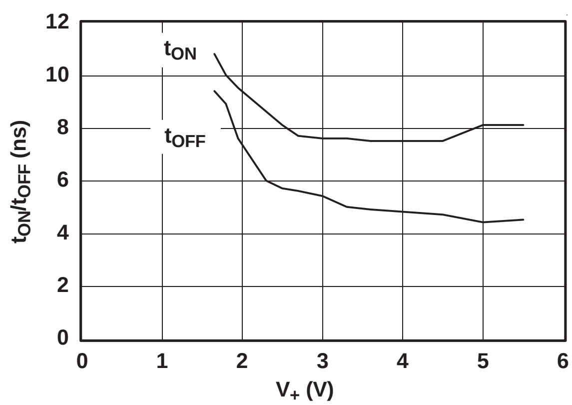


Figure 15. t_{ON} and t_{OFF} vs Supply Voltage

Table 1. PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	NC1	Normally closed
2	COM1	Common
3	IN2	Digital control pin to connect COM to NC
4	GND	Digital ground
5	NC2	Normally closed
6	COM2	Common
7	IN1	Digital control pin to connect COM to NC
8	V_+	Power Supply

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
r_{on}	Resistance between COM and NC ports when the channel is ON
r_{peak}	Peak on-state resistance over a specified voltage range
$r_{on\Delta}$	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-down condition, $V_+ = 0$
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC) in the OFF state under worst-case input and output conditions
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC) in the ON state and the output (NC) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NC) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NC) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance, and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

PARAMETER MEASUREMENT INFORMATION

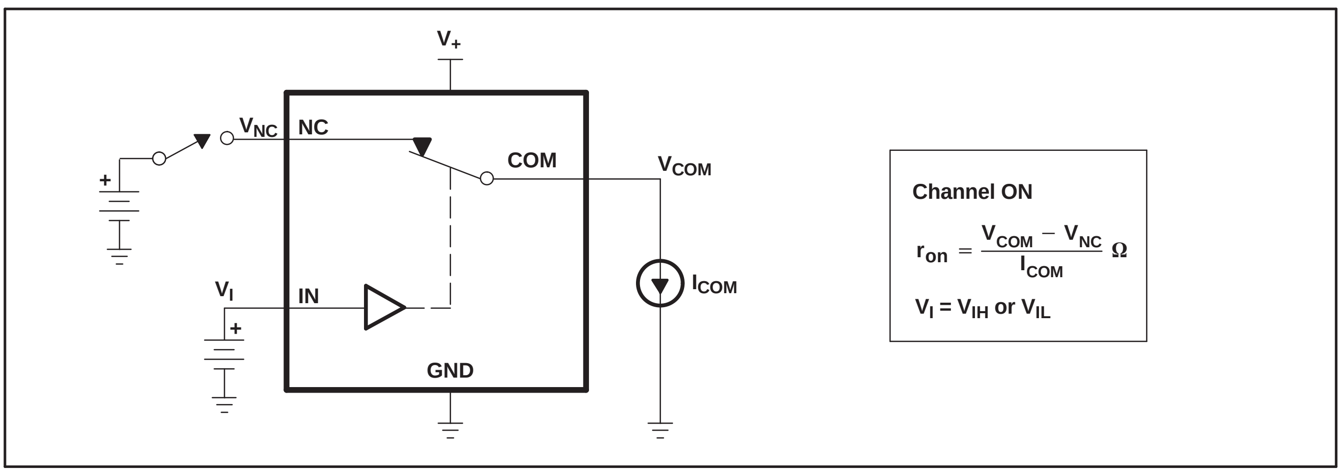


Figure 16. ON-State Resistance (r_{on})

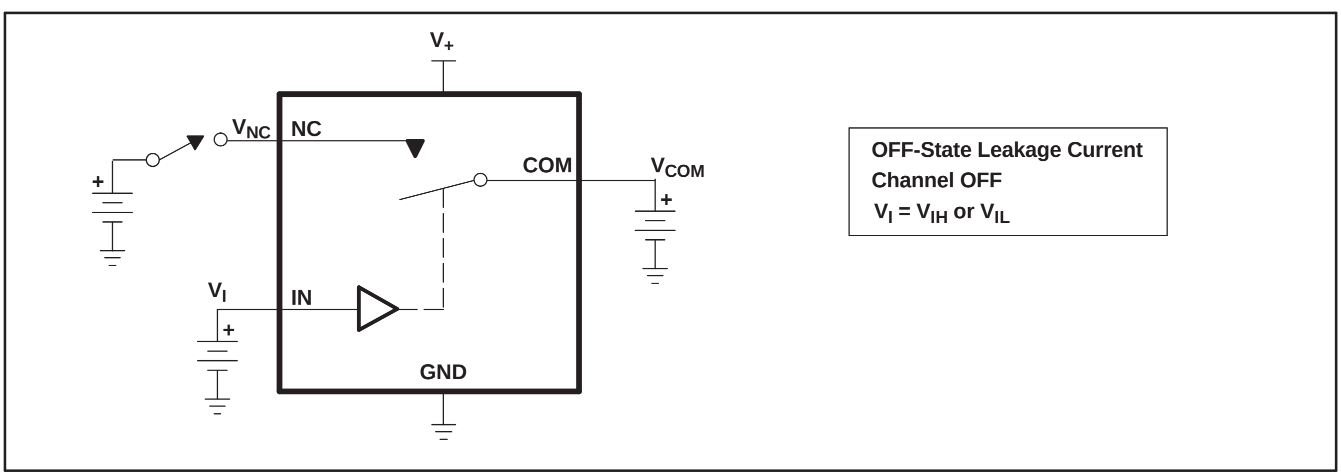


Figure 17. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWR(FF)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

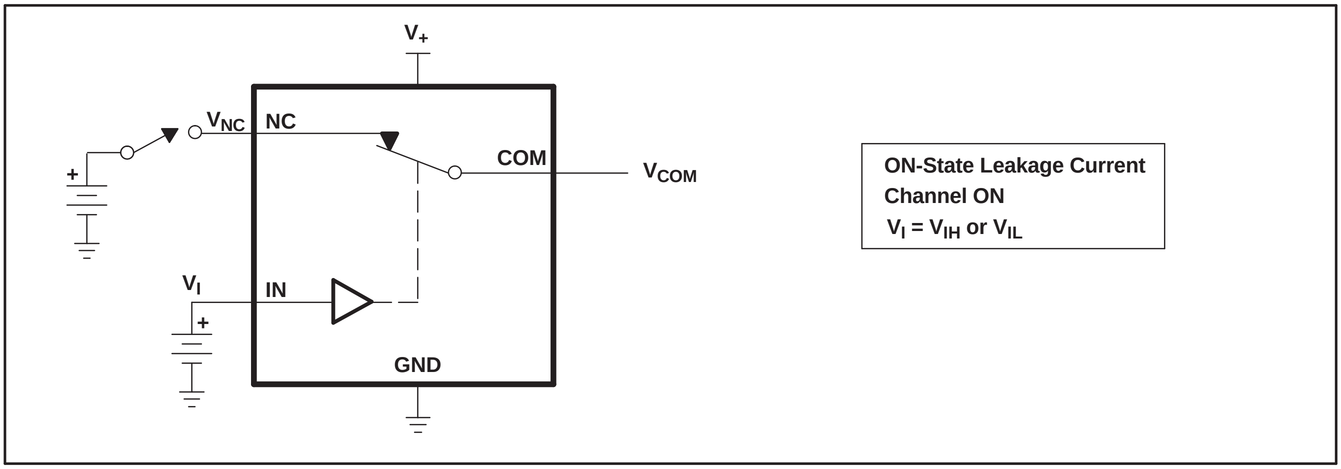


Figure 18. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

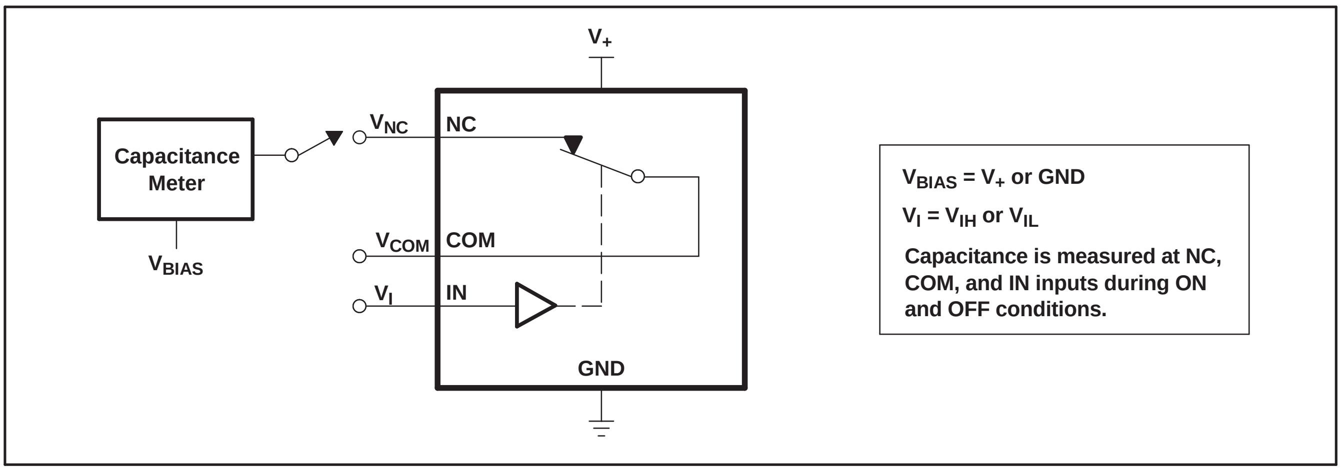
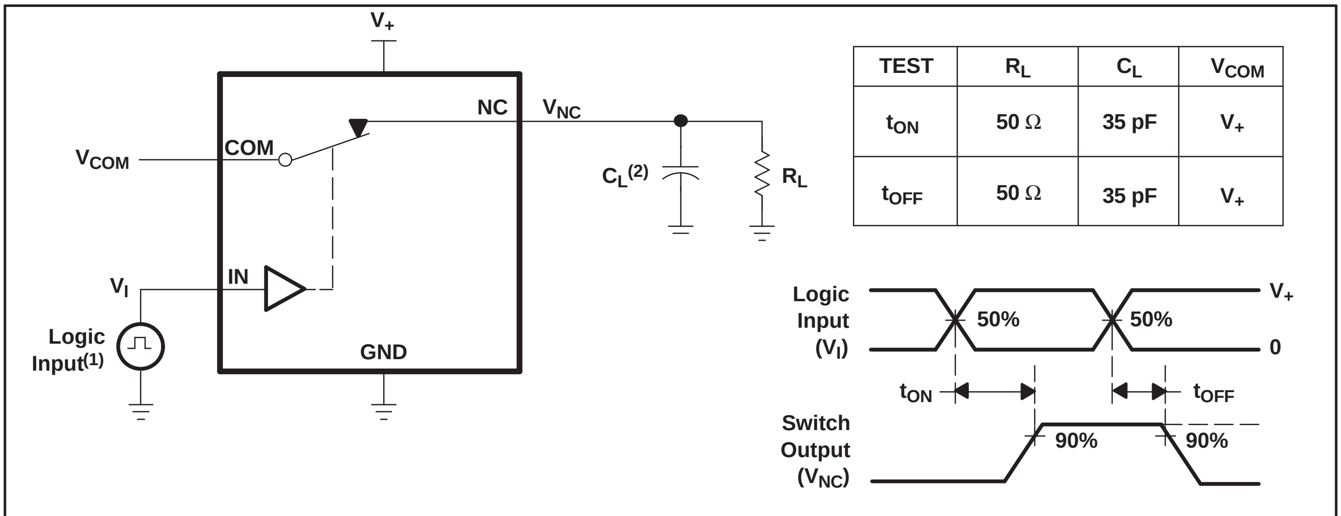


Figure 19. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V+
t_{OFF}	50 Ω	35 pF	V+

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 20. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

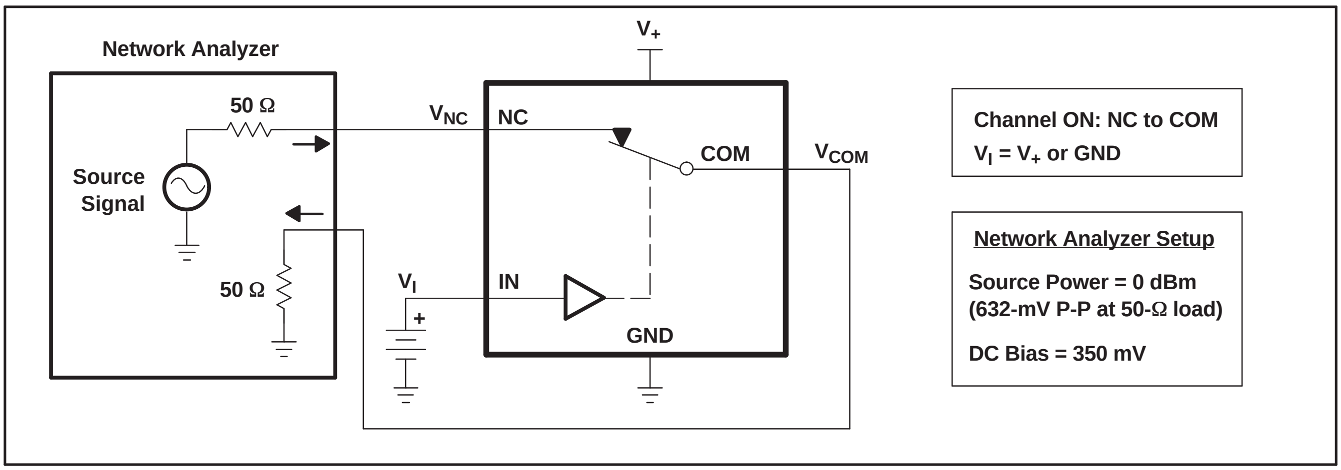


Figure 21. Bandwidth (BW)

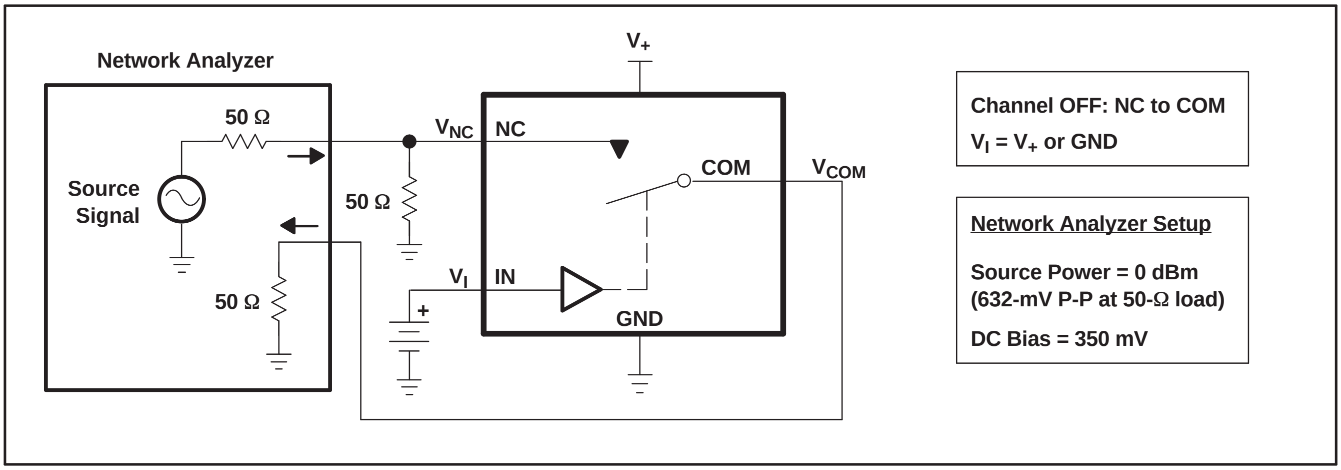


Figure 22. OFF Isolation (O_{ISO})

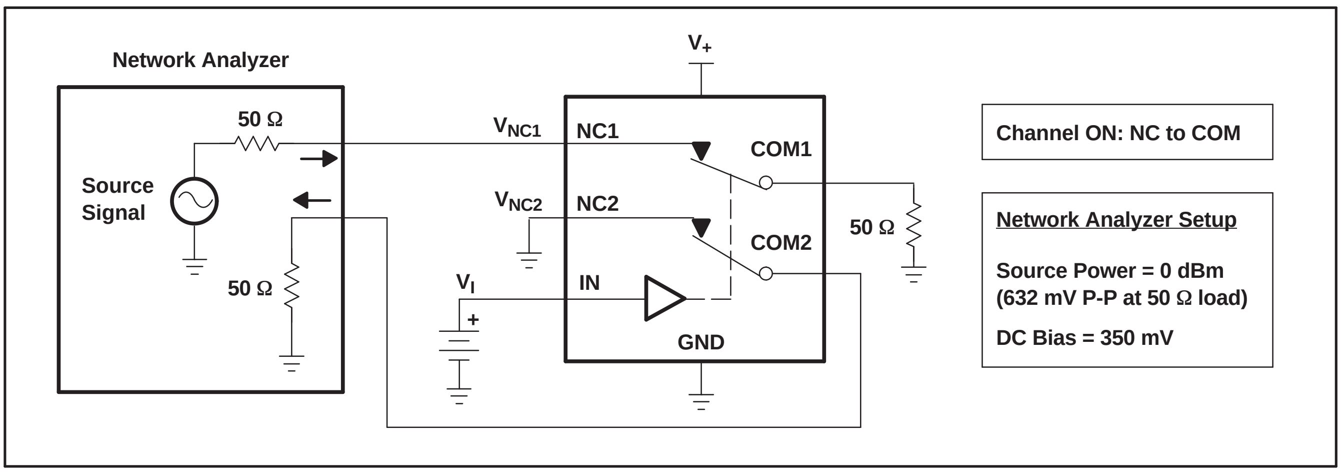
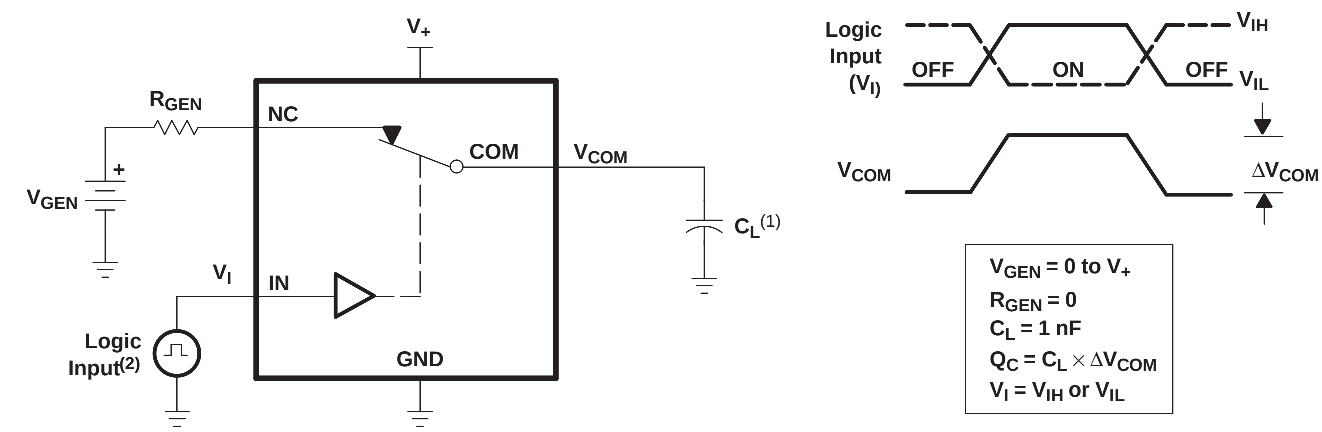
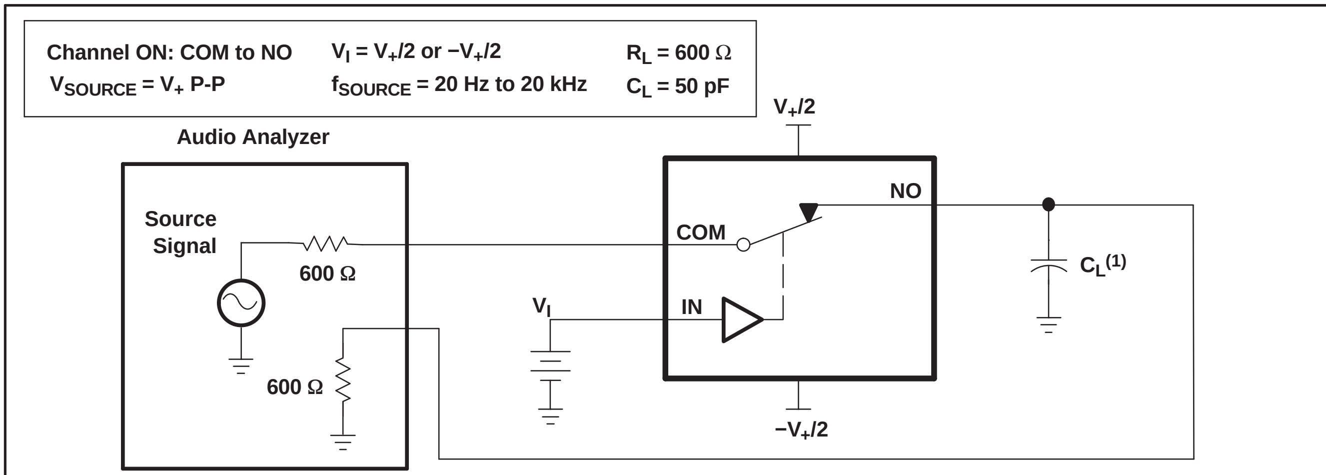


Figure 23. Crosstalk (X_{TALK})



(1) C_L includes probe and jig capacitance.
(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 24. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 25. Total Harmonic Distortion (THD)

REVISION HISTORY

Changes from Revision #IMPLIED (May 2005) to Revision A	Page
• Updated package options information.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TS5A23167DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAPR	Samples
TS5A23167DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAPR	Samples
TS5A23167DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAPR	Samples
TS5A23167YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	J87	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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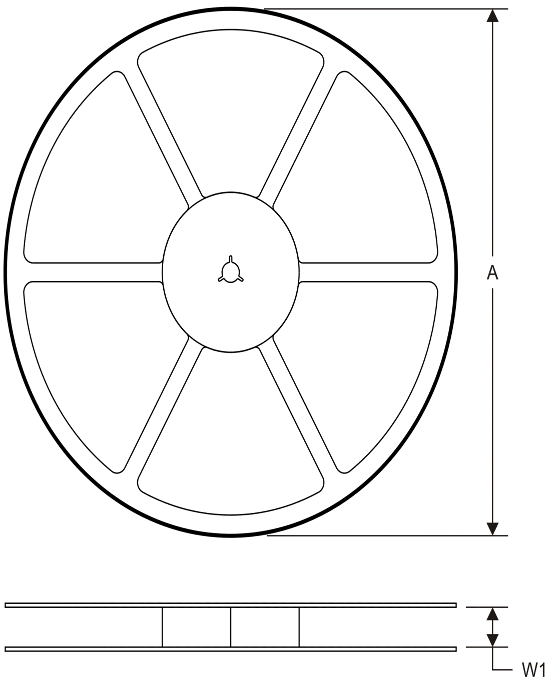
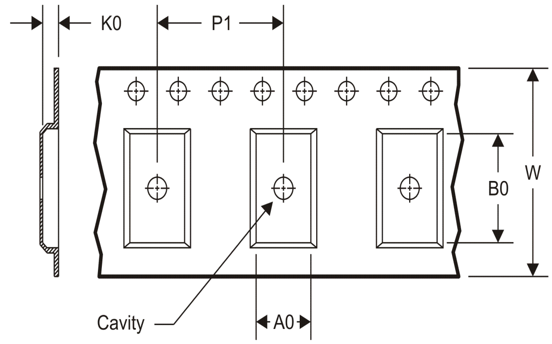
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



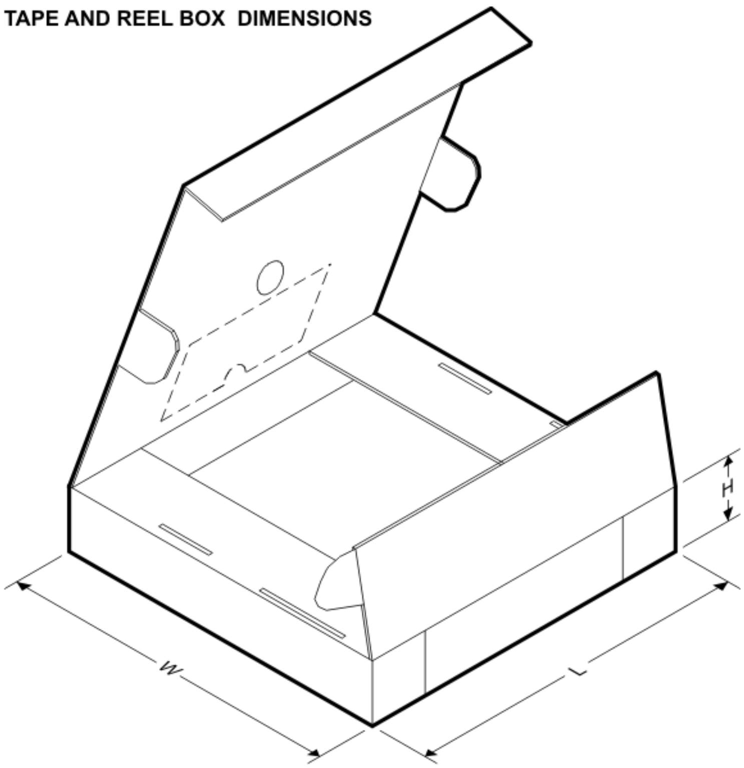
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23167DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A23167YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

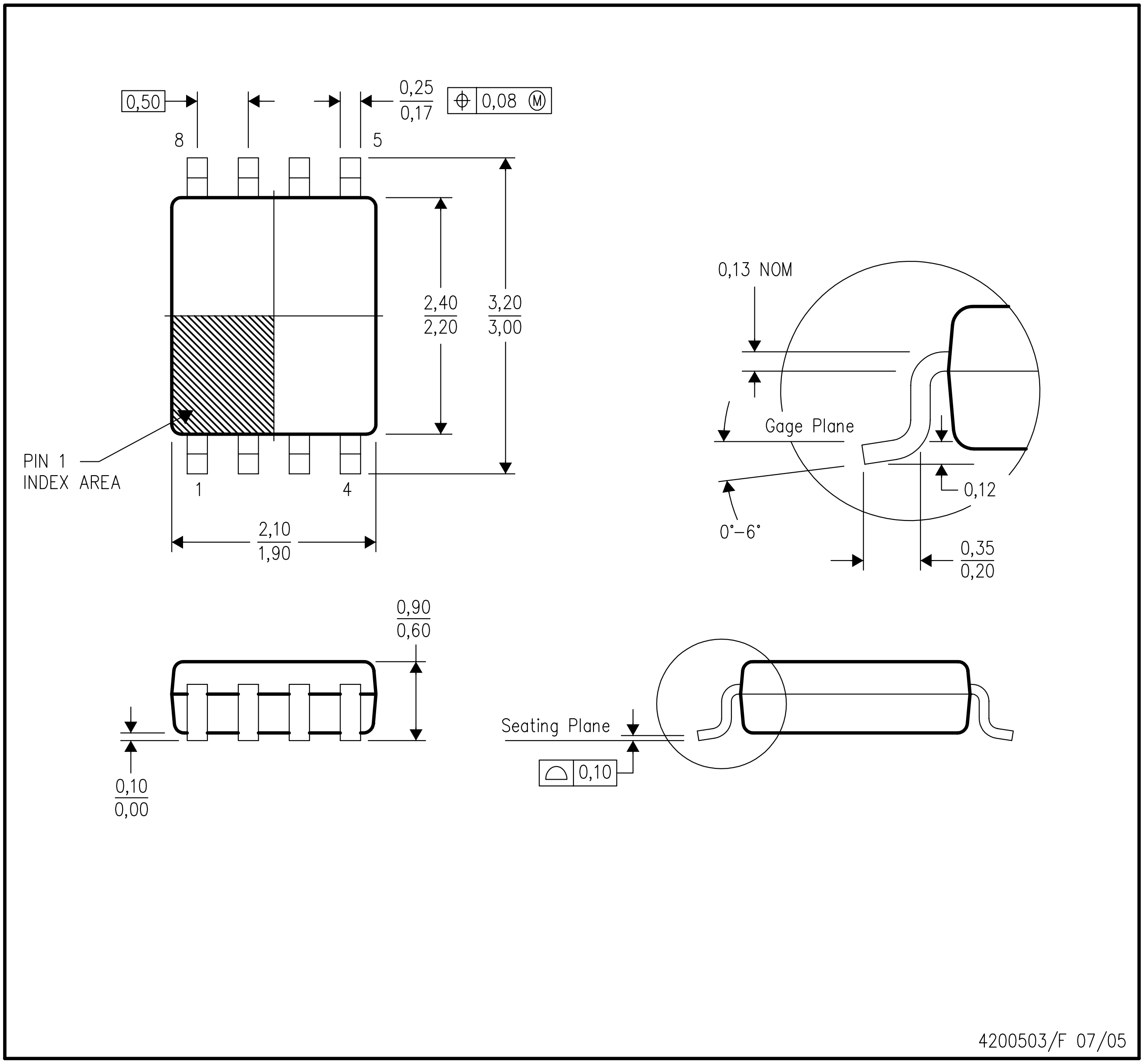
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

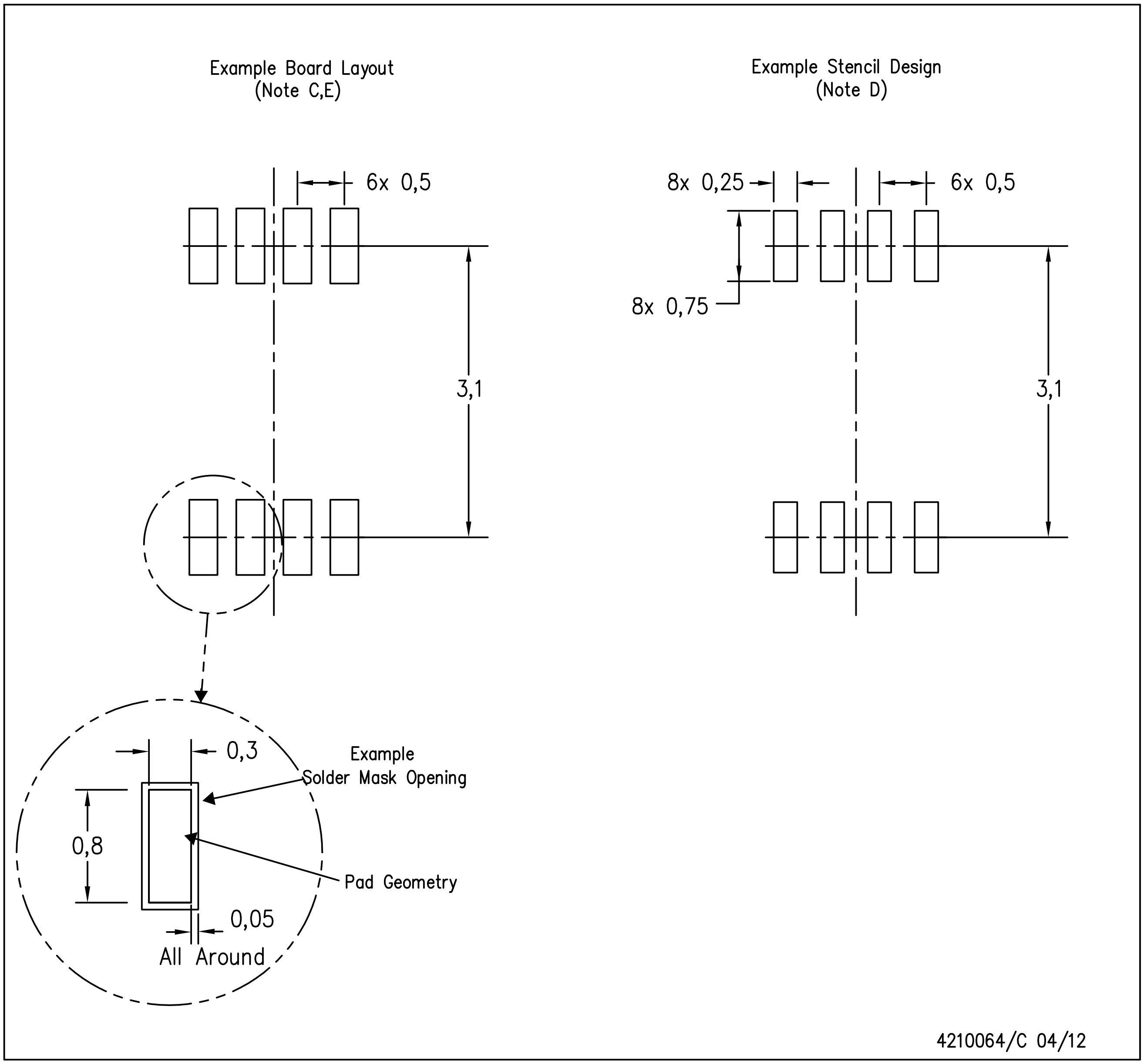
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23167DCUR	US8	DCU	8	3000	202.0	201.0	28.0
TS5A23167YZPR	DSBGA	YZP	8	3000	220.0	220.0	34.0

DCU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



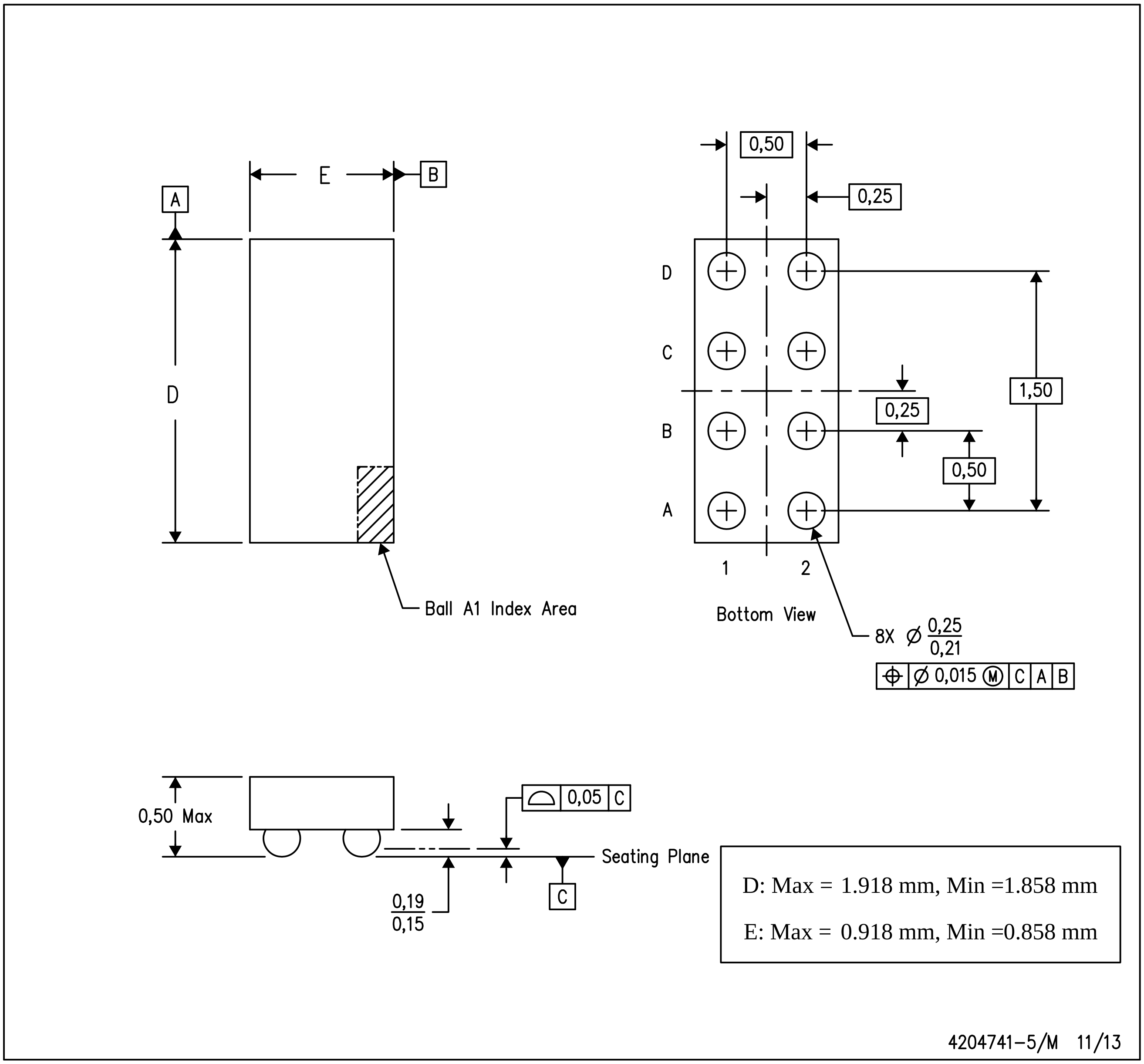
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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