

## Description

The TS5A4594 is a single-pole single-throw (SPST) analog switch that is designed to operate from 2 V to 5.5 V. This device can handle both digital and analog signals, and signals up to  $V_+$  can be transmitted in either direction.

## Applications

- Sample-and-Hold Circuits
- Battery-Powered Equipment (Cellular Phones, PDAs)
- Audio and Video Signal Routing
- Communication Circuits
- PCMCIA Cards

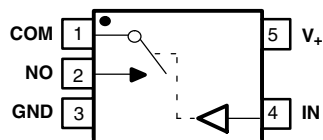
## Features

- Low ON-State Resistance (8 Ω)
- ON-State Resistance Flatness (1.5 Ω)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection (5 pC Max)
- 450-MHz –3-dB Bandwidth at 25°C
- Low Total Harmonic Distortion (THD) (0.04%)
- 2-V to 5.5-V Single-Supply Operation
- Specified at 5-V and 3.3-V Nodes
- –82-dB OFF-Isolation at 1 MHz
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- 0.5-nA Max OFF Leakage
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- TTL/CMOS-Logic Compatible

## Summary of Characteristics

$V_+ = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

SOT-23 OR SC-70 PACKAGE  
(TOP VIEW)



FUNCTION TABLE

IN	NO TO COM, COM TO NO
L	OFF
H	ON

Configuration	Single Pole Single Throw (SPST)
Number of channels	1
ON-state resistance ( $r_{on}$ )	8 Ω
ON-state resistance flatness ( $r_{on(Flat)}$ )	1.5 Ω
Turn-on/turn-off time ( $t_{ON}/t_{OFF}$ )	17 ns/14 ns
Charge injection ( $Q_C$ )	5 pC
Bandwidth (BW)	450 MHz
OFF isolation ( $O_{ISO}$ )	–82 dB at 1 MHz
Total harmonic distortion (THD)	0.04%
Leakage current ( $I_{COM(OFF)}/I_{NO(OFF)}$ )	±0.5 nA
Power-supply current ( $I_+$ )	0.25 μA
Package option	5-pin SOT-23 or SC-70

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	SOT (SOT-23) – DBV	Tape and reel	TS5A4594DBVR	JSA_
	SOT (SC-70) – DCK	Tape and reel	TS5A4594DCKR	JS_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.



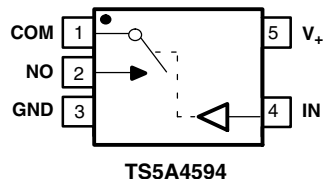
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# TS5A4594

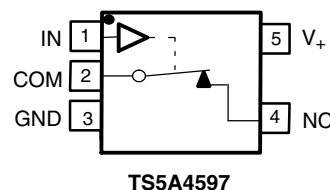
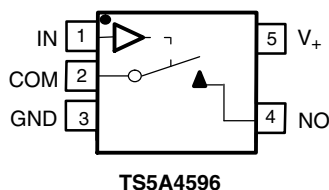
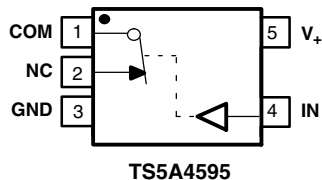
## SINGLE-CHANNEL 8-Ω SPST ANALOG SWITCH

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### Pin Configurations



#### Available in Other Pin Configurations



### Absolute Minimum and Maximum Ratings<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_+$	Supply voltage range <sup>(3)</sup>	-0.3	6	V
$V_{NO}$ $V_{COM}$	Analog voltage range <sup>(3)(4)</sup>	-0.3	$V_+ + 0.3$	V
$I_K$	Analog port diode current $V_{NO}, V_{COM} < 0$	-50		mA
$I_{NO}$ $I_{COM}$	On-state switch current $V_{NO}, V_{COM} = 0$ to $V_+$	-20	20	mA
$I_{NO}$ $I_{COM}$	On-state switch current (pulsed at 1 ms, 10% duty cycle) $V_{NO}, V_{COM} = 0$ to $V_+$	-40	40	mA
$V_I$	Digital input voltage range <sup>(3)(4)</sup>	-0.3	6	V
$I_{IK}$	Digital input clamp current $V_I < 0$	-50		mA
$I_+$	Continuous current through $V_+$		100	mA
$I_{GND}$	Continuous current through GND	-100		mA
$\theta_{JA}$	Package thermal impedance <sup>(5)</sup>	DBV package		206
		DCK package		252
$T_{stg}$	Storage temperature range	-65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(3) All voltages are with respect to ground, unless otherwise specified.

(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(5) The package thermal impedance is calculated in accordance with JESD 51-7.

## Electrical Characteristics for 5-V Supply<sup>(1)</sup>

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{IH} = 2.4\text{ V}$ ,  $V_{IL} = 0.8\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V
ON-state resistance	$r_{on}$	$V_{NO} = 3.5\text{ V}$ , $I_{COM} = 10\text{ mA}$ , Switch ON, See Figure 13	25°C Full	4.5 V		5	8 10	Ω
ON-state resistance flatness	$r_{on(flat)}$	$V_{NO} = 1.5\text{ V}, 2.5\text{ V}, 3.5\text{ V}$ , $I_{COM} = 10\text{ mA}$ , Switch ON, See Figure 13	25°C Full	4.5 V		0.5	1.5 2	Ω
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1\text{ V}, V_{COM} = 4.5\text{ V}$ , or $V_{NO} = 4.5\text{ V}, V_{COM} = 1\text{ V}$ , Switch OFF, See Figure 14	25°C Full	5.5 V	-0.5 -5	0.01	0.5 5	nA
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1\text{ V}, V_{NO} = 4.5\text{ V}$ , or $V_{COM} = 4.5\text{ V}, V_{NO} = 1\text{ V}$ , Switch OFF, See Figure 14	25°C Full	5.5 V	-0.5 -5	0.01	0.5 5	nA
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1\text{ V}, V_{COM} = 1\text{ V}$ , or $V_{NO} = 4.5\text{ V}, V_{COM} = 4.5\text{ V}$ , or $V_{NO} = 1\text{ V}, 4.5\text{ V}, V_{COM} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	5.5 V	-1 -10	0.01	1 10	nA
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}, V_{NO} = 1\text{ V}$ , or $V_{COM} = 4.5\text{ V}, V_{NO} = 4.5\text{ V}$ , or $V_{COM} = 1\text{ V}, 4.5\text{ V}, V_{NO} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	5.5 V	-1 -10	0.01	1 10	nA
<b>Digital Control Input (IN)</b>								
Input logic high	$V_{IH}$		Full		2.4		5.5	V
Input logic low	$V_{IL}$		Full		0		0.8	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = V_+ \text{ or } 0$	25°C Full	5 V	-0.5 -5	0.01	0.5 5	μA

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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### Electrical Characteristics for 5-V Supply<sup>(1)</sup> (continued)

$V_+ = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t <sub>ON</sub>	V <sub>NO</sub> = 3 V, R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF, See Figure 17		25°C	5 V		12	17	ns
				Full	4.5 V to 5.5 V		19		
Turn-off time	t <sub>OFF</sub>	V <sub>COM</sub> = 3 V, R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF, See Figure 17		25°C	5 V		9	14	ns
				Full	4.5 V to 5.5 V		17		
Charge injection	Q <sub>C</sub>	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0 C <sub>L</sub> = 1 nF, See Figure 20		25°C	5 V		2	5	pC
NO OFF capacitance	C <sub>NO(OFF)</sub>	V <sub>NO</sub> = 0 V, f = 1 MHz Switch OFF, See Figure 16		25°C	5 V		6.5		pF
COM OFF capacitance	C <sub>COM(OFF)</sub>	V <sub>COM</sub> = 0 V, f = 1 MHz, Switch OFF, See Figure 16		25°C	5 V		6.5		pF
NO ON capacitance	C <sub>NO(ON)</sub>	V <sub>NO</sub> = 0 V, f = 1 MHz, Switch ON, See Figure 16		25°C	5 V		13		pF
COM ON capacitance	C <sub>COM(ON)</sub>	V <sub>COM</sub> = 0 V, f = 1 MHz, Switch ON, See Figure 16		25°C	5 V		13		pF
Digital input capacitance	C <sub>I</sub>	V <sub>I</sub> = 0 V, See Figure 16		25°C	5 V		3		pF
Bandwidth	BW	R <sub>L</sub> = 50 Ω, Signal = 0 dBm, Switch ON, See Figure 18		25°C	5 V		450		MHz
OFF isolation	O <sub>ISO</sub>	R <sub>L</sub> = 50 Ω, V <sub>NO</sub> = 1 V <sub>RMS</sub> f = 1 MHz, C <sub>L</sub> = 5 pF Switch OFF, See Figure 19		25°C	5 V		−82		dB
Total harmonic distortion	THD	R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF, V <sub>SOURCE</sub> = 5 V <sub>p-p</sub> , f = 20 Hz to 20 kHz, See Figure 21		25°C	5 V		0.04		%
Supply									
Positive supply current	I <sub>+</sub>	V <sub>I</sub> = V <sub>+</sub> or GND, Switch ON or OFF		25°C	5.5 V		0.01	0.25	μA
				Full	5.5 V		1		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

## Electrical Characteristics for 3-V Supply<sup>(1)</sup>

$V_+ = 2.7 \text{ V to } 3.6 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{\text{COM}}, V_{\text{NO}}$				0		$V_+$	V
ON-state resistance	$r_{\text{on}}$	$V_{\text{NO}} = 1.5 \text{ V}$ , $I_{\text{COM}} = 10 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	2.7 V		9.5	16 20	Ω
ON-state resistance flatness	$r_{\text{on(flat)}}$	$V_{\text{NO}} = 1.5 \text{ V}, 2.5 \text{ V}$ , $I_{\text{COM}} = 10 \text{ mA}$ , Switch ON, See Figure 13	25°C Full	2.7 V		1.8	6 7	Ω
NO OFF leakage current	$I_{\text{NO(OFF)}}$	$V_{\text{NO}} = 1 \text{ V}, V_{\text{COM}} = 3 \text{ V}$ , or $V_{\text{NO}} = 3 \text{ V}, V_{\text{COM}} = 1 \text{ V}$ , Switch OFF, See Figure 14	25°C Full	3.6 V	-0.5 -5	0.01	0.5 5	nA
COM OFF leakage current	$I_{\text{COM(OFF)}}$	$V_{\text{COM}} = 1 \text{ V}, V_{\text{NO}} = 3 \text{ V}$ , or $V_{\text{COM}} = 3 \text{ V}, V_{\text{NO}} = 1 \text{ V}$ , Switch OFF, See Figure 14	25°C Full	3.6 V	-0.5 -5	0.01	0.5 5	nA
NO ON leakage current	$I_{\text{NO(ON)}}$	$V_{\text{NO}} = 1 \text{ V}, V_{\text{COM}} = 1 \text{ V}$ , or $V_{\text{NO}} = 3 \text{ V}, V_{\text{COM}} = 3 \text{ V}$ , or $V_{\text{NO}} = 1 \text{ V}, 3 \text{ V}, V_{\text{COM}} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	3.6 V	-1 -10	0.01	1 10	nA
COM ON leakage current	$I_{\text{COM(ON)}}$	$V_{\text{COM}} = 1 \text{ V}, V_{\text{NO}} = 1 \text{ V}$ , or $V_{\text{COM}} = 3 \text{ V}, V_{\text{NO}} = 3 \text{ V}$ , or $V_{\text{COM}} = 1 \text{ V}, 3 \text{ V}, V_{\text{NO}} = \text{Open}$ , Switch ON, See Figure 15	25°C Full	3.6 V	-1 -10	0.01	1 10	nA
<b>Digital Control Input (IN)</b>								
Input logic high	$V_{\text{IH}}$		Full		2		5.5	V
Input logic low	$V_{\text{IL}}$		Full		0		0.8	V
Input leakage current	$I_{\text{IH}}, I_{\text{IL}}$	$V_i = V_+ \text{ or } 0$	25°C Full	3.6 V	-0.5 -5	0.01	0.5 5	nA

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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### Electrical Characteristics for 3-V Supply<sup>(1)</sup> (continued)

$V_+ = 2.7 \text{ V to } 3.6 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t <sub>ON</sub>	V <sub>NO</sub> = 2 V, R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF, See Figure 17		25°C	3 V	20	30	ns	
				Full	2.7 V to 3.6 V		35		
Turn-off time	t <sub>OFF</sub>	V <sub>COM</sub> = 2 V, R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF, See Figure 17		25°C	3 V	15	25	ns	
				Full	2.7 V to 3.6 V		30		
Charge injection	Q <sub>C</sub>	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0, C <sub>L</sub> = 1 nF, See Figure 20		25°C	3 V	1	4	pC	
NO OFF capacitance	C <sub>NO(OFF)</sub>	V <sub>NO</sub> = 0 V, f = 1 MHz, Switch OFF, See Figure 16		25°C	3 V	6.5		pF	
COM OFF capacitance	C <sub>COM(OFF)</sub>	V <sub>COM</sub> = 0 V, f = 1 MHz, Switch OFF, See Figure 16		25°C	3 V	6.5		pF	
NO ON capacitance	C <sub>NO(ON)</sub>	V <sub>NO</sub> = 0 V, f = 1 MHz, Switch ON, See Figure 16		25°C	3 V	13		pF	
COM ON capacitance	C <sub>COM(ON)</sub>	V <sub>COM</sub> = 0 V, f = 1 MHz, Switch ON, See Figure 16		25°C	3 V	13		pF	
Digital input capacitance	C <sub>I</sub>	V <sub>I</sub> = 0 V, See Figure 16		25°C	3 V	3		pF	
Bandwidth	BW	R <sub>L</sub> = 50 Ω, Signal = 0 dBm Switch ON, See Figure 18		25°C	3 V	450		MHz	
OFF isolation	O <sub>ISO</sub>	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, V <sub>NO</sub> = 1 V <sub>RMS</sub> , Switch OFF, See Figure 19		25°C	3 V	−82		dB	
Total harmonic distortion	THD	R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF, V <sub>SOURCE</sub> = 3 V <sub>p-p</sub> , f = 20 Hz to 20 kHz, See Figure 21		25°C	3 V	0.09		%	
Supply									
Positive supply current	I <sub>+</sub>	V <sub>I</sub> = V <sub>+</sub> or GND, Switch ON or OFF		25°C	5.5 V	0.01	0.25	μA	
				Full			0.5		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

## TYPICAL PERFORMANCE

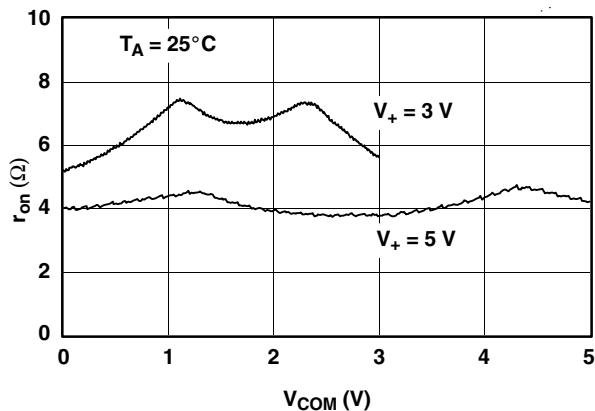


Figure 1.  $r_{on}$  vs  $V_{COM}$

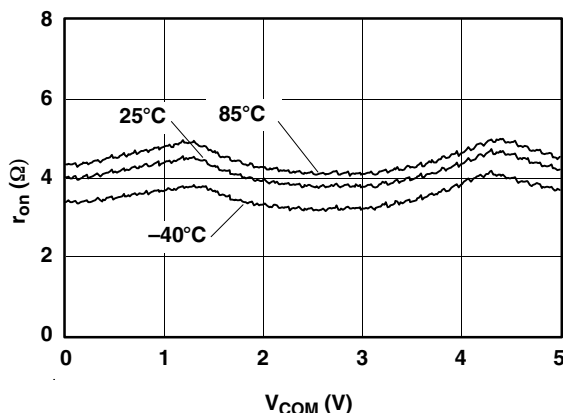


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 5V$ )

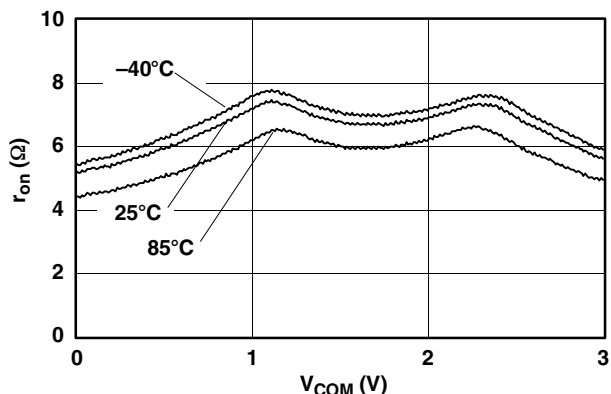


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3V$ )

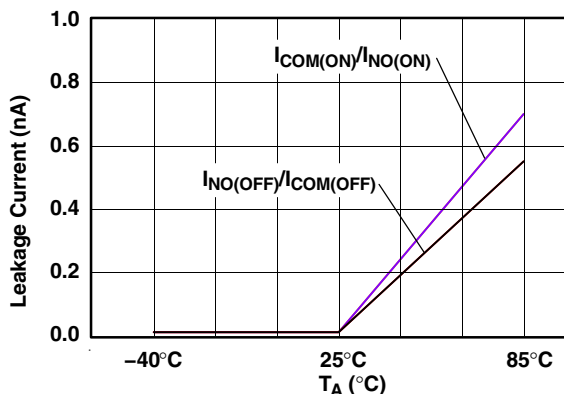


Figure 4. Leakage Current vs Temperature ( $V_+ = 5V$ )

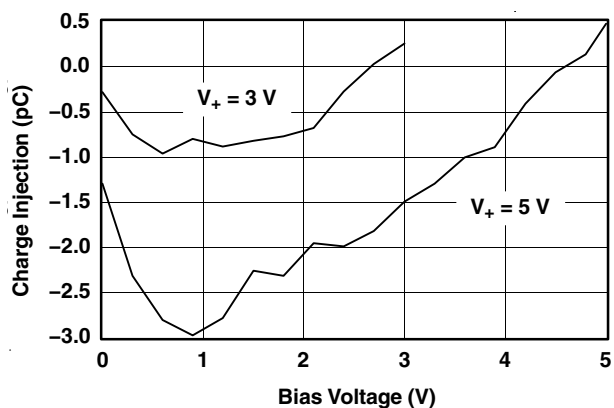


Figure 5. Charge-Injection ( $Q_C$ ) vs  $V_{COM}$

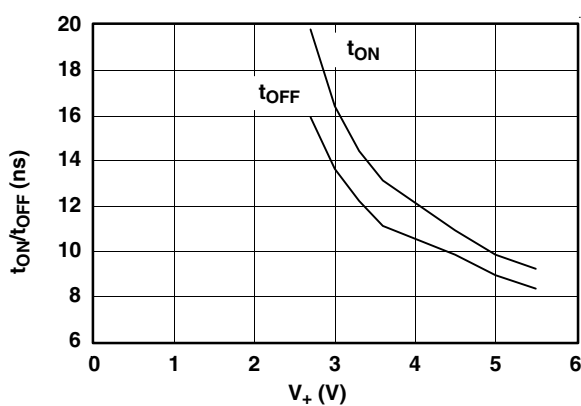
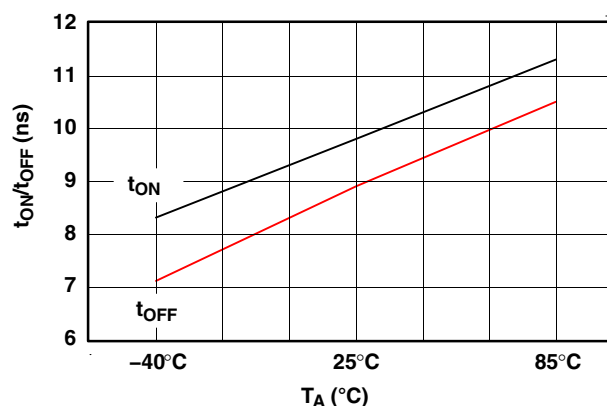
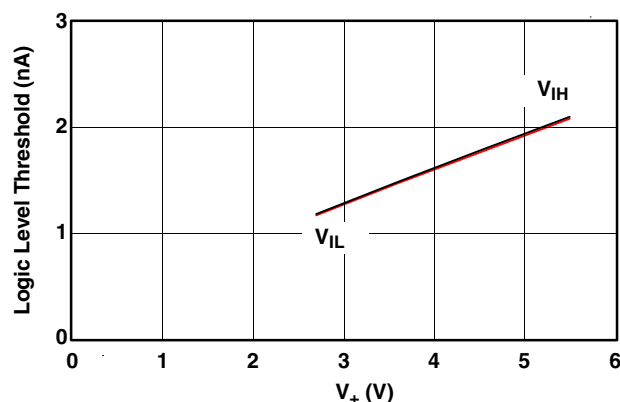


Figure 6.  $t_{ON}$  and  $t_{OFF}$  vs Supply Voltage

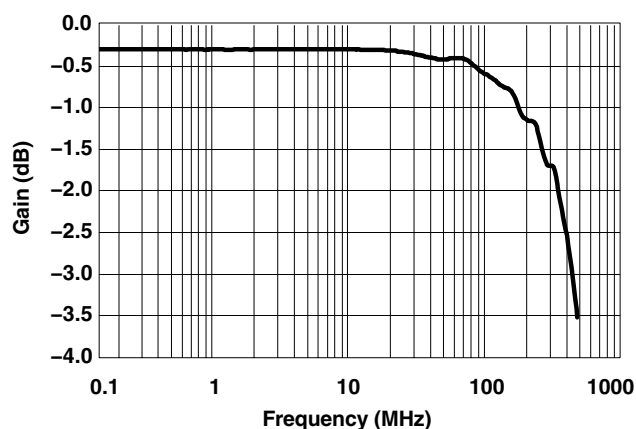
**TYPICAL PERFORMANCE (continued)**



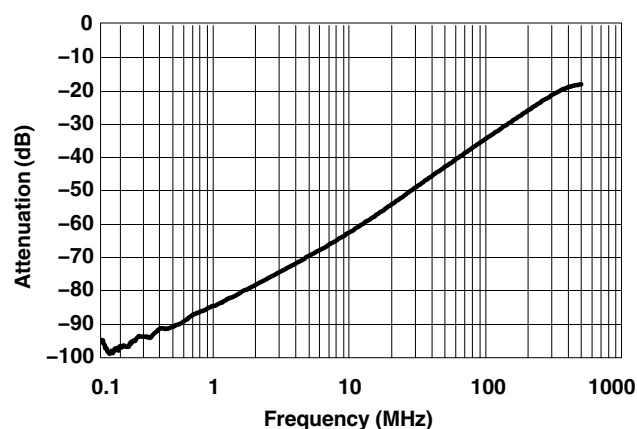
**Figure 7.  $t_{ON}$  and  $t_{OFF}$  vs Temperature ( $V_+ = 5\text{ V}$ )**



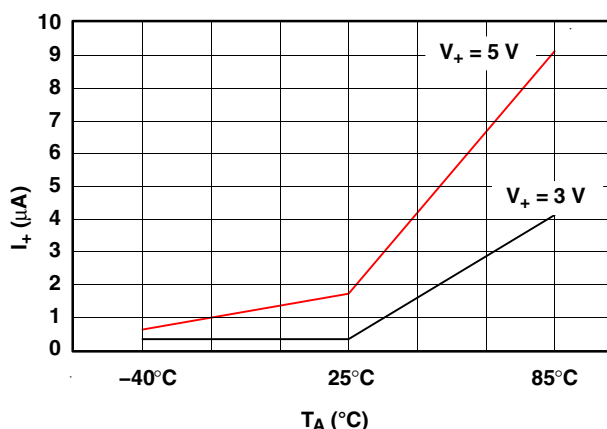
**Figure 8. Logic-Level Threshold vs  $V_+$**



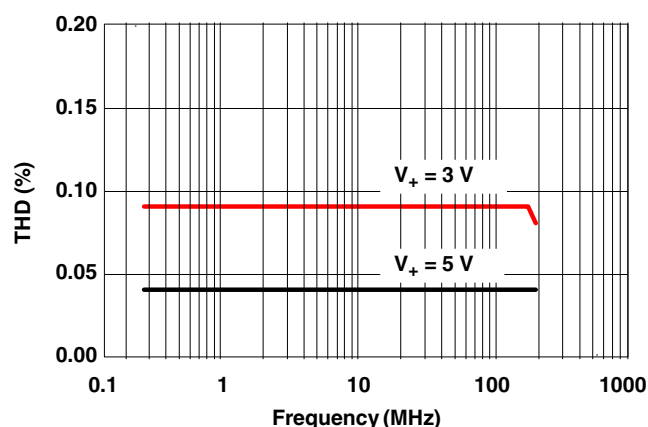
**Figure 9. Bandwidth (Gain vs Frequency) ( $V_+ = 5\text{ V}$ )**



**Figure 10. OFF Isolation vs Frequency**



**Figure 11. Power-Supply Current vs Temperature**



**Figure 12. Total Harmonic Distortion vs Frequency**



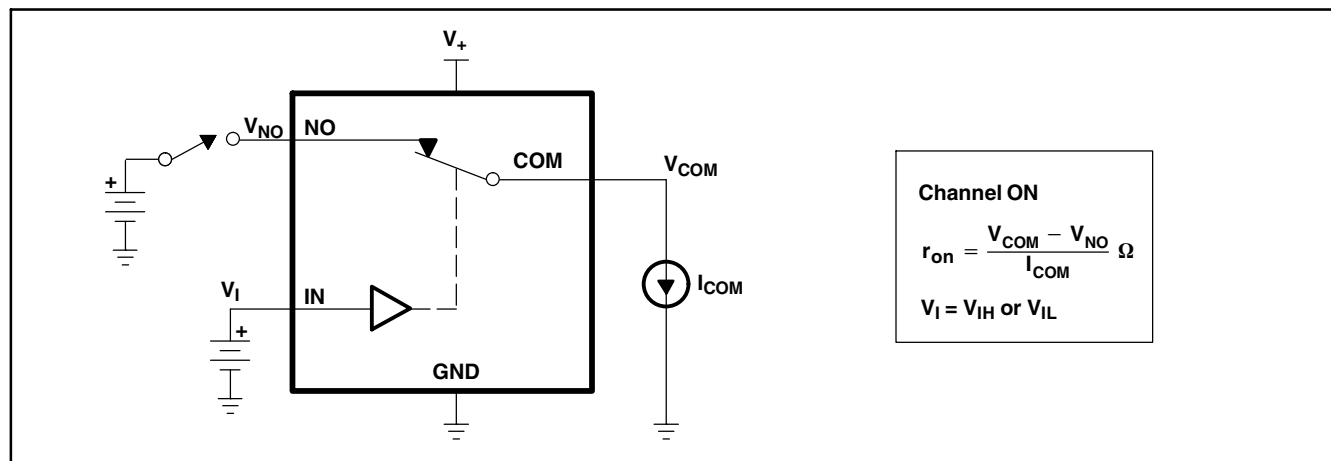
**PIN DESCRIPTION**

PIN NUMBER	NAME	DESCRIPTION
1	COM	Common
2	NO	Normally open
3	GND	Digital ground
4	IN	Digital control pin to connect COM to NO
5	V <sub>+</sub>	Power supply

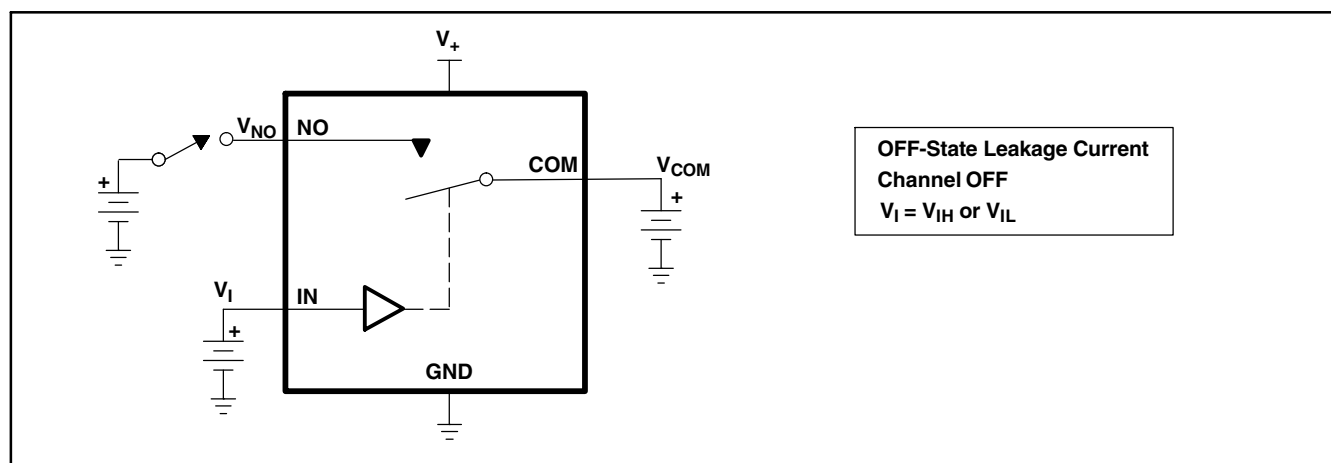
**PARAMETER DESCRIPTION**

SYMBOL	DESCRIPTION
V <sub>COM</sub>	Voltage at COM
V <sub>NO</sub>	Voltage at NO
r <sub>on</sub>	Resistance between COM and NO ports when the channel is ON
r <sub>on(flat)</sub>	Difference between the maximum and minimum value of r <sub>on</sub> in a channel over the specified range of conditions
I <sub>NO(OFF)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
I <sub>NO(ON)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
I <sub>COM(OFF)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state
I <sub>COM(ON)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V <sub>IH</sub>	Minimum input voltage for logic high for the control input (IN)
V <sub>IL</sub>	Maximum input voltage for logic low for the control input (IN)
V <sub>I</sub>	Voltage at the control input (IN)
I <sub>IH</sub> , I <sub>IL</sub>	Leakage current measured at the control input (IN)
t <sub>ON</sub>	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t <sub>OFF</sub>	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
Q <sub>C</sub>	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, Q <sub>C</sub> = C <sub>L</sub> × ΔV <sub>COM</sub> , C <sub>L</sub> is the load capacitance, and ΔV <sub>COM</sub> is the change in analog output voltage.
C <sub>NO(OFF)</sub>	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
C <sub>NO(ON)</sub>	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
C <sub>COM(OFF)</sub>	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
C <sub>COM(ON)</sub>	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C <sub>I</sub>	Capacitance of control input (IN)
O <sub>ISO</sub>	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I <sub>+</sub>	Static power-supply current with the control (IN) pin at V <sub>+</sub> or GND

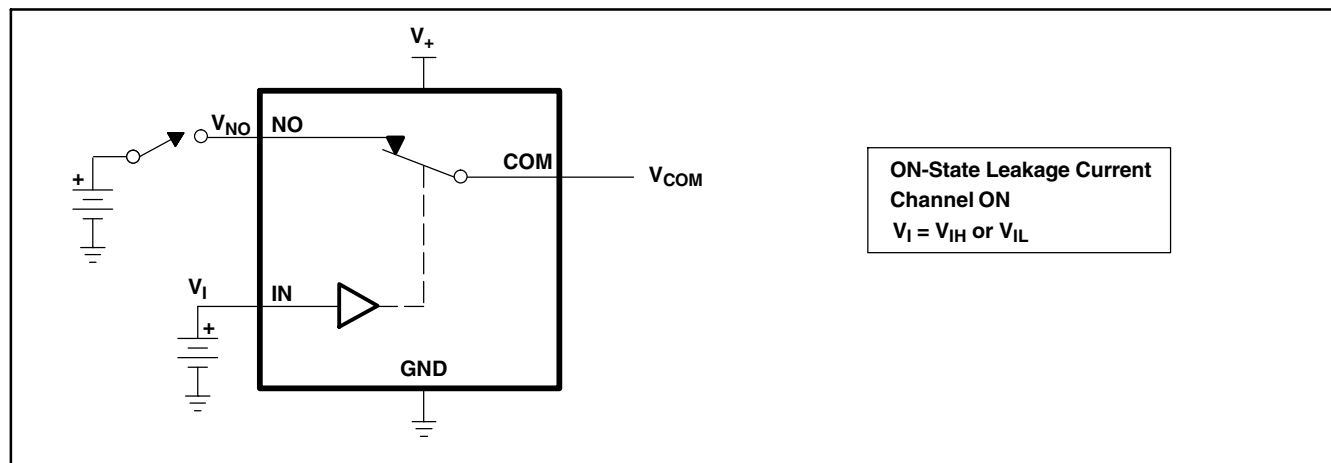
## PARAMETER MEASUREMENT INFORMATION



**Figure 13. ON-State Resistance ( $r_{on}$ )**



**Figure 14. OFF-State Leakage Current ( $I_{COM(OFF)}$ ,  $I_{NO(OFF)}$ )**



**Figure 15. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NO(ON)}$ )**

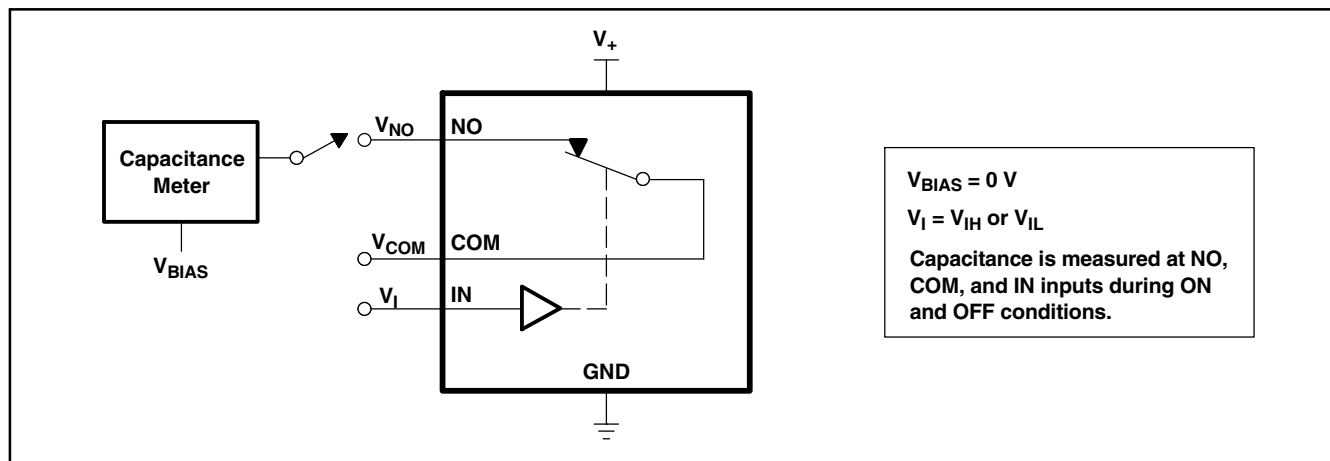
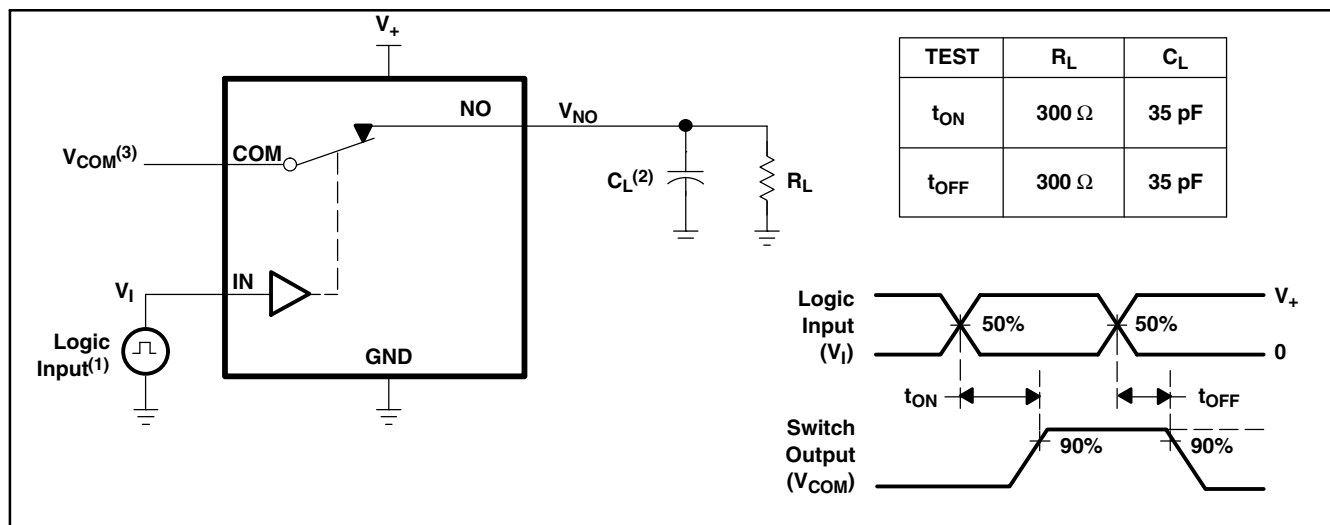


Figure 16. Capacitance ( $C_I$ ,  $C_{COM(OFF)}$ ,  $C_{COM(ON)}$ ,  $C_{NO(OFF)}$ ,  $C_{NO(ON)}$ )



- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50\ \Omega$ ,  $t_r < 5\text{ ns}$ ,  $t_f < 5\text{ ns}$ .  
 (2)  $C_L$  includes probe and jig capacitance.  
 (3) See Electrical Characteristics for  $V_{COM}$ .

Figure 17. Turn-On ( $t_{ON}$ ) and Turn-Off Time ( $t_{OFF}$ )

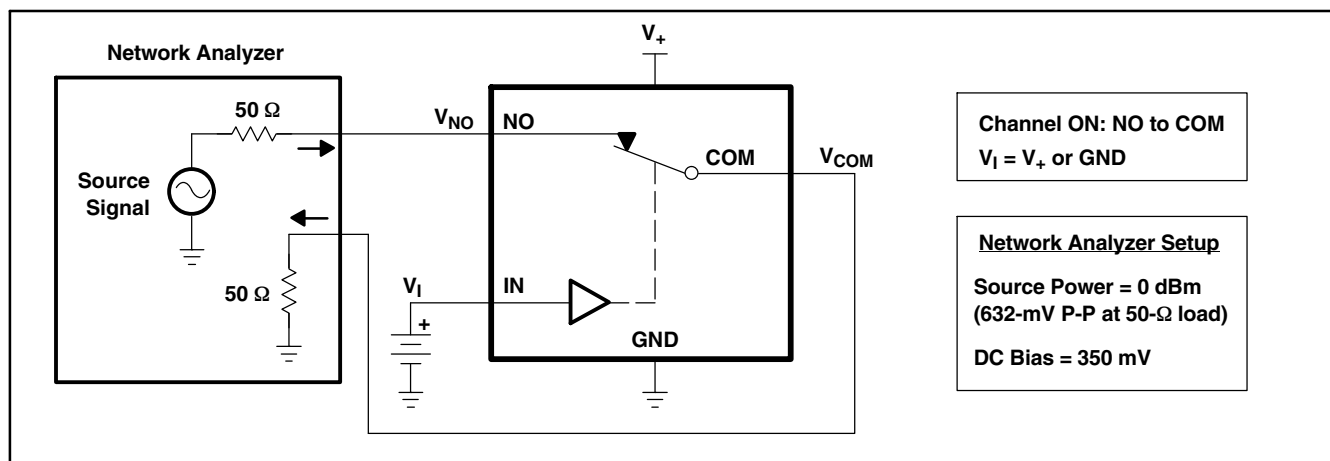
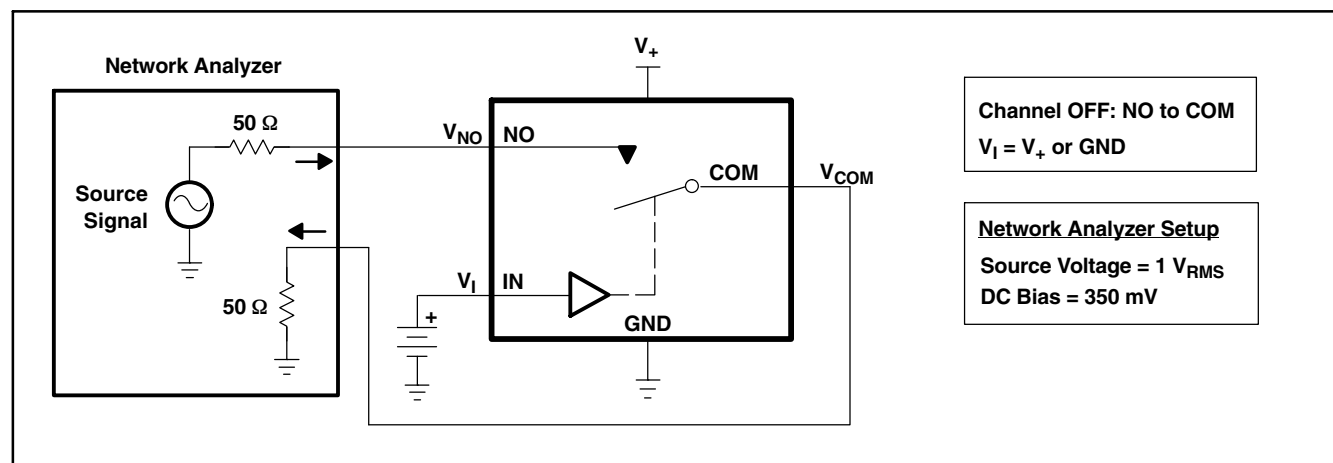
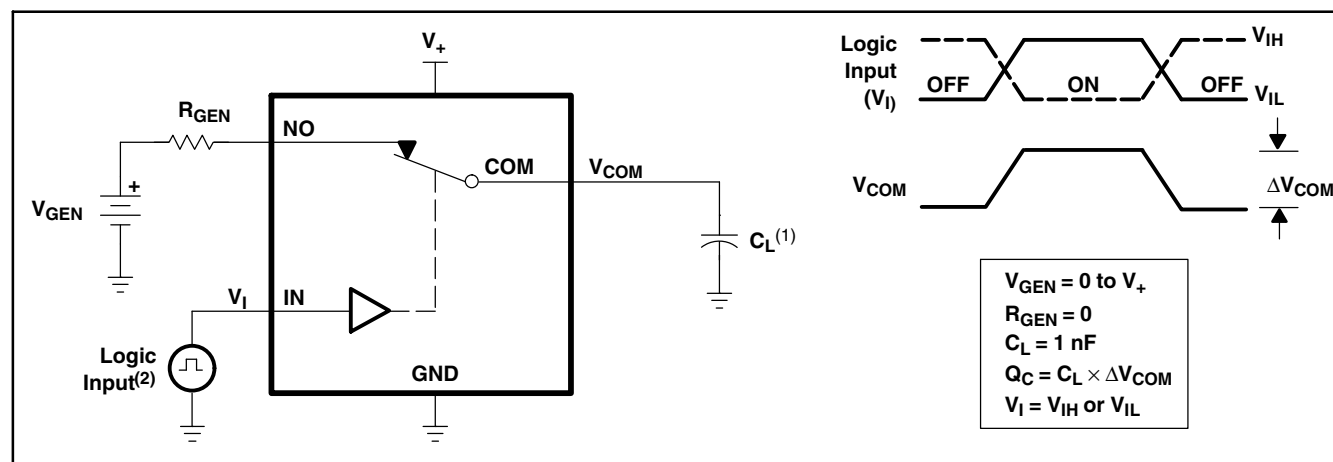


Figure 18. Bandwidth (BW)



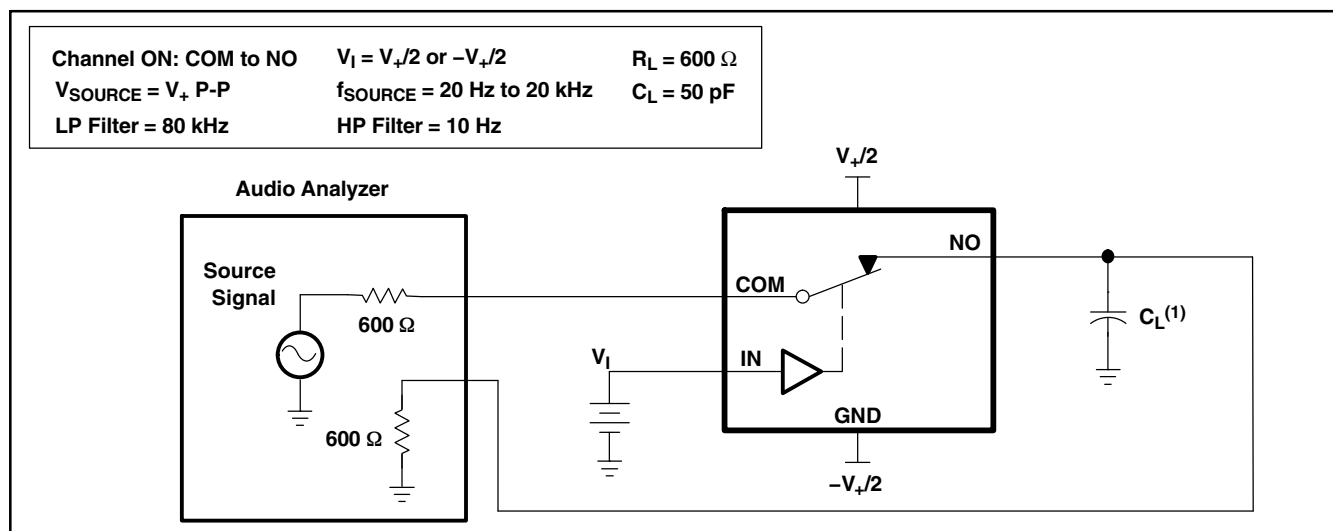
**Figure 19. OFF Isolation ( $O_{ISO}$ )**



(1)  $C_L$  includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.

**Figure 20. Charge Injection ( $Q_C$ )**



(1)  $C_L$  includes probe and jig capacitance.

**Figure 21. Total Harmonic Distortion (THD)**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TS5A4594DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JSAR	<a href="#">Samples</a>
TS5A4594DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JSAR	<a href="#">Samples</a>
TS5A4594DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JSAR	<a href="#">Samples</a>
TS5A4594DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JS5 ~ JSF ~ JSR)	<a href="#">Samples</a>
TS5A4594DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JS5 ~ JSF ~ JSR)	<a href="#">Samples</a>
TS5A4594DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JS5 ~ JSF ~ JSR)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A4594DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A4594DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
TS5A4594DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A4594DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TS5A4594DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TS5A4594DCKR	SC70	DCK	5	3000	180.0	180.0	18.0



DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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