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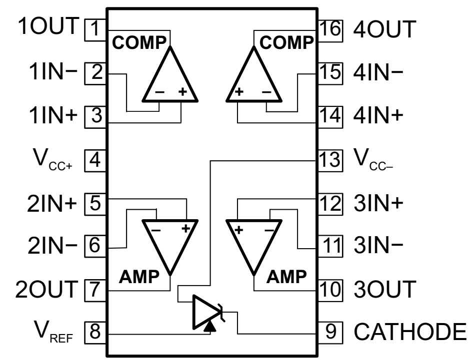
FEATURES

- OPERATIONAL AMPLIFIERS
  - Low Supply Current…200 μA/A
  - Medium Speed…2.1 MHz
  - Low-Level Output Voltage Close to V_{CC-}…0.1 V Typ (R_L = 10 kΩ)
  - Input Common-Mode Voltage Range Includes Ground
- COMPARATORS
  - Low Supply Current…200 μA/A (V_{CC} = 5 V)
  - Input Common-Mode Voltage Range Includes Ground
  - Low Output Saturation Voltage… Typically 250 mV (I_{sink} = 4 mA)
- VOLTAGE REFERENCE
  - Adjustable Output Voltage…V_{REF} to 36 V
  - Sink Current Capability…1 mA to 100 mA
  - 0.4% (A Grade) and 1% (Standard Grade) Precision
  - Latch-Up Immunity

APPLICATIONS

- Switch-Mode Power Supplies
- Battery Chargers
- Voltage and Current Sensing
- Power-Good, Overvoltage, Undervoltage, Overcurrent Detection
- Window Comparators
- Alarms, Detectors, and Sensors

D (SOIC) OR PW (TSSOP) PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TSM102 and TMS102A combine the building blocks of a dual operational amplifier, a dual comparator, and a precision voltage reference, all of which often are used to implement a wide variety of power-management functions, including overcurrent detection, undervoltage/overvoltage detection, power-good detection, window comparators, error amplifiers, etc. Additional applications include alarm and detector/sensor applications.

The TSM102A offers a tight V_{REF} tolerance of 0.4% at 25°C. The TSM102 and TSM102A are characterized for operation from –40°C to 85°C.

ORDERING INFORMATION

T_A	MAX V_{REF} TOLERANCE (25°C)	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	A grade: 0.4% precision	SOIC – D	Tube of 75	TSM102AID	TSM102AI
			Reel of 2500	TSM102AIDR	
		TSSOP – PW	Tube of 90	TSM102AIPW	SN102AI
			Reel of 2000	TSM102AIPWR	
	Standard grade: 1% precision	SOIC – D	Tube of 75	TSM102ID	TSM102I
			Reel of 2500	TSM102IDR	
		TSSOP – PW	Tube of 90	TSM102IPW	SN102I
			Reel of 2000	TSM102IPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Absolute Maximum Ratings[1]

over free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage			36	V
V_{ID}	Input differential voltage			36	V
V_I	Input voltage range		–0.3	36	V
I_{KA}	Voltage reference cathode current			100	mA
θ_{JA}	Package thermal impedance[2][3]	D package		73	°C/W
		PW package		108	
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{CC+} – V_{CC–}$	Supply voltage	3	30	V
V_{ID}	Comparator differential input voltage		$V_{CC+} – V_{CC–}$	V
V_{KA}	Cathode-to-anode voltage	V_{REF}	36	V
I_K	Reference cathode current	1	100	mA
T_A	Operating free-air temperature	–40	85	°C

Total Device Electrical Characteristics

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{CC}	Total supply current, excluding reference cathode current	V_{CC+} = 5 V, $V_{CC–}$ = 0 V, No load	25°C		0.8	1.5	mA
			Full range			2	

Operational Amplifier Electrical Characteristics

V_{CC+} = 5 V, V_{CC-} = GND, R1 connected to V_{CC}/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage			25°C		1	4.5	mV
				Full range			6.5	
αV_{IO}	Input offset voltage drift			25°C		10		μV/°C
I_{IO}	Input offset current			25°C		5	20	nA
				Full range			40	
I_{IB}	Input bias current			25°C		20	100	nA
				Full range			200	
A_{VD}	Large-signal voltage gain	V_{CC+} = 30 V, R1 = 10 kΩ, V_O = 5 V to 25 V		25°C	50	100		V/mV
				Full range	25			
k_{SVR}	Supply-voltage rejection ratio	V_{CC+} = 5 V to 30 V		25°C	80	100		dB
V_{ICM}	Input common-mode voltage			25°C	V_{CC-}		V_{CC+} – 1.8	V
				Full range	V_{CC-}		V_{CC+} – 2.2	
CMRR	Common-mode rejection ratio	V_{CC+} = 30 V, V_{ICM} = 0 V to V_{CC+} – 1.8 V		25°C	70	90		dB
I_{SC}	Short-circuit current	V_{ID} = ±1 V, V_O = 2.5 V	Source	25°C	3	6		mA
			Sink		3	6		
V_{OH}	High-level output voltage	V_{CC+} = 30 V, R_L = 10 kΩ		25°C	27	28		V
				Full range	26			
V_{OL}	Low-level output voltage	R_L = 10 kΩ		25°C		130	170	mV
				Full range			200	
SR	Slew rate	V_{CC} = ±15 V, C_L = 100 pF, V_I = ±10 V, R_L = 10 kΩ		25°C	1.3	2		V/μs
GBW	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz		25°C	1.4	2.1		MHz
Φm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		25°C		45		°
THD	Total harmonic distortion			25°C		0.01		%
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		19		$nV/\sqrt{Hz}$

Comparator Electrical Characteristics

V_{CC+} = 5 V, V_{CC-} = GND (unless otherwise noted)

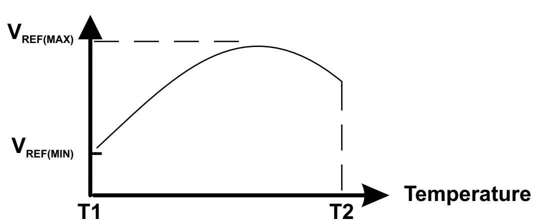
PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C			5	mV
			Full range			9	
V_{ID}	Comparator differential input voltage		Full range			V_{CC+}	V
I_{IO}	Input offset current		25°C			50	nA
			Full range			150	
I_{IB}	Input bias current		25°C			250	nA
			Full range			400	
I_{OH}	High-level output current	V_{ID} = 1 V, V_{CC} = V_O = 30 V	25°C		0.1		nA
			Full range			1	µA
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{sink} = 4 mA	25°C		250	400	mV
			Full range			700	
A_{VD}	Large-signal voltage gain	V_{CC+} = 15 V, R1 = 15 kΩ, V_O = 1 V to 11 V	25°C		200		V/mV
I_{sink}	Output sink current	V_O = 1.5 V, V_{ID} = –1 V	25°C	6	16		mA
V_{ICM}	Input common-mode voltage range		25°C	0		V_{CC+} – 1.5	V
			Full range	0		V_{CC+} – 2	
t_{RESP}	Response time (1)	R1 = 5.1 kΩ to V_{CC+}, V_{REF} = 1.4 V	25°C		1.3		µs
$t_{RESP,large}$	Large-signal response time	R1 = 5.1 kΩ to V_{CC+}, V_{REF} = 1.4 V, V_I = TTL	25°C		300		ns

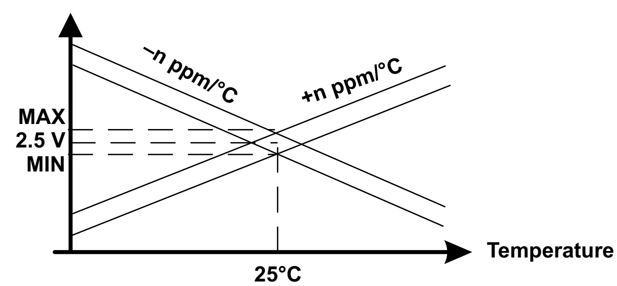
(1) The response-time specification is for 100-mV input step with 5-mV overdrive. For larger overdrive signals, 300 ns can be obtained.

Voltage-Reference Electrical Characteristics

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage[1]	TSM102	$V_{KA} = V_{REF}$, I_K = 10 mA, See Figure 1	25°C	2.475	2.5	2.525	V
		TSM102A		25°C	2.49	2.5	2.51	
ΔV_{REF}	Reference input voltage deviation over temperature range[1]		$V_{KA} = V_{REF}$, I_K = 10 mA, See Figure 1	Full range		7	30	mV
$\frac{V_{REF}}{T}$	Average temperature coefficient of reference input voltage[2]		$V_{KA} = V_{REF}$, I_K = 10 mA	Full range		±22	±100	ppm/°C
$\frac{V_{REF}}{V_{KA}}$	Ratio of change in reference voltage to change in cathode voltage		V_{KA} = 3 V to 36 V, I_K = 10 mA, See Figure 2	25°C		–1.1	–2	mV/V
I_{REF}	Reference input current		I_K = 10 mA, R1 = 10 kΩ, R2 = ∞, See Figure 2	25°C		1.5	2.5	µA
				Full range			3	
ΔI_{REF}	Reference input current deviation over temperature range		I_K = 10 mA, R1 = 10 kΩ, R2 = ∞, See Figure 2	Full range		0.5	1	µA
I_{min}	Minimum cathode current for regulation		$V_{KA} = V_{REF}$, See Figure 1	25°C		0.5	1	mA
$I_{K,OFF}$	Off-state cathode current		See Figure 3	25°C		180	500	nA

(1) ΔV_{REF} is defined as the difference between the maximum and minimum values obtained over the full temperature range.
$\Delta V_{REF} = V_{REF(MAX)} - V_{REF(MIN)}$
(2) The temperature coefficient is defined as the slopes (positive and negative) of the voltage vs temperature limits within which the reference voltage is specified.





PARAMETER MEASUREMENT INFORMATION

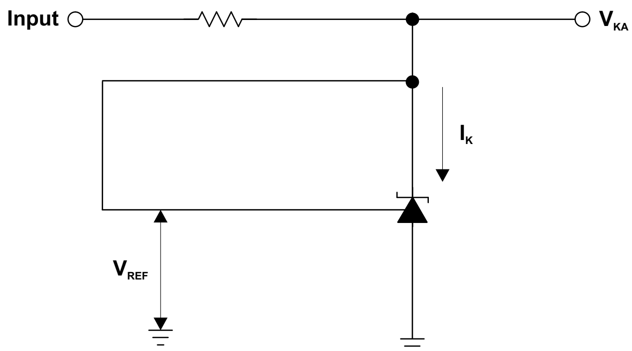


Figure 1. Test Circuit for $V_{KA} = V_{REF}$

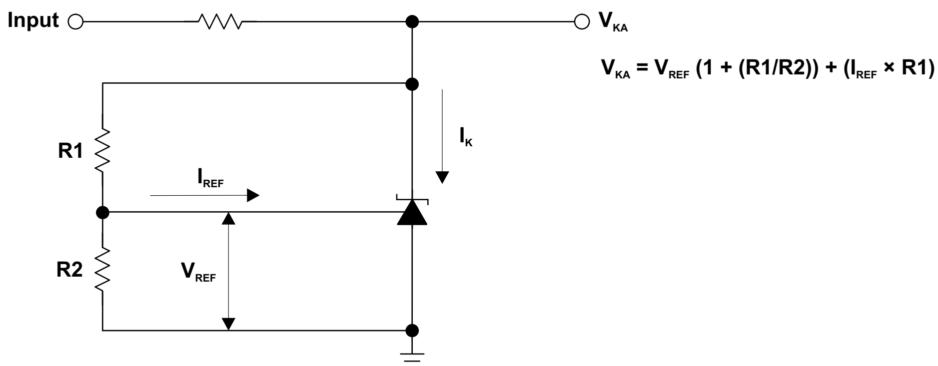


Figure 2. Test Circuit for $V_{KA} > V_{REF}$

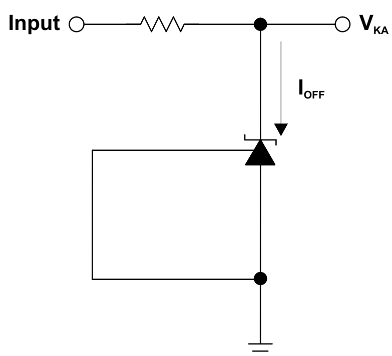


Figure 3. Test Circuit for I_{OFF}

TYPICAL CHARACTERISTICS

AMPLIFIER TOTAL HARMONIC DISTORTION
vs
FREQUENCY

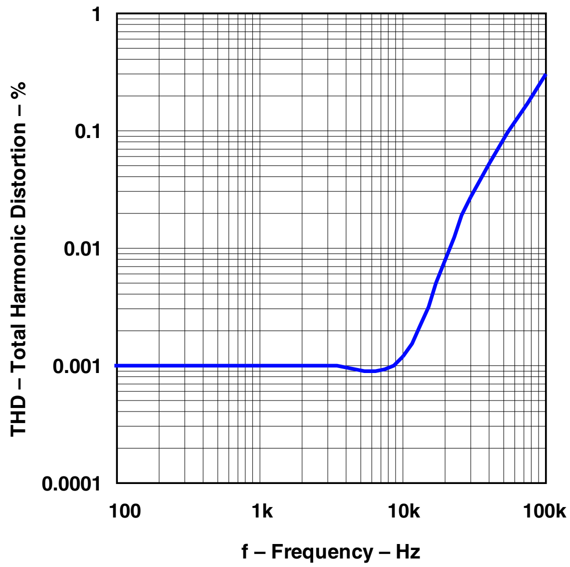


Figure 4.

AMPLIFIER NOISE VOLTAGE
vs
FREQUENCY

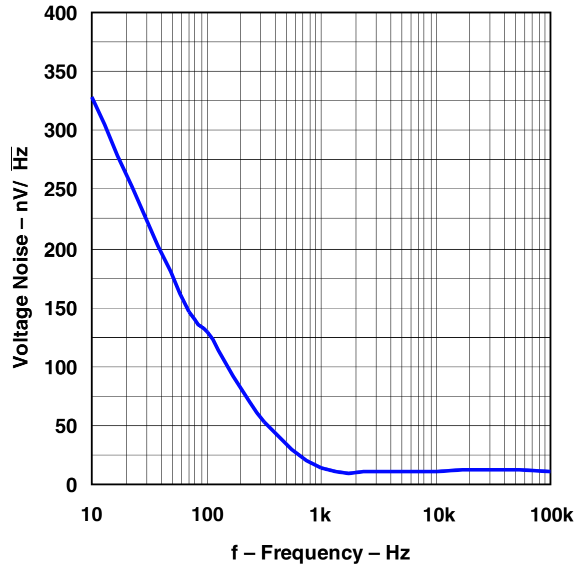


Figure 5.

GAIN AND PHASE
vs
FREQUENCY

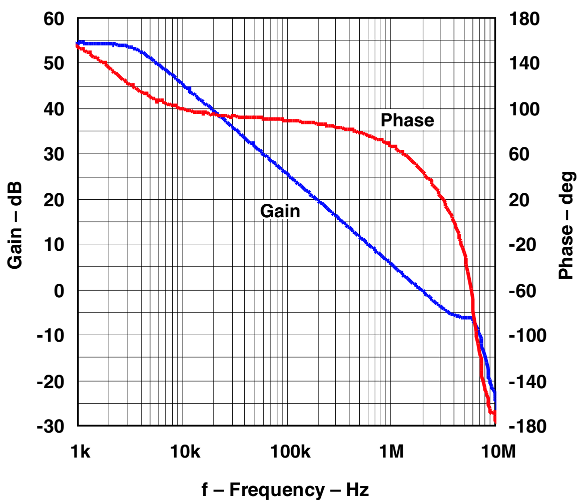


Figure 6.

V_{REF} STABILITY
vs
CAPACITANCE

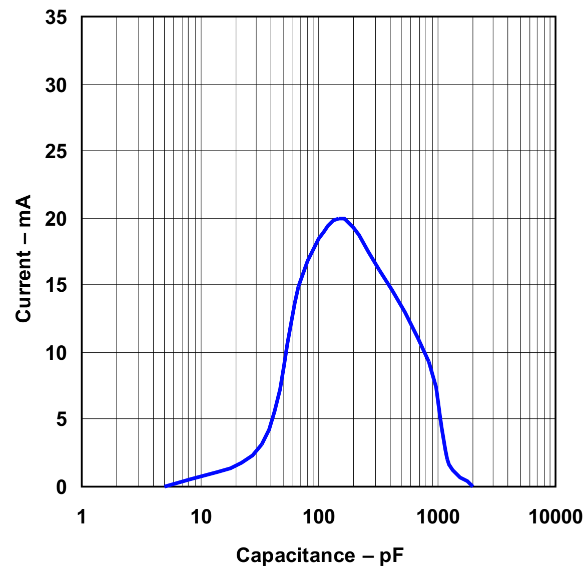


Figure 7.

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS (continued)

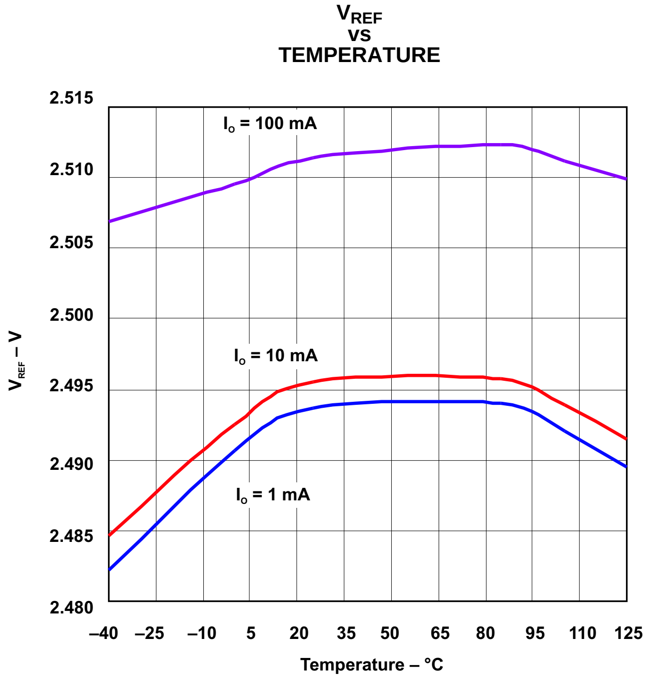

Figure 8.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSM102AID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102AI	Samples
TSM102AIDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102AI	Samples
TSM102AIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102AI	Samples
TSM102AIDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102AI	Samples
TSM102AIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102AI	Samples
TSM102AIPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102AI	Samples
TSM102AIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102AI	Samples
TSM102AIPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102AI	Samples
TSM102ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102I	Samples
TSM102IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102I	Samples
TSM102IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102I	Samples
TSM102IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102I	Samples
TSM102IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102I	Samples
TSM102IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102I	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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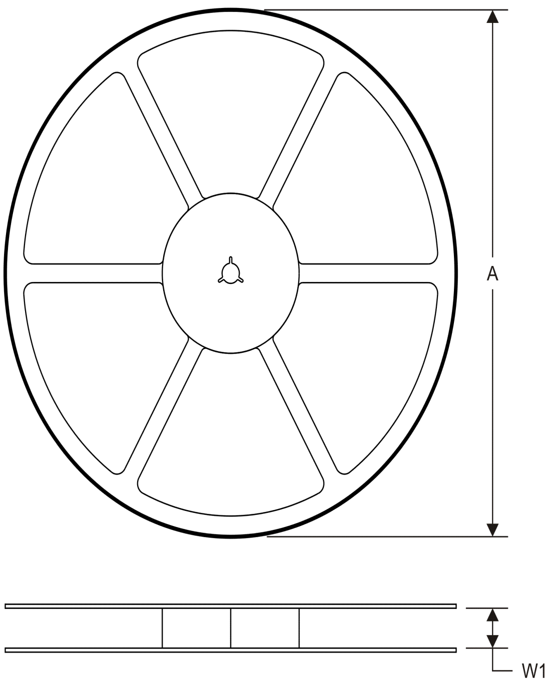
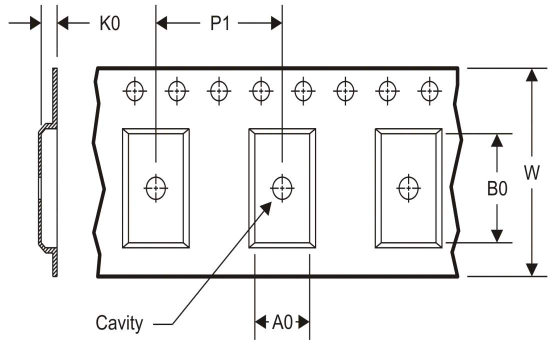
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



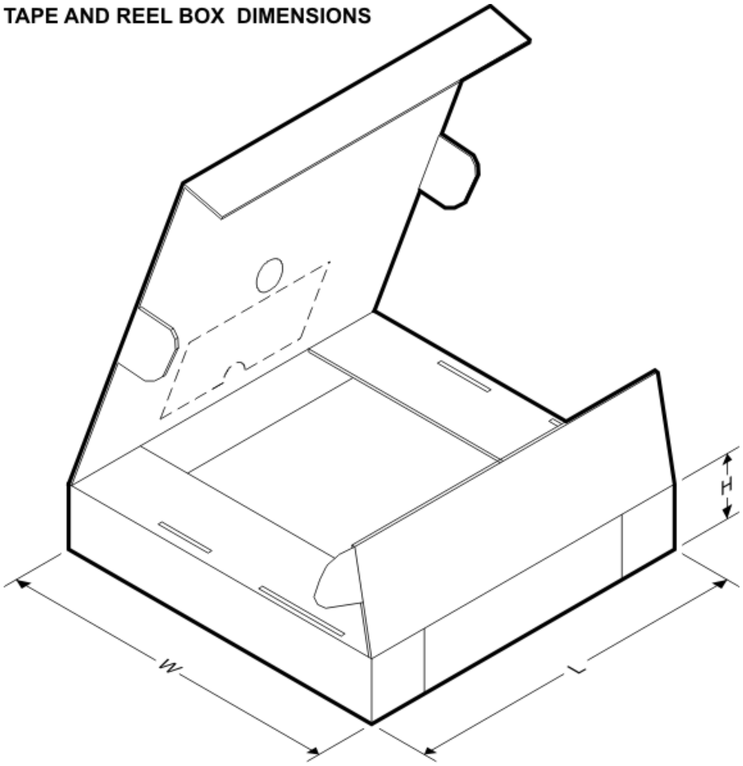
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSM102AIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TSM102AIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TSM102IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TSM102IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

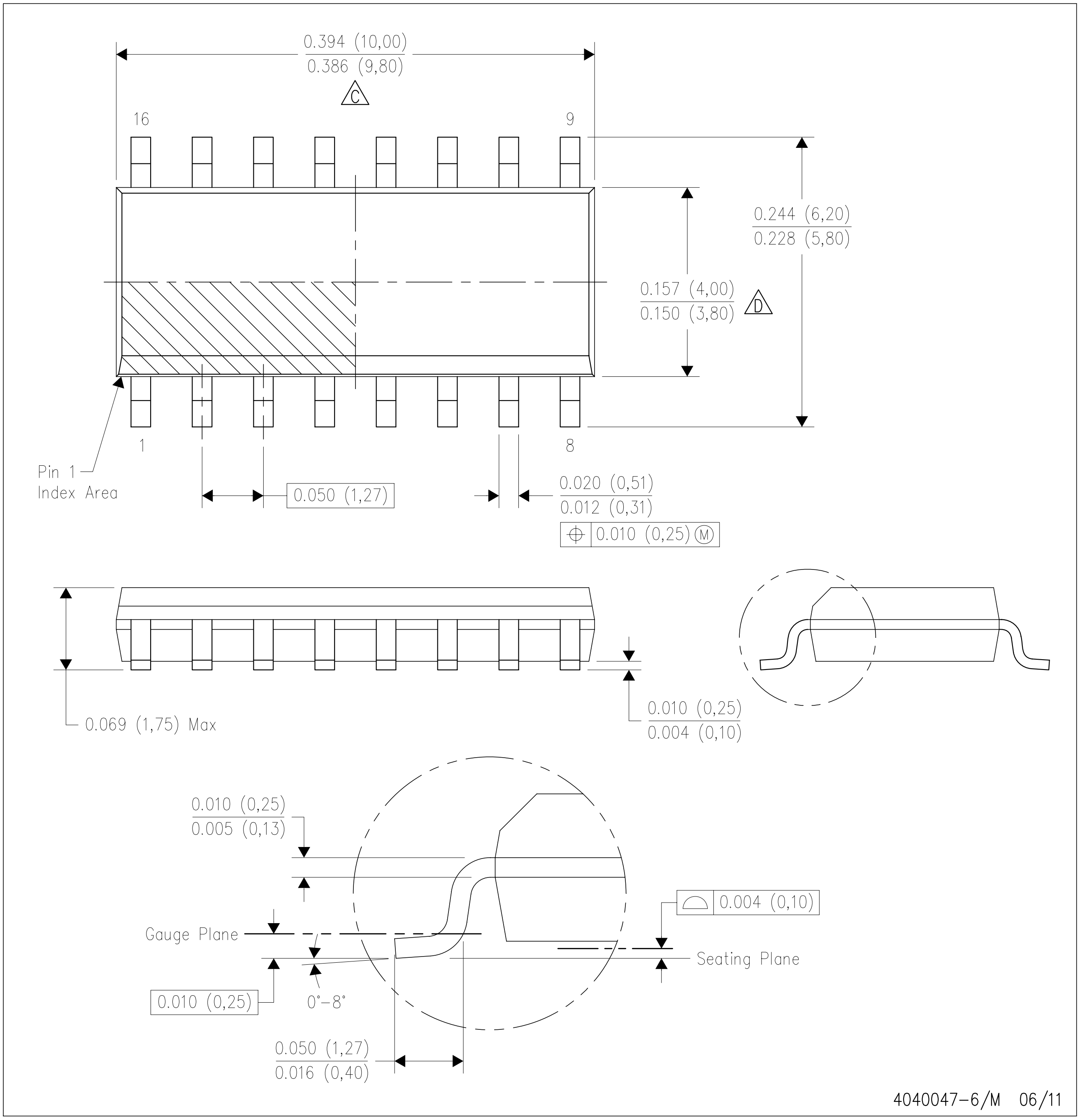
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

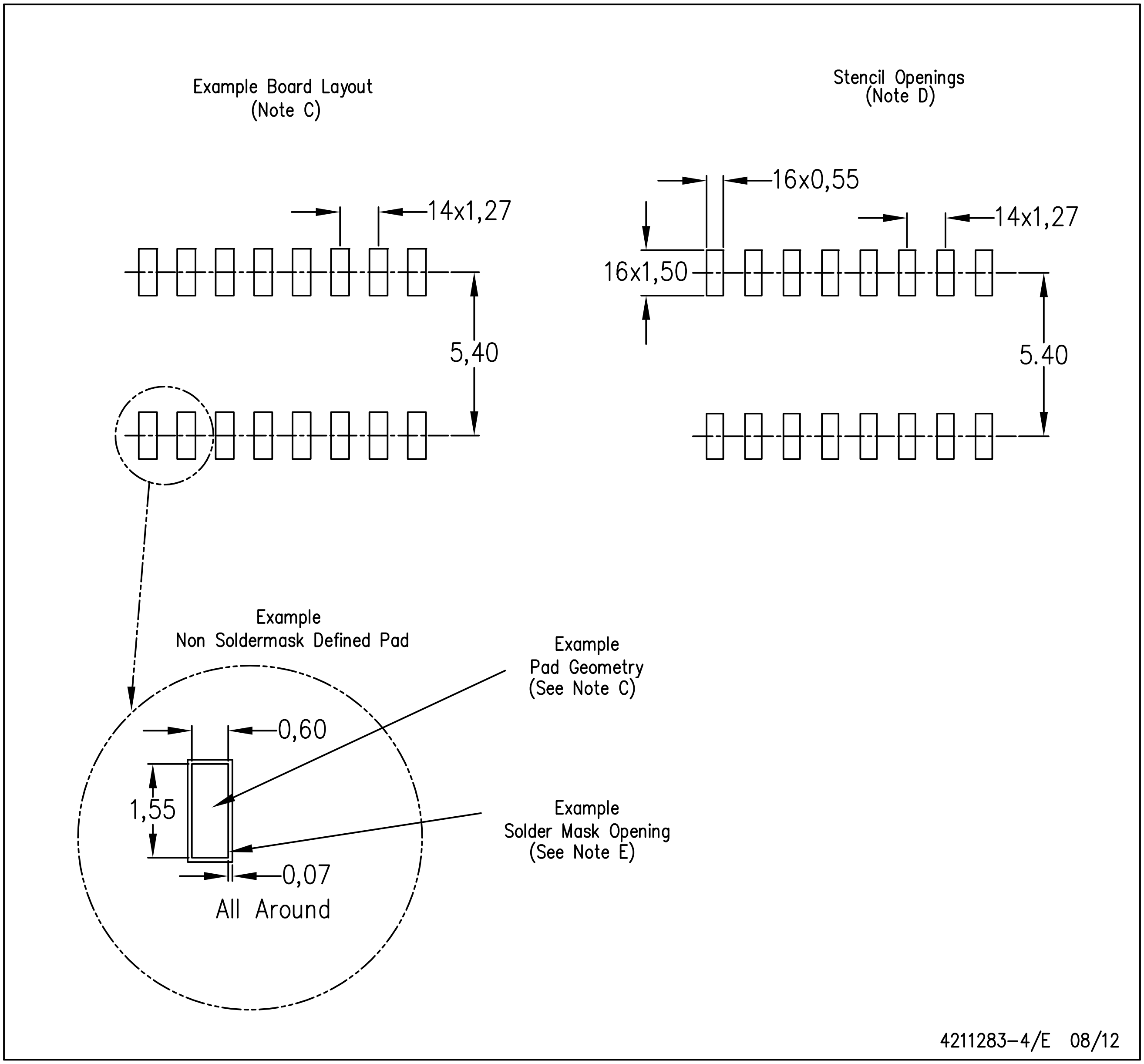
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSM102AIDR	SOIC	D	16	2500	367.0	367.0	38.0
TSM102AIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TSM102IDR	SOIC	D	16	2500	367.0	367.0	38.0
TSM102IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



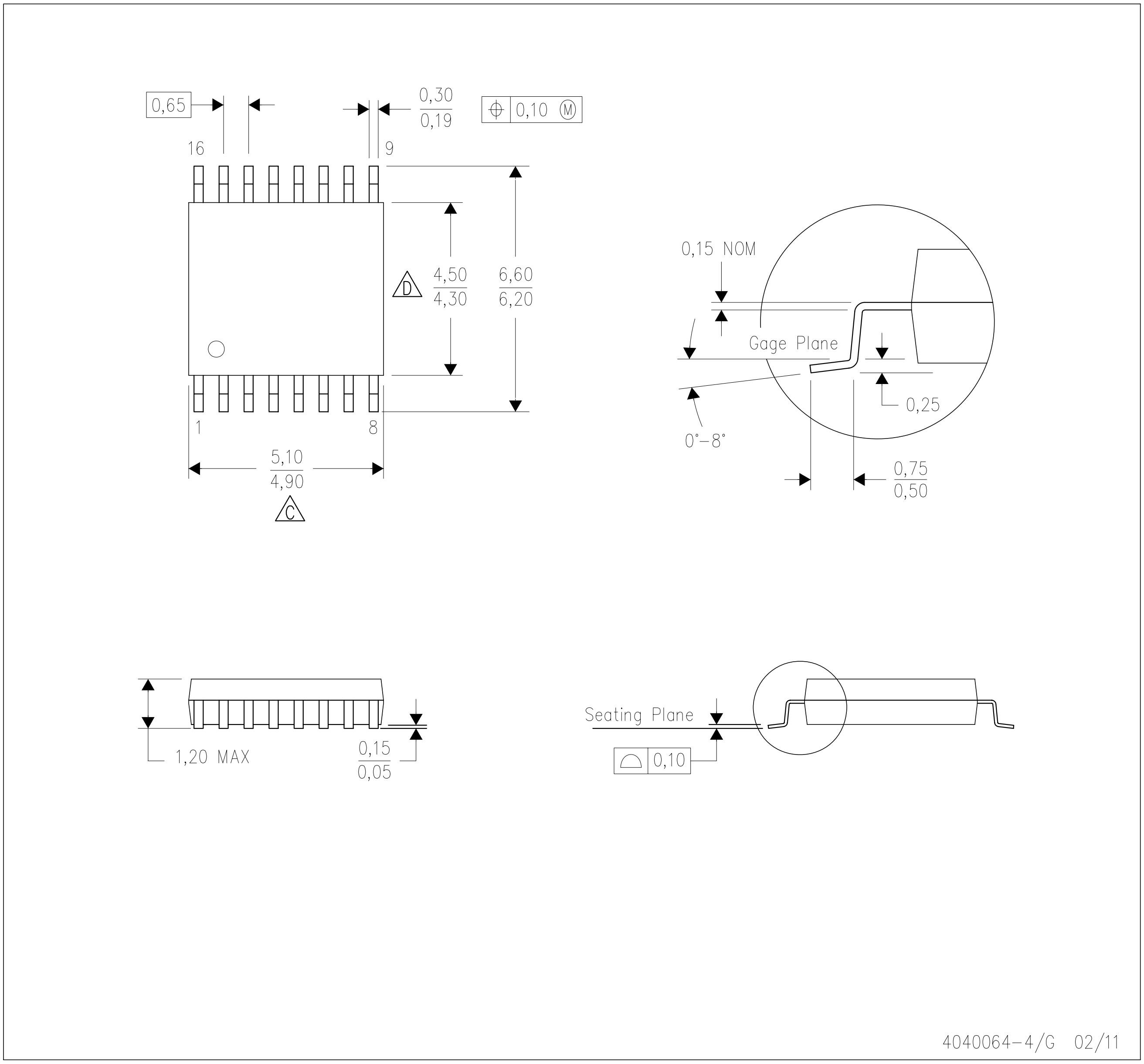
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AC.

D (R-PDSO-G16) PLASTIC SMALL OUTLINE



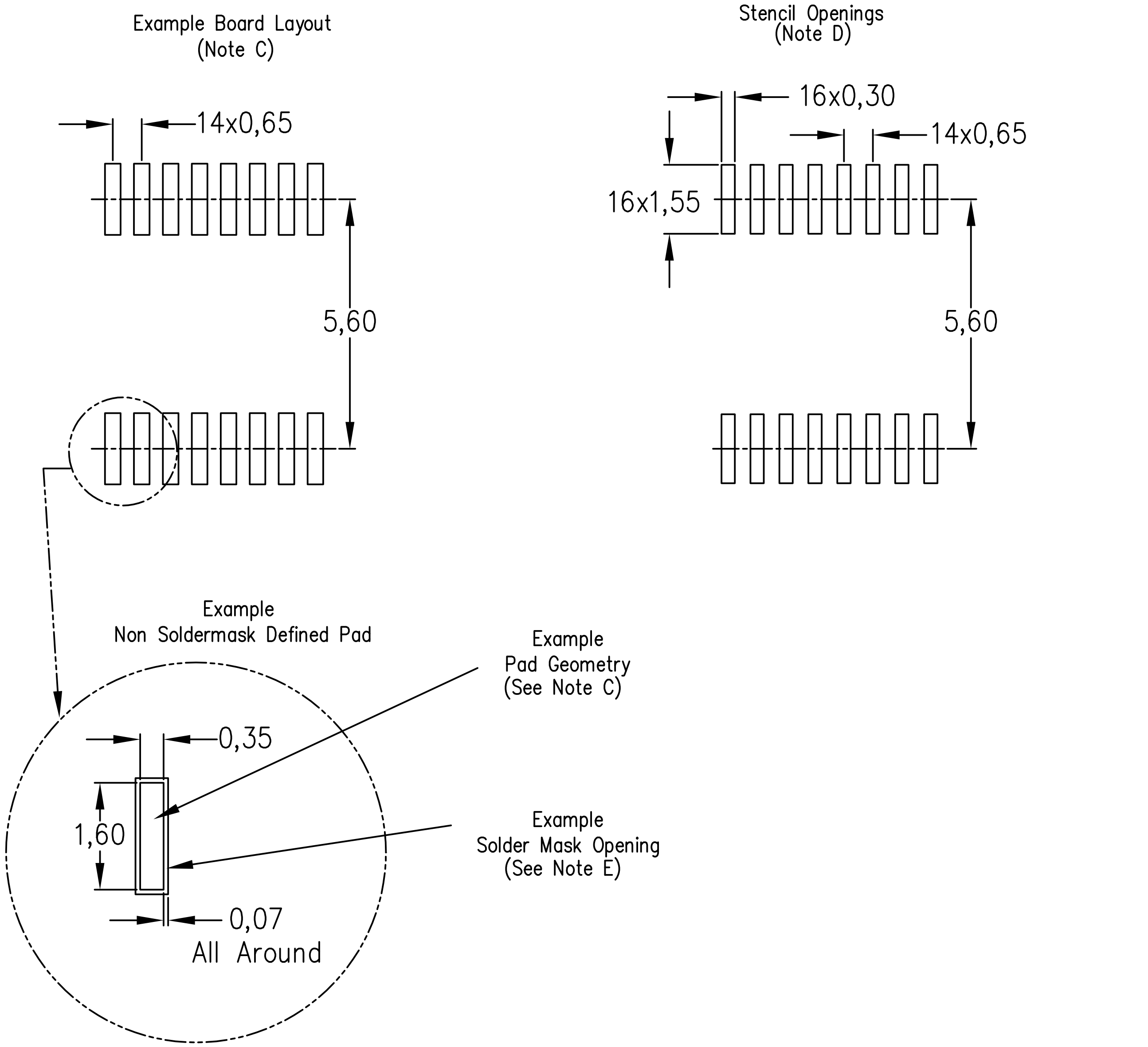
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



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- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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