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Dual Channel, High-Voltage – Multi-Level Output Fully Integrated Ultrasound Transmitter

Check for Samples: TX517

FEATURES

Output Voltage:

- Up to 200Vpp in Differential Mode

Peak Output Current: ±2.5A

Multi-Level Output

Differential: 17 LevelsSingle Ended: 5 Levels

· Integrated:

Level Translator

Driver

High Voltage Output Stages

- CW output

TX Output Update Rate

- Up to 100MSPS

Minimal External Components

Small Package: BGA 13x13mm

APPLICATIONS

Medical Ultrasound

High Voltage Signal Generator

DESCRIPTION

The TX517 is a fully integrated, dual channel, high voltage Transmitter. It is specifically designed for demanding medical Ultrasound applications that require a Multi-level high-voltage pulse pattern. The output stages are designed to deliver typically ±2.5A peak output currents, with 200Vpp swings.

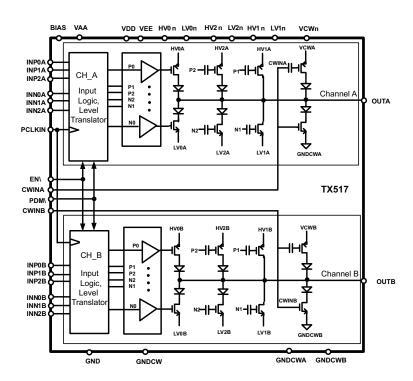
The TX517 is a complete transmitter solution with low-voltage input logic, level translators, gate drivers and P-channel and N-Channel MOSFETs for each channel.

The TX517 also incorporates a CW output stage.

The TX517 is available in a BGA package that is Lead-Free (RoHS compliant) and Green. It is specified for operation from 0°C to 85°C.

17 Level Pulser Chip:

The chip consists of two 5-level channels to form a single 17-level transmitter cell when used in conjunction with a transformer. It is designed to drive the transducer not only at various output levels, but also to modulate the width of the output pulses to obtain the added flexibility of pulse-width-modulation spectral shaping.





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

PACKAGED DEVICES	PACKAGE TYPE	TYPE PACKAGE MARKING TRANSPORT MEDIA, QUANTITY		ECO STATUS ⁽²⁾
TX517IZCQ	BGA-144	TX517	Tray	Pb-Free, Green

- (1) NOTE: These Packages conform to Lead-Free and Green Manufacturing Specifications
- (2) Eco-Status information: Additional details including specific material content can be accessed at www.ti.com/leadfree

GREEN: Ti defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1% of total product weight.

N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree.

Pb-FREE: Ti defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

DEVICE INFORMATION

BGA-144 PINS TOP VIEW 2 3 4 5 6 7 8 9 10 11 12 Α HV2E GND HV1B HV0B VCWB EN\ VAAB NC NC INP1B INN1B INP2B Α В LV1B NC LV1B LV1B LV1B LV1B **GND** NC NC **GND** VAAC INN2B В С OUTB LV1B LV1B LV1B LV1B LV1B CWINE VEE VEE VEE VEE INN0B C D NC LV1B LV1B LV1B LV1B LV1B GNDCWE VEE VEE VEE VEE INP0B D Ε LV2B I V1B LV1B LV1B IV1B VFF VFF VFF VFF PCI KIN Ε F VEE VEE LV1B LV1B LV1B LV1B VEE VEE G G LV1A VEE VEE Н LV2A LV1A LV1A LV1A VDDA VEE VEE VEE VEE CWINA н LV1A LV1A J LV1A GNDCWA VEE VEE INP0A NC LV1A LV1A LV1A LV1A VEE VEE Κ OUTA LV1A LV1A LV1A LV1A LV1A **GND** VEE VEE VEE VEE INN0A Κ L NC I V1A LV1A I V1A LV1A I V1A GND NC NC GND VAAD INN2A М HV2A GND HV1A HV0A VCWA PDM VAAA BIAS NC INP14 INN1A INP2A 2 3 4 5 6 7 8 9 10 11 12



PIN FUNCTIONS

PIN NAME	PIN FUNCTIONS DESCRIPTION
	DESCRIPTION
SUPPLIES	1 11 10 1 (0.5)
VAAx	Input Logic Supply (+2.5V)
VDD	+5V Driver Supply
VEE	–5V Driver Supply
HV0A, HV0B	Positive Supply of Low-voltage FET Output stage; Channel A and B
LV0A, LV0B	Negative Supply of Low-voltage FET Output stage; Channel A and B
HV2A, HV2B	Positive Supply of Intermediate voltage FET Output stage; this stage includes an internal de-glitcher circuit.Channel A and B
LV2A, LV2B	Negative Supply of Intermediate voltage FET Output stage; this stage includes an internal de-glitcher circuit.Channel A and B
HV1A, HV1B	Positive Supply of High-voltage FET Output stage; Channel A and B
LV1A, LV1B	Negative Supply of High-voltage FET Output stage; Channel A and B
VCWA, VCWB	Supply connections for CW FET output stage; Channel A and B
GND	Ground connection; Driver
GNDCWA, GNDCWB	Ground connection for CW FET output stage of Channel A and B
BIAS	Connect to VAA (+2.5V); used for internal biasing; high-impedance input
INPUTS	
INP0A, INP0B	Logic input signal for the Low-voltage P-FET stage of channel A and B; Low = ON, High = OFF . Controls HV0A, HV0B. High impedance input.
INNOA, INNOB	Logic input signal for the Low-voltage N-FET stage of channel A and B; Low = OFF , High = ON . Controls LV0A, LV0B. High impedance input.
INP2A, INP2B	Logic input signal for the Intermediate voltage P-FET stage of channel A and B; Low = ON, High = OFF . Controls HV2A, HV2B. High impedance input.
INN2A, INN2B	Logic input signal for the Intermediate Voltage N-FET stage of channel A and B; Low = OFF, High = ON . Controls LV2A, LV2B. High impedance input.
INP1A, INP1B	Logic input signal for the High-voltage P-FET stage of channel A and B; Low = ON, High = OFF . Controls HV1A, HV1B. High impedance input.
INN1A, INN1B	Logic input signal for the High-voltage N-FET stage of channel A and B; Low = OFF, High = ON. Controls LV1A, LV1B. High impedance input.
CWINA	CW gate input signal for A output. An input '1' means that current sinks from OUTA. An input '0' means that current sources from OUTA. This pin directly accesses the output A CW FET gates.
CWINB	CW gate input signal for B output. An input '1' means that current sinks from OUTB. An input '0' means that current sources from OUTB. This pin directly accesses the output B CW FET gates.
EN	Logic Input for non-CW path; use the Enable-pin to select between input data being latched or transparent operation. Low = input data will be retimed by the internal (T&H) at the rate of the applied clock at PCLKIN. High = use this mode when operating the TX517 without a clock. When High (1) the input data will bypass the (T&H). This pin is a common control for Channel A and B. High impedance input.
PDM	Power-down control input non-CW path; Low = power-down, High = normal operation. The PDM-pin controls the voltage translation circuits which draw some quiescent power. This pin is a common control for Channel A and B. High impedance input.
PCLKIN	Clock input for usage in latch (T&H) mode. When clock signal is high, the (T&H) circuit is in track mode. When clock signal is low, the (T&H) is in hold mode. This pin is a common clock input for both Channel A and B. High impedance input.
OUTPUTS	
OUTA	Output Channel A
OUTB	Output Channel B
	•



ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground potential (GND = 0V); over operating free-air temperature (unless otherwise noted) (1)

		VALUE	UNIT
M	High-Voltage, Positive Supply HV1,2 referred to OUTA/B, see also Max. delta voltage	-0.3 to +80	V
V_{DS}	High-Voltage, Positive Supply HV0 referred to OUTA/B, see also Max. delta voltage	-0.3 to +6	V
	High-Voltage VCWA/B supply referred to GNDCWA/B	-0.3 to +16	V
V	High-Voltage, Negative Supply LV1,2 referred to OUTA/B, see also Max. delta voltage	-40 to +0.3	V
V_{DS}	High-Voltage, Negative Supply LV0 referred to OUTA/B, see also Max. delta voltage	-6 to +0.3	V
	Max. delta voltage: HV1-LV1 and HV2 – LV2	110	V
	Max. delta voltage: HV0 – LV0	12	V
VDD	Driver Supply, positive	-0.3 to +6	V
VEE	Driver Supply, negative	-6 to +0.3	V
VAA	Logic Supply Voltage	-0.3 to +6	V
	Logic Inputs (INPx, INNx, EN, PDM, PCLKIN, U)	-0.3 to +6	V
	CW inputs (CWINA, CWINB)	-0.3 to +11	V
	Peak Solder Temperature ⁽²⁾	260	°C
TJ	Maximum junction temperature, any condition (3)	150	°C
TJ	Maximum junction temperature, continuous operation, long term reliability (4)	125	°C
Tstg	Storage temperature range	-65 to 150	°C
	НВМ	500	V
ESD ratings	CDM	750	V
	MM	200	V

⁽¹⁾ Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.

(2) Device complies with JSTD-020D.

THERMAL INFORMATION

	THERMAL METRIC ⁽¹⁾	TX517	LINITO
	THERMAL METRIC"	BGA (144) (ZCQ) PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	28	
θ_{JCtop}	Junction-to-case (top) thermal resistance	3.8	°C/W
θ_{JB}	Junction-to-board thermal resistance	11.3	C/VV
Ψ_{JT}	Junction-to-top characterization parameter	0.2	
Power	TA = 25°C	3.57	
Rating ⁽²⁾⁽³⁾ (TJ = 125°C)	TA = 85°C	1.47	W

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

(2) This data was taken with the JEDEC High-K test PCB.

⁽³⁾ The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.

⁽⁴⁾ The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

⁽³⁾ Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase and long-term reliability starts to be reduced. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and reliability.

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RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
VAA	2.38	2.5	3.3	V
VDD	4.75	5.0	5.25	V
VEE	-5.25	-5.0	-4.75	V
HV0A, HV0B	0	1.9	5	V
LV0A, LV0B	-5	-1.9	0	V
HV2A, HV2B	0	32	70	V
LV2A, LV2B	-30	-11.9	0	V
HV1A, HV1B	>HV0 and >HV2	61	70	V
LV1A, LV1B	-30	-20.9	<lv0 <lv2<="" and="" td=""><td>V</td></lv0>	V
VCWA, VCWB	0	11	15	V
Maximum DELTA between HV1 to LV1 and HV2 to LV2			100	V
INNx, INPx, EN, PDM, PCLKIN, U	0		VAA	V
INCWA, INCWB	0	5	10	V
INNxx, INPxx input sample rate	1		100	Msps
INNxx, INPXX input unit interval	10		1000	ns
PCLKIN input frequency	1		100	MHz
Ambient Temperature, T _A	0		85	°C



ELECTRICAL CHARACTERISTICS

All Specifications at: T_A = 0 to 85°C, VAA = 2.5V, VDD = 5V, VEE = -5V, HV0 = 1.9V, LV0= -1.9V, HV2 = 32V, LV2=-11.9V, HV1 = +61.1V, LV1= -20.9V, VCW =11V, R_L=100 Ω to GND for OUTA, R_L=100 Ω to GND for OUTB, unless otherwise noted. The parameter results are applicable to both OUTA and OUTB, and they are measured using Non-Latch Mode unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
HV0/L\	/0 SIGNAL PATH – DC PERFORMANCE						
	P-CHANNEL						
	Effective resistance, RDSon + Rdiode	HV0 = 2 V, OUTX = -750 mV to -1.25 V	6.5	9.5	13	Ω	А
	Effective resistance variation	Max output power to Min output power, load = 100 Ω to 0 V			12%		С
	Output saturation current	$R_L = 5 \Omega$ to -30 V	-3.1	-1.3	-1	Α	А
	Output voltage			1.0		V	С
	N-CHANNEL						
	Effective resistance, RDSon + Rdiode	LV0 = -2V, OUTX = 750 mV to 1.25 V	2.5	5	8.5	Ω	А
	Effective Resistance Variation	Max output power to Min output power, Load = 100 Ω to 0 V			5	%	С
	Output saturation current	R _L = 5 Ω to +30 V	1.4	1.8	3.1	Α	А
	Output voltage			-1.2		V	С
HV0/L\	/0 SIGNAL PATH – AC PERFORMANCE						
	Single-tone output frequency		1		100	Msps	В
	2 nd Order harmonic distortion (when using transformer bridge)	f = 5.0 MHz square wave, measured using transformer at secondary coil with RL = 100 Ω		35		dBc	С
t _r	Output rise time	10% to 90% of 0 V to +Vout Figure 8		4.5		ns	С
t _f	Output fall time	10% to 90% of 0 V to -Vout Figure 8		1		ns	С
t_{pr}, t_{pf}	Propagation Delay	Input 50% to Output 50% Figure 8		30		ns	В
HV2/L\	/2 SIGNAL PATH – DC PERFORMANCE						
	P-CHANNEL						
	Effective resistance, RDSon + Rdiode	HV2 = 30 V to HV2 = 20 V	4.5	9	12.5	Ω	Α
	Effective resistance variation	Max output power to Min output power, load = 100 Ω to 0 V			12%		С
	Output saturation current	HV2 = 60 V; $R_L = 5 \Omega$ to GND	-4.1	-2.3	-1.8	Α	Α
	Output voltage			28.5		V	С
	N-CHANNEL						
	Effective resistance, RDSon + Rdiode	LV2 = -10 V to LV2 = -12 V	1.5	4.5	7.5	Ω	Α
	Effective resistance variation	Max output power to Min output power, load = 100 Ω to 0 V			4%		С
	Output saturation current	LV2 = -60 V; $R_L = 5$ Ω to GND	2.4	3.0	5.0	Α	Α
	Output Voltage			-10.5		V	С
HV2/L\	/2 SIGNAL PATH – AC PERFORMANCE						
	Single-tone Output Frequency		1		100	Msps	В
	2 nd Order harmonic distortion when using transformer bridge	$f=5.0~\text{MHz}$ square wave, measured using transformer at secondary coil with RL = 100 Ω		50		dBc	С
t _r	Output rise time	10% to 90% of 0 V to +Vout Figure 8		7.5		ns	С
t _f	Output fall time	10% to 90% of 0 V to -Vout Figure 8	-	3		ns	С
t _{pr} , t _{pf}	Propagation delay	Input 50% to Output 50% Figure 8		25		ns	В

⁽¹⁾ Test levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.



ELECTRICAL CHARACTERISTICS

All Specifications at: $T_A = 0$ to 85°C, VAA = 2.5V, VDD = 5V, VEE = -5V, HV0 = 1.9V, LV0 = -1.9V, HV2 = 32V, LV2 = -11.9V, HV1 = +61.1V, LV1 = -20.9V, VCW = 11V, $R_L = 100\Omega$ to GND for OUTA, $R_L = 100\Omega$ to GND for OUTB, unless otherwise noted. The parameter results are applicable to both OUTA and OUTB, and they are measured using Non-Latch Mode unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
HV1/LV1 SIGNAL PATH – DC PERFORMANCE						
P-CHANNEL						
Effective resistance, RDSon + Rdiode	HV1 = 60 V to HV1 = 50 V	2.5	7	12.5	Ω	Α
Effective resistance variation	Max output power to Min output power load = 100 Ω to GND			11%		С
Output saturation current	HV1 = 60 V; R_L = 5 Ω to GND	-4.1	-2.5	-2	Α	Α
Output voltage			58		V	С
N-CHANNEL						
Effective resistance, RDSon + Rdiode	LV1 = -20 V to -10 V	1	2	4.5	Ω	А
Effective resistance variation	Max output power to Min output power load = 100 Ω to 0 V			3%		С
Output saturation current	LV1 = -60 V ; R _L = 5Ω to GND	2.9	3.4	4.1	Α	А
Output voltage			-20		V	С
IV1/LV1 SIGNAL PATH – AC PERFORMANCE						
Single-tone output frequency		1		100	Msps	В
2 nd Order harmonic distortion (when using transformer bridge)	f = 5.0 MHz square wave, measured using transformer at secondary coil with RL = 100 Ω		60		dBc	С
Output rise time	10% to 90% of 0 V to +Vout Figure 8		6.5		ns	С
Output fall time	10% to 90% of 0 V to –Vout Figure 8		3		ns	С
_{pr} , t _{pf} Propagation Delay	Input 50% to Output 50% Figure 8		25		ns	В

⁽¹⁾ Test levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

ELECTRICAL CHARACTERISTICS

All Specifications at: $T_A = 0$ to 85°C, VAA = 2.5V, VDD = 5V, VEE = -5V, HV0 = 1.9V, LV0 = -1.9V, HV2 = 32V, LV2 = -11.9V, HV1 = +61.1V, LV1 = -20.9V, VCW = 11V, $R_L = 100 \Omega$ to GND for OUTA, $R_L = 100 \Omega$ to GND for OUTB, unless otherwise noted. The parameter results are applicable to both OUTA and OUTB, and they are measured using Non-Latch Mode unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)		
CW SIGNAL PATH – DC PERFORMANCE	N SIGNAL PATH – DC PERFORMANCE							
P-CHANNEL								
Effective resistance, RDSon + Rdiode	VCW = 4.5 Vto 5.5 V	9	21	31	Ω	А		
Effective resistance variation	Max output power to Min output power, load = 100 Ω to 0 V			30%		С		
Output saturation current	$R_L = 5 \Omega$ to -20 V	-0.16	-0.12	-0.06	Α	A		
Output voltage			8		V	С		
N-CHANNEL								
Effective resistance, RDSon + Rdiode	OUTX = 1 V to 2 V	9	14	18	Ω	A		
Effective resistance variation	Max output power to Min output power, load = 100 Ω to 0 V			10%		С		
Output saturation current	$R_L = 5 \Omega$ to 20 V	0.29	0.35	0.44	Α	A		
Output voltage			30		mV	С		

⁽¹⁾ Test levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.



ELECTRICAL CHARACTERISTICS (continued)

All Specifications at: $T_A = 0$ to 85°C, VAA = 2.5V, VDD = 5V, VEE = -5V, HV0 = 1.9V, LV0 = -1.9V, HV2 = 32V, LV2 = -11.9V, HV1 = +61.1V, LV1 = -20.9V, VCW = 11V, $R_L = 100 \Omega$ to GND for OUTA, $R_L = 100 \Omega$ to GND for OUTB, unless otherwise noted. The parameter results are applicable to both OUTA and OUTB, and they are measured using Non-Latch Mode unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
cw s	IGNAL PATH – AC PERFORMANCE ⁽²⁾		•				
	Single-tone output frequency		0.5		10	MHz	В
	and a late of the co	f = 1MHz, measured using transformer at secondary coil with R_L = 100 Ω		47		dBc	С
	2 nd Order harmonic distortion	f = 5 MHz, measured using transformer at secondary coil with R_L = 100 Ω		33		dBc	С
	Slew Rate + (Positive Edge)	20% to 80% of Voutpp, measured using transformer at		0.6		V/ns	С
	Slew Rate – (Negative Edge)	secondary coil with RL = 100 Ω		0.45		V/ns	С
t _r	Output rise time	10% to 90% of 0 V to +Vout Figure 8		30		ns	С
t _f	Output fall time	10% to 90% of 0 V to –Vout Figure 8		10		ns	С
$t_{pr},\ t_{pf}$	Propagation Delay	Input 50% to Output 50% Figure 8		25		ns	В
	AC-coupled gate drive time constant for P-CHANNEL		10	20	30	μs	С
CW IN	IPUT CHARACTERISTIC						
	High input voltage		1.05			V	В
	Low input voltage				0.35	V	В
	Low input current	CWINX=0V		0	1	μA	В
	High input current	CWINX=5.0V		25	40	μA	В
	Input Gate Charge	CWINX = 0 V to 5.0 V or 5.0 V to 0 V		550		pC	С
LOGI	C CHARACTERISTICS – INNXX, INPXX, EN	PDM PCLKIN pins					
		INNxx, INPxx, PCLKIN @ 10 MHz		6			
	Input capacitance	EN\ @ 10 MHz		9		pF	С
		PDM\ @ 10 MHz		4			
	Logic high input voltage	VAA=2.375V to 3.6V	0.55*VAA		VAA	V	В
	Logic low input voltage	VAA=2.375V to 3.6V	0		0.8	V	В
	Logic low input current			0.2	10	μA	В
	Logic high input current			0.2	10	μA	В
	Minimum clock period, tper	Figure 9, PCLKIN	10			ns	В
	Minimum clock high time, tmin	Figure 9, PCLKIN	2.0			ns	В
t _s	Setup time	Figure 9, PCLKIN, INNxx, INPxx	0			ns	В
t _h	Hold time	Figure 9, PCLKIN, INNxx, INPxx	1.5			ns	В
OUTP	UT CHARACTERISTIC				U.		
	Output resistance	Power Down Mode (Hi-Z Output) VTEST = 20 V		1		GΩ	С
	Output capacitance	Power Down Mode (Hi-Z Output) @1 to 100 MHZ		165		pF	С
	Leakage current	Power Down Mode (Hi-Z Output) VTEST = 0V		0.001	10	μA	А
INTER	RNAL GATE CHARGE CHARACTERISTICS						
		HV0/LV0 internal FET gates driven from VEE to VDD or VDD to VEE		3.5		nC	С
	Input gate charge ⁽³⁾	HV1/LV1 internal FET gates driven from VEE to VDD or VDD to VEE		4.6		nC	С
		HV2/LV2 internal FET gates driven rom VEE to VDD or VDD to VEE		7		nC	С

⁽¹⁾ Test levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

⁽²⁾ TX517 CW outputs are complimentary. Thus a transformer is needed to enable CW output.

³⁾ Input gate charge is the amount of charge to change the internal FET gates of a given output from either a low to a high state or from a high to a low state. Each gate charge value applies to both the P and N type FET for the given output. These values can be used to estimate the amount of dynamic current that needs to be provided to the VDD and VEE power supplies in order to switch the internal FET's at a given sampling rate.



ELECTRICAL CHARACTERISTICS

All Specifications at: $T_A = 0$ to 85°C, VAA = 2.5V, VDD = 5V, VEE = -5V, HV0 = 1.9V, LV0 = -1.9V, HV2 = 32V, LV2 = -11.9V, HV1 = +61.1V, LV1 = -20.9V, VCW = 11V, R_L= 100Ω to GND for OUTA, R_L= 100 Ω to GND for OUTB, unless otherwise noted. The parameter results are applicable to both OUTA and OUTB, and they are measured using Non-Latch Mode unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	TEST LEVEL ⁽¹⁾
POWER SUPPLY							
Total Quiescent Current (PW Mode) Power supply VDD	INPxx = 1, INNxx = 0, PCLKIN= 0 or 1			13	15	mA	А
Total Quiescent Current (PW Mode) Power supply VEE	INPxx = 1, INNxx = 0, PCLKIN= 0 or 1		-10	-8		mA	А
Total Quiescent Current (PW Mode) Power supply VAA	INPxx = 1, INNxx = 0, PCLKIN= 0 or 1		-3	-2		mA	А
	Input pattern = 10 cycle square wave, 5%	HV0/LV0		17	23		
Dynamic Current Consumption (PW Mode) Power supply VDD	duty cycle at 10 Msps (5 MHz) on noted signal path. Load = transformer and 100	HV1/LV1		18	23	mA	В
. ee. eapp., 122	ohm differential load, see Figure 10.	HV2/LV2		20.5	23		
	Input pattern = 10 cycle square wave, 5%	HV0/LV0	-15	-10			
Dynamic Current Consumption (PW Mode) Power supply VEE	duty cycle at 10 Msps (5 MHz) on noted signal path. Load = transformer and 100	HV1/LV1	-15	-10.5		mA	В
· circl capply 122	ohm differential load, see Figure 10.	HV2/LV2	-15	-12.5			
	Input pattern = 10 cycle square wave, 5%	HV0/LV0	-4	-2.3			
Dynamic Current Consumption (PW Mode) Power supply VAA	duty cycle at 10 Msps (5 MHz) on noted signal path. Load = transformer and 100	HV1/LV1	-4	-2.5		mA	В
	ohm differential load, see Figure 10.	HV2/LV2	-4	-2.5			
Dynamic Current Consumption (PW Mode) Power supply HV0	Input pattern = 10 cycle square wave, 5% (5 MHz) on noted signal path. Load = transdifferential load, see Figure 10.			2	4	mA	В
Dynamic Current Consumption (PW Mode) Power supply LV0	Input pattern = 10 cycle square wave, 5% duty cycle at 10 Msps (5 MHz) on noted signal path. Load = transformer and 100 ohm differential load, see Figure 10.			-2		mA	В
Dynamic Current Consumption (PW Mode) Power supply HV1	Input pattern = 10 cycle square wave, 5% duty cycle at 10 Msps (5 MHz) on noted signal path. Load = transformer and 100 ohm differential load, see Figure 10.			41	60	mA	В
Dynamic Current Consumption (PW Mode) Power supply LV1	Input pattern = 10 cycle square wave, 5% (5 MHz) on noted signal path. Load = transdifferential load, see Figure 10.		-55	-41		mA	В
Dynamic Current Consumption (PW Mode) Power supply HV2	Input pattern = 10 cycle square wave, 5% Msps(5 MHz) on noted signal path. Load = ohm differential load, see Figure 10.			22	60	mA	В
Dynamic Current Consumption (PW Mode) Power supply LV2	Input pattern = 10 cycle square wave, 5% (5 MHz) on noted signal path. Load = transdifferential load, see Figure 10.		-35	-22		mA	В
	Input pattern = 10 cycle square wave, 5%	HV0/LV0		0.15	0.25		
Total Power Dissipation for device only (PW Mode)	duty cycle at 10 Msps on noted signal path. Load = transformer and 100 ohm	HV1/LV1		1.1	1.7	W	В
(I w Mode)	differential load, see Figure 10.	HV2/LV2		0.6	0.8		
Dynamic Current Consumption (CW Mode) Power supply VCWA + VCWB	Input pattern = 10 cycle square wave, 100% duty cycle at 10 Msps on CW signal path. Load = transformer and 100 ohm differential load, see Figure 10. EN\= 0 or 1, PCLKIN = 0 or 1			62	100	mA	В
Total Power Dissipation for device only (CW Mode)	Input pattern = 10 cycle square wave, 100% duty cycle at 10 Msps (5 MHz) on noted signal path. Load = transformer and 100 ohm differential load, see Figure 10. EN\ = 0 or 1, PCLKIN = 0 or 1			310	400	mW	В
Supply (HVx, LVx) Slew Rate Limit					10	V/ms	В
POWER-DOWN CHARACTERISTIC		-			,		
Power-Down Dissipation	Power Down Mode (Hi-Z Output) PDM\ = 0, INPxx = 1, INNxx = 0 PCLKIN = 0 or 1			3	15	mW	А

⁽¹⁾ Test levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.



ELECTRICAL CHARACTERISTICS (any level to any level transitions – 17 level output, 289 unique transitions $^{(1)}$)

All Specifications at: $T_A = 0$ °C to 85°C, VAA = 2.5V, VDD = 5V, VEE = -5V, HV0 = 1.9V, LV0= -1.9V, HV2 = 32V, LV2 = -11.9V, HV1 = +61.1V, LV1 = -20.9V, VCW = 11V, $R_L = 100 \Omega$ to GND for OUTA, $R_L = 100\Omega$ to GND for OUTB, unless otherwise noted.

PARAMETER	CONDITIONS	MIN TYP MAX	UNITS	TEST LEVEL ⁽²⁾
POWER UP/DOWN TIMING				
Power down time		100	ns	С
Power up time		100	ns	С
HVX/LVX SIGNAL PATH – AC PERFORMANCE	•		•	
Mean normalized output rise time	10% to 90% of 0 to 1, 20MHz	5	ns	С
Mean delay (relative to clock edge of 1st sample)	0-20 MHz	23	ns	С
Delay standard deviation	0-20 MHz	1.2	ns	С
Phase standard deviation	5 MHz	0.01	cycles	С
Priase standard deviation	20 MHz	0.03	cycles	С
Gain standard deviation	5 MHz	4	%	С
	20 MHz	8	%	С

⁽¹⁾ These parameters are measured on the differential output starting from 1 of 17 possible states to every other possible state. Therefore, 17X17 = 289 unique transitions.

⁽²⁾ Test levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.



TYPICAL CHARACTERISTICS

 $All \ Specifications \ at: \ T_A = 25^{\circ}C, \ VAA = +2.5V, \ VDD = +5V. \ VEE = -5V, \ HV0 = 1.9V, \ LV0 = -1.9V, \ HV2 = 32V, \ LV2 = -11.9V, \ LV2 = -11.9V, \ LV3 = -11.9V, \ LV4 = -11.9V, \ LV5 = -11.9V, \ LV5 = -11.9V, \ LV6 = -11.9V, \ LV7 = -11.9V, \ LV7 = -11.9V, \ LV8 = -11.9V, \ LV9 = -11.9$ HV1 = +61.1V, LV1 = -20.9V, VCW = 11V, R_L = 100 Ω to GND for OUTA, R_L = 100 Ω to GND for OUTB, unless otherwise noted.

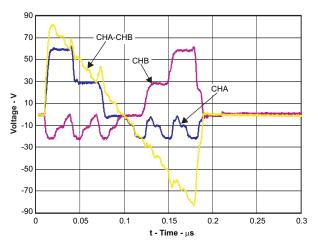


Figure 1. 17-level Outputs with 10ns Pulse Width (100MSPS)

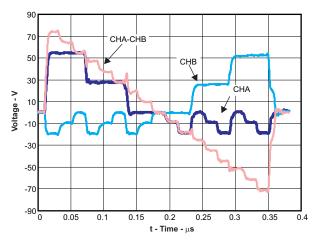


Figure 2. 17-level Outputs with 20ns Pulse Width (50MSPS)

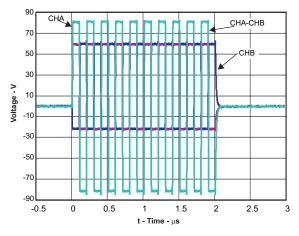


Figure 3. 5MHz 3-level 10 Cycles Outputs



TYPICAL CHARACTERISTICS (continued)

All Specifications at: $T_A = 25^{\circ}C$, VAA = +2.5V, VDD = +5V. VEE = -5V, HV0 = 1.9V, LV0 = -1.9V, HV2 = 32V, LV2 = -11.9V, HV1 = +61.1V, LV1 = -20.9V, VCW = 11V, $R_L = 100\Omega$ to GND for OUTA, $R_L = 100\Omega$ to GND for OUTB, unless otherwise noted

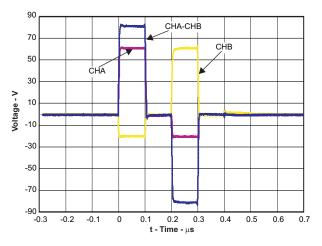


Figure 4. 3-level Outputs with 100ns Pulse Width (10MSPS)

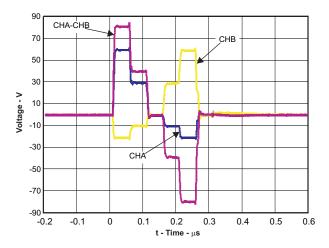


Figure 5. 5MHz 5-level Outputs

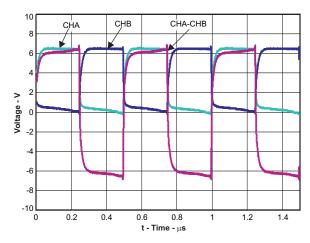


Figure 6. 2MHz CW Outputs



APPLICATION INFORMATION

Table 1. Truth Table

Description	EN	PDM	PCLKIN	CWINA	CWINB	INPxx ⁽¹⁾	INNxx ⁽¹⁾
Power Down (Hi-Z Output)	1	0	x ⁽²⁾	0	0	1	0
CW Mode	Х	0	х	0/1	1/0	1	0
Non-Latch Mode	1	1	х	0	0	0/1	0/1
Latch Mode	0	1	0/1	0	0	0/1	0/1

- (1) The logic device driving the inputs of the TX517 should include means to prevent a 'shoot-thru' fault condition. Any input combination that would result in an INP-input to be Low (0) and an INN-input to be High (1) at the same time on the same output (OUTA or OUTB) could result in permanent damage to the TX517. See also disallowed logic state table. Table 3 is provided for an example of how to properly drive the TX517 data inputs INPxx and INNxx.
- X = don't care state. However, in order to prevent excessive power consumption it is recommended that all unused inputs be tied off to a logic high or logic low. The logic inputs to the device have no internal tie-off's.

Table 2. Disallowed Logic States

Description	EN	PDM	PCLKIN	CWINA	CWINB	INPxA	INNxA	INPxB	INNxB
Disallowed mode 1 (1)	х	Х	х	х	х	0	1	x	x
Disallowed mode 2 ⁽¹⁾	х	Х	х	х	х	х	х	0	1
Disallowed mode 3 ⁽²⁾	х	0	х	х	х	х	1	x	x
Disallowed mode 4 ⁽²⁾	х	0	х	х	х	х	х	x	1
Disallowed mode 5 ⁽²⁾	х	0	х	х	х	0	х	x	x
Disallowed mode 6 ⁽²⁾	х	0	х	х	х	х	х	0	x
Disallowed mode 7 ⁽³⁾	0	Х	0	х	х	х	х	x	x

- This logic state causes a 'shoot-thru' fault condition that could result in permanent damage to the TX517.
- This logic state causes a high power consumption condition in the internal logic circuitry of the TX517 and could result in a long term reliability failure of the TX517.
- This disallowed logic state is only valid for DC conditions. i.e. it is not allowed to keep PCLKIN at a low logic state when EN\ is at a low logic state. This causes a high power consumption condition in the internal logic circuitry of the TX517. However, it is acceptable to drive EN\ low and drive PCLKIN with a clock waveform under the recommended operating conditions for PCLKIN.

Table 3. Example Input Data Set of a 17-Level Output⁽¹⁾

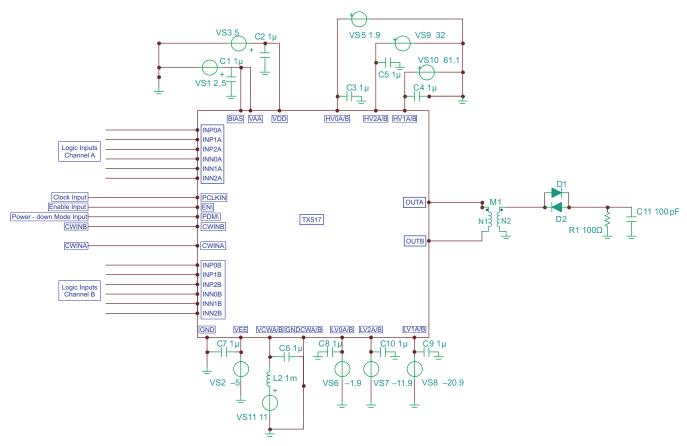
Output Level	INP0A	INP2A	INP1A	INP1B	INP2B	INP0B	INN0A	INN2A	INN1A	INN1B	INN2B	INN0B
8	0	0	1	0	0	0	0	0	0	1	0	0
7	0	0	1	0	0	0	0	0	0	0	1	0
6	0	0	1	0	0	1	0	0	0	0	0	1
5	0	1	0	0	0	0	0	0	0	1	0	0
4	0	1	0	0	0	0	0	0	0	0	1	0
3	0	1	0	0	0	1	0	0	0	0	0	1
2	1	0	0	0	0	0	1	0	0	1	0	0
1	1	0	0	0	0	0	1	0	0	0	1	0
0	1	0	0	0	0	1	1	0	0	0	0	1
-1	0	0	0	0	0	1	0	1	0	0	0	1
-2	0	0	0	0	0	1	0	0	1	0	0	1
-3	1	0	0	0	1	0	1	0	0	0	0	0
-4	0	0	0	0	1	0	0	1	0	0	0	0
-5	0	0	0	0	1	0	0	0	1	0	0	0
-6	1	0	0	1	0	0	1	0	0	0	0	0
-7	0	0	0	1	0	0	0	1	0	0	0	0
-8	0	0	0	1	0	0	0	0	1	0	0	0
off state	0	0	0	0	0	0	0	0	0	0	0	0

The levels listed in this table are active high; the P signals need to be inverted before driving the chip. This note is only applicable to THIS particular table ("the example input data set of a 17-level output).



Table 4. Power Supplies Sequence

	1	2	3	4
Power-up	Driver Supplies(VEE, VAA, VDD)	LV1	HV1	LV2, LV0, HV0, HV2, VCW
Power-down	VCW, HV2, HV0, LV0, LV2	HV1	LV1	Driver Supplies (VDD, VAA, VEE)

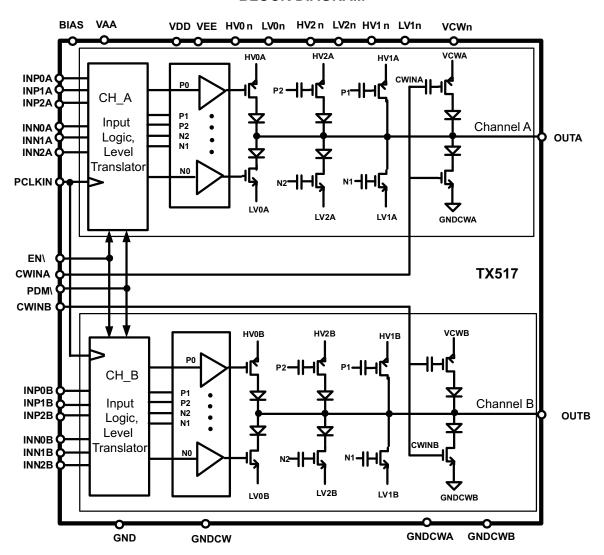


- A. Diodes D1, D2 placeholders only; choose appropriate model (e.g. MMBD3004S)
- B. Load resistor R1, and capacitor C11 usage and values may vary depending on final configuration
- C. Bypass capacitors and values on all supplies are placeholders only. Capacitors between various supply rails may also be necessary.
- D. Inductors (ferrite beads) L1, L2 are optional components
- E. Voltages levels on the voltage supplies correspond to the ones used at simulation

Figure 7. Typical Device Configuration



BLOCK DIAGRAM



TIMING RELATED INFORMATION

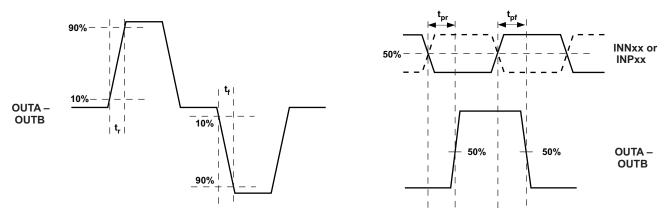


Figure 8. Output Timing Information



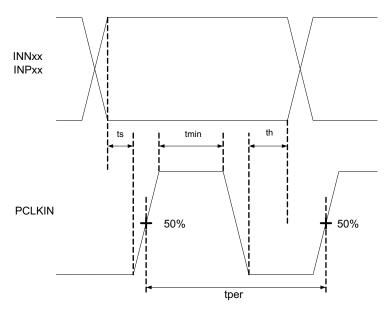
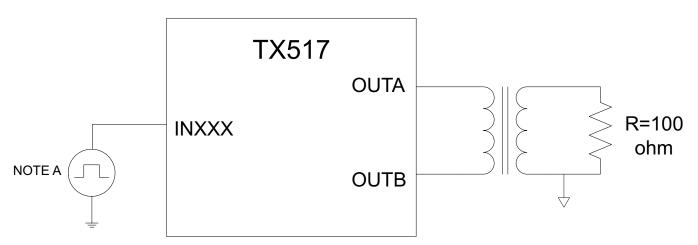


Figure 9. Timing Waveform for Latch Mode



Note A: This signal is supplied by a function generator with the following characteristics: 0 to 2.5V square wave, tr/tf < 3ns, frequency as noted in the electrical characteristics.

Figure 10. Loading for Power Consumption Tests



REVISION HISTORY

Cł	Changes from Original (September 2011) to Revision A							
•	Fixed duty cycle typo, changed duty cycle from 5% to 100% for "Dynamic Current Consumption (CW Mode) Power supply VCWA + VCWB" in the ELECTRICAL CHARACTERISTICS table.	9						
•	Fixed duty cycle typo, changed duty cycle from 5% to 100% for "Total Power Dissipation for device only (CW Mode)" in the ELECTRICAL CHARACTERISTICS table.	9						



PACKAGE OPTION ADDENDUM

5-Jan-2012

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TX517IZCQ	ACTIVE	NFBGA	ZCQ	144	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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