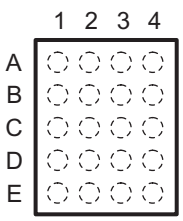
SD CARD VOLTAGE-TRANSLATION TRANSCEIVER

Check for Samples: TXS0206A

FEATURES

- **Level Translator**
  - **V_{CCA} and V_{CCB} Range of 1.1 V to 3.6 V**
  - **Fast Propagation Delay (4.4 ns Max When Translating Between 1.8 V and 3 V)**
- **ESD Protection Exceeds JESD 22**
  - **2500-V Human-Body Model (A114-B)**
  - **250-V Machine Model (A115-A)**
  - **1500-V Charged-Device Model (C101)**

YFP PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS

	1	2	3	4
A	DAT2A	V_{CCA}	WP	DAT2B
B	DAT3A	CD	V_{CCB}	DAT3B
C	CMDA	GND	GND	CMDB
D	DAT0A	CLKA	CLKB	DAT0B
E	DAT1A	CLK-f	EN	DAT1B

DESCRIPTION/ORDERING INFORMATION

The TXS0206A is a level shifter for interfacing microprocessors with MultiMediaCards (MMCs), secure digital (SD) cards, and Memory Stick™ cards.

The voltage-level translator has two supply voltage pins. V_{CCA} as well as V_{CCB} can be operated over the full range of 1.1 V to 3.6 V. The TXS0206A enables system designers to easily interface applications processors or digital basebands to memory cards and SDIO peripherals operating at a different I/O voltage level.

The TXS0206A is offered in a 20-bump wafer chip scale package (WCSP). This package has dimensions of 1.96 mm × 1.56 mm, with a 0.4-mm ball pitch for effective board-space savings. Memory cards are widely used in mobile phones, PDAs, digital cameras, personal media players, camcorders, set-top boxes, etc. Low static power consumption and small package size make the TXS0206A an ideal choice for these applications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	WCSP – YFP (Pb-free)	Tape and reel	TXS0206AYFPR	BTR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

REFERENCE CIRCUIT

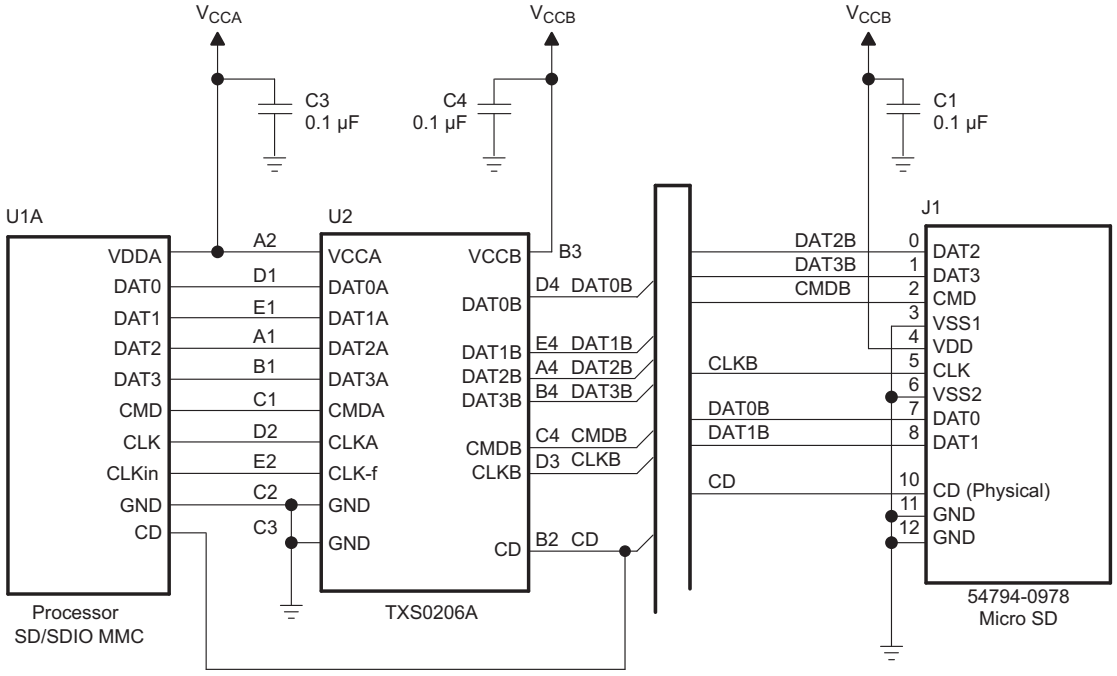


Figure 1. Interfacing With SD/SDIO Card

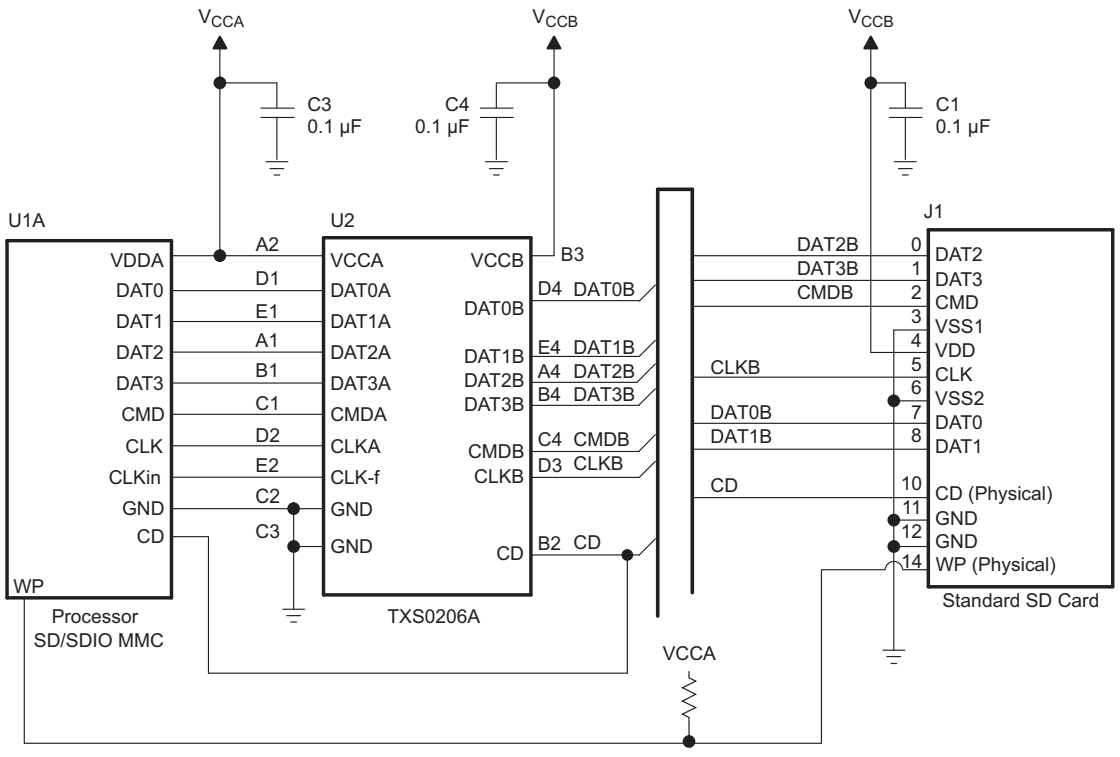
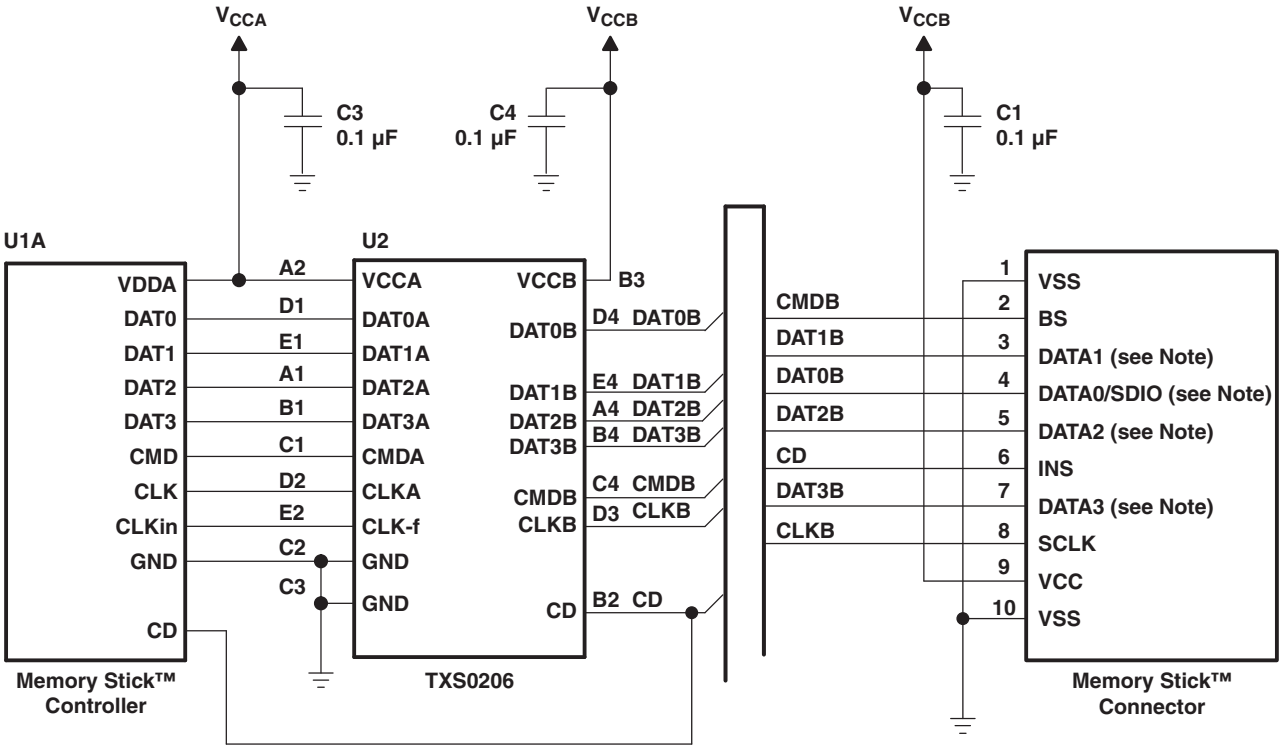


Figure 2. Interfacing With Seperate WP and CD Pin



NOTE: The TXS0206A has integrated pullup resistor values that dynamically change value depending on whether a low or high signal is being transmitted through the device. When the output is low, the TXS0206A internal pullup value is 40 kΩ, and when the output is high, the internal pullup value change to a value of 4 kΩ. For MSA and MSH Memory Stick™ memory cards, to ensure that a valid V_{IH} (i.e., receiver input voltage high) is achieved, the internal pulldown resistors for these memory cards are not smaller than a 10-kΩ value. See the *Application Information* section of this data sheet, which explains the impact of adding too heavy (i.e., <10-kΩ value) of a pulldown resistor to the data lines of the TXS0206A device and the resulting 4-kΩ pullup/10-kΩ pulldown voltage divider network, which has a direct impact on the V_{IH} of the signal being sent into the Memory Stick™.

Figure 3. Interfacing With Memory Stick™ Card

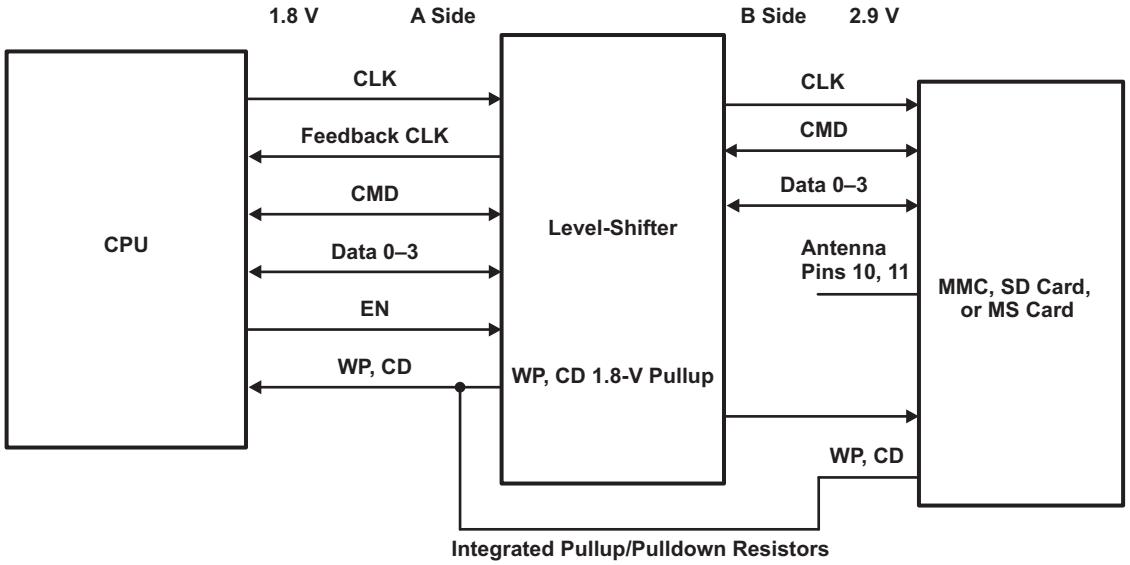


Figure 4. Typical Application Circuit

LOGIC TABLE

EN	TRANSLATOR I/Os
L	Disabled, pulled to V_{CCA}, V_{CCB} through 40 kΩ
H	Active

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
A1	DAT2A	I/O	Data bit 2 connected to host. Referenced to V_{CCA}. Includes a 40-kΩ pullup resistor to V_{CCA}.
A2	V_{CCA}	Pwr	A-port supply voltage. V_{CCA} powers all A-port I/Os and control inputs.
A3	WP	O	Connected to write protect on the mechanical connector. The WP pin has an internal 100-kΩ pullup resistor to V_{CCA}.
A4	DAT2B	I/O	Data bit 2 connected to memory card. Referenced to V_{CCB}. Includes a 40-kΩ pullup resistor to V_{CCB}.
B1	DAT3A	I/O	Data bit 3 connected to host. Referenced to V_{CCA}. Includes a 40-kΩ pullup resistor to V_{CCA}.
B2	CD	O	Connected to card detect on the mechanical connector. The CD pin has an internal 100-kΩ pullup resistor to V_{CCA}.
B3	V_{CCB}	Pwr	B-port supply voltage. V_{CCB} powers all B-port I/Os.
B4	DAT3B	I/O	Data bit 3 connected to memory card. Referenced to V_{CCB}. Includes a 40-kΩ pullup resistor to V_{CCB}.
C1	CMDA	I/O	Command bit connected to host. Referenced to V_{CCA}. Includes a 40-kΩ pullup resistor to V_{CCA}.
C2, C3	GND		Ground
C4	CMDB	I/O	Command bit connected to memory card. Referenced to V_{CCB}. Includes a 40-kΩ pullup resistor to V_{CCB}.
D1	DAT0A	I/O	Data bit 0 connected to host. Referenced to V_{CCA}. Includes a 40-kΩ pullup resistor to V_{CCA}.
D2	CLKA	I	Clock signal connected to host. Referenced to V_{CCA}.
D3	CLKB	O	Clock signal connected to memory card. Referenced to V_{CCB}.
D4	DAT0B	I/O	Data bit 0 connected to memory card. Referenced to V_{CCB}. Includes a 40-kΩ pullup resistor to V_{CCB}.
E1	DAT1A	I/O	Data bit 1 connected to host. Referenced to V_{CCA}. Includes a 40-kΩ pullup resistor to V_{CCA}.
E2	CLK-f	O	Clock feedback to host for resynchronizing data to a processor. Leave unconnected if not used.
E3	EN	I	Enable/disable control. Pull EN low to place all outputs in Hi-Z state. Referenced to V_{CCA}.
E4	DAT1B	I/O	Data bit 1 connected to memory card. Referenced to V_{CCB}. Includes a 40-kΩ pullup resistor to V_{CCB}.

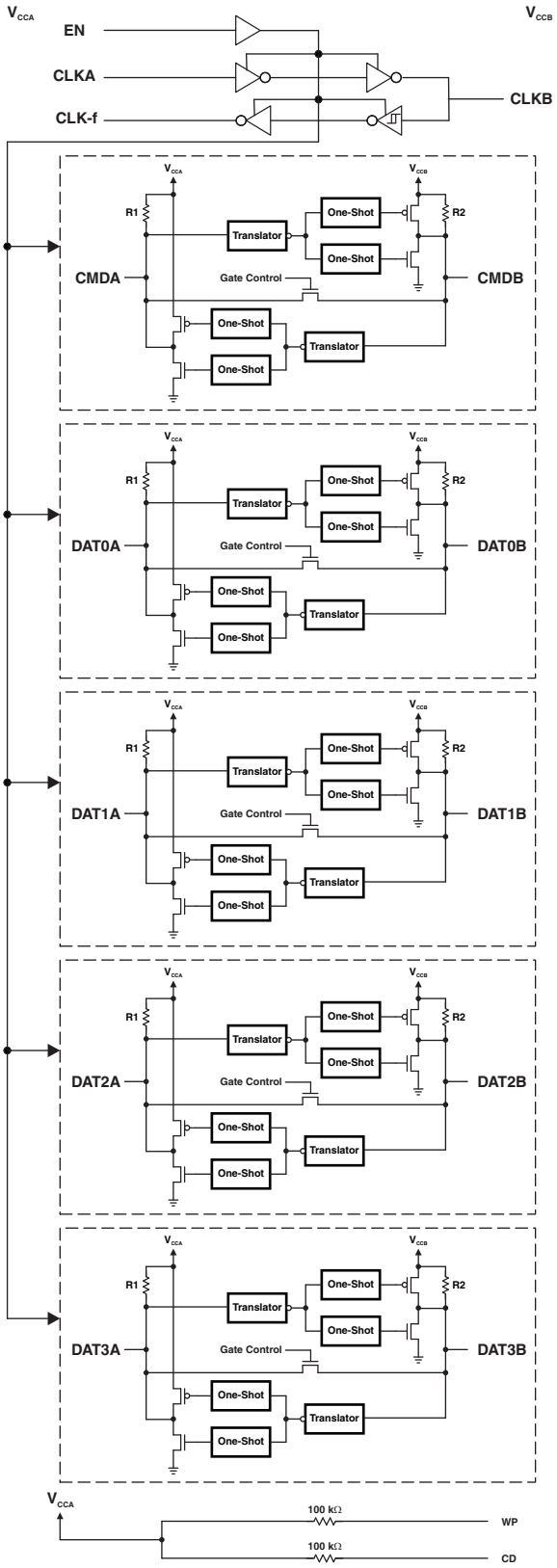
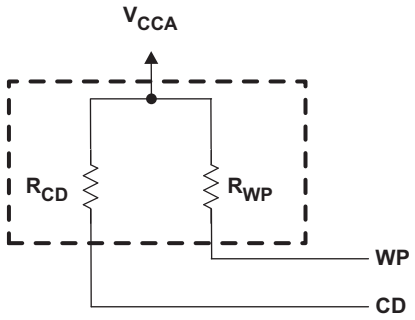


Figure 5. Logic Diagram



RESISTORS	
R_{WP}, R_{CD}	100 kΩ
Tolerance	±30%

Figure 6. WP, CD Pullup Resistors

ABSOLUTE MAXIMUM RATINGS(1)
Level Translator

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	4.6	V
V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state	A port	–0.5	4.6	V
		B port	–0.5	4.6	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE RATINGS

			UNIT
θ_{JA}	Package thermal impedance(1)	117	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)
Level Translator

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.1	3.6	V
V_{CCB}	Supply voltage				1.1	3.6	V
V_{IH}	High-level input voltage	A-Port CMD and DATA I/Os B-Port CMD and DATA I/Os	1.1 V to 1.95 V	1.1 V to 1.95 V	V_{CCI} – 0.2	V_{CCI}	V
			1.95 V to 3.6 V	1.95 V to 3.6 V			
		EN and CLKA	1.1 V to 3.6 V	1.1 V to 3.6 V	V_{CCI} x 0.65	V_{CCI}	
V_{IL}	Low-level input voltage	A-Port CMD and DATA I/Os B-Port CMD and DATA I/Os	1.1 V to 1.95 V	1.1 V to 1.95 V	0	0.15	V
			1.95 V to 3.6 V	1.95 V to 3.6 V			
		EN and CLKA	1.1 V to 3.6 V	1.1 V to 3.6 V	0	V_{CCI} x 0.35	
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current (CLK-f output)		1.1 V to 3.6 V	1.1 V to 3.6 V		–100	µA
			1.1 V to 1.3 V			–0.5	mA
			1.4 V to 1.6 V			–1	
			1.65 V to 1.95 V			–2	
			2.3 V to 2.7 V			–4	
			3 V to 3.6 V			–8	
I_{OL}	Low-level output current (CLK-f output)		1.1 V to 3.6 V	1.1 V to 3.6 V		100	µA
			1.1 V to 1.3 V			0.5	mA
			1.4 V to 1.6 V			1	
			1.65 V to 1.95 V			2	
			2.3 V to 2.7 V			4	
			3 V to 3.6 V			8	
I_{OH}	High-level output current (CLK output)		1.1 V to 3.6 V	1.1 V to 3.6 V		–100	µA
				1.1 V to 1.3 V		–0.5	mA
				1.4 V to 1.6 V		–1	
				1.65 V to 1.95 V		–2	
				2.3 V to 2.7 V		–4	
				3 V to 3.6 V		–8	
I_{OL}	Low-level output current (CLK output)		1.1 V to 3.6 V	1.1 V to 3.6 V		100	µA
				1.1 V to 1.3 V		0.5	mA
				1.4 V to 1.6 V		1	
				1.65 V to 1.95 V		2	
				2.3 V to 2.7 V		4	
				3 V to 3.6 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS
Level Translator

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP(1)	MAX	UNIT
V_{OH}	A port (CLK-f output)	I_{OH} = –100 µA	1.1 V to 3.6 V	1.65 V to 3.6 V	V_{CCA} * 0.8			V
		I_{OH} = –0.5 mA	1.1 V		0.8			
		I_{OH} = –1 mA	1.4 V		1.05			
		I_{OH} = –2 mA	1.65 V		1.2			
		I_{OH} = –4 mA	2.3 V		1.75			
		I_{OH} = –8 mA	3 V		2.3			
	A port (DAT and CMD outputs)	I_{OH} = –20 µA	1.1 V to 3.6 V		V_{CCA} × 0.8			
V_{OL}	A port (CLK-f output)	I_{OL} = 100 µA	1.1 V to 3.6 V	1.65 V to 3.6 V			V_{CCA} × 0.2	V
		I_{OL} = 0.5 mA	1.1 V				0.35	
		I_{OL} = 1 mA	1.4 V				0.35	
		I_{OL} = 2 mA	1.65 V				0.45	
		I_{OL} = 4 mA	2.3 V				0.55	
		I_{OL} = 8 mA	3 V				0.7	
	A port (DAT and CMD outputs)	I_{OL} = 135 µA	1.1 V	1.65 V to 3.6 V			0.4	V
		I_{OL} = 180 µA	1.4 V				0.4	
		I_{OL} = 220 µA	1.65 V				0.4	
		I_{OL} = 300 µA	2.3 V				0.4	
		I_{OL} = 400 µA	3 V				0.55	
V_{OH}	B port (CLK output)	I_{OH} = –100 µA	1.1 V to 3.6 V	1.65 V to 3.6 V	V_{CCB} × 0.8			V
		I_{OH} = –2 mA		1.65 V	1.2			
		I_{OH} = –4 mA		2.3 V	1.75			
		I_{OH} = –8 mA		3 V	2.3			
	B port (DAT output)	I_{OH} = –20 µA		1.65 V to 3.6 V	V_{CCB} × 0.8			

(1) All typical values are at T_A = 25°C.

ELECTRICAL CHARACTERISTICS
Level Translator (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	TYP(1)	MAX	UNIT
V_{OL}	B port	I_{OL} = 100 µA		1.1 V to 3.6 V	1.65 V to 3.6 V			V_{CCB} × 0.2	V
		I_{OL} = 2 mA			1.65 V			0.45	
		I_{OL} = 4 mA			2.3 V			0.55	
		I_{OL} = 8 mA			3 V			0.7	
	B port (DAT output)	I_{OL} = 135 µA		1.1 V to 3.6 V	1.65 V to 3.6 V			0.4	V
		I_{OL} = 220 µA			1.65 V			0.4	
		I_{OL} = 300 µA			2.3 V			0.4	
		I_{OL} = 300 µA			3 V			0.55	
I_I	Control inputs	V_I = V_{CCA} or GND			1.65 V to 3.6 V			±1	µA
I_{CCA}		V_I = V_{CCI}	I_O = 0	1.1 V to 3.6 V	1.65 V to 3.6 V			7	µA
I_{CCB}		V_I = V_{CCI}	I_O = 0	1.1 V to 3.6 V	1.65 V to 3.6 V			11	µA
C_{io}	A port						5.5	6.5	pF
	B port						7	9.5	
C_i	Control inputs	V_I = V_{CCA} or GND					3.5	4.5	pF
	Clock input						3	4	

TIMING REQUIREMENTS
V_{CCA} = 1.2 V ± 0.1 V

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
Data rate	Command	Push-pull driving		40		40	Mbps
		Open-drain driving		1		1	
	Clock	Push-pull driving		40		40	MHz
	Data			40		40	Mbps
t_W Pulse duration	Command	Push-pull driving	25		25		ns
		Open-drain driving	1		1		µs
	Clock	Push-pull driving	10		8.3		ns
	Data		25		25		ns

TIMING REQUIREMENTS
V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
Data rate	Command	Push-pull driving		60		60	Mbps
		Open-drain driving		1		1	
	Clock	Push-pull driving		60		60	MHz
	Data			60		60	Mbps
t_W Pulse duration	Command	Push-pull driving	17		17		ns
		Open-drain driving	1		1		µs
	Clock	Push-pull driving	8.3		8.3		ns
	Data		17		17		ns

TIMING REQUIREMENTS
V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
Data rate	Command	Push-pull driving		60		60	Mbps
		Open-drain driving		1		1	
	Clock	Push-pull driving		55		55	MHz
	Data			60		60	Mbps
t_w Pulse duration	Command	Push-pull driving	17		17		ns
		Open-drain driving	1		1		µs
	Clock	Push-pull driving	9		9		ns
	Data		17		17		ns

SWITCHING CHARACTERISTICS
V_{CCA} = 1.2 V ± 0.1 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	CMDA	CMDB		5.7		4.4	ns
	CMDB	CMDA		6.7		5.8	
	CLKA	CLKB		6.2		4.5	
	DATxA	DATxB		7.6		7.5	
	DATxB	DATxA		6.3		4.6	
	CLKA	CLK-f		12		7.9	
t_{en}	EN	B-port		1		1	µs
	EN	A-port		1		1	
t_{dis}	EN	B-port		412		363	ns
	EN	A-port		423		422	
t_{rA}	CMDA rise time		3.5	8.4	3.4	8.1	ns
	CLK-f rise time		1	4.7	1	4.1	
	DATxA rise time		3.5	8.4	3.4	8.1	
t_{rB}	CMDB rise time		1.4	6.5	0.6	3.1	ns
	CLKB rise time		0.6	5.9	0.5	4.3	
	DATxB rise time		1.4	10.9	0.6	5	
t_{fA}	CMDA fall time		2.4	5.7	2	5.1	ns
	CLK-f fall time		0.8	2.5	0.8	3	
	DATxA fall time		2.4	5.7	1.9	5.1	
t_{fB}	CMDB fall time		1.2	5.4	0.6	3.6	ns
	CLKB fall time		0.6	6.3	0.5	4	
	DATxB fall time		0.6	6.3	0.5	3.6	
$t_{SK(O)}$	Channel-to-channel skew			1		1	ns
Max data rate	Command	Push-pull driving		40		40	Mbps
		Open-drain driving		1		1	
	Clock			40		60	MHz
	Data			40		40	Mbps

SWITCHING CHARACTERISTICS
V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	CMDA	CMDB		4.9		3.3	ns
	CMDB	CMDA		5.6		3.6	
	CLKA	CLKB		5.4		3.4	
	DATxA	DATxB		5		4.4	
	DATxB	DATxA		5.4		3.5	
	CLKA	CLK-f		10.2		5.7	
t_{en}	EN	B-port		1		1	µs
	EN	A-port		1		1	
t_{dis}	EN	B-port		411		411	ns
	EN	A-port		413		361	
t_{rA}	CMDA rise time		2.1	4.5	2.1	4.1	ns
	CLK-f rise time		0.6	2.5	0.6	2.3	
	DATxA rise time		1.8	4.5	1.8	4.2	
t_{rB}	CMDB rise time		1.4	6.6	0.7	3.8	ns
	CLKB rise time		0.5	5.8	0.5	4.4	
	DATxB rise time		1.4	10.8	0.7	8	
t_{fA}	CMDA fall time		0.4	3.4	0.3	2.9	ns
	CLK-f fall time		0.3	2.8	0.3	2.8	
	DATxA fall time		0.4	3.4	0.3	2.9	
t_{fB}	CMDB fall time		1.1	6.3	0.6	3.7	ns
	CLKB fall time		0.6	8.7	0.5	4.1	
	DATxB fall time		1.2	7	0.2	4	
$t_{SK(O)}$	Channel-to-channel skew			1		1	ns
Max data rate	Command	Push-pull driving		60		60	Mbps
		Open-drain driving		1		1	
	Clock			60		60	MHz
	Data			60		60	Mbps

SWITCHING CHARACTERISTICS
V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	CMDA	CMDB		5.3		3.2	ns
	CMDB	CMDA		5.1		3	
	CLKA	CLKB		4.8		3.1	
	DATxA	DATxB		5.1		3.2	
	DATxB	DATxA		9.6		5.1	
	CLKA	CLK-f		6.8		4.2	
t_{en}	EN	B-port		1		1	µs
	EN	A-port		1		1	
t_{dis}	EN	B-port		410		364	ns
	EN	A-port		396		398	
t_{rA}	CMDA rise time		1.4	4.2	1.4	4.2	ns
	CLK-f rise time		0.5	1.5	0.5	1.4	
	DATxA rise time		1.4	3.4	1.3	3	
t_{rB}	CMDB rise time		1.4	6.4	0.9	4	ns
	CLKB rise time		0.6	5.9	0.5	4.4	
	DATxB rise time		1.4	14	0.9	14	
t_{fA}	CMDA fall time		0.8	2.3	0.8	2.3	ns
	CLK-f fall time		0.4	1.3	0.4	1.3	
	DATxA fall time		0.8	2.2	0.7	2	
t_{fB}	CMDB fall time		0.8	6.2	0.8	5	ns
	CLKB fall time		0.6	7.8	0.5	4.3	
	DATxB fall time		0.7	6.8	0.6	5	
$t_{SK(O)}$	Channel-to-channel skew			1		1	ns
Max data rate	Command	Push-pull driving		60		60	Mbps
		Open-drain driving		1		1	
	Clock			55		55	MHz
	Data			60		60	Mbps

OPERATING CHARACTERISTICS

T_A = 25°C, V_{CCA} = 1.2 V

PARAMETER			TEST CONDITIONS	V_{CCB} TYP		UNIT
				1.8 V	3.3 V	
C_{pdA} (1)	A-port input, B-port output	CLK Enabled	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	15.1	15	pF
		DATA Enabled		9.26	9.19	
	B-port input, A-port output	DATA Enabled		12.4	11.9	
	A-port input, B-port output	CLK Disabled		0.1	0.1	
		DATA Disabled		1.3	1.3	
	B-port input, A-port output	DATA Disabled		0.1	0.1	

(1) Power dissipation capacitance per transceiver

OPERATING CHARACTERISTICS (continued)

T_A = 25°C, V_{CCA} = 1.2 V

PARAMETER			TEST CONDITIONS	V_{CCB} TYP		UNIT
				1.8 V	3.3 V	
C_{pdB} (1)	A-port input, B-port output	DATA Enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	26.7	30.3	pF
	B-port input, A-port output	CLK Enabled		25.6	27	
		DATA Enabled		16.38	19.91	
	A-port input, B-port output	DATA Disabled		0.1	0.1	
	B-port input, A-port output	CLK Disabled		0.1	0.1	
		DATA Disabled		1.1	0.8	

OPERATING CHARACTERISTICS

T_A = 25°C, V_{CCA} = 1.8 V

PARAMETER			TEST CONDITIONS	V_{CCB} TYP		UNIT
				1.8 V	3.3 V	
C_{pdA} (1)	A-port input, B-port output	CLK Enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	17.5	17.1	pF
		DATA Enabled		9.96	9.82	
	B-port input, A-port output	DATA Enabled		15.6	14	
	A-port input, B-port output	CLK Disabled		0.1	0.1	
		DATA Disabled		1.3	1.3	
	B-port input, A-port output	DATA Disabled		0.1	0.1	
C_{pdB} (1)	A-port input, B-port output	DATA Enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	26	28.5	pF
	B-port input, A-port output	CLK Enabled		25.8	27	
		DATA Enabled		16.69	19.60	
	A-port input, B-port output	DATA Disabled		0.1	0.1	
	B-port input, A-port output	CLK Disabled		0.1	0.1	
		DATA Disabled		1.1	0.8	

(1) Power dissipation capacitance per transceiver

OPERATING CHARACTERISTICS

T_A = 25°C, V_{CCA} = 3.3 V

PARAMETER			TEST CONDITIONS	V_{CCB} TYP		UNIT
				1.8 V	3.3 V	
C_{pdA} (1)	A-port input, B-port output	CLK Enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	17.5	17.1	pF
		DATA Enabled		12.50	13.29	
	B-port input, A-port output	DATA Enabled		15.6	14	
	A-port input, B-port output	CLK Disabled		0.1	0.1	
		DATA Disabled		1.3	1.3	
	B-port input, A-port output	DATA Disabled		0.1	0.1	

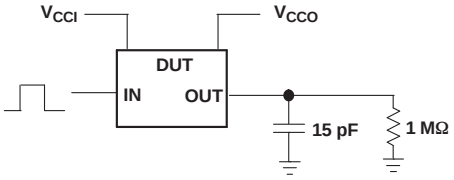
(1) Power dissipation capacitance per transceiver

OPERATING CHARACTERISTICS (continued)

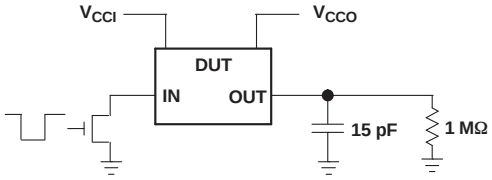
T_A = 25°C, V_{CCA} = 3.3 V

PARAMETER			TEST CONDITIONS	V_{CCB} TYP		UNIT
				1.8 V	3.3 V	
C_{pdB} (1)	A-port input, B-port output	DATA Enabled	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	26	28.5	pF
	B-port input, A-port output	CLK Enabled		25.8	27	
		DATA Enabled		16.67	19.92	
	A-port input, B-port output	DATA Disabled		0.1	0.1	
	B-port input, A-port output	CLK Disabled		0.1	0.1	
		DATA Disabled		1.1	0.8	

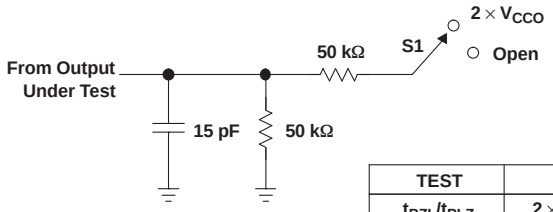
PARAMETER MEASUREMENT INFORMATION



DATA RATE, PULSE DURATION, PROPAGATION DELAY, OUTPUT RISE AND FALL TIME MEASUREMENT USING A PUSH-PULL DRIVER

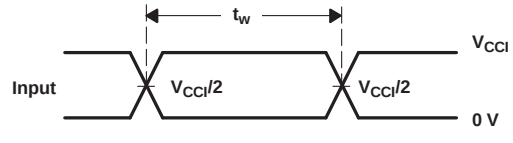


DATA RATE, PULSE DURATION, PROPAGATION DELAY, OUTPUT RISE AND FALL TIME MEASUREMENT USING AN OPEN-DRAIN DRIVER

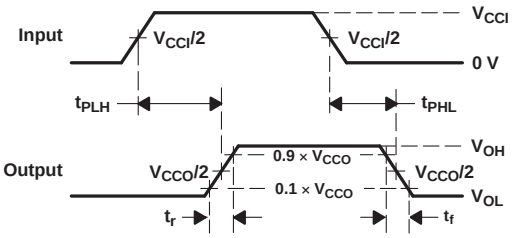


TEST	S1
t_{PZL}/t_{PLZ} t_{PHZ}/t_{PZH}	$2 \times V_{CCO}$ Open

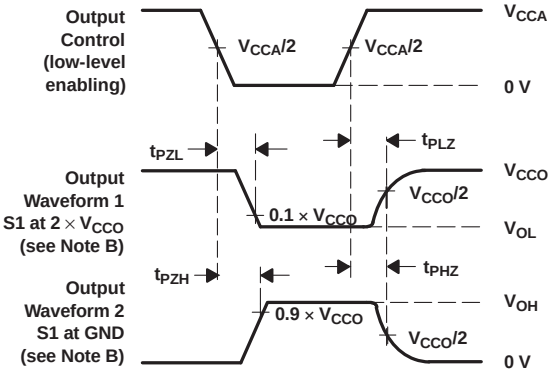
LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

Figure 7. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

The TXS0206A has integrated pullup resistors on the data and command ports and their values dynamically change. When the port is in a low signal state, there is a nominal pullup resistor value of 40 kΩ, and power consumption is minimized. When the port is in a high signal state, the nominal pullup resistor value changes to 4 kΩ, and simultaneous switching performance is improved as a result. The threshold at which the resistance changes is approximately $V_{CCx}/2$.

When using the TXS0206A device with MMCs, SD, and Memory Stick™ to ensure that a valid receiver input voltage high (V_{IH}) is achieved, the value of any pulldown resistors (external or internal to a memory card) must not be smaller than a 10-kΩ value. The impact of adding too heavy (i.e., <10-kΩ value) a pulldown resistor to the data and command lines of the TXS0206A device and the resulting 4-kΩ pullup / 10-kΩ pulldown voltage divider network has a direct impact on the V_{IH} of the signal being sent into the memory card and its associated logic.

The resulting V_{IH} voltage for the 10-kΩ pulldown resistor value would be:

$V_{CC} \times 10\ k\Omega / (10\ k\Omega + 4\ k\Omega) = 0.714 \times V_{CC}$

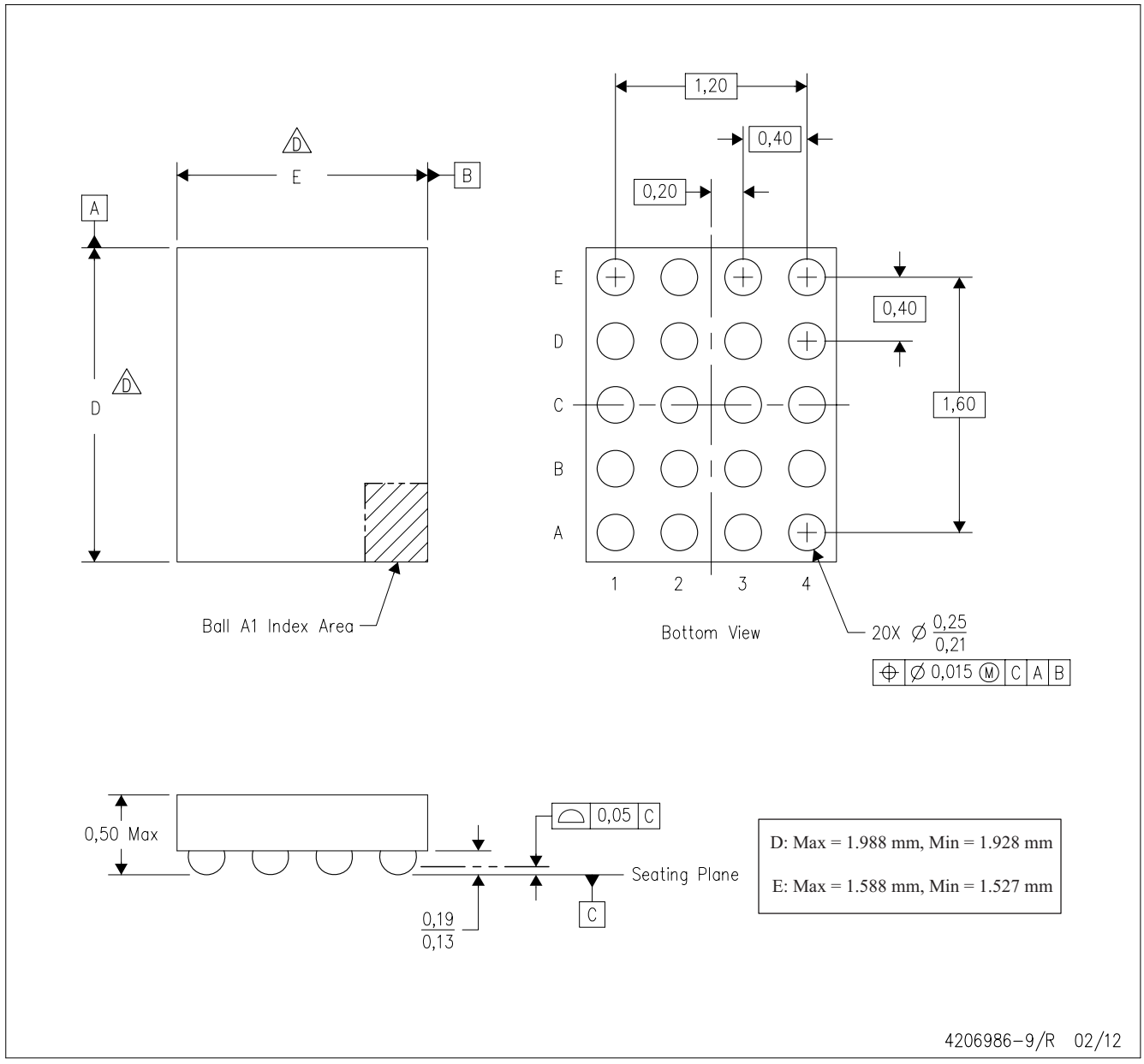
This is marginally above a valid input high voltage for a 1.8-V signal (i.e., $0.65 \times V_{CC}$).

The resulting V_{IH} voltage for 20-kΩ pulldown resistor value would be:

$V_{CC} \times 20\ k\Omega / (20\ k\Omega + 4\ k\Omega) = 0.833 \times V_{CC}$

Which is above the valid input high voltage for a 1.8-V signal of $0.65 \times V_{CC}$.

YFP (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population.
2 x 2 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

NanoFree is a trademark of Texas Instruments

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS0206AYFPR	ACTIVE	DSBGA	YFP	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TXS0206A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

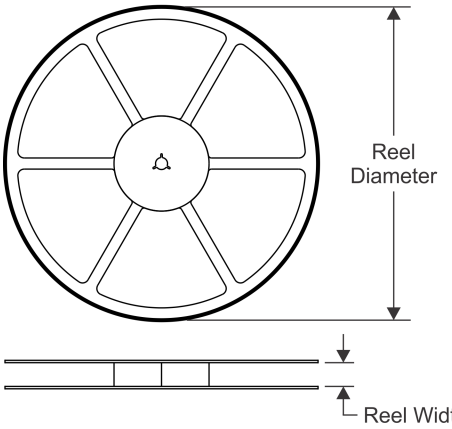
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

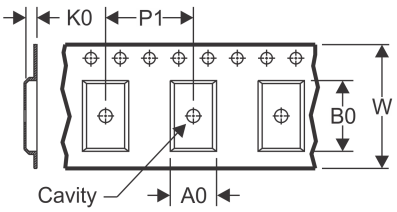
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

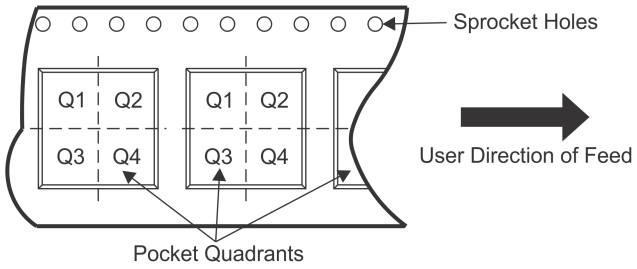


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

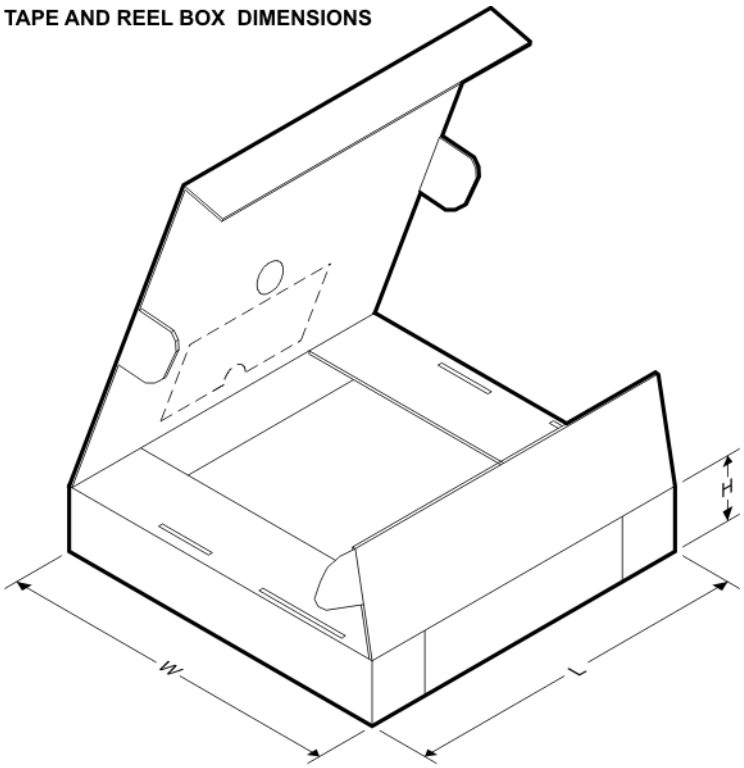
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0206AYFPR	DSBGA	YFP	20	3000	180.0	8.4	1.66	2.06	0.56	4.0	8.0	Q1

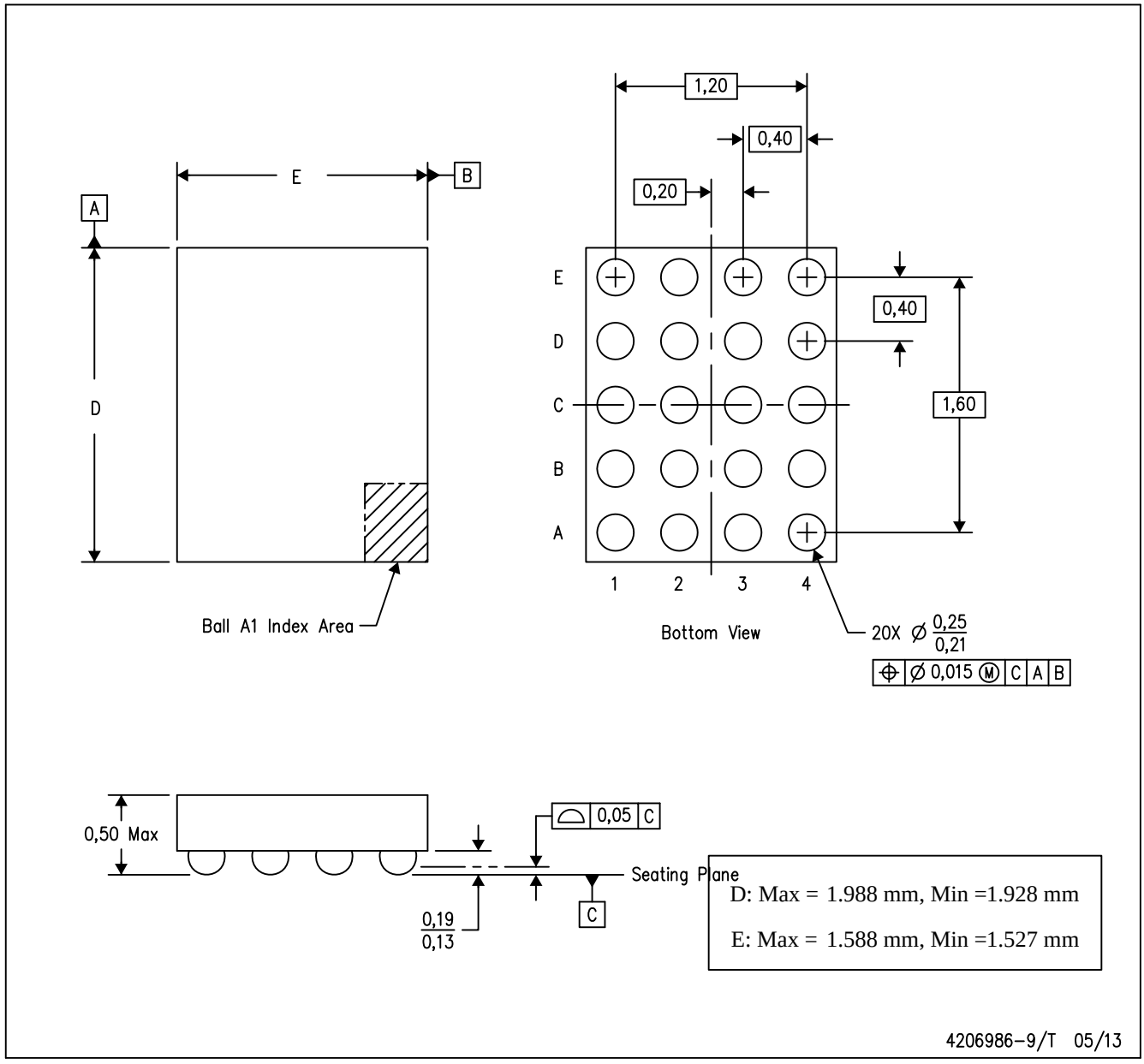
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0206AYFPR	DSBGA	YFP	20	3000	182.0	182.0	17.0

YFP (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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