SINGLE 9-A HIGH-SPEED LOW-SIDE MOSFET DRIVER WITH ENABLE

Check for Samples: UCC27321-Q1, UCC27322-Q1

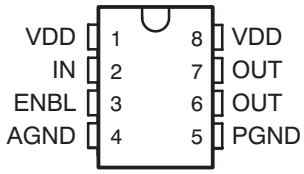
FEATURES

- **Qualified for Automotive Applications**
- **Industry-Standard Pinout With Addition of Enable Function**
- **High Peak-Current Drive Capability of ±9 A at the Miller Plateau Region Using TrueDrive™ Technology**
- **Efficient Constant-Current Sourcing Using a Unique Bipolar and CMOS Output Stage**
- **TTL-/CMOS-Compatible Inputs Independent of Supply Voltage**
- **20-ns Typical Rise and 15-ns Typical Fall Times With 10-nF Load**
- **Typical Propagation Delay Times of 25 ns With Input Falling and 35 ns With Input Rising**
- **4-V to 15-V Supply Voltage**
- **Available in Thermally Enhanced MSOP PowerPAD™ Package With 4.7°C/W θ_{JC}**
- **Rated From –40°C to 125°C**
- **TrueDrive Output Architecture Using Bipolar and CMOS Transistors in Parallel**

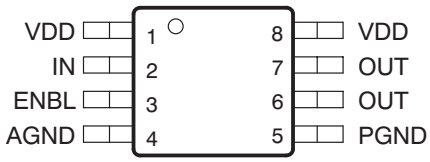
APPLICATIONS

- **Switch-Mode Power Supplies**
- **DC/DC Converters**
- **Motor Controllers**
- **Line Drivers**
- **Class-D Switching Amplifiers**
- **Pulse Transformer Driver**

D PACKAGE
(TOP VIEW)

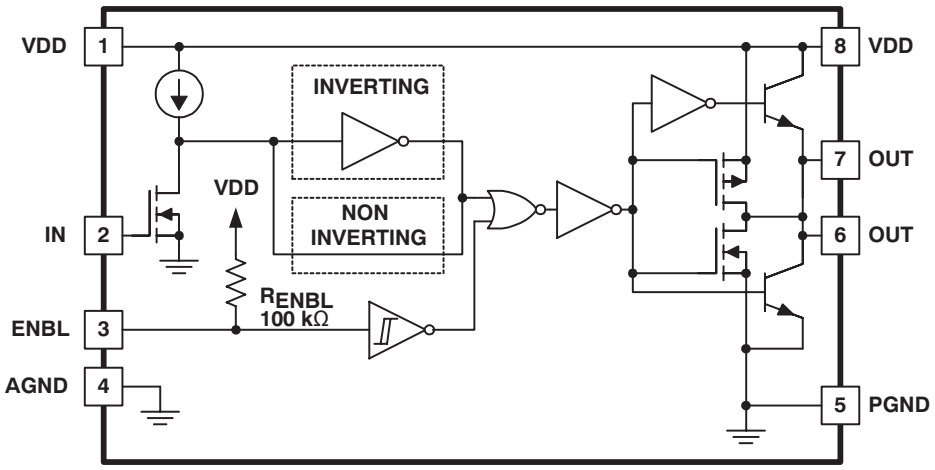


DGN PACKAGE
(TOP VIEW)



DESCRIPTION

The UCC37321/2 family of high-speed drivers delivers 9 A of peak drive current in an industry-standard pinout. These drivers can drive the largest of MOSFETs for systems requiring extreme Miller current due to high dV/dt transitions. This eliminates additional external circuits and can replace multiple components to reduce space, design complexity, and assembly cost. Two standard logic options are offered, inverting (UCC37321) and noninverting (UCC37322).



INPUT/OUTPUT TABLE

	ENBL	IN	OUT
INVERTING UCC37321	0	0	0
	0	1	0
	1	0	1
	1	1	0
NON INVERTING UCC37322	0	0	0
	0	1	0
	1	0	0
	1	1	1

Using a design that inherently minimizes shoot-through current, the outputs of these devices can provide high gate drive current where it is most needed at the Miller plateau region during the MOSFET switching transition. A unique hybrid output stage paralleling bipolar and MOSFET transistors (TrueDrive) allows efficient current delivery at low supply voltages. With this drive architecture, UCC37321/2 can be used in industry standard 6-A, 9-A and many 12-A driver applications. Latch-up and ESD protection circuits are also included. Finally, the UCC37321/2 provides an enable (ENBL) function to have better control of the operation of the driver applications. ENBL is implemented on pin 3, which was previously left unused in the industry-standard pinout. It is internally pulled up to VDD for active-high logic and can be left open for standard operation.

In addition to SOIC-8 (D) package offerings, the UCC37321/2 also comes in the thermally enhanced but tiny 8-pin MSOP PowerPAD (DGN) package. The PowerPAD package drastically lowers the thermal resistance to extend the temperature operation range and improve the long-term reliability.

ORDERING INFORMATION(1)

$T_A = T_J$	OUTPUT CONFIGURATION	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	Inverting	SOIC – D	Reel of 2500	UCC27321QDRQ1	27321Q
	Noninverting	SOIC – D	Reel of 2500	UCC27322QDRQ1	27322Q
		PowerPAD – DGN	Reel of 2500	UCC27322QDGNRQ1	EACQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Table 1. TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	4	—	Common ground for input stage. This ground should be connected very closely to the source of the power MOSFET which the driver is driving. Grounds are separated to minimize ringing affects due to output switching di/dt,l which can affect the input threshold.
ENBL	3	I	Enable input for the driver with logic-compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to VDD with a 100-kΩ resistor for active-high operation. The output state when the device is disabled is low, regardless of the input state.
IN	2	I	Input signal of the driver, which has logic-compatible threshold and hysteresis.
OUT	6, 7	O	Driver outputs that must be connected together externally. The output stage is capable of providing 9-A peak drive current to the gate of a power MOSFET.
PGND	5	—	Common ground for output stage. This ground should be connected very closely to the source of the power MOSFET which the driver is driving. Grounds are separated to minimize ringing affects due to output switching di/dt, which can affect the input threshold.
VDD	1, 8	I	Supply voltage and the power input connections for this device. These pins must be connected together externally.

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage		–0.3 V to 16 V
I_O	Output current, OUT		0.6 A
V_I	Input voltage	IN	–5 V to 6 V or V_{DD} + 0.3 V (whichever is larger)
		ENBL	–5 V to 6 V or V_{DD} + 0.3 V (whichever is larger)
P_D	Power dissipation at T_A = 25°C	D package	650 mW
		DGN package	3 W
T_J	Junction operating temperature		–55°C to 150°C
T_{stg}	Storage temperature		–65°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

POWER DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING(1) T_A = 70°C (mW)	DERATING FACTOR(1) T_A > 70°C (mW/°C)
D (SOIC-8)	42	84 to 160(2)	344 to 655(2)	6.25 to 11.9(2)
DGN (MSOP-8 PowerPAD)(3)	4.7	50 to 59(2)	1370	17.1

(1) 125°C operating junction temperature is used for power rating calculations.
(2) The range of values indicates the effect of the PCB. These values are intended to give the system designer an indication of the best- and worst-case conditions. In general, the system designer should attempt to use larger traces on the PC board where possible to spread the heat away form the device more effectively. For information on the PowerPAD package, see the technical brief, *PowerPad™ Thermally Enhanced Package*, Texas Instruments literature number SLMA002 and the application brief, *PowerPad™ Made Easy*, Texas Instruments literature number SLMA004.
(3) The PowerPAD thermal pad is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.

OVERALL ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 V to 15 V, T_J = T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Static operating current	UCC27321	IN = Low, ENBL = Low, V_{DD} = 15 V		150	225	µA
					440	650	
			IN = High, ENBL = Low, V_{DD} = 15 V		370	550	
					370	550	
		UCC27322	IN = Low, ENBL = High, V_{DD} = 15 V		150	225	
					450	650	
			IN = High, ENBL = High, V_{DD} = 15 V		75	125	
					675	1000	

INPUT (IN) ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 V to 15 V, T_J = T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Logic 1 input threshold		2			V
V_{IL}	Logic 0 input threshold				1	V
	Input current	0 V ≤ V_{IN} ≤ V_{DD}	–10	0	10	µA
	Latch-up protection(1)		500			mA

(1) Specified by design

OUTPUT (OUT) ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 V to 15 V, T_J = T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Peak output current(1) (2)	V_{DD} = 14 V		9		A
V_{OH}	High-level output voltage	V_{OH} = V_{DD} – V_{OUT}, I_{OUT} = –10 mA		150	300	mV
V_{OL}	Low-level output voltage	I_{OUT} = 10 mA		11	25	mV
	Output resistance high(3)	I_{OUT} = –10 mA, V_{DD} = 14 V		15	25	Ω
	Output resistance low(3)	I_{OUT} = 10 mA, V_{DD} = 14 V		1.1	2.5	Ω
	Latch-up protection(1)		500			mA

(1) Specified by design
(2) The pullup/pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The pulsed output current rating is the combined current from the bipolar and MOSFET transistors.
(3) The pullup/pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

ENABLE (ENBL) ELECTRICAL CHARACTERISTICS

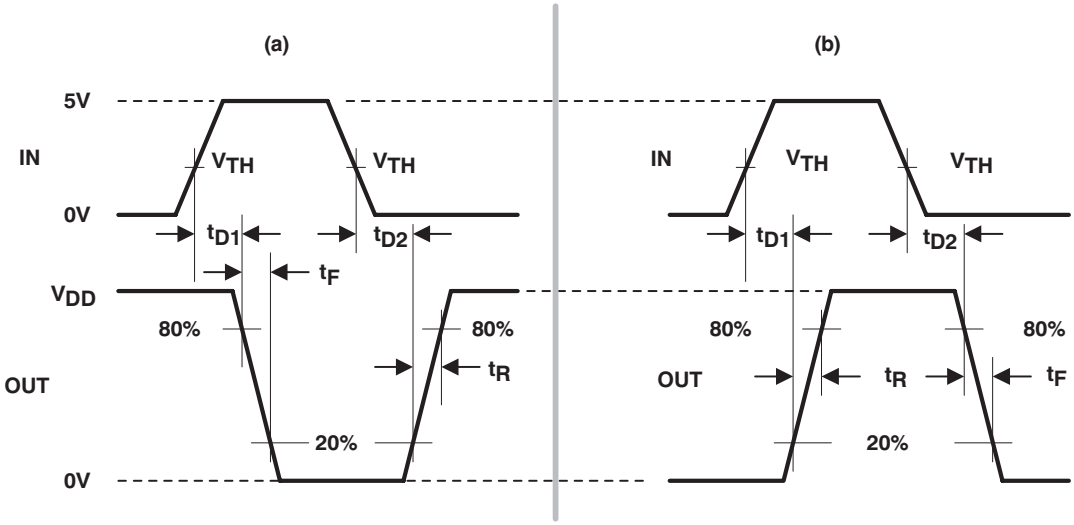
V_{DD} = 4.5 V to 15 V, T_J = T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{EN_H}	Enable rising threshold voltage	Low-to-high transitions	1.5	2.2	2.7	V
V_{EN_L}	Enable falling threshold voltage	High-to-low transition	1.1	1.65	2	V
	Hysteresis		0.18	0.55	0.9	V
$R_{(ENBL)}$	Enable impedance	V_{DD} = 14 V, ENBL = Low	75	100	145	kΩ
t_{D3}	Propagation delay time	C_{LOAD} = 10 nF (see Figure 2)		60	95	ns
t_{D4}	Propagation delay time	C_{LOAD} = 10 nF (see Figure 2)		60	95	ns

SWITCHING CHARACTERISTICS

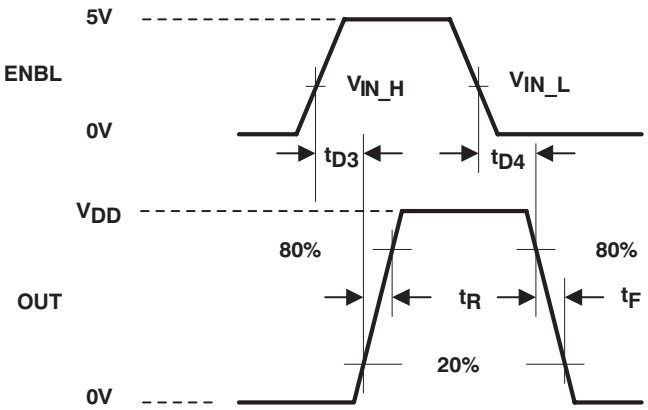
V_{DD} = 4.5 V to 15 V, T_J = T_A = –40°C to 125°C (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time (OUT)	C_{LOAD} = 10 nF		20	75	ns
t_F	Fall time (OUT)	C_{LOAD} = 10 nF		20	35	ns
t_{D1}	Delay time, IN rising (IN to OUT)	C_{LOAD} = 10 nF		25	75	ns
t_{D2}	Delay time, IN falling (IN to OUT)	C_{LOAD} = 10 nF		35	75	ns



A. The 20% and 80% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 1. Switching Waveforms for (a) Inverting Driver and (b) Noninverting Driver



A. The 20% and 80% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 2. Switching Waveforms for Enable to Output

TYPICAL CHARACTERISTICS

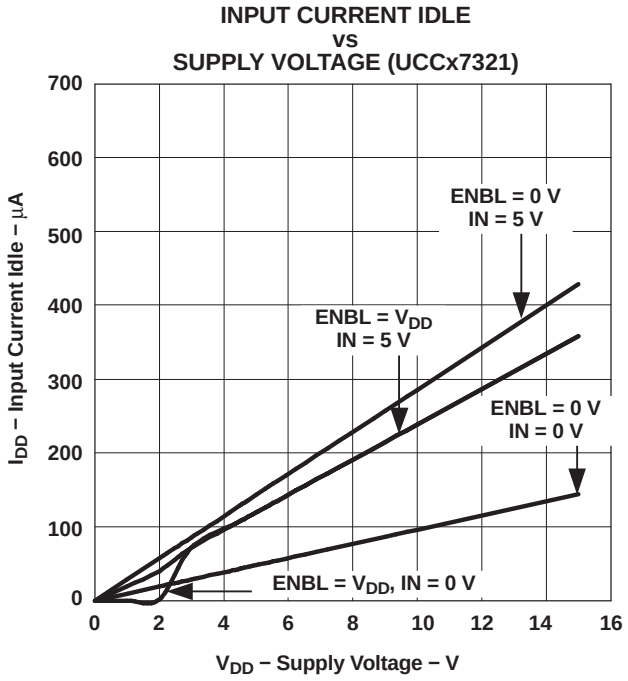


Figure 3.

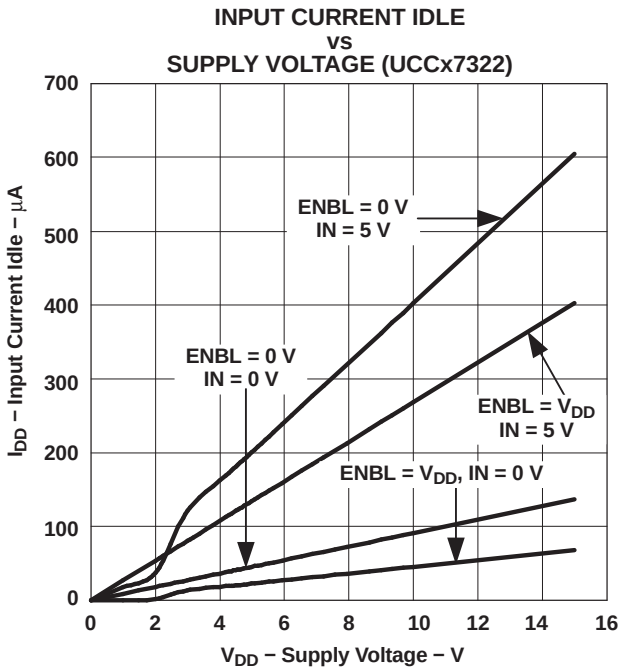
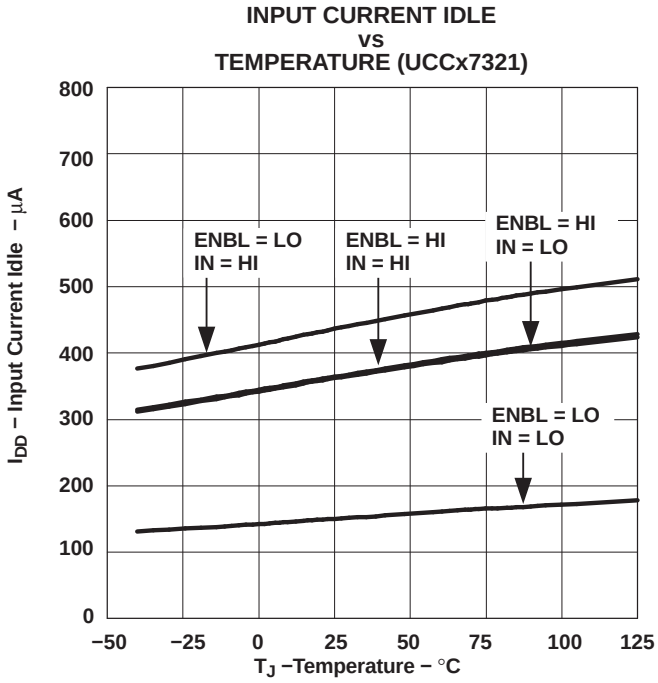


Figure 4.



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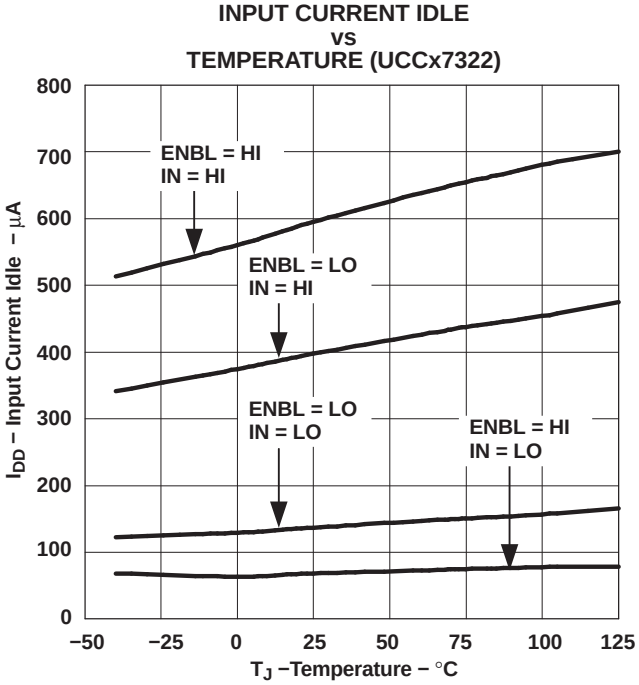
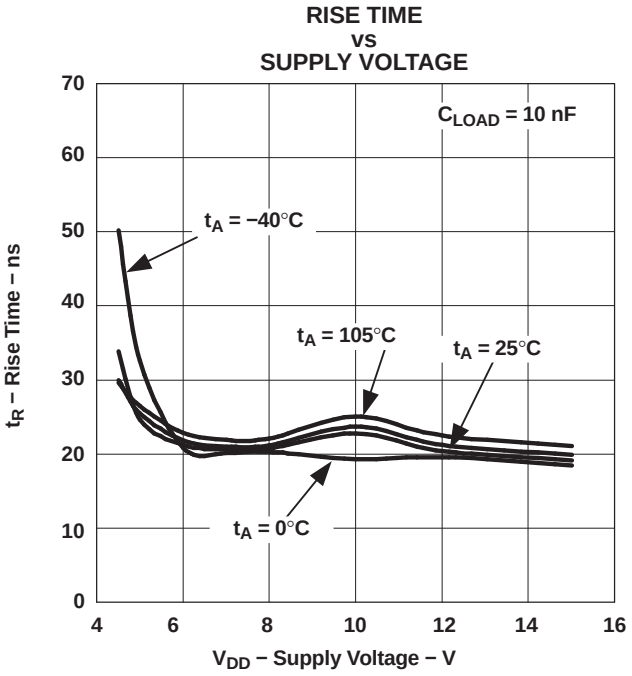


Figure 6.

TYPICAL CHARACTERISTICS (continued)



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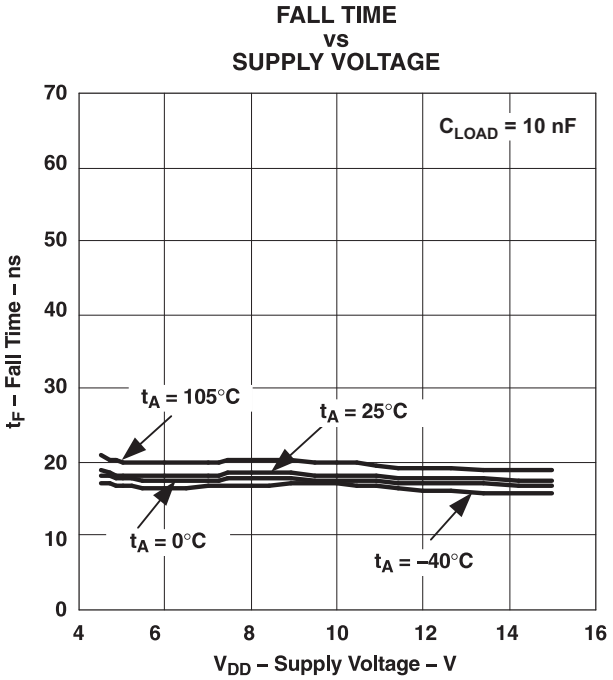

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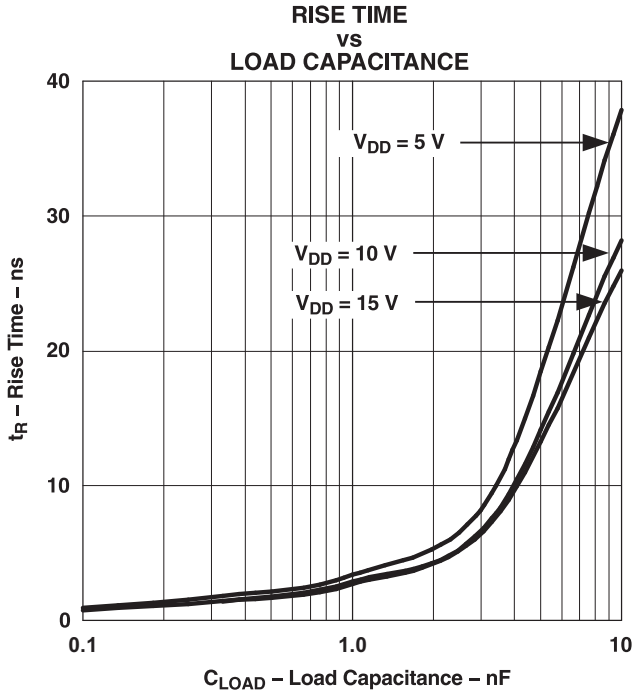

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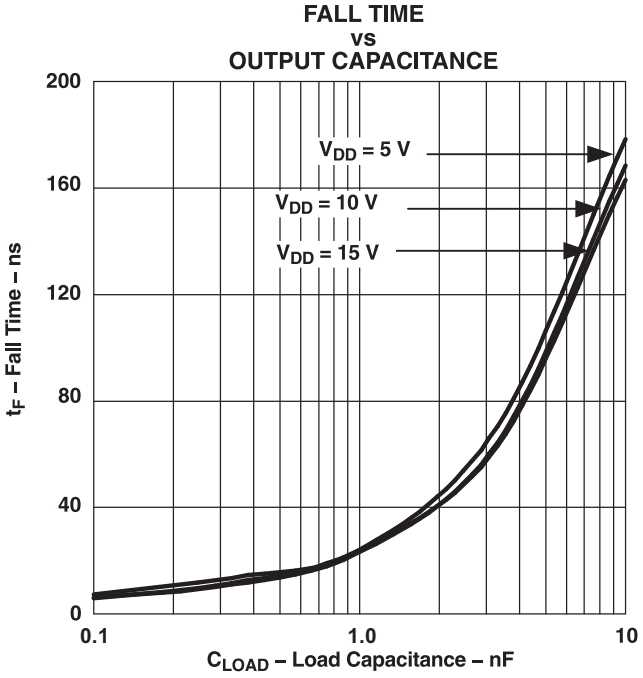
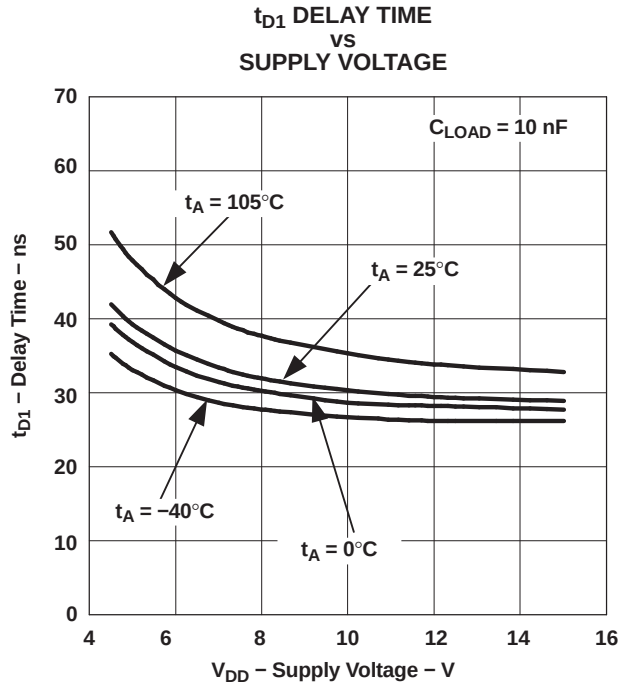


Figure 10.

TYPICAL CHARACTERISTICS (continued)



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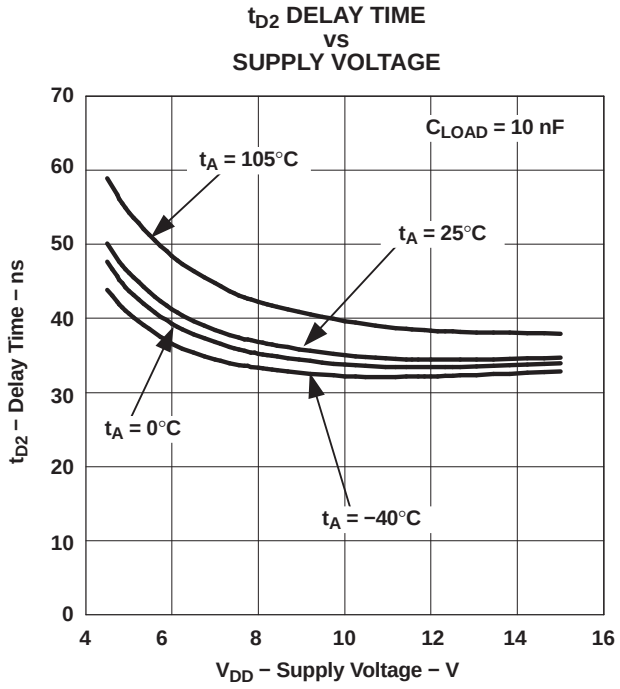

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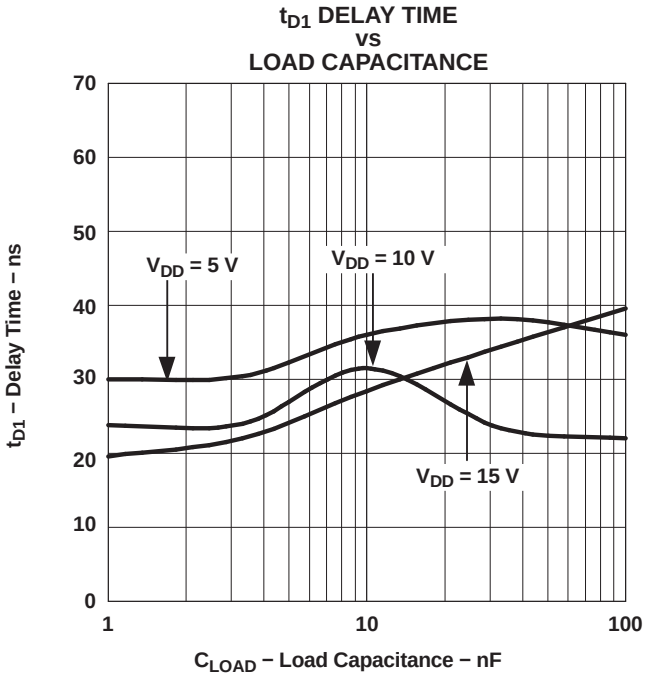

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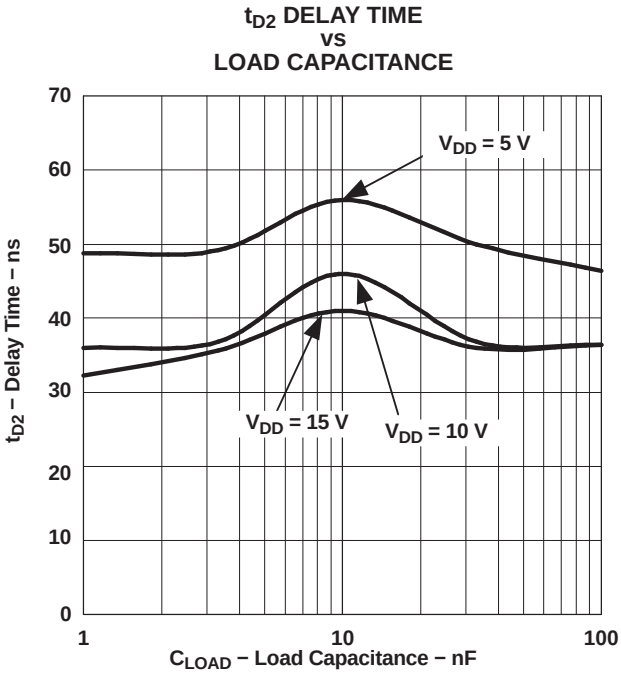
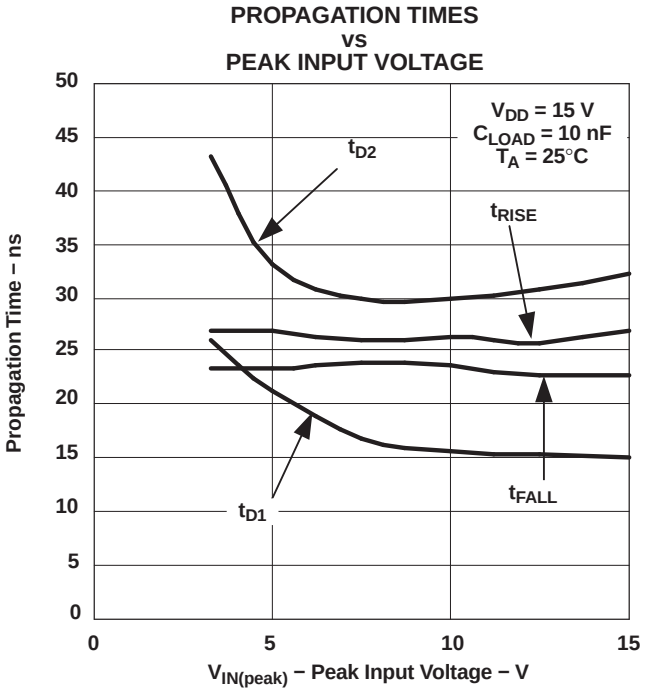


Figure 14.

TYPICAL CHARACTERISTICS (continued)



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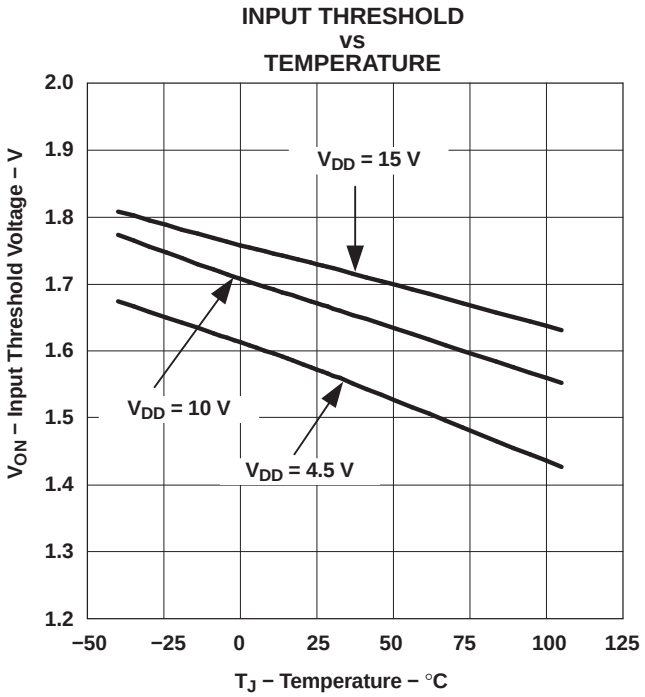

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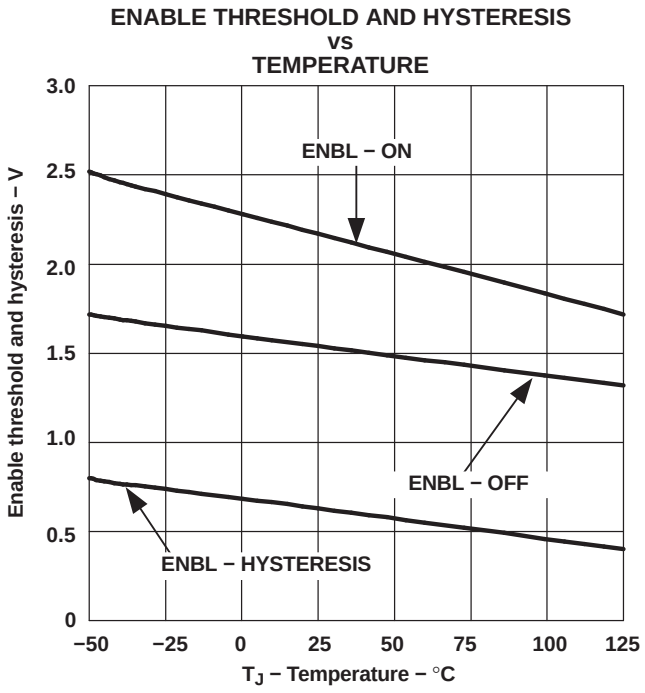

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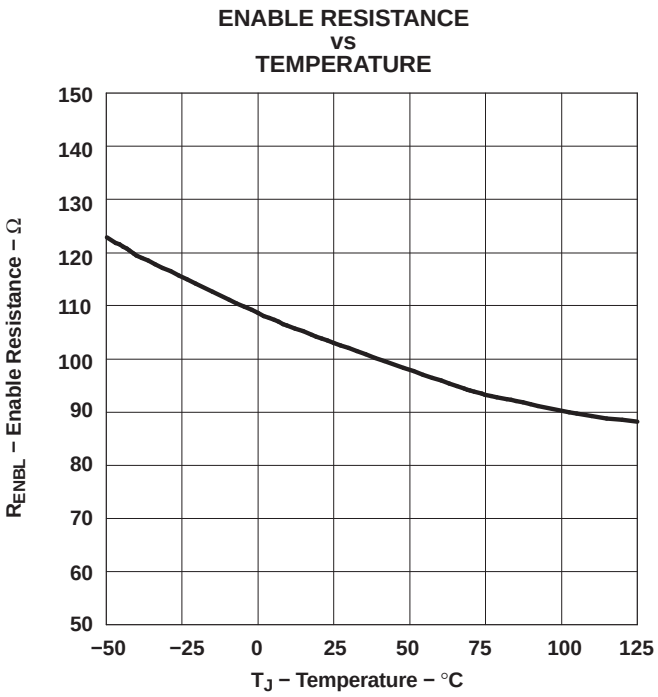
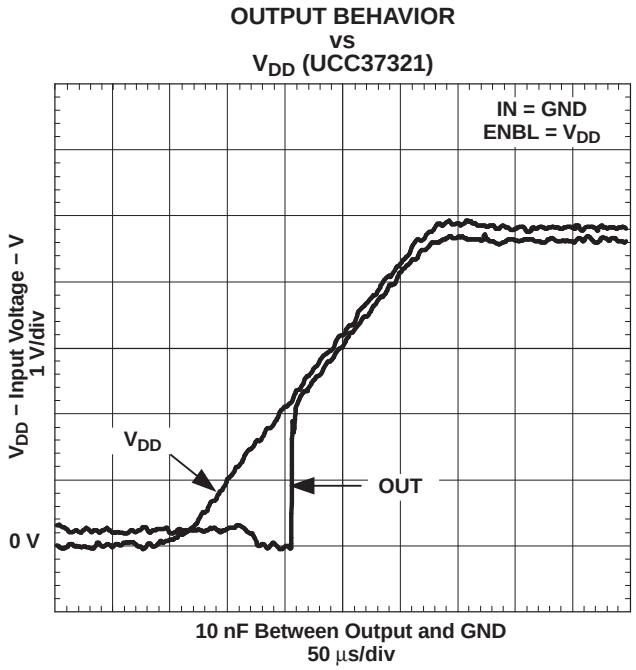


Figure 18.

TYPICAL CHARACTERISTICS (continued)



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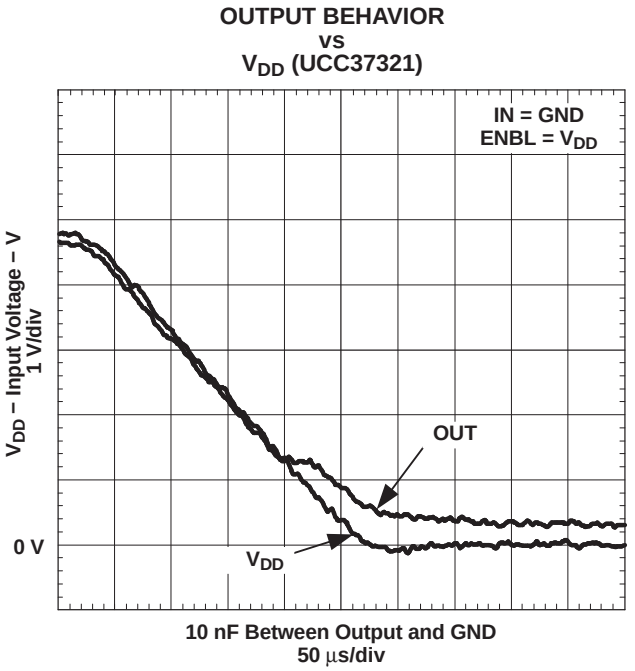

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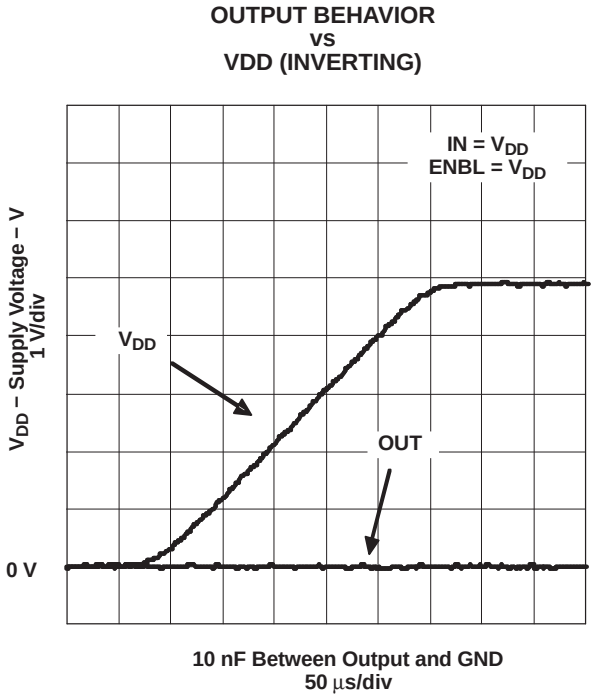

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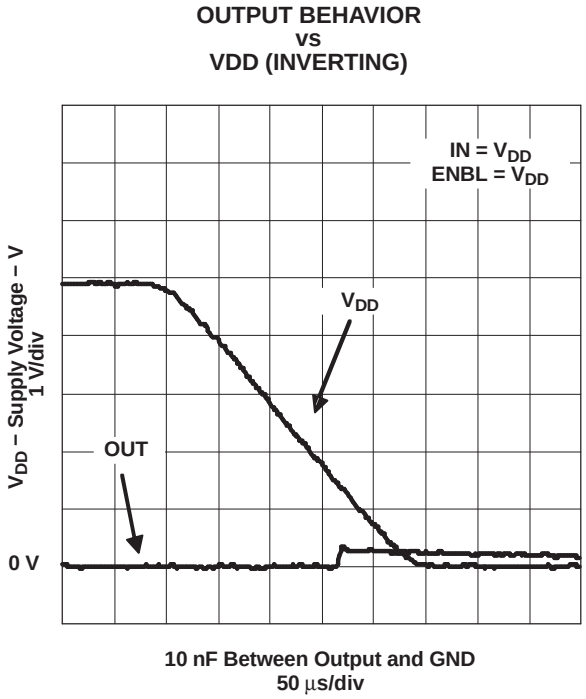


Figure 22.

TYPICAL CHARACTERISTICS (continued)

OUTPUT BEHAVIOR vs VDD (UCC37322)

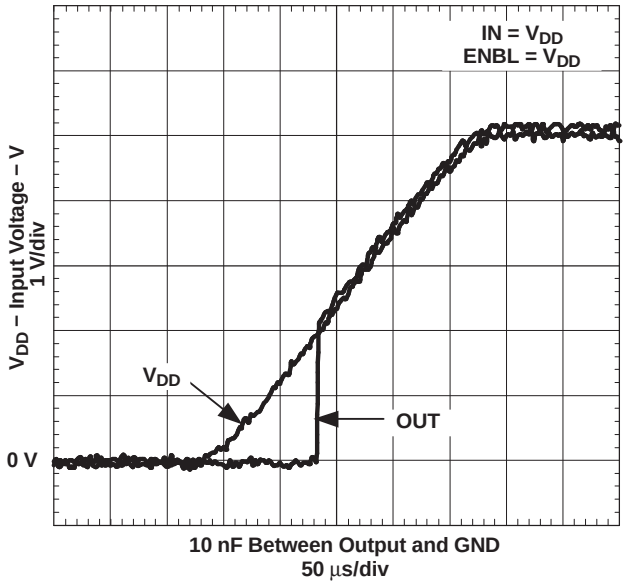


Figure 23.

OUTPUT BEHAVIOR vs VDD (UCC37322)

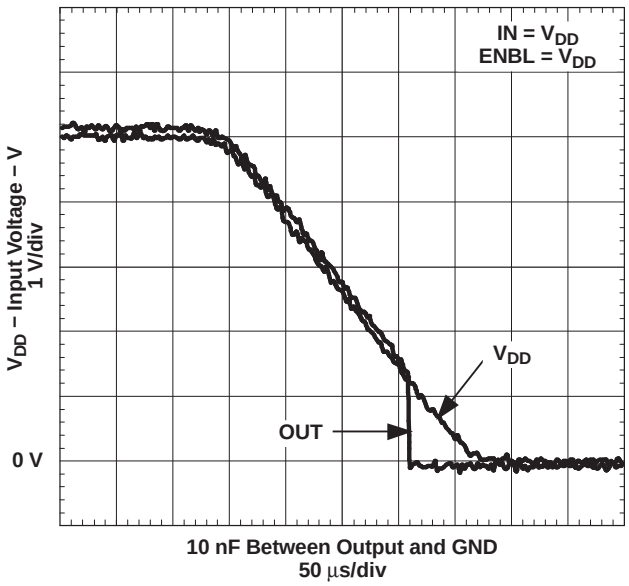


Figure 24.

OUTPUT BEHAVIOR vs VDD (NON-INVERTING)

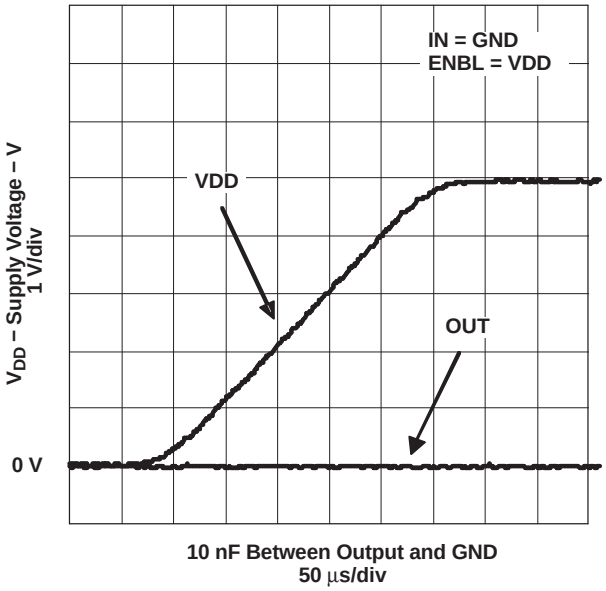


Figure 25.

OUTPUT BEHAVIOR vs VDD (NON-INVERTING)

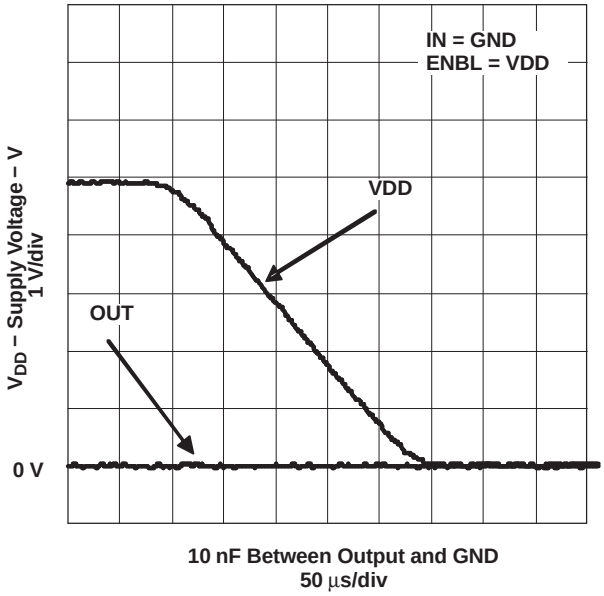


Figure 26.

APPLICATION INFORMATION

General Information

The UCC37321 and UCC37322 drivers serve as an interface between low-power controllers and power MOSFETs. They can also be used as an interface between DSPs and power MOSFETs. High-frequency power supplies often require high-speed, high-current drivers such as the UCC37321/2 family. A leading application is the need to provide a high-power buffer stage between the PWM output of the control device and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the device drives the power device gates through a drive transformer. Synchronous rectification supplies also have the need to drive multiple devices simultaneously, which can present an extremely large load to the control circuitry.

The inverting driver (UCC37321) is useful for generating inverted gate-drive signals from controllers that have only outputs of the opposite polarity. For example, this driver can provide a gate signal for ground-referenced, N-channel synchronous rectifier MOSFETs in buck derived converters. This driver can also be used for generating a gate-drive signal for a P-channel MOSFET from a controller that is designed for N-channel applications.

MOSFET gate drivers are generally used when it is not feasible to have the primary PWM regulator device directly drive the switching devices for one or more reasons. The PWM device may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases, there may be a desire to minimize the effect of high-frequency switching noise by placing the high-current driver physically close to the load. Also, newer devices that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high-impedance input to a driver such as the UCC37321/2. Finally, the control device may be under thermal stress due to power dissipation, and an external driver can help by moving the heat from the controller to an external package.

Input Stage

The IN threshold has a 3.3-V logic sensitivity over the full range of VDD voltages; yet, it is equally compatible with 0-V to VDD signals. The inputs of UCC37321/2 family of drivers are designed to withstand 500-mA reverse current without either damage to the device or logic upset. In addition, the input threshold turnoff of the UCC37321/2 has been slightly raised for improved noise immunity. The input stage of each driver should be driven by a signal with a short rise or fall time. This condition is satisfied in typical power-supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The IN input of the driver functions as a digital gate, and is not intended for applications where a slow-changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help dissipate power from the device package, as discussed in the *Thermal Considerations* section.

Output Stage

The TrueDrive output stage is capable of supplying ±9-A peak current pulses and swings to both VDD and GND and can encourage even the most stubborn MOSFETs to switch. The pullup/pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the internal MOSFET. This means that in many cases, external Schottky clamping diodes are not required.

This unique bipolar and MOSFET hybrid output architecture (TrueDrive) allows efficient current sourcing at low supply voltages. The UCC37321/2 family delivers 9 A of gate drive where it is most needed during the MOSFET switching transition—at the Miller plateau region—providing improved efficiency gains.

Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC27321/2 drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver.[1]

Two circuits are used to test the current capabilities of the UCC27321/2 driver. In each case, external circuitry is added to clamp the output near 5 V while the device is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test, there is a transient period when the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The circuit in Figure 27 is used to verify the current-sink capability when the output of the driver is clamped at approximately 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCC27321 is found to sink 9 A at VDD = 15 V.

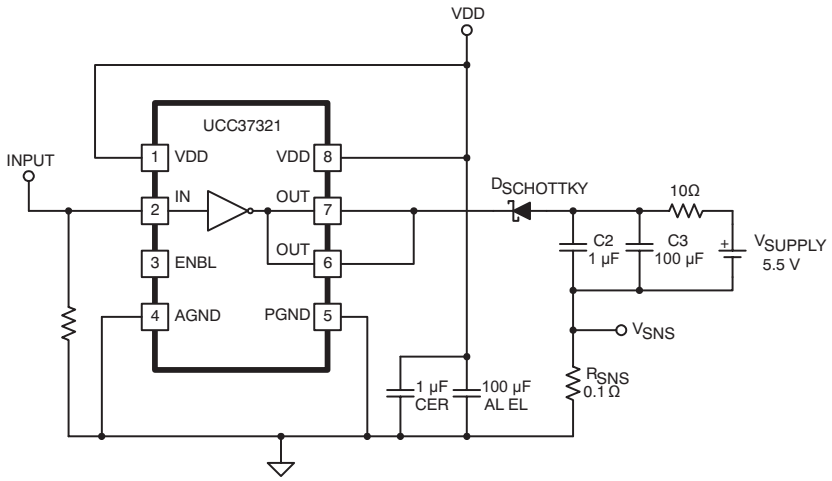


Figure 27. Sink Current Test Circuit

The circuit in Figure 28 is used to test the current-source capability with the output clamped to approximately 5 V with a string of Zener diodes. The UCC27321 is found to source 9 A at VDD = 15 V.

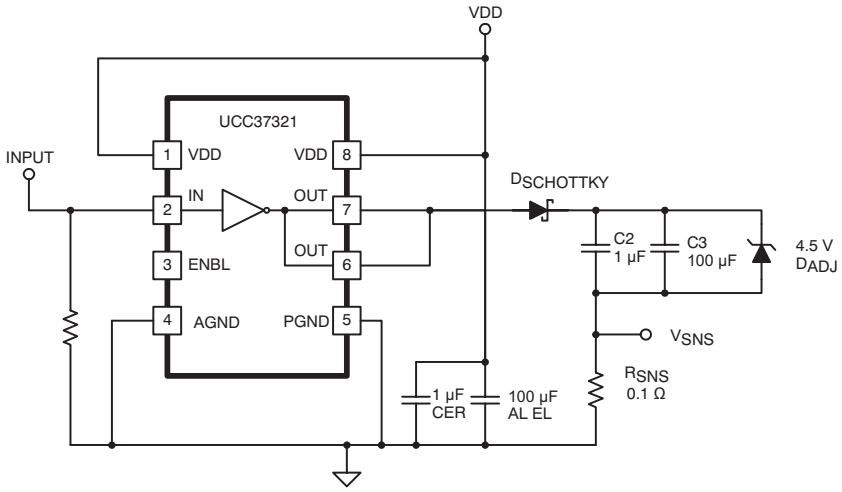


Figure 28. Source Current Test Circuit

It should be noted that the current-sink capability is slightly stronger than the current source capability at lower VDD. This is due to the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET and the current sink has an N-channel MOSFET.

In a large majority of applications, it is advantageous that the turnoff capability of a driver is stronger than the turnon capability. This helps to ensure that the MOSFET is held off during common power-supply transients that may turn the device back on.

Operational Circuit Layout

It can be a significant challenge to avoid the overshoot/undershoot and ringing issues that can arise from circuit layout. The low impedance of these drivers and their high di/dt can induce ringing between parasitic inductances and capacitances in the circuit. Utmost care must be used in the circuit layout.

In general, position the driver physically as close to its load as possible. Place a 1-µF bypass capacitor as close to the output side of the driver as possible, connecting it to pins 1 and 8. Connect a single trace between the two VDD pins (pin 1 and pin 8); connect a single trace between PGND and AGND (pin 5 and pin 4). If a ground plane is used, it may be connected to AGND; do not extend the plane beneath the output side of the package (pins 5–8). Connect the load to both OUT pins (pins 7 and 6) with a single trace on the adjacent layer to the component layer; route the return current path for the output on the component side, directly over the output path.

Extreme conditions may require decoupling the input power and ground connections from the output power and ground connections. The UCCx7321/2 has a feature that allows the user to take these extreme measures, if necessary. There is a small amount of internal impedance of about 15 Ω between the AGND and PGND pins; there is also a small amount of impedance (approximately 30 Ω) between the two VDD pins. In order to take advantage of this feature, connect a 1-µF bypass capacitor between VDD and PGND (pins 5 and 8) and connect a 0.1-µF bypass capacitor between VDD and AGND (pins 1 and 4). Further decoupling can be achieved by connecting between the two VDD pins with a jumper that passes through a 40-MHz ferrite bead and connects bias power only to pin 8. Even more decoupling can be achieved by connecting between AGND and PGND with a pair of anti-parallel diodes (anode connected to cathode and cathode connected to anode).

VDD

Although quiescent VDD current is very low, total supply current is higher, depending on the OUT current and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from:

$I_{OUT} = Q_g \times f$

where f is frequency.

For the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface-mount components is highly recommended. A 0.1-µF ceramic capacitor should be located closest to the VDD-to-ground connection. In addition, a larger capacitor (such as 1-µF) with relatively low ESR should be connected in parallel, to help deliver the high-current peaks to the load. The parallel combination of capacitors should present a low-impedance characteristic for the expected current levels in the driver application.

Drive Current and Power Requirements

The UCC37321/2 family of drivers is capable of delivering 9 A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn an N-channel device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. An N-channel MOSFET is used in this discussion because it is the most common type of switching device used in high-frequency power-conversion equipment.

References 1 and 2 contain detailed discussions of the drive current required to drive a power MOSFET and other capacitive-input switching devices. Much information is provided in tabular form to give a range of the current required for various devices at various frequencies. The information pertinent to calculating gate-drive current requirements is summarized here; the original document is available from the TI web site (www.ti.com).

When a driver is tested with a discrete capacitive load, it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$E = ½CV^2$

where C is the load capacitor and V is the bias voltage feeding the driver.

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by:

$P = 2 \times ½CV^2f$

where f is the switching frequency.

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate-drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as:

$P = 10\ nF \times (12)^2 \times (300\ kHz) = 0.432\ W$

With a 12-V supply, this equates to a current of:

$I = P / V = 0.432\ W / 12\ V = 0.036\ A$

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the on and off states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence Q_g = CeffV to provide the following equation for power:

$P = C \times V^2 \times f = Q_g \times V \times f$

This equation allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

ENABLE

UCC37321/2 provides an enable input for improved control of the driver operation. This input also incorporates logic-compatible thresholds with hysteresis. The input is internally pulled up to VDD with a 100-kΩ resistor for active-high operation. When ENBL is high, the device is enabled, and when ENBL is low, the device is disabled. The default state of the ENBL pin is to enable the device, and therefore can be left open for standard operation. The output state when the device is disabled is low, regardless of the input state. See the truth table (Table 2) for operation using enable logic.

The ENBL input is compatible with both logic signals and slow-changing analog signals. It can be directly driven, or a power-up delay can be programmed with a capacitor between ENBL and AGND.

Table 2. Input/Ouput Table

	ENBL	IN	OUT
Inverting UCC37321	0	0	0
	0	1	0
	1	0	1
	1	1	0
Non-inverting UCC37322	0	0	0
	0	1	0
	1	0	0
	1	1	1

Thermal Information

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. For a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC27321/2 family of drivers is available in two different packages to cover a range of application requirements.

As shown in Power Dissipation Ratings, the SOIC-8 (D) package has a power rating of approximately 0.5 W at T_A = 70°C. This limit is imposed in conjunction with the power derating factor also given in the table. Note that the power dissipation in our earlier example is 0.432 W with a 10-nF load, 12-V V_{DD}, switched at 300 kHz. Thus, only one load of this size could be driven using the D package. The difficulties with heat removal limit the drive available in the older packages.

The MSOP PowerPAD package (DGN) significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As illustrated in Reference 3, the PowerPAD packages offer a lead-frame die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the package, reducing the θ_{JC} to 4.7°C/W. Data is presented in Reference 3 to show that the power dissipation can be quadrupled in the PowerPAD package when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference 4. This allows a significant improvement in heatsink capability over that available in the D package and is shown to more than double the power capability of the D package.

NOTE

The PowerPAD thermal pad is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.

References

1. Power Supply Seminar SEM-1400 Topic 2: *Design And Application Guide For High Speed MOSFET Gate Drive Circuits*, Laszlo Balogh (SLUP133)
2. *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits*, Bill Andreycak (SLUA105)
3. *PowerPad Thermally Enhanced Package* (SLMA002)
4. *PowerPAD Made Easy* (SLMA004)

Related Products

Table 3. Related Products

PRODUCT	DESCRIPTION	PACKAGE
UCC37323/4/5	Dual 4-A low-side drivers	MSOP-8 PowerPAD, SOIC-8, PDIP-8
UCC27423/4/5	Dual 4-A low-side drivers with enable	MSOP-8 PowerPAD, SOIC-8, PDIP-8
TPS2811/12/13	Dual 2-A low-side drivers with internal regulator	TSSOP-8, SOIC-8, PDIP-8
TPS2814/15	Dual 2-A low-side drivers with two inputs per channel	TSSOP-8, SOIC-8, PDIP-8
TPS2816/17/18/19	Single 2-A low-side driver with internal regulator	5-pin SOT-23
TPS2828/29	Single 2-A low-side driver	5-pin SOT-23

REVISION HISTORY

Changes from Revision B (January 2011) to Revision C	Page
• Changed enable impedance from 135 kΩ to 145 kΩ	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UCC27321QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27321Q	Samples
UCC27322QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	EACQ	Samples
UCC27322QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27322Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

OTHER QUALIFIED VERSIONS OF UCC27321-Q1, UCC27322-Q1 :

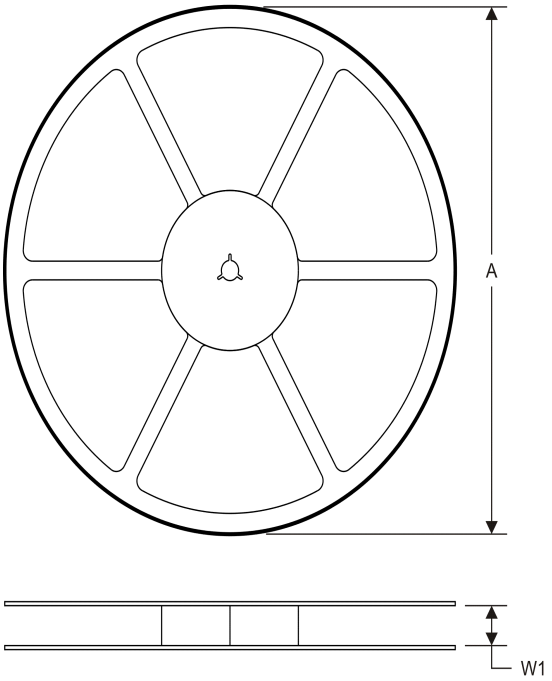
- Catalog: UCC27321, UCC27322
- Enhanced Product: UCC27322-EP

NOTE: Qualified Version Definitions:

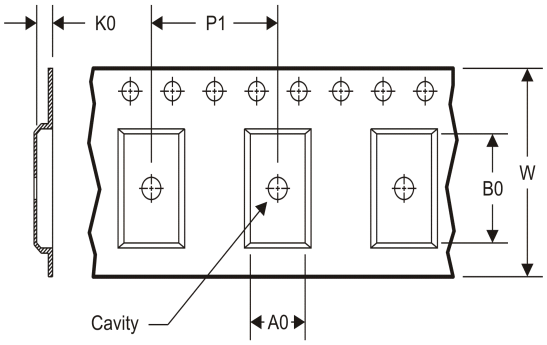
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



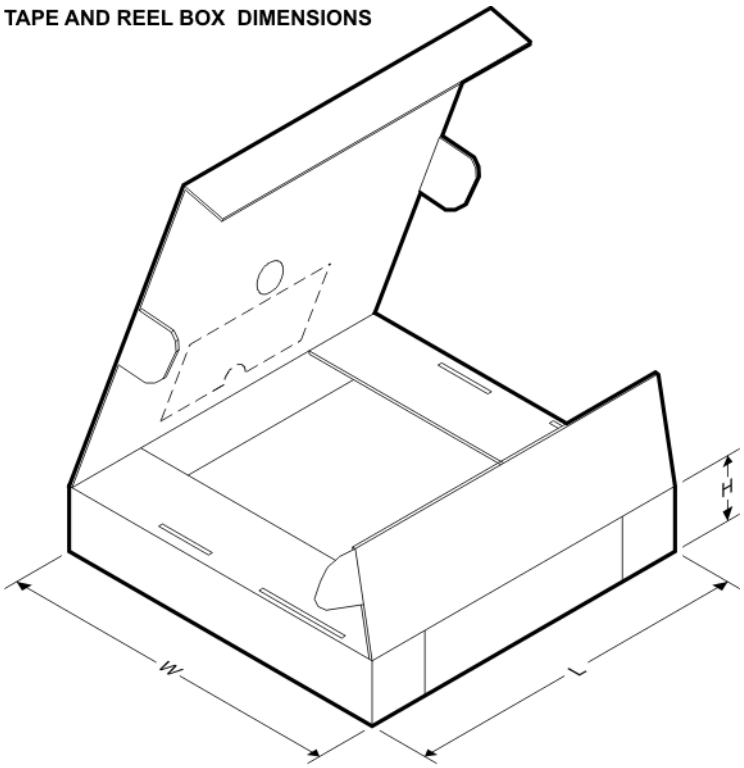
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27321QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27322QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27322QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

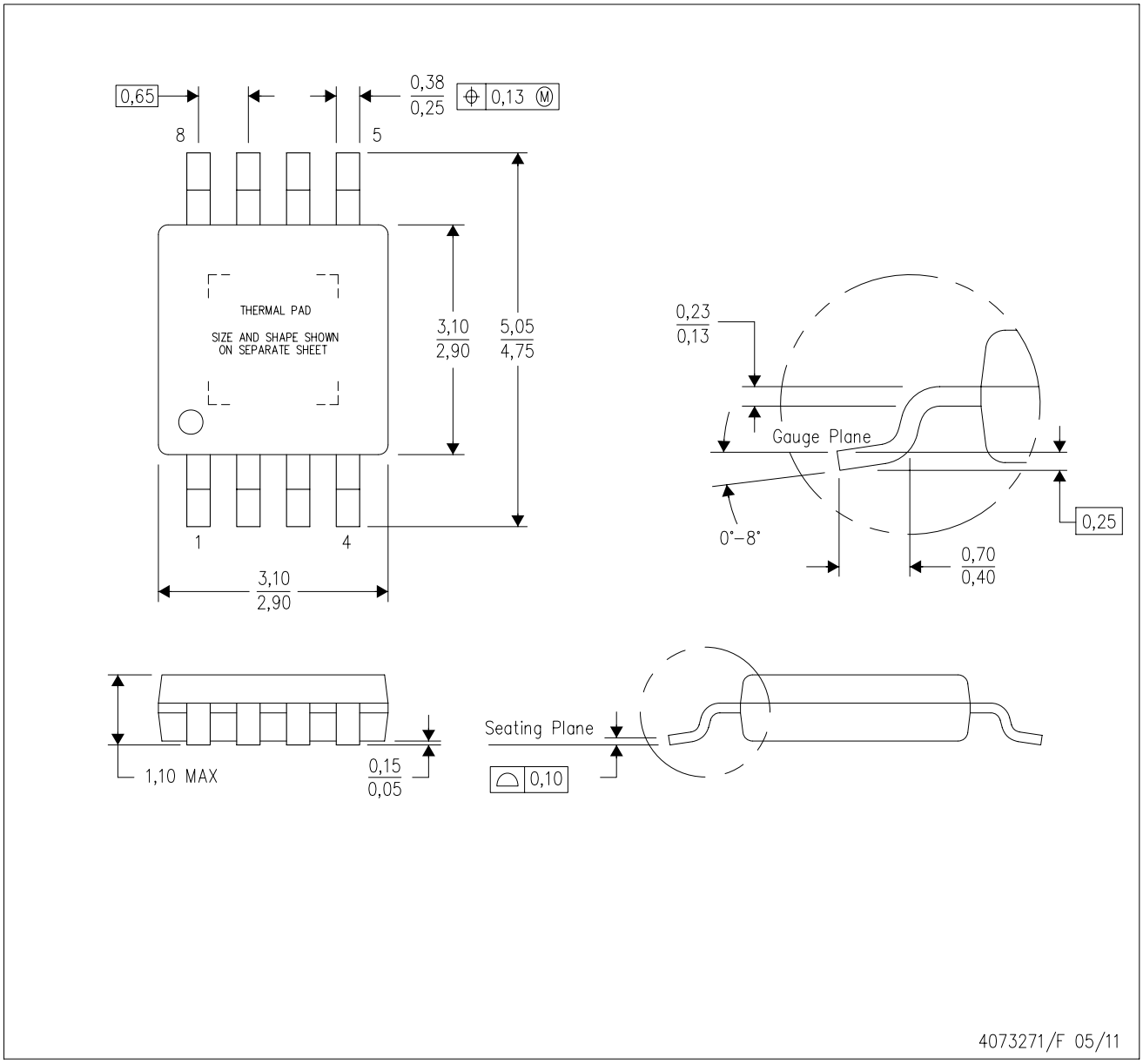
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27321QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
UCC27322QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	367.0	367.0	35.0
UCC27322QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

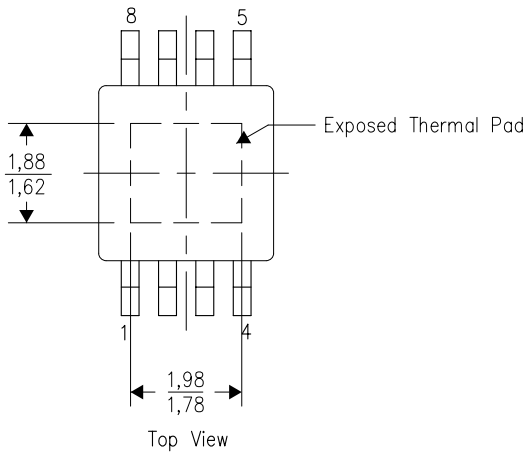
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



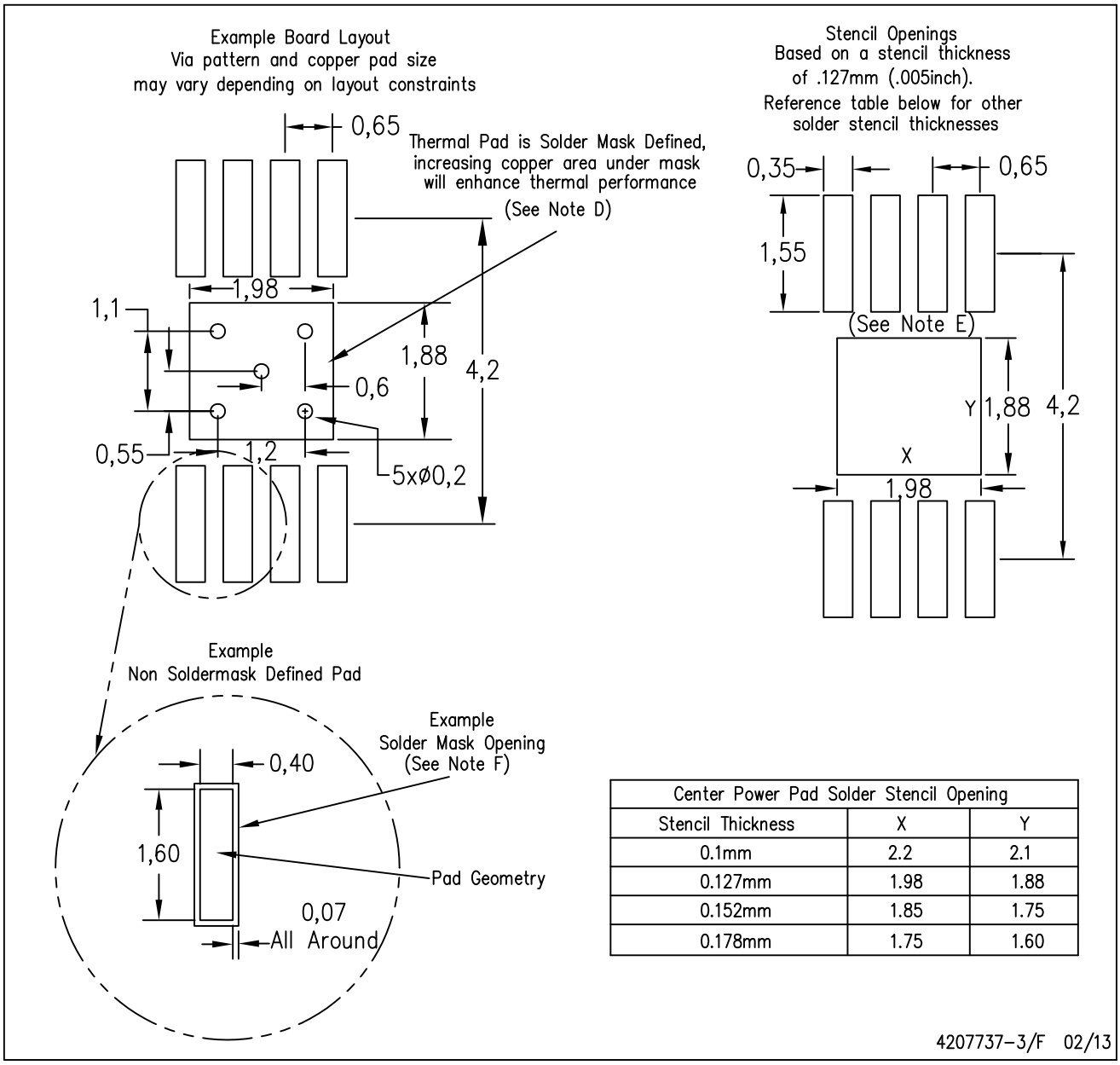
Exposed Thermal Pad Dimensions

4206323–3/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

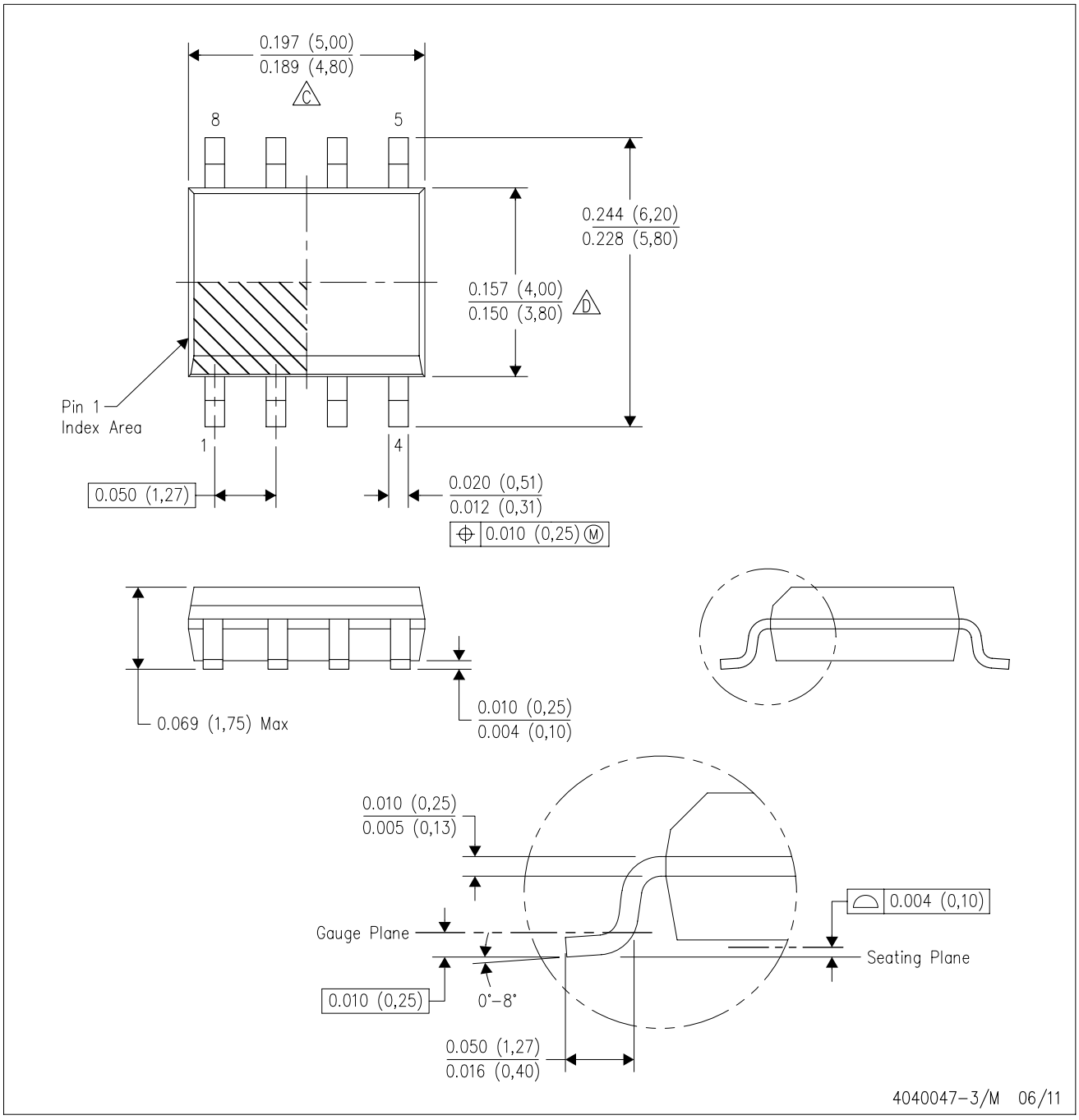


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.2	2.1
0.127mm	1.98	1.88
0.152mm	1.85	1.75
0.178mm	1.75	1.60

4207737–3/F 02/13

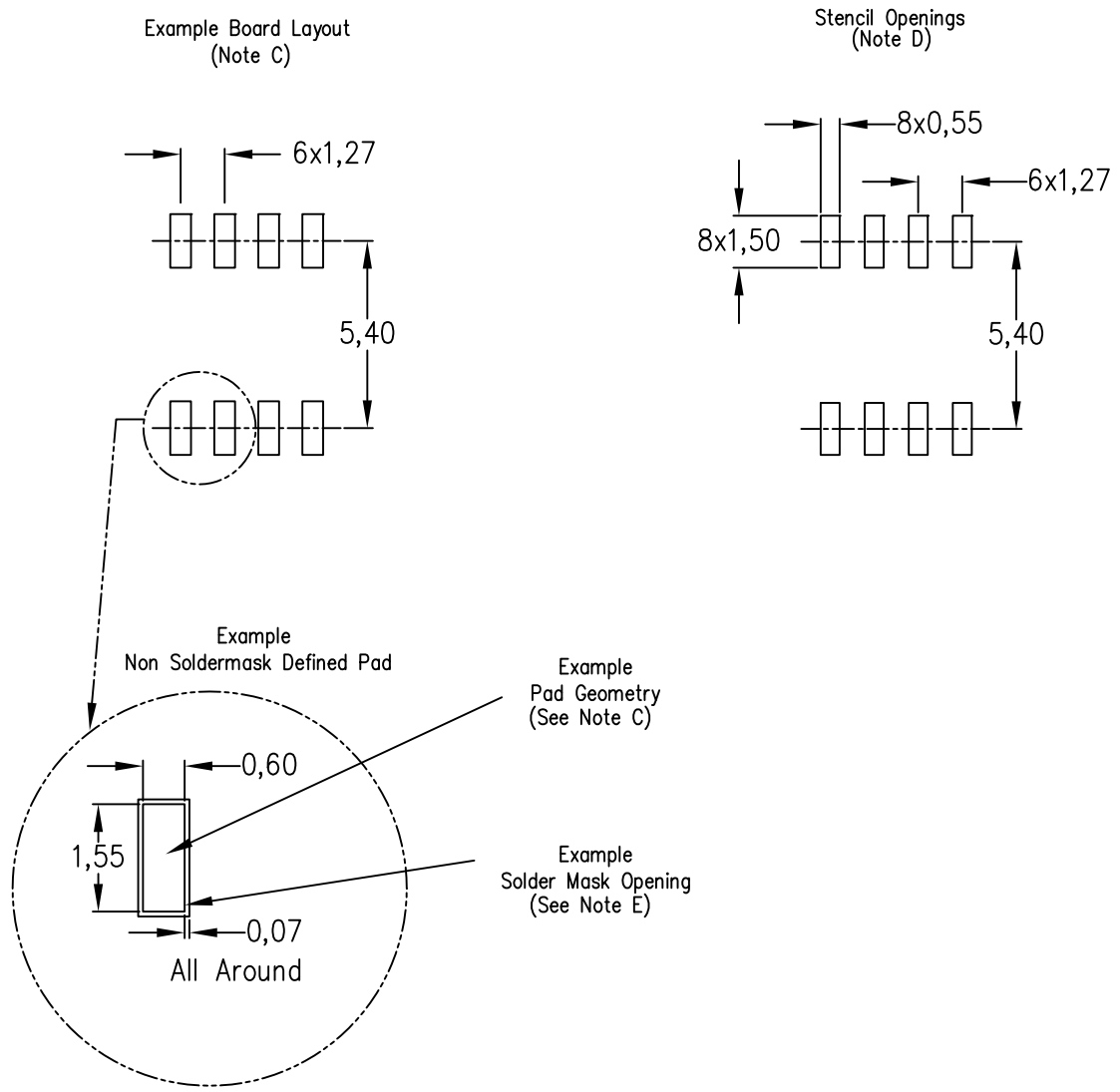
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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