Digital Control Compatible Single Low-Side ±4-A MOSFET Driver with Current Sense

Check for Samples: UCD7100

FEATURES

- **Adjustable Current Limit Protection**
- **3.3-V, 10-mA Internal Regulator**
- **DSP/µC Compatible Inputs**
- **Single ±4-A TrueDrive™ High Current Driver**
- **10-ns Typical Rise and Fall Times with 2.2-nF Loads**
- **25-ns Input-to-Output Propagation Delay**
- **25-ns Current Sense to Output Delay**
- **Programmable Current Limit Threshold**
- **Digital Output Current Limit Flag**
- **4.5-V to 15-V Supply Voltage Range**
- **Rated from -40°C to 105°C**
- **Lead(Pb)-Free Packaging**

APPLICATIONS

- **Digitally Controlled Power Supplies**
- **DC/DC Converters**
- **Motor Controllers**
- **Line Drivers**

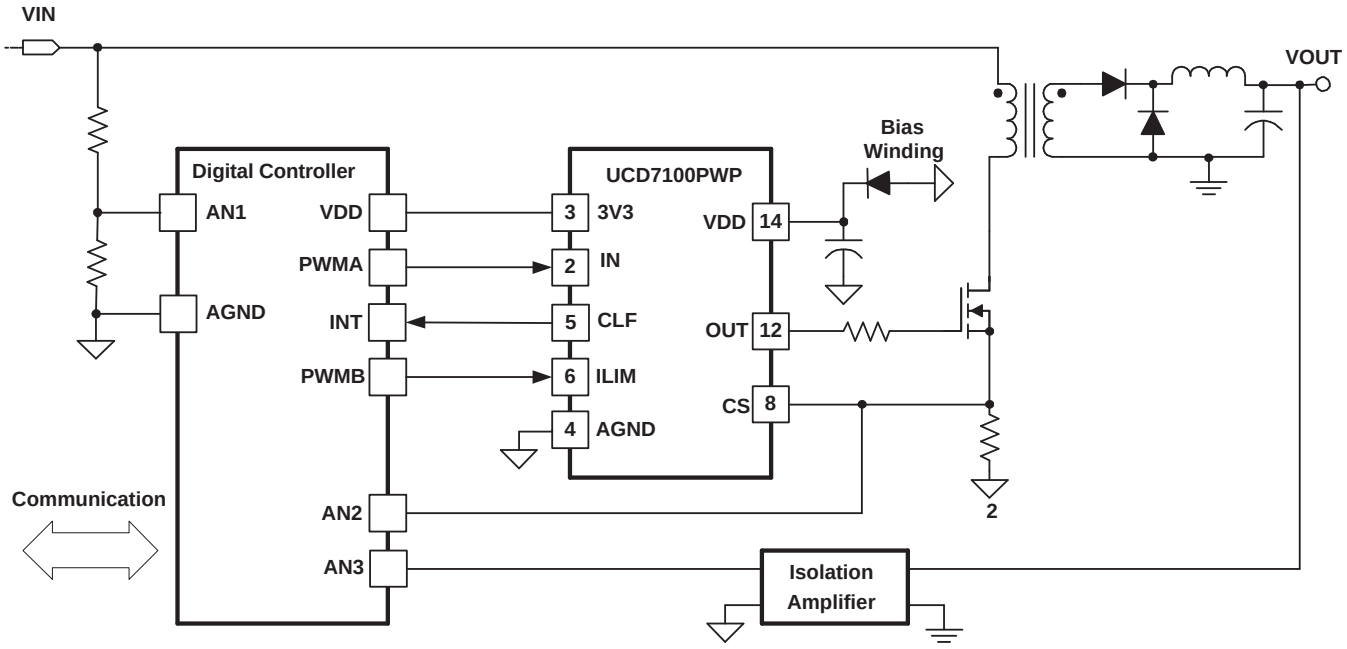
DESCRIPTION

The UCD7100 is a member of the UCD7K family of digital control compatible drivers for applications utilizing digital control techniques or applications requiring fast local peak current limit protection.

The UCD7100 is a low-side ±4-A high-current MOSFET gate driver. It allows the digital power controllers such as UCD9110 or UCD9501 to interface to the power stage in single ended topologies. It provides a cycle-by-cycle current limit function with programmable threshold and a digital output current limit flag which can be monitored by the host controller. With a fast 25-ns cycle-by-cycle current limit protection, the driver can turn off the power stage in the unlikely event that the digital system can not respond to a failure situation in time.

For fast switching speeds, the UCD7100 output stage uses the TrueDrive™ output architecture, which delivers rated current of ±4 A into the gate of a MOSFET during the Miller plateau region of the switching transition. It also includes a 3.3-V, 10-mA linear regulator to provide power to the digital controller.

TYPICAL APPLICATION DIAGRAMS



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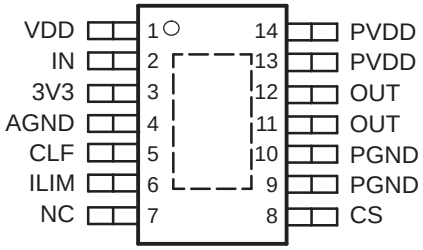
TrueDrive, PowerPAD are trademarks of Texas Instruments.

DESCRIPTION (CONT.)

The UCD7000 driver family is compatible with standard 3.3-V I/O ports of DSPs, Microcontrollers, or ASICs. UCD7100 is offered in a PowerPAD™ HTSSOP-14.

CONNECTION DIAGRAMS

PWP–14 PACKAGE
(TOP VIEW)



NC − No internal connection

ORDERING INFORMATION

Temperature Range	110-V HV Startup Circuit	Packaged Devices(1) (2)
		PowerPAD™ HTSSOP-14 (PWP)
-40°C to 105°C	No	UCD7100PWP

(1) HTSSOP-14 (PWP) package is available taped and reeled. Add R suffix to device type (e.g. UCD7100PWPR) to order quantities of 2,000 devices per reel for the PWP package.
(2) These products are packaged in Pb-Free and Green lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.

ABSOLUTE MAXIMUM RATINGS(1) (2)

SYMBOL	PARAMETER		UCD7100	UNIT
V_{DD}	Supply Voltage		16	
I_{DD}	Supply Current	Quiescent	20	mA
		Switching, T_A = 25°C, T_J = 125°C, V_{DD} = 12 V	200	
V_{OUT}	Output Gate Drive Voltage	OUT	-1 V to VDD	V
$I_{OUT(sink)}$	Output Gate Drive Current	OUT	4.0	A
$I_{OUT(source)}$			-4.0	
	Analog Input	ISET, CS	-0.3 to 3.6	V
		ILIM	-0.3 to 3.6	
	Digital I/O's	IN, CLF	-0.3 to 3.6	
	Power Dissipation	T_A = 25°C, T_J = 125°C, (PWP-14)	2.67	W
T_J	Junction Operating Temperature		-55 to 150	°C
T_{str}	Storage Temperature		-65 to 150	
HBM	ESD Rating	Human body model	2000	V
CDM		Change device model	500	
T_{SOL}	Lead Temperature (Soldering, 10 sec)		+300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Supply Voltage, VDD	4.25	12	14.5	V
Supply bypass capacitance	1			µF
Reference bypass capacitance	0.22			
Operating junction temperature	-40		105	°C

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V, 4.7-µF capacitor from V_{DD} to GND, $T_A = T_J$ = -40°C to 105°C, (unless otherwise noted).

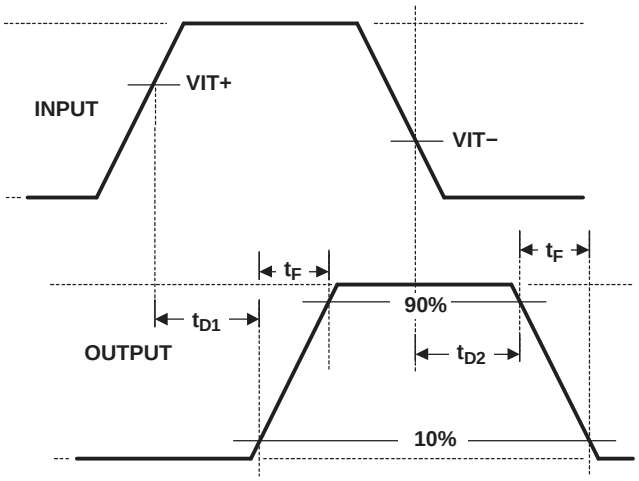
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION					
Supply current, OFF	V_{DD} = 4.2 V		200	400	µA
Supply current	Outputs not switching IN = LOW		1.5	2.5	mA
LOW VOLTAGE UNDER-VOLTAGE LOCKOUT					
VDD UVLO ON		4.25	4.5	4.75	V
VDD UVLO OFF		4.05	4.25	4.45	
VDD UVLO hysteresis		150	250	350	mV
REFERENCE / EXTERNAL BIAS SUPPLY					
3V3 initial set point	T_A = 25°C	3.267	3.3	3.333	V
3V3 over temperature		3.234	3.3	3.366	
3V3 load regulation	I_{LOAD} = 1 mA to 10 mA, VDD = 5 V		1	6.6	mV
3V3 line regulation	VDD = 4.75 V to 12 V, I_{LOAD} = 10 mA		1	6.6	
Short circuit current	VDD = 4.75 to 12 V	11	20	35	mA
3V3 OK threshold, ON	3.3 V rising	2.9	3.0	3.1	V
3V3 OK threshold, OFF	3.3 V falling	2.7	2.8	2.9	
INPUT SIGNAL					
HIGH, positive-going input threshold voltage (VIT+)		1.65		2.08	V
LOW negative-going input threshold voltage (VIT-)		1.16		1.5	
Input voltage hysteresis, (VIT+ - VIT-)		0.6		0.8	
Frequency				2	MHz
CURRENT LIMIT (ILIM)					
ILIM internal current limit threshold	ILIM = OPEN	0.466	0.50	0.536	V
ILIM maximum current limit threshold	I_{LIM} = 3.3 V	0.975	1.025	1.075	V
ILIM current limit threshold	I_{LIM} = 0.75 V	0.700	0.725	0.750	
ILIM minimum current limit threshold	I_{LIM} = 0.25 V	0.21	0.23	0.25	mV
CLF output high level	CS > I_{LIM} , I_{LOAD} = -7 mA	2.64			V
CLF output low level	CS ≤ I_{LIM}, I_{LOAD} = 7 mA			0.66	
Propagation delay from IN to CLF	IN rising to CLF falling after a current limit event		10	20	ns

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 12 V, 4.7-µF capacitor from V_{DD} to GND, $T_A = T_J$ = -40°C to 105°C, (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE COMPARATOR					
Bias voltage	Includes CS comp offset	5	25	50	mV
Input bias current			–1		uA
Propagation delay from CS to OUTx	I_{LIM} = 0.5 V, measured on OUTx, CS = threshold + 60 mV		25	40	ns
Propagation delay from CS to CLF	I_{LIM} = 0.5 V, measured on CLF, CS = threshold + 60 mV		25	50	
CURRENT SENSE DISCHARGE TRANSISTOR					
Discharge resistance	IN = low, resistance from CS to AGND	10	35	75	Ω
OUTPUT DRIVERS					
Source current (1)	V_{DD} = 12 V, IN = high, OUT = 5 V		4		A
Sink current (1)	V_{DD} = 12 V, IN = low, OUT = 5 V		4		
Source current(1)	V_{DD} = 4.75 V, IN = high, OUT = 0		2		
Sink current (1)	V_{DD} = 4.75 V, IN = low, OUT = 4.75 V		3		
Rise time, t_R (1)	C_{LOAD} = 2.2 nF, V_{DD} = 12 V		10	20	ns
Fall time, t_F (1)	C_{LOAD} = 2.2 nF, V_{DD} = 12 V		10	15	
Output with V_{DD} < UVLO	V_{DD} = 1.0 V, I_{SINK} = 10 mA		0.8	1.2	V
Propagation delay from IN to OUTx, t_{D1}	C_{LOAD} = 2.2 nF, V_{DD} = 12 V, CLK rising		20	35	ns

(1) Ensured by design. Not 100% tested in production.



NOTE

The 10% and 90% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

FUNCTIONAL BLOCK DIAGRAM

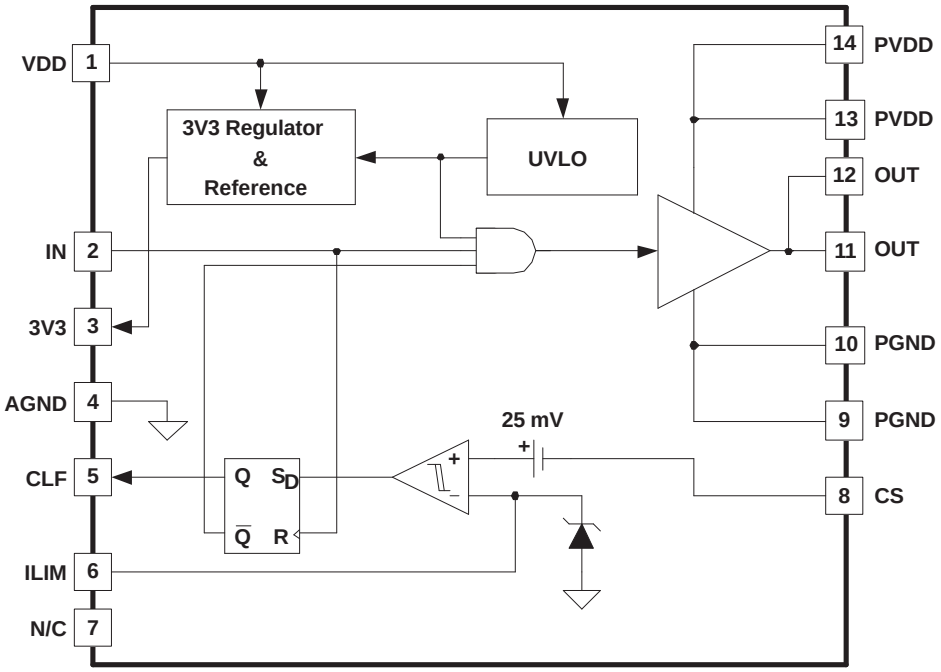


Figure 1. UCD7100

TERMINAL FUNCTIONS

UCD7100		PIN NAME	I/O	FUNCTION
HTSSOP -14 PIN #	DFN-14 PIN #			
1	1	VDD	I	Supply input pin to power the driver. The UCD7K devices accept an input range of 4.25 V to 15 V. Bypass the pin with at least 4.7 µF of capacitance.
2	2	IN	I	The IN pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt trigger comparator which isolates the internal circuitry from any external noise.
3	3	3V3	O	Regulated 3.3-V rail. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. Place 0.22-µF of ceramic capacitance from the pin to ground.
4	4	AGND	-	Analog ground return.
5	5	CLF	O	Current limit flag. When the CS level is greater than the ILIM voltage minus 25 mV, the output of the driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the UCD7K device receives the next rising edge on the IN pin.
6	6	ILIM	I	Current limit threshold set pin. The current limit threshold can be set to any value between 0.25 V and 1.0 V.
7	7	NC	-	No Connection.
8	8	CS	I	Current sense pin. Fast current limit comparator connected to the CS pin is used to protect the power stage by implementing cycle-by-cycle current limiting.
9	9	PGND	-	Power ground return. Connect the two PGNDs together. These ground pins should be connected very closely to the source of the power MOSFET.
10	10	PGND	-	Power ground return. Connect the two PGNDs together. These ground pins should be connected very closely to the source of the power MOSFET.
11	11	OUT	O	The high-current TrueDrive™ driver output. Connect the two OUT pins together.
12	12	OUT	O	The high-current TrueDrive™ driver output. Connect the two OUT pins together.
13	13	PVDD	I	Supply pin provides power for the output drivers. It is not connected internally to the VDD supply rail. Connect the two PVDD pins together.
14	14	PVDD	I	Supply pin provides power for the output drivers. It is not connected internally to the VDD supply rail. Connect the two PVDD pins together.

APPLICATION INFORMATION

The UCD7100 is part of a family of digital compatible drivers targeting applications utilizing digital control techniques or applications that require local fast peak current limit protection.

Supply

The UCD7K devices accept an input range of 4.5 V to 15 V. The device has an internal precision linear regulator that produces the 3V3 output from this VDD input. A separate pin, PVDD, not connected internally to the VDD supply rail provides power for the output drivers. In all applications the same bus voltage supplies the two pins. It is recommended that a low value of resistance be placed between the two pins so that the local capacitance on each pin forms low pass filters to attenuate any switching noise that may be on the bus.

Although quiescent VDD current is low, total supply current will be higher, depending on the gate drive output current required by the switching frequency. Total V_{DD} current is the sum of quiescent V_{DD} current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_G), average OUT current can be calculated from:

$I_{OUT} = Q_G \times f$, where f is frequency.

For high-speed circuit performance, a V_{DD} bypass capacitor is recommended to prevent noise problems. A 4.7-µF ceramic capacitor should be located close to the V_{DD} to ground connection. A larger capacitor with relatively low ESR should be connected to the PVDD pin, to help deliver the high current peaks to the load. The capacitors should present a low impedance characteristic for the expected current levels in the driver application. The use of surface mount components for all bypass capacitors is highly recommended.

Reference / External Bias Supply

All devices in the UCD7K family are capable of supplying a regulated 3.3-V rail to power various types of external loads such as a microcontroller or an ASIC. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. For normal operation, place a minimum of 0.22 µF of ceramic capacitance from the reference pin to ground.

Input

The IN pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt Trigger comparator which isolates the internal circuitry from any external noise.

If limiting the rise or fall times to the power device is desired, then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help remove power dissipation from the package.

Current Sensing and Protection

A very fast current limit comparator connected to the CS pin is used to protect the power stage by implementing cycle-by-cycle current limiting.

The current limit threshold is equal to the lesser of the positive inputs at the current limit comparator. The current limit threshold can be set to any value between 0.25 V and 1.0 V by applying the desired threshold voltage to the current limit (ILIM) pin. When the CS level is greater than the ILIM voltage minus 25 mV, the output of the driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the UCD7K device receives the next rising edge on the IN pin.

When the CS voltage is below ILIM, the driver output will follow the PWM input. The CLF digital output flag can be monitored by the host controller to determine when a current limit event occurs and to then apply the appropriate algorithm to obtain the desired current limit profile.

One of the main benefits of this local protection feature is that the UCD7K devices can protect the power stage if the software code in the digital controller becomes corrupted and hangs up. If the controller's PWM output stays high, the local current sense circuit will turn off the driver output when an over-current condition occurs. The system would likely go into a retry mode because; most DSP and microcontrollers have on-board watchdog, brown-out, and other supervisory peripherals to restart the device in the event that it is not operating properly. But these peripherals typically do not react fast enough to save the power stage. The UCD7K's local current limit comparator provides the required fast protection for the power stage.

The CS threshold is 25 mV below the ILIM voltage. This way, if the user attempts to command zero current (I_{LIM} < 25 mV) while the CS pin is at ground, for example at start-up, the CLF flag latches high until the IN pin receives a pulse. At start-up it is necessary to ensure that the ILIM pin always greater than the CS pin for the handshaking to work as described below. If for any reason the CS pin comes to within 25 mV of the ILIM pin during start-up, then the CLF flag is latched high and the digital controller must poll the UCD7K device, by sending it a narrow IN pulse. If the fault condition is not present the IN pulse resets the CLF signal to low indicating that the UCD7K device is ready to process power pulses.

Handshaking

The UCD7K family of devices have a built-in handshaking feature to facilitate efficient start-up of the digitally controlled power supply. At start-up the CLF flag is held high until all the internal and external supply voltages of the UCD7K device are within their operating range. Once the supply voltages are within acceptable limits, the CLF goes low and the device will process input drive signals. The micro-controller should monitor the CLF flag at start-up and wait for the CLF flag to go LOW before sending power pulses to the UCD7K device.

Driver Output

The high-current output stage of the UCD7K device family is capable of supplying ±4-A peak current pulses and swings to both VDD and GND. The driver outputs follows the state of the IN pin provided that the VDD and 3V3 voltages are above their respective under-voltage lockout threshold.

The drive output utilizes Texas Instruments' TrueDrive™ architecture, which delivers rated current into the gate of a MOSFET when it is most needed during the Miller plateau region of the switching transition providing efficiency gains.

TrueDrive™ consists of pullup/ pulldown circuits using bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. This hybrid output stage also allows efficient current sourcing at low supply voltages.

Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the external MOSFET. This means that in many cases, external-schottky-clamp diodes are not required.

Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCD7K drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver device. See Reference [1]

Drive Current and Power Requirements

The UCD7K family of drivers can deliver high current into a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. A MOSFET is used in this discussion because it is the most common type of switching device used in high frequency power conversion equipment.

Reference [1] discusses the current required to drive a power MOSFET and other capacitive-input switching devices.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E = \frac{1}{2} \times CV^2 \tag{1}$$

where C is the load capacitor and V is the bias voltage feeding the driver.

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by the following:

$$P = \frac{1}{2} \times CV^2 \times f \tag{2}$$

where f is the switching frequency.

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as:

$$P = 10\ nF \times 12^2 \times 300\ kHz = 0.432\ W \tag{3}$$

With a 12-V supply, this would equate to a current of:

$$I = \frac{P}{V} = \frac{0.432\ W}{12\ V} = 0.036\ A \tag{4}$$

The actual current measured from the supply was 0.037 A, and is very close to the predicted value. But, the I_{DD} current that is due to the device internal consumption should be considered. With no load the device current drawn is 0.0027 A. Under this condition the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable current due to cross-conduction in the output stages of the driver. However, these small current differences are buried in the high frequency switching spikes, and are beyond the measurement capabilities of a basic lab setup. The measured current with 10-nF load is close to the value expected.

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_G, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence $Q_G = C_{EFF} \times V$ to provide the following equation for power:

$$P = C \times V^2 \times f = Q_G \times V \times f \tag{5}$$

This equation allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a power driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCD7K family of drivers is available in PowerPAD™ TSSOP package to cover a range of application requirements. Both have the exposed pads to relieve thermal dissipation from the semiconductor junction.

As illustrated in Reference [2], the PowerPAD™ packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board (PCB) directly underneath the device package, reducing the Θ_{JC} down to 4.7°C/W. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference [3].

Note that the PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

Circuit Layout Recommendations

In a power driver operating at high frequency, it is a significant challenge to get clean waveforms without much overshoot/undershoot and ringing. The low output impedance of these drivers produces waveforms with high di/dt. This tends to induce ringing in the parasitic inductances. Utmost care must be used in the circuit layout. It is advantageous to connect the driver IC as close as possible to the leads. The driver device layout has the analog ground on the opposite side of the output, so the ground should be connected to the bypass capacitors and the load with copper trace as wide as possible. These connections should also be made with a small enclosed loop area to minimize the inductance.

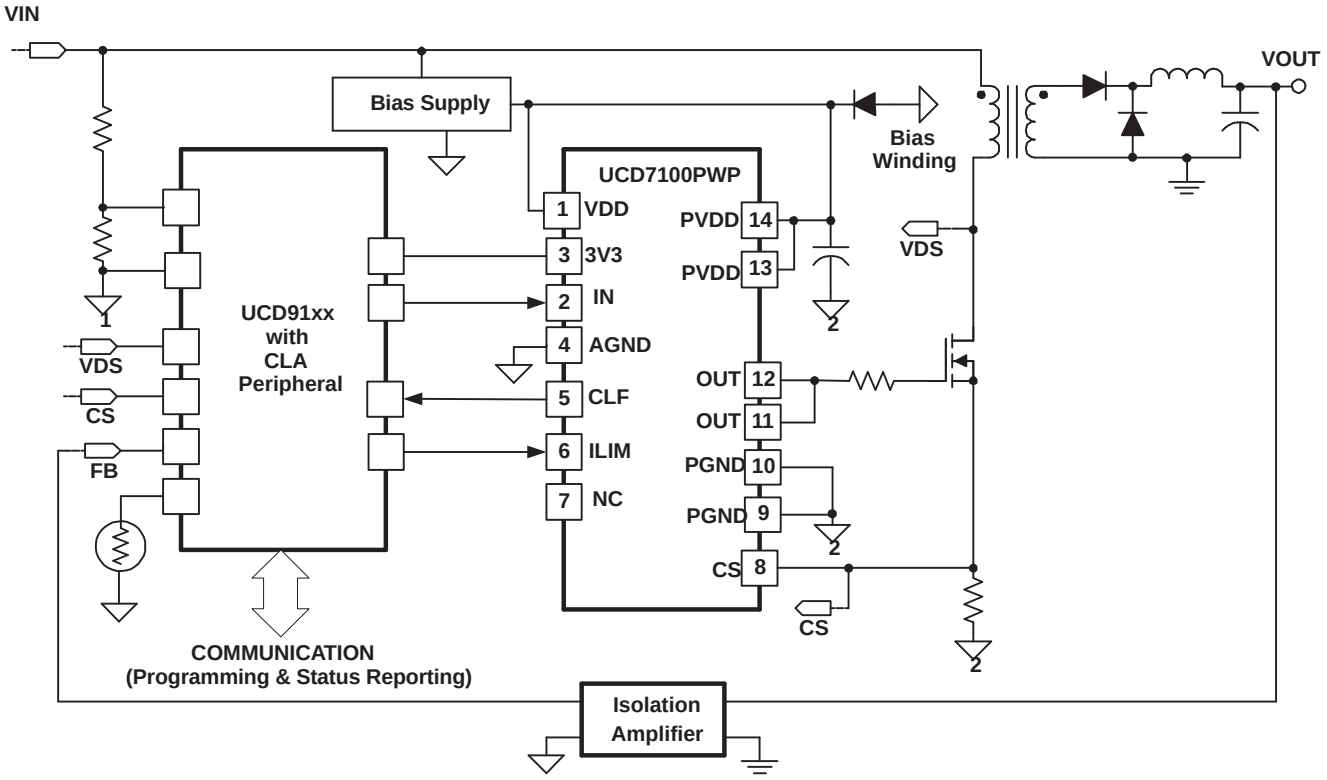


Figure 2. Isolated Forward Converter

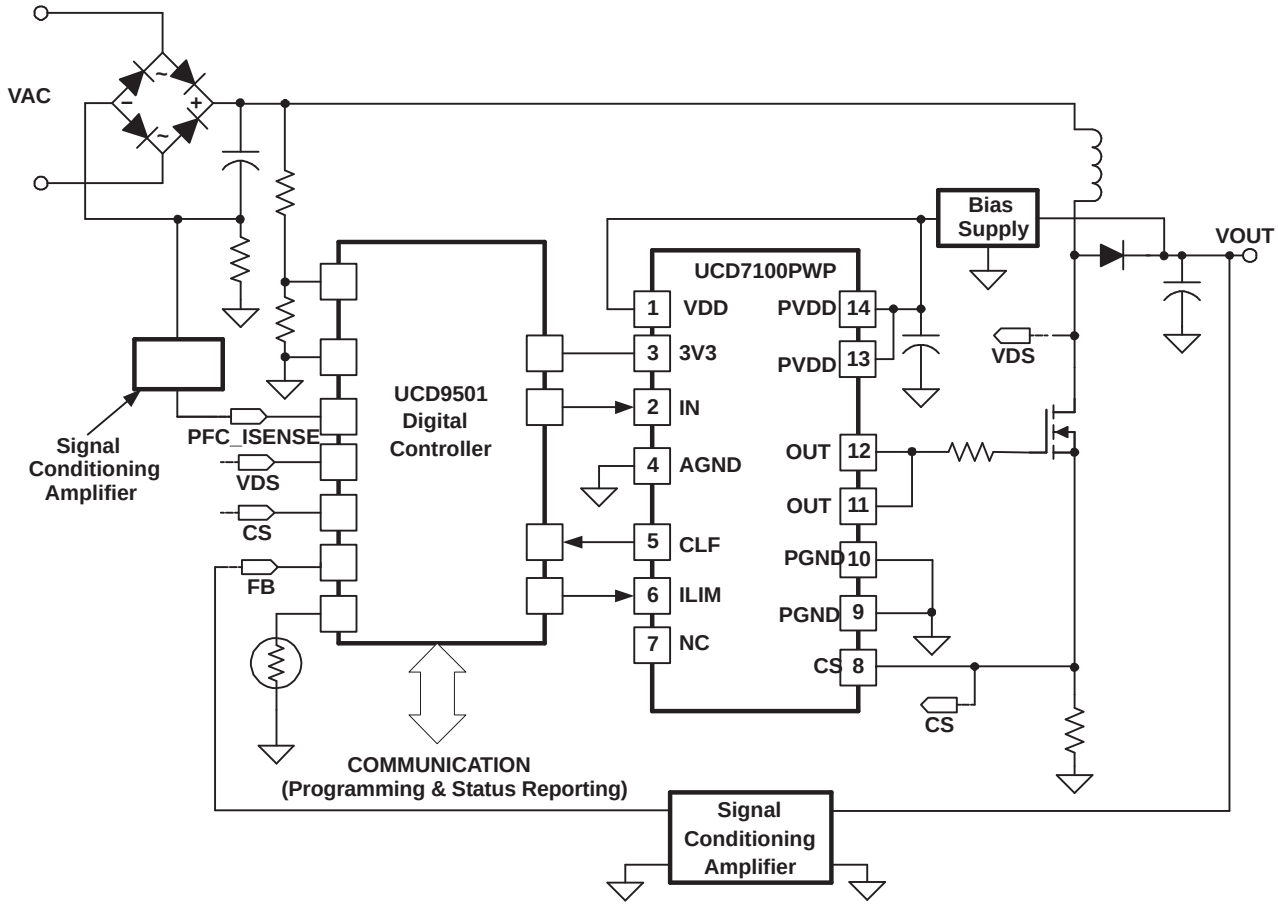


Figure 3. PFC Boost Front-End Power Supply

TYPICAL CHARACTERISTICS

UVLO THRESHOLDS vs TEMPERATURE

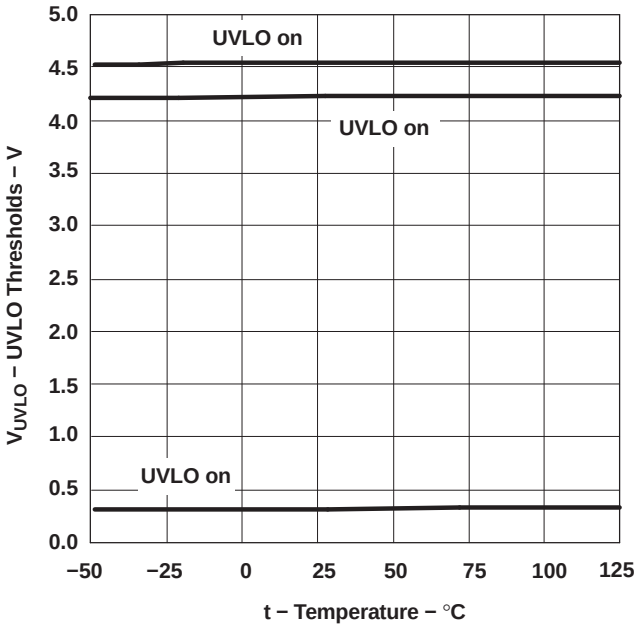


Figure 4.

3V3 REFERENCE VOLTAGE vs TEMPERATURE

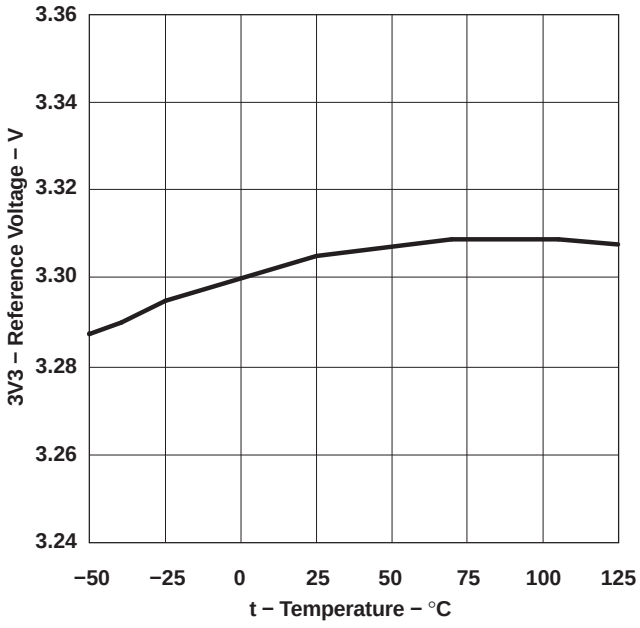


Figure 5.

3V3 SHORT CIRCUIT CURRENT vs TEMPERATURE

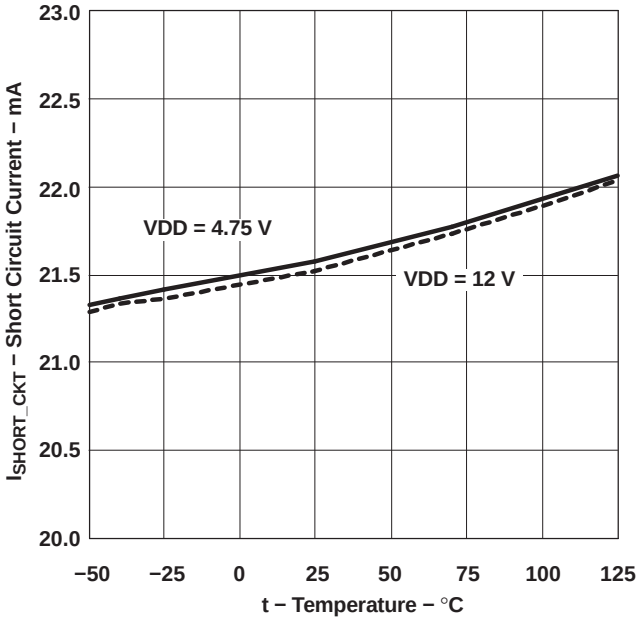


Figure 6.

INPUT THRESHOLDS vs TEMPERATURE

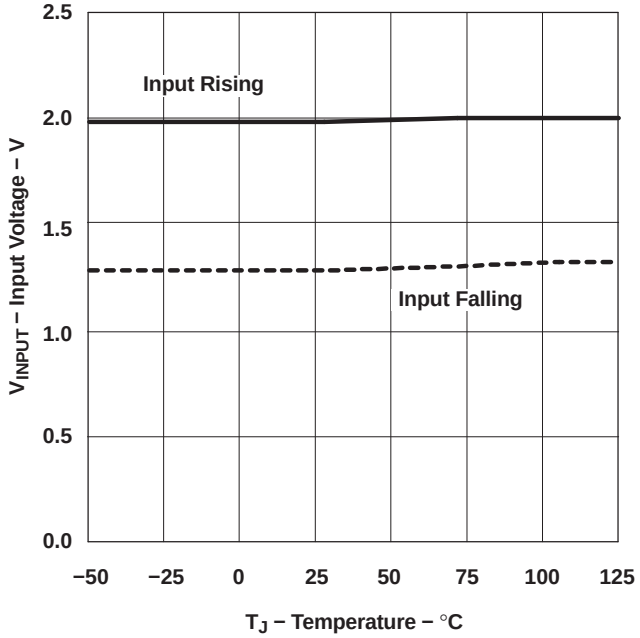


Figure 7.

TYPICAL CHARACTERISTICS (continued)

OUTPUT RISE TIME AND FALL TIME
vs
TEMPERATURE (V_{DD} = 12 V
)

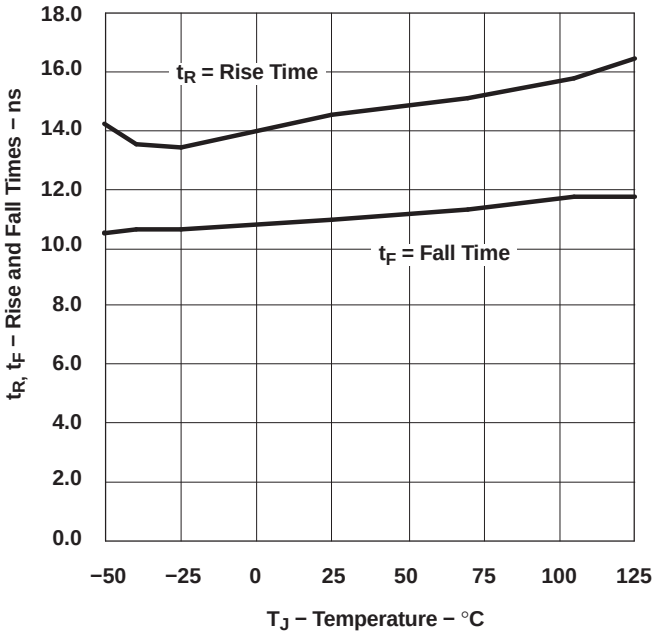


Figure 8.

RISE TIME
vs
SUPPLY VOLTAGE

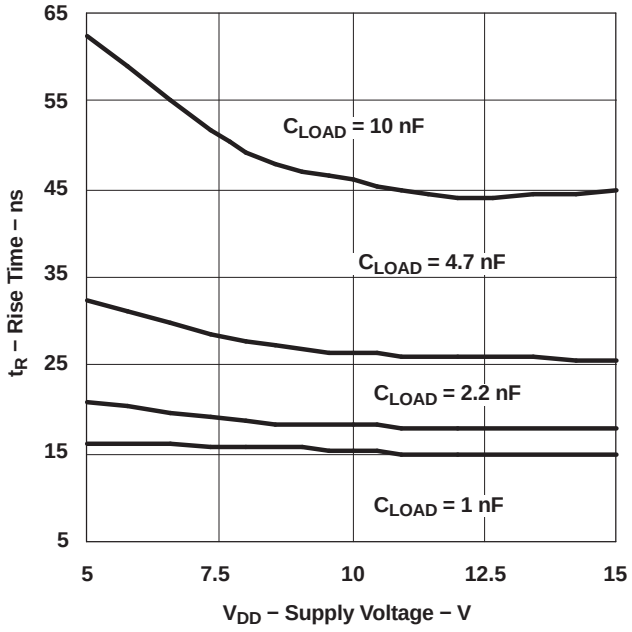


Figure 9.

FALL TIME
vs
SUPPLY VOLTAGE

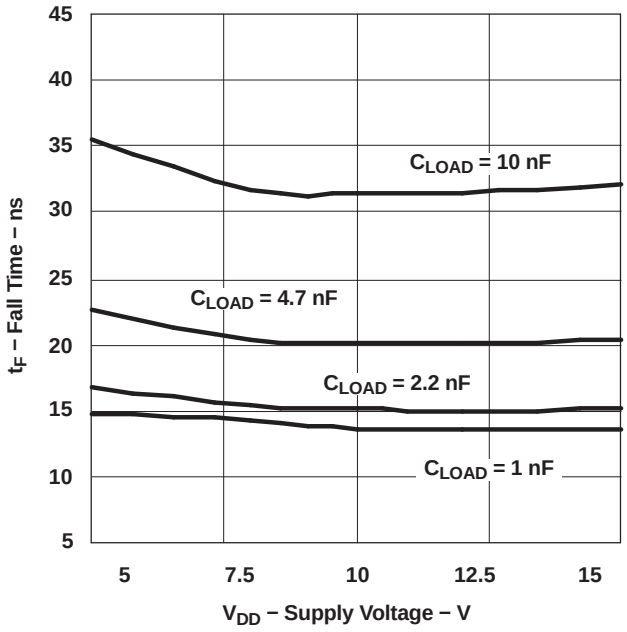


Figure 10.

PROPAGATION DELAY RISING
vs
SUPPLY VOLTAGE

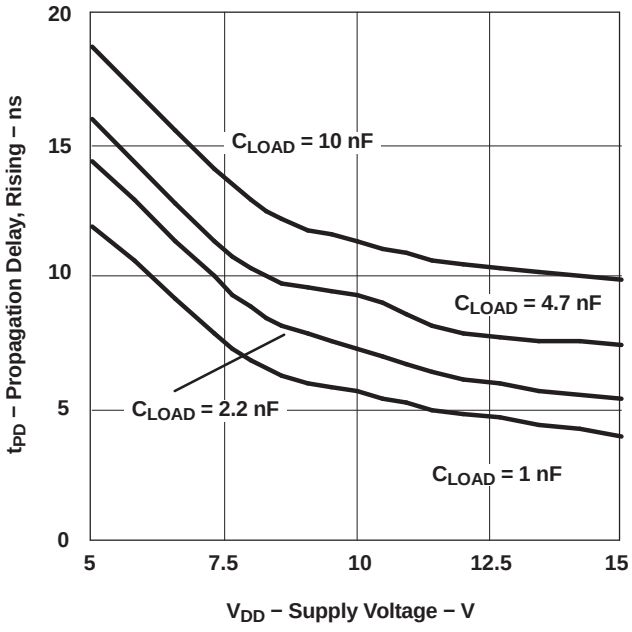


Figure 11.

TYPICAL CHARACTERISTICS (continued)

PROPAGATION DELAY FALLING vs SUPPLY VOLTAGE

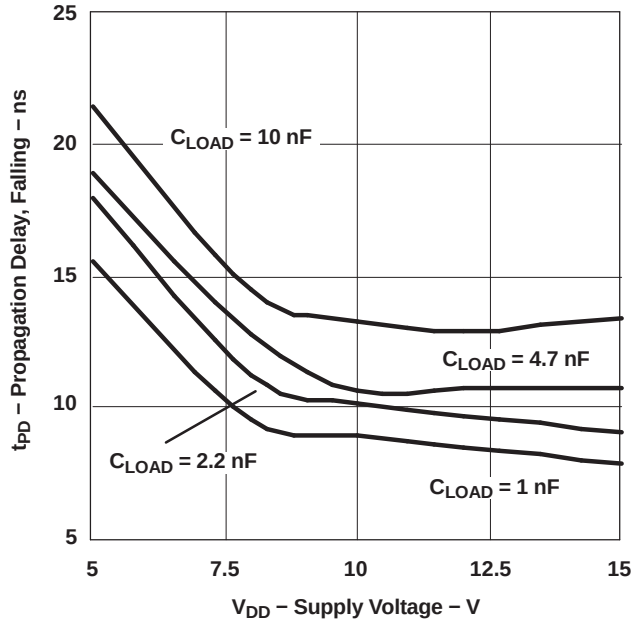


Figure 12.

DEFAULT CURRENT LIMIT THRESHOLD vs TEMPERATURE

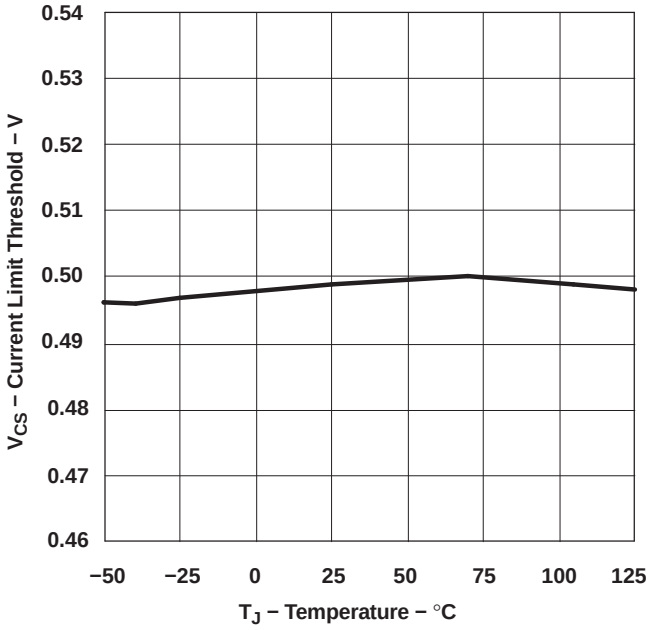


Figure 13.

CS TO OUTx PROPAGATION DELAY vs TEMPERATURE

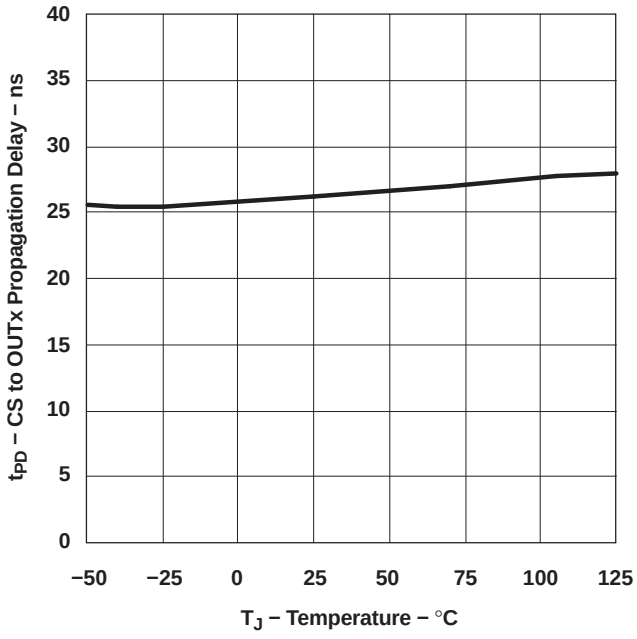


Figure 14.

CS TO CLF PROPAGATION DELAY vs TEMPERATURE

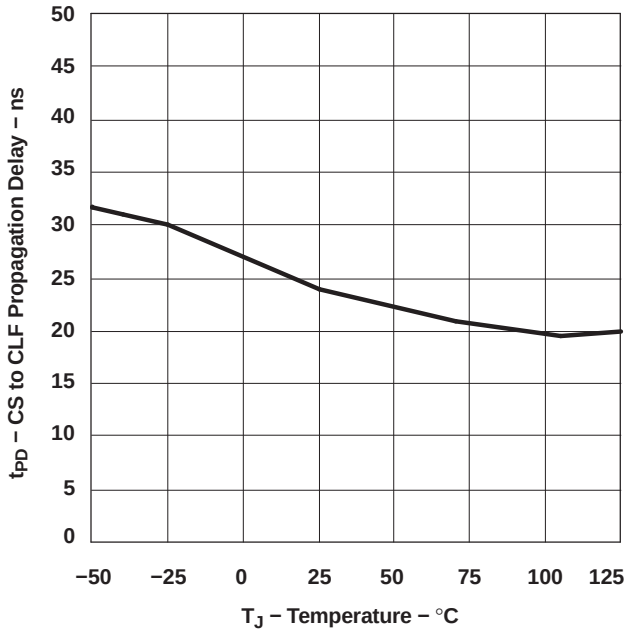


Figure 15.

TYPICAL CHARACTERISTICS (continued)

IN TO OUT PROPAGATION DELAY
vs
TEMPERATURE

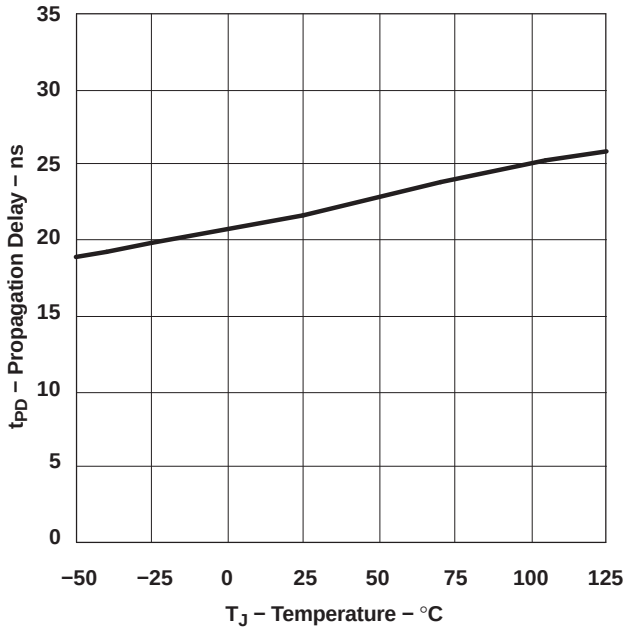


Figure 16.

START-UP BEHAVIOR AT V_{DD} = 12 V (INPUT TIED TO 3V3)

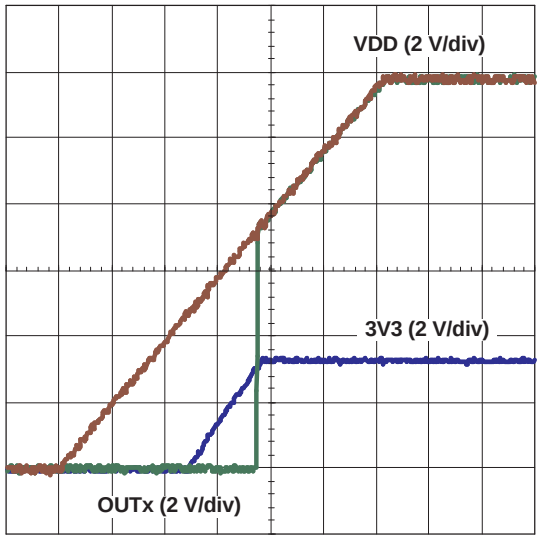


Figure 17.

SHUT DOWN BEHAVIOR AT V_{DD} = 12 V (INPUT TIED TO 3V3)

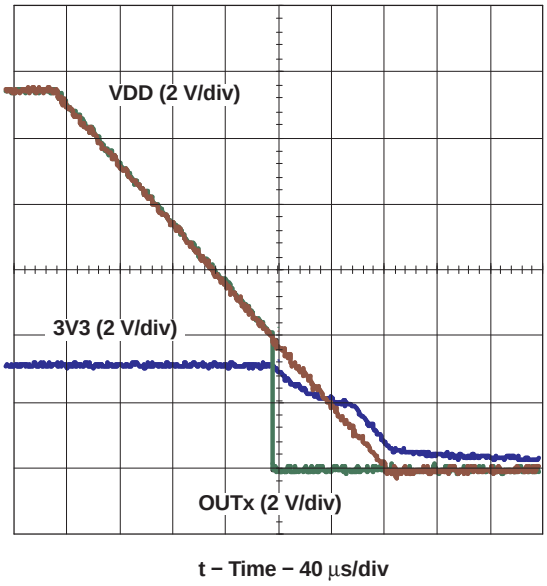


Figure 18.

START-UP BEHAVIOR AT V_{DD} = 12 V (INPUT SHORTED TO GND)

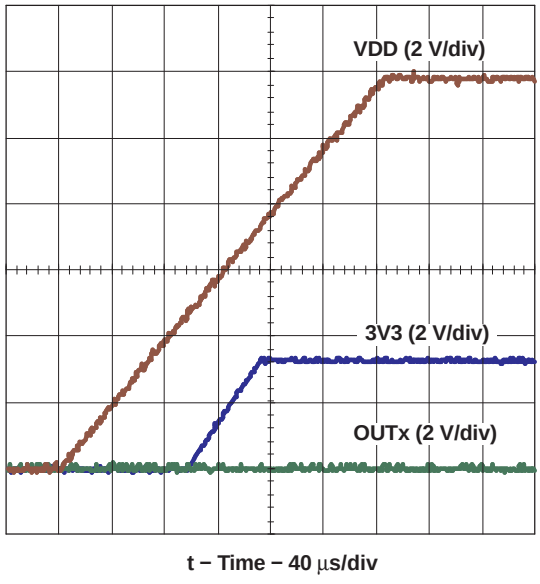


Figure 19.

TYPICAL CHARACTERISTICS (continued)

SHUT DOWN BEHAVIOR AT V_{DD} = 12 V (INPUT SHORTED TO GND)

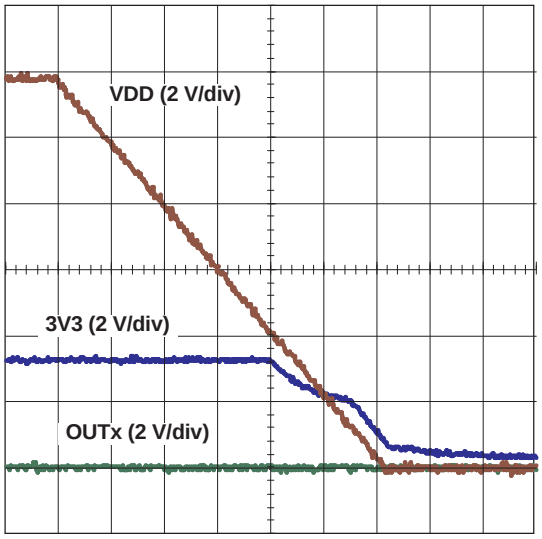


Figure 20.

OUTPUT RISE AND FALL TIME (V_{DD} = 12 V, C_{LOAD} = 10 NF)

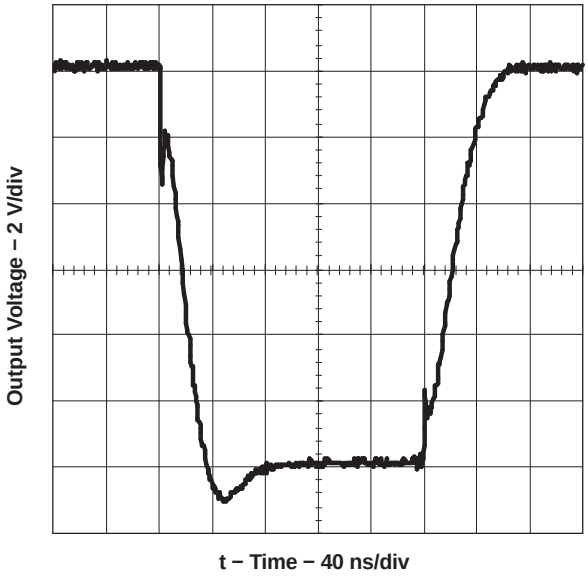


Figure 21.

REFERENCES

1. Power Supply Seminar SEM−1400 Topic 2: Design And Application Guide For High Speed MOSFET Gate Drive Circuits, by Laszlo Balogh, Texas Instruments Literature No. SLUP133.
2. Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002
3. Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004

RELATED PRODUCTS

PRODUCT	DESCRIPTION	FEATURES
UCD7200	Dual Low Side ±4-A Drivers with Independent CS	3V3, CS(1) (2)
UCD7201	Dual Low Side ±4-A Drivers with Common CS	3V3, CS(1) (2)
UCD7230	±4A Synchronous Buck Driver with CS	3V3, CS(1) (2)
UCD9110	Digital Power Controller for High Performance Single-loop Applications	

(1) 3V3 = 3.3V linear regulator.
(2) CS = current sense and current limit function.

REVISION HISTORY

DATE	REVISION	CHANGE DESCRIPTION
3/4/05	SLUS651	Initial release
4/29/09	SLUS651B	Removed QFN package option and all references.
5/21/10	SLUS651C	Removed part numbers, UCD7500, UCD7600, UCD7601 and UCD9501 from Related Products Section.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UCD7100PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD7100	Samples
UCD7100PWPG4	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD7100	Samples
UCD7100PWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD7100	Samples
UCD7100PWPRG4	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD7100	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

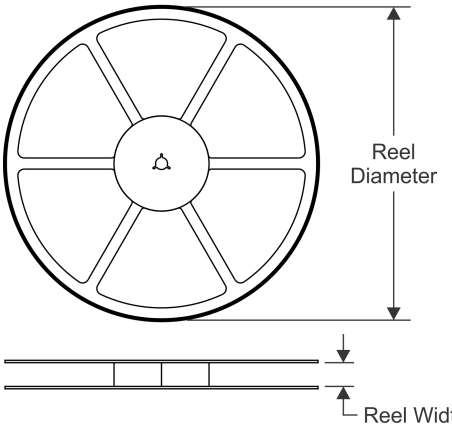
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

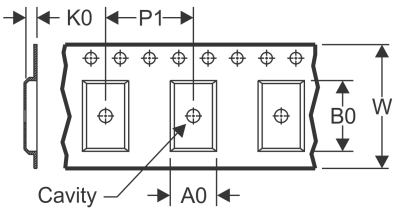
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

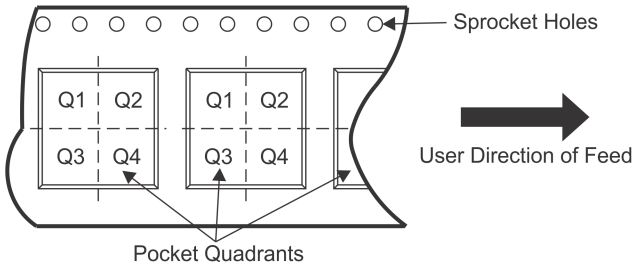


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

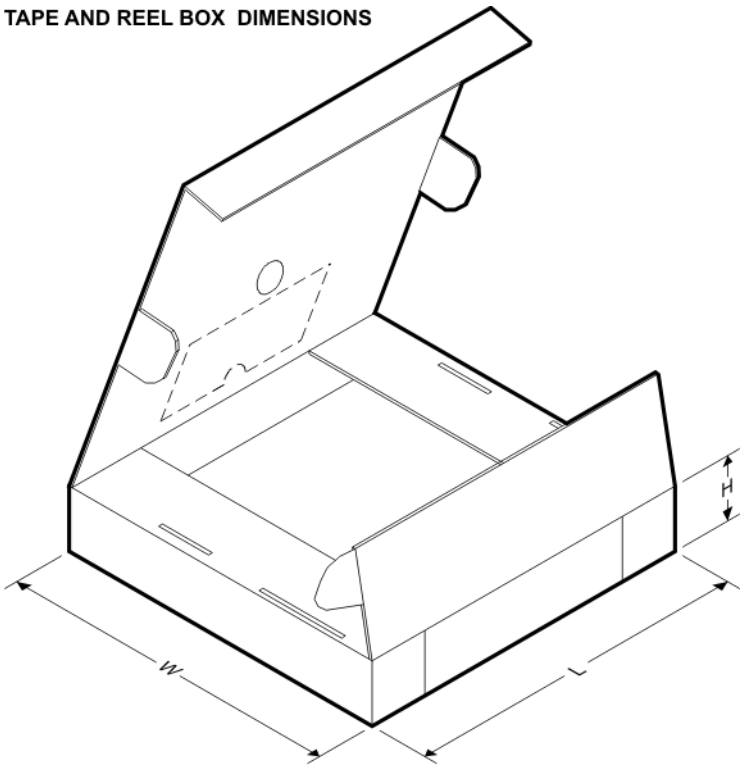
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD7100PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

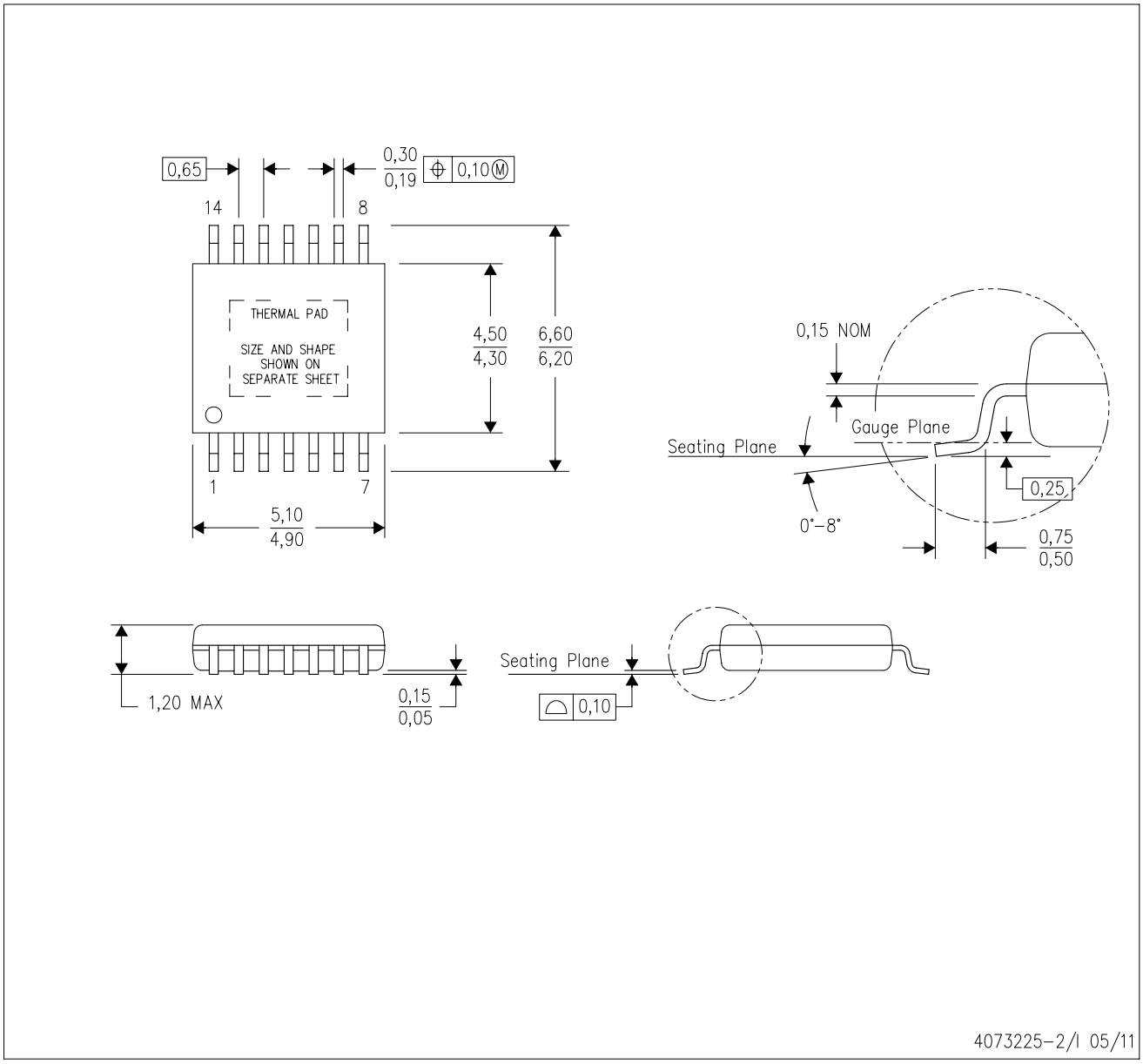
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD7100PWPR	HTSSOP	PWP	14	2000	367.0	367.0	35.0

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

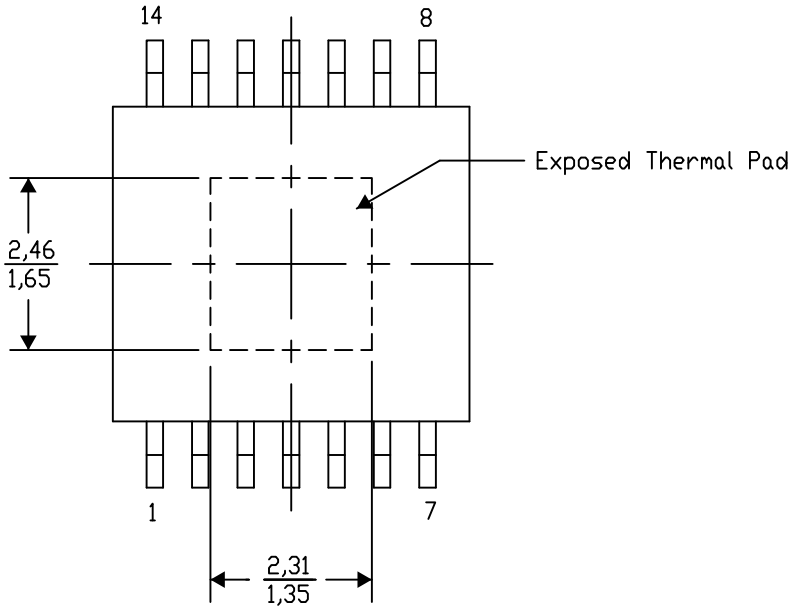
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–2/AD 01/13

NOTE: A. All linear dimensions are in millimeters

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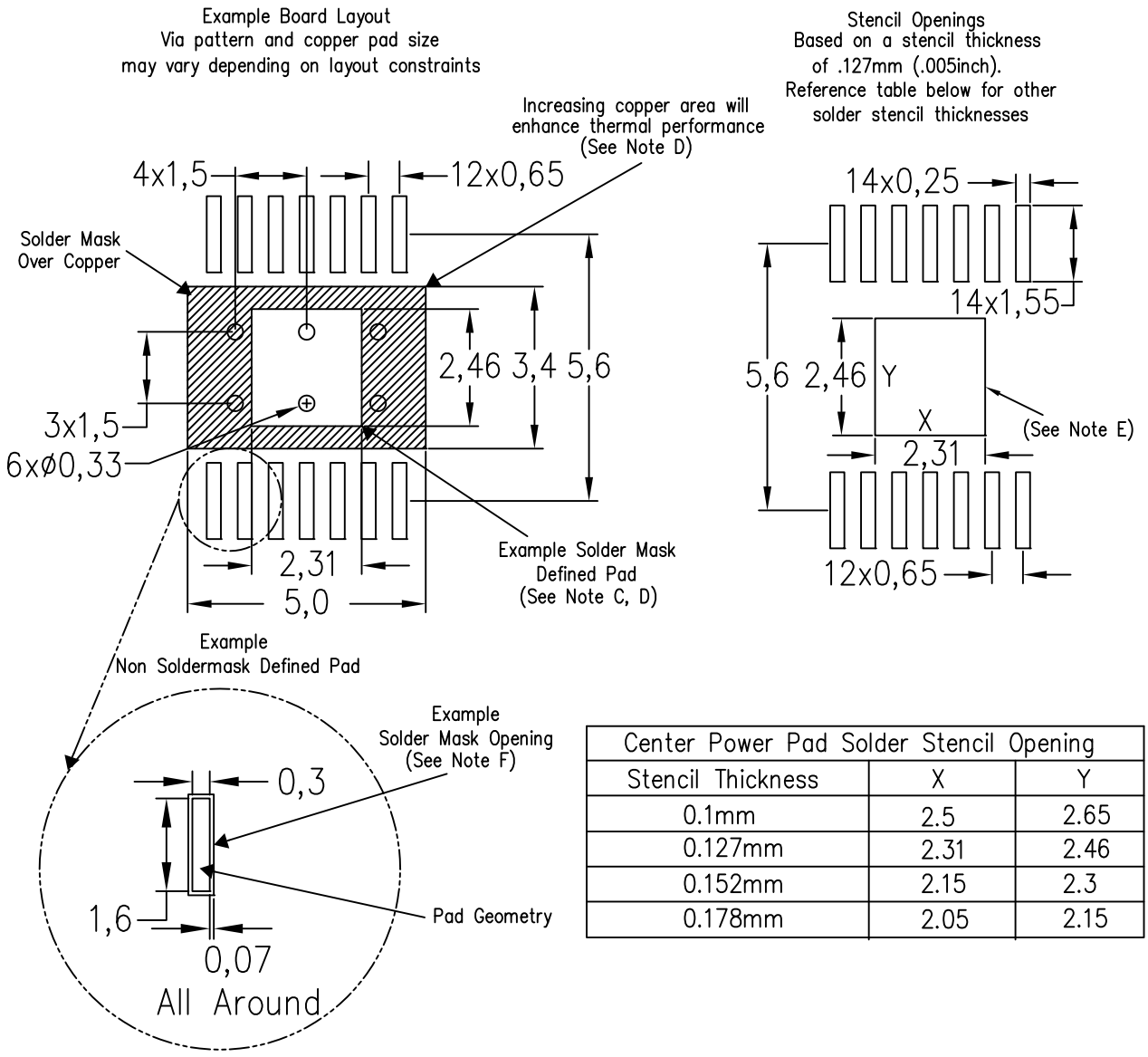
PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/S 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

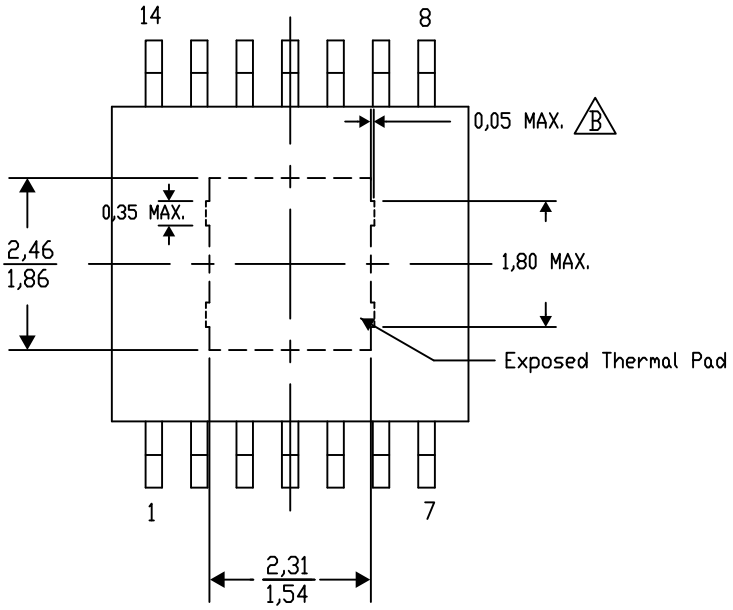
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–44/AD 01/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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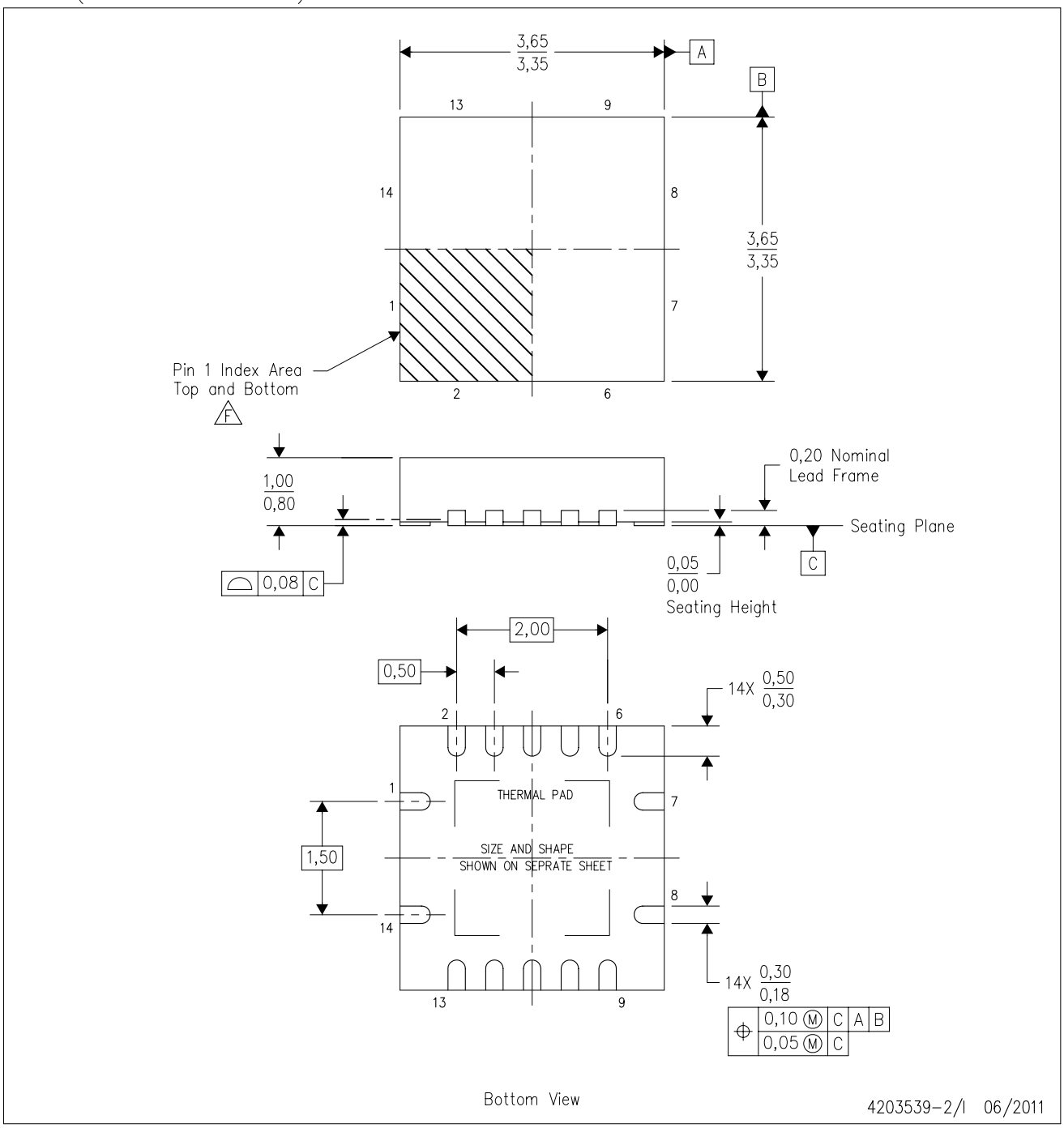
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

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